CSE31 : Lab #11 – FSM

Overview

This lab will make you go through the exercises of creating Finite State Machines. They are useful to model system that behaves in a certain way or have some properties. Refer to the lecture slides and the readings on how to draw these and what the symbols mean. Briefly, they are machines made out of *states*. You can change from one state to another by consuming one input. That change would be denoted using an arc between two states with the notation Input/Output where Input is the consumed data and Output is the result of changing states.

Reading : P&H Appendix B

(Exercise) Create FSM

Consider the design of a finite state machine (FSM) with two 1-bit inputs (clk and CE), and one 2-bit output (X). clk is the clock signal and CE is the "count enable" signal. While CE=1, the FSM behaves as a "binary counter", i.e. its output cycles through the pattern 00, 01, 10 11, 00, moving from one output value to the next on each positive edge of clk. If CE = 0 the output value remains unchanged. (it will remain in the same state if it is not enabled)

Note that FSM has no reset input signal. You can assume that it starts up in any legal state. (hint: think about how many total states there are and it should start counting anywhere in the repeating sequence).

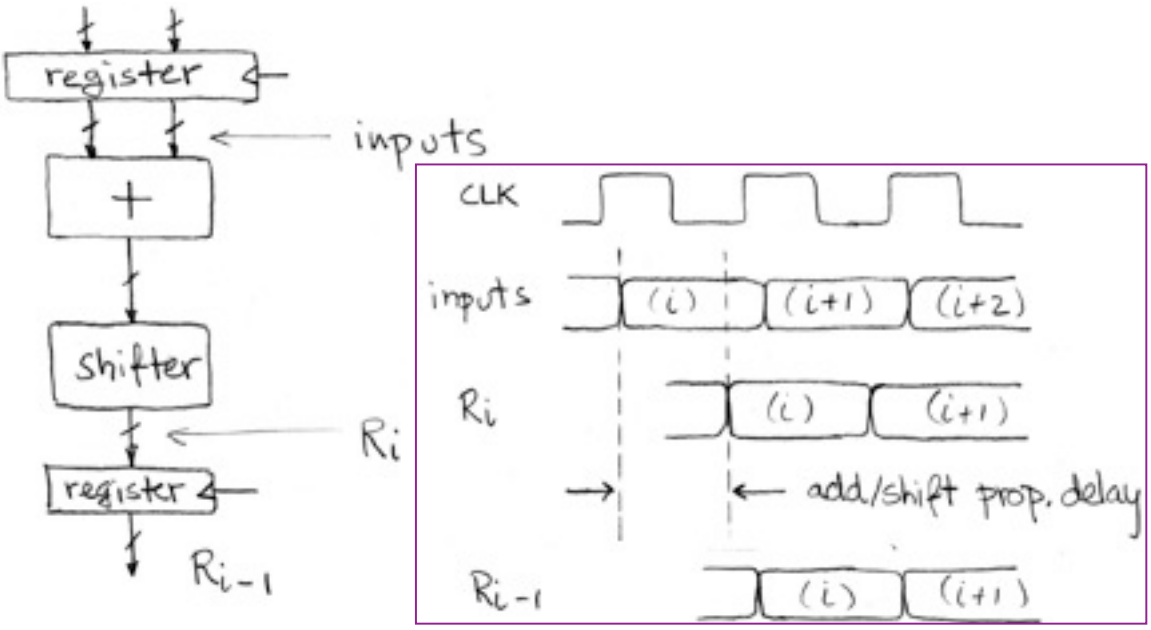
Sketch the state transition diagram that represents the behavior of this FSM in the style of the lecture notes. You may draw this using paper or using your computer. Either show it to your TA or attached it with the submission to this lab assignment.

Q1. What is the minimum number of states you need for this FSM?

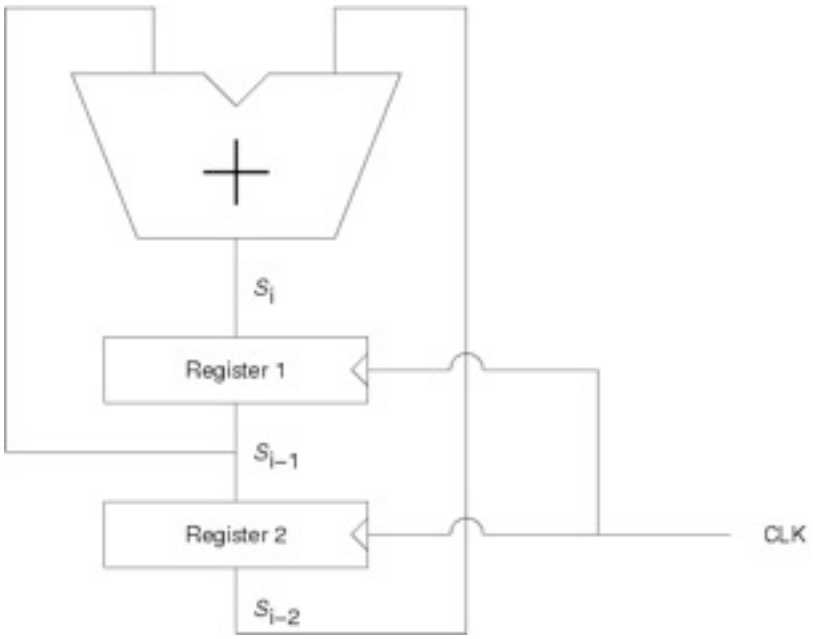
Q2. What is the relation between the state and the output? (ie are they always the same value or different)

(Exercise) Create fsm2.c

Recall the following from Lecture 21 for the circuit on the left and timing diagram on the right:



Clk controls the registers and output of the registers changes on the rising-edge of the clock (Clk). **Draw the timing diagram** on the right for the circuit below with 1 adder and 2 registers for 5 cycles.



Initial State: Register 1 holds '1' and register 2 holds '0'

Q3. What are the first 10 values of "Register 2" in the first 10 cycles?

Q4. What operation or function does this FSM perform?

Q5. Write a C program that does the same operation or function and returns the value stored in "Register 2" as a function of the number of clock ticks since the FSM started.

What to hand in

When you are done with this lab assignment, you are ready to submit your work. Make sure you have done the following **before** you press Submit:

- Answers to Q1-Q5.
- Attach FSM drawing, fsm2.c and Timing Diagram
- List of collaborators
