

Electroencephalography Acquisition System: Analog Design

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Abstract

Electroencephalography (EEG) is a sensitive and weak biosignal that varies from person to person. It is easily affected by noise and artifacts. Hence, maintaining the signal integrity to design an EEG acquisition system is crucial. This article proposes an analog design for acquiring EEG signals. The proposed design consists of eight blocks: (1) a radio-frequency interference filter and electro-static discharge protection, (2) a preamplifier and second-order high-pass filter with feedback topology and an unblocking mechanism, (3) a driven right leg circuit, (4) two-stage main and variable amplifiers, (5) an eight-order anti-aliasing filter, (6) a six-order 50-Hz notch filter (optional), (7) an opto-isolator circuit, and (8) an isolated power supply. The maximum gain of the design is approximately 94 dB, and its bandwidth ranges from approximately 0.18 to 120 Hz. The depth of the 50-Hz notch filter is -35 dB. Using this filter is optional because it causes EEG integrity problems in frequencies ranging from 40 to 60 Hz.

Electroencephalography (EEG) is a biosignal that is widely used in research and clinical practices, including pain quantification,¹ brain-computer interface applications (e.g. wheelchair control),^{2,3} sleep studies,⁴ anesthetic depth monitoring,⁵ and diagnosis of conditions (e.g., epilepsy, head injuries, dizziness, brain tumors, psychiatric conditions).⁵⁻⁷ This signal starts at a frequency of

0.1 to 0.7 Hz and ends at 30 to 100 Hz. It has an amplitude range from 10 to 100 μ V.⁷⁻⁹ It is easily affected by noise and artifacts. The signal must be acquired properly to retain quality and extract useful information, and this can be challenging.

The major challenges of designing a proper EEG acquisition system are high-frequency noises, undesired direct current (DC) components, voltage amplification level, phase distortion, 50-Hz powerline interferences, and isolation of the signal and supply sources. Historically, different designs have been proposed for handling these challenges.¹⁰⁻²⁰ All of these designs aim to reduce the imperfections of analog signal conditioning and to ensure signal integrity. Similarly, this article presents a system that would help resolve the above-mentioned challenges.

Methods

The proposed EEG acquisition system is shown in Figure 1. It includes eight blocks: (1) a radio-frequency interference(RFI) filter and electro-static discharge (ESD) protection, (2) a preamplifier and second-order high-pass filter with feedback topology and an unblocking mechanism, (3) a driven right leg (DRL) circuit, (4) two-stage main and variable amplifiers, (5) an eight-order anti-aliasing filter, (6) a six-order 50-Hz notch filter (optional), (7) an opto-isolator circuit, and (8) an isolated power supply.

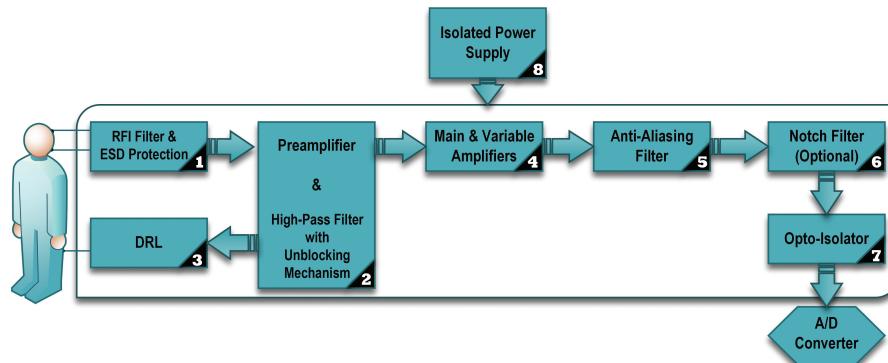


Figure 1. Block diagram of the proposed electroencephalography acquisition system. Abbreviations used: RFI, radio frequency interference; ESD, electro-static discharge; DRL, driven right leg; A/D, analog to digital.

The circuit schematic of the proposed system is illustrated in the supplemental material for this article (available online at www.aami.org/bit). Each block is explained in detail in the following sections.

Block 1: RFI Filter and ESD Protection

The first block is an RFI filter and ESD protection, which cancels out RFI and harmful DC components. RFI usually is rectified by integrated circuits and is converted into DC offset voltage. It is undesired for the system. In addition, ESD and high-voltage stresses from defibrillation would damage the system. That is why developing a prudent method to address these issues is essential. By using previously described techniques,^{21,22} a circuit is presented (part 1 of online supplemental material). In this circuit, at inputs, the resistors R_1 and R_2 maintain a DC-coupled path and act as current limiters to the electrodes. The capacitors C_1 , C_2 , and C_3 eliminate high-frequency currents from electrosurgery or ablation procedures. Moreover, C_1 reduces possible common-mode rejection errors from the mismatch of resistors and capacitors (R_1 with R_2 and C_2 with C_3 , respectively). In addition, R_1 and R_2 and C_1 , C_2 , and C_3 form a low-pass filter. R_3 and R_4 are placed to maintain high immunity against common-mode signals. Diodes D_1 , D_2 , D_3 , and D_4 are used to protect preamplifier inputs against high-voltage stresses. These diodes provide safety for both the patient and the preamplifier.

Block 2: Preamplifier and High-Pass Filter with Unblocking Mechanism

The second block in the proposed system consists of three sub-circuits, which are preamplifier, high-pass filter, and unblocking mechanism (part 2 in the online supplemental material). Because of its vital role in the general performance of the system, this block is an essential part of the proposed circuit. It acts as the first amplifying stage of the EEG signal. Simultaneously, it eliminates undesired low-frequency components.

Preamplifier. EEG signal has a low voltage amplitude and carries a lot of common-mode interferences. Hence, it is necessary to select a suitable preamplifier. To this end, applied

instrumentation amplifiers can augment faint differential signals in the presence of significant common-mode interferences.²³ Studies showed that INA128 and AD620 are good choices for instrumentation amplifiers.^{21,24} They are low noise, low drift, and small DC offset. Their buffered inputs provide a high input impedance and a high common-mode rejection rate (CMRR). These amplifiers have a reference pin that could be used for filtering purposes. We use this pin for designing a high-pass filter with feedback topology in the next section. According to the INA128 datasheet,²⁵ it could handle up to ± 40 V without being damaged. We apply this amplifier in the proposed system (part 2.1 of the online supplemental material). The R_g value determines the preamplifier gain level by $1 + 50 \text{ k}\Omega/R_g$.

High-pass filter. The EEG electrodes usually are polarizable up to 2.5 V.²¹ In addition, the movement artifacts could produce a DC value on the scalp of the subject. These DC components are considerably higher than the original EEG signals and could saturate the analog part of the acquisition system. To avoid saturation in the analog circuit, a high-pass filter with a small cut-off frequency is required. With inspiration from Lin et al.,²⁶ we present a second-order high-pass filter by feedback topology. This filter is illustrated in part 2.2 of the online supplemental material. The advantage of this filter is that it avoids the use of capacitors in series. Some of the problems with the use of capacitors in series (especially large ones), such as their high equivalent series resistance, voltage coefficient, and other nonidealities, can be avoided.

Unblocking mechanism. The small cut-off frequency in high-pass filters results in a large time constant value. Therefore, any overload in the system will make the system require more time to get back to a normal condition. With inspiration from Prutchi and Norris,²² we present an unblocking mechanism that changes the time constant of the filter. It includes a full-wave rectifier (part 2.3 of the online supplemental material), a comparator (part 2.4 of the online supplemental material), and two analog switches (part 2.2 of the online supplemental material). When an overload occurs in the system,

the full-wave rectifier converts the alternating current input to a DC value and feeds the noninverted pin of the comparator. Upon comparing the input pins, the comparator output increases and activates analog switches. As a result, the cut-off frequency of the high-pass filter is increased to a high value, resulting in a small time constant value. This temporary change will help settle down the saturated circuit in less time. When the circuit settles down, the analog switches would be deactivated, thereby causing the characteristics of the high-pass filter to return to their original values.

Block 3: DRL Circuit

The third block is the DRL circuit. It effectively reduces the common-mode interferences from the human body, especially in an unshielded environment. The most critical common-mode interference is 50-Hz powerline noise, which may be collected by a human body acting as an antenna. To reduce this interference, a DRL circuit is established with inspiration and some customization of previously described circuits.^{21,24} The circuit is displayed in part 3 of the online supplemental material. It feeds the amplified common-mode signals back to the human body to attenuate them. Studies show that the DLR can reject the interferences better than the instrumentation amplifier by more than 20 dB.^{21,27}

Block 4: Main and Variable Amplifier

The fourth block, which is the main and variable amplifying unit, is necessary for two reasons. The first reason is delivering EEG signals with an appropriate voltage level to A/D converter (ADC). For example, for an input range of $\pm 1,000 \mu\text{V}$, if the standard input range of ADC is $\pm 5 \text{ V}$, a gain of $5,000 \text{ V/V}$ would be required to bring the signal to $\pm 5 \text{ V}$.²⁸ The second reason is that the voltage range of EEG signals varies for different people and in different conditions, and because the characteristics of ADCs vary. A two-stage amplifier therefore is proposed. As shown in part 4 of the online supplemental material, the gain of amplifier A9 can be adjusted by changing the R_{24} potentiometer value.

Block 5: Anti-Aliasing Filter

The fifth block is a low-pass filter that removes all unwanted high-frequency components and band limits the signal. This filter is called an anti-aliasing filter because it can avoid aliasing high-frequency components to the desired components in a digitization process. According to Nyquist sampling theory,²⁹ the sampling rate should be at least twice that of the highest frequency components that exist in the signal passband. Therefore, EEG can be digitized with a minimum sampling rate of 250 Hz (higher sampling rate [e.g., 512 or 1,024 Hz] is strongly encouraged) if the high cut-off frequency of this filter is equal to or less than than 125 Hz. To this end, this article presents an eight-order anti-aliasing filter using the quad amplifier of OPA4227 (OPA227 quad package), as shown in part 5 of the online supplemental material. OPA4227 is used in our proposed filter because it is a high-precision quad amplifier package with characteristics that include high CMRR, low noise, low undesired offset voltage, and low input bias current, thereby making it appropriate for data acquisition³⁰ and the design of active filters.^{24,31}

Block 6: 50-Hz Notch Filter

The sixth block is the notch filter that eliminates 50-Hz powerline interference. This block is optional in the circuit described here because it creates substantial phase distortion in the frequencies adjacent to the center frequency of the filter. This interference can be effectively reduced by techniques such as using the DRL circuit, maintaining a high CMRR in the circuit, using coaxial cables, and environmental shielding. If these techniques cannot be met, then a notch filter could help improve the performance of the circuit. The circuit schematic of the notch filter is illustrated in part 6 of the online supplemental material.

Block 7: Opto-Isolator Circuit

The digital part of the EEG acquisition system is considerably more sensitive to voltage stress than the analog part. In addition, analog circuits may harm sensitive digital circuits under certain conditions. Therefore, it is necessary to ensure that the

analog and digital circuits are properly connected and to prevent the interferences from entering the digital part. To this end, this article applies a linear optical isolation circuit, as described previously.²²

As shown in part 7 of the online supplemental material, section A has the duty of prebiasing the light-emitting diode driver by applying a negative offset voltage to the inverting pin of A18. Simultaneously, a gain-adjusted version of the EEG signal would be present at the noninverting pin of A18. As a result, A18 would run the optical isolator IC through T1. This IC feeds back a control voltage at the inverted pin of A18 by flowing the photodiode current to R_{37} . It makes the circuit highly linear to the matched photodiode characteristics in the optical isolator IC. After a current-to-voltage conversion, the regenerated signal would be available at the noninverted pin of A19. Section B of this circuit is a voltage follower to nullify the signal offset. The circuit advantage is that it could act highly linear against aging, temperature swings, LED drive current dynamics, or LED nonlinearity.

Block 8: Isolated Power Supply

Leakage current and electromagnetic interference (EMI) are common risks that may disrupt the acquisition process or cause considerable damage to both human and hardware. Therefore, ensuring safety for both sides is important. In the same vein, with inspiration from Figure 12 in Prutchi and Norris²² (while applying changes to the voltage range), an isolated power supply is presented here. The circuit is shown in part 8 of the online supplemental material. Two separate power supplies are used for analog and digital parts. A 15-V medical-grade adapter provides the input to this circuit. This circuit uses two DC/DC converters of PWR1312 and PWR1315. These converters are capable of handling up to 4 kV and have a leakage current of 4 μ A, thereby making them appropriate for medical purposes.³² PWR1312 produces an isolated 5 V and a ground for the digital part. PWR1315 supplies the analog part with an isolated ± 5 V. The galvanic isolation of DC/DC converter eliminates the risk of leakage currents, but the risk of EMI remains. The EMI suppres-

sion filter therefore is added to the power supply circuit.

Results

The high cut-off frequency of an RFI filter is almost 758 Hz, which is enough to eliminate RFI. By setting R_g to 5 k Ω , the preamplifier gain is 20.83 dB for the EEG signal. According to the INA128 datasheet, the preamplifier has a CMMR range of 100 to 120 dB and an input impedance range of 10 to 100 G Ω .²⁵ The low cut-off frequency of the high-pass filter is approximately 0.18 Hz. As a result, the undesired DC components can be removed. In overload conditions, the unblocking mechanism varies the filter cut-off frequency from 0.18 to 303 Hz. As a result, the system returns to normal conditions in a few milliseconds instead of a few seconds. The low cut-off frequency of the DRL circuit is approximately 104 Hz. This circuit amplifies the common-mode voltage with a gain of 31.8 dB and reinjects it to the body. As a result, a floating ground is formed. Main and variable amplifiers have an adjustable gain from 41.73 to 73.32 dB. These amplifiers provide the most appropriate level of gain for each person and each ADC, thereby improving the quality of the acquisition process.

The high cut-off frequency of the anti-aliasing filter is approximately 120 Hz. It is capable of achieving -40 dB of attenuation at 410 Hz. Therefore, it retains information and guarantees the quality of the A/D conversion process. This filter has a constant group delay with a maximum swing of 17 μ s in its passband. Thus, the phase distortion is almost eliminated. Due to the filter sensitivity, a maximum tolerance of 5% must be maintained when choosing the circuit components to avoid unexpected phase distortion. Notch filter has an attenuation depth of -35 dB in 50-Hz frequency. However, it creates a phase distortion in the frequency range of 40 to 60 Hz. As a result, the use of this filter is optional in the proposed system.

Finally, the frequency response for the high-pass, anti-aliasing, and notch filters are shown in Figures 2, 3, and 4, respectively. As illustrated, all filters have a flat amplitude and a constant group delay in their bandwidth.

In summary, the advantages of this design are its unblocking mechanism, flat

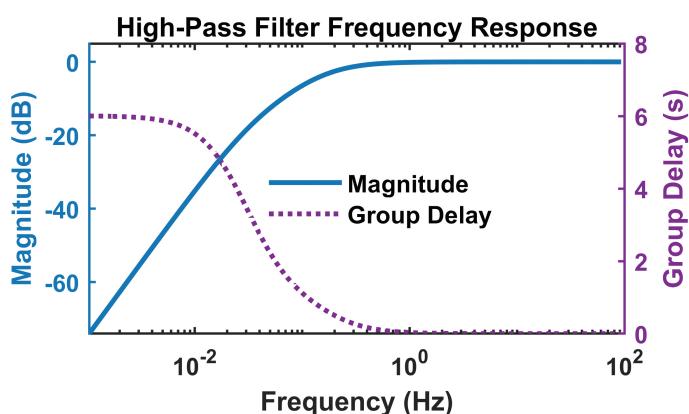


Figure 2. Frequency response of the high-pass filter.

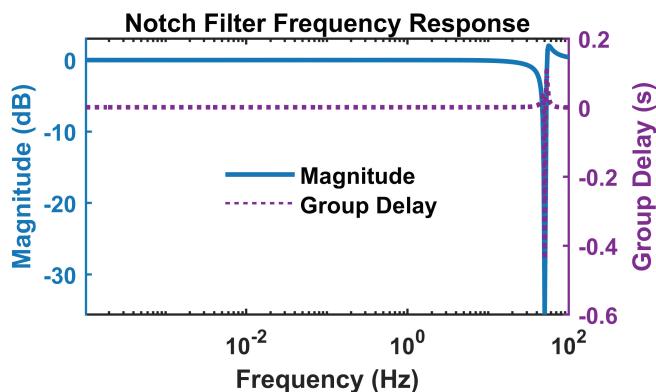


Figure 3. Frequency response of the anti-aliasing filter.

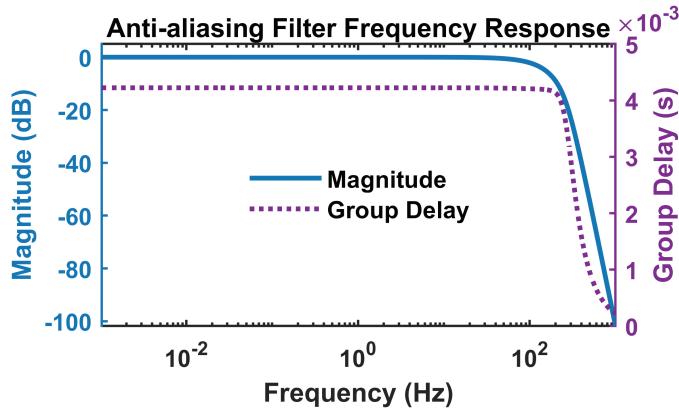


Figure 4. Frequency response of the notch filter.

frequency response, linear phase response, and multiple-step safety system. However, the cost and power consumption of this design are limitations when designing a multichannel system, and these limitations should be addressed in future works. To our knowledge, unblocking mechanism and phase analysis have not been evaluated in existing works.

Because of the diversity of parts, models, and suppliers, an exact estimation of building cost is not possible. However, the authors

estimate that this design would cost approximately \$120 (USD) per channel. Running tests on a prototype (with some changes) may lower the total cost (especially for high numbers of channels).

Conclusion and Future Work

The analog design for an EEG acquisition system described here has a bandwidth from 0.18 to 120 Hz. In addition, it has a tunable gain from 62.5 to 94.15 dB. The frequency response of the design has a flat magnitude and a linear phase. In addition, the design can protect humans and hardware against abnormal situations. Hence, it is the belief of the authors that this design would meet medical standards requirements for EEG acquisition.

The goal of future work is to reduce power consumption and to achieve a complete design of the EEG acquisition system, accompanied by digital parts. In this case, its application in a mobile-based neurofeedback designation for home healthcare, as a brain-computer interface, may be possible.

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