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QUIZ 3

1. What types of transfers must a computer’s interconnection structure (e.g. bus) support?
   * + Memory to processor: This instruction stores the memory in the processor and executes it based on the given instruction.
     + Processor to Memory: This instruction makes modifications to the memory once it is executed.
     + Input/ Output to Processor: the I/O module processes and reads the data from the input/output device
     + Processor to Input/ Output: This instruction sends data to the peripherals.
2. Consider a 64-bit microprocessor with a 16-bit external data bus which is driven by a 32-MHz input clock. If it has a bus cycle with a minimum duration equal to 8 input clock cycles,
   1. what is one bus cycle equal to in nanoseconds?

6.4 \* 10^-9 nanosec

* 1. what is the maximum data transfer rate across the bus that the microprocessor can sustain, in bytes/sec?
     + 16 bits \* 32 MHz/ 8cycles = 64 bits per sec

1. If a processor has 64-bit instructions that starts with a 3 byte opcode, how many bits are needed for the program counter and the instruction register?

8 bits = 1 byte for he opcode

3 byte opcode = 24 bits.

64 bits - 24 bits (the 3 byte opcode) = 40 bits

1. Consider a hypothetical microprocessor that has a 16-bit address bus and 16-bit data bus whose program counter and address registers are 16 bits wide. What is the maximum memory address space that the processor can access directly if it is connected to a “8-bit memory”?

Hypothetical microprocessor address =16 bits

Program counter & register = 16 bits

bus data = 16 bits

8 bit memory = 1= 1byte

Accessed processor = 2^16 = 64K

Max data memory address = 64k \* 1 byte = 64Kbytes