AN2606
Application note

STM32 microcontroller system memory boot mode

Introduction

The bootloader is stored in the internal boot ROM memory (system memory) of STM32 devices. It is programmed by ST during production. Its main task is to download the application program to the internal Flash memory through one of the available serial peripherals (USART, CAN, USB, I^2C, SPI, etc.). A communication protocol is defined for each serial interface, with a compatible command set and sequences. This document applies to the products listed in *Table 1*. They are referred as STM32 throughout the document.

This application note describes the supported peripherals and hardware requirements to be considered when using the bootloader of STM32 devices. However the specifications of the low-level communication protocol for each supported serial peripheral are documented in separate documents as referred in *Section 2: Related documents*.

Table 1. Applicable products

Type	Part number or product series	
Microcontrollers	STM32F0 Series:	STM32F03xxx, STM32F04xxx, STM32F05xxx, STM32F07xxx, STM32F09xxx
	STM32F1 Series.	
	STM32F2 Series.	
	STM32F3 Series:	STM32F301xx, STM32F302xx, STM32F303xx, STM32F318xx, STM32F328xx, STM32F334xx, STM32F358xx, STM32F373xx, STM32F378xx, STM32F398xx
	STM32F4 Series:	STM32F401xx, STM32F405xx, STM32F407xx, STM32F410xx, STM32F411xx, STM32F412xx, STM32F413xx, STM32F415xx, STM32F417xx, STM32F423xx, STM32F427xx, STM32F429xx, STM32F437xx, STM32F439xx, STM32F446xx, STM32F469xx, STM32F479xx
	STM32F7 Series:	STM32F722xx, STM32F723xx, STM32F732xx, STM32F733xx, STM32F745xx, STM32F746xx, STM32F756xx, STM32F765xx, STM32F767xx, STM32F769xx, STM32F777xx, STM32F779xx
	STM32G0 Series:	STM32G030xx, STM32G031xx, STM32G041xx, STM32G07xxx, STM32G08xxx
	STM32G4 Series:	STM32G431xx, STM32G441xx, STM32G47xxx, STM32G48xxx
	STM32H7 Series:	STM32H74xxx, STM32H75xxx, STM32H7A3xx, STM32H7B3xx
	STM32L0 Series.	
	STM32L1 Series:	STM32L100xx, STM32L151xx, STM32L152xx, STM32L162xx
	STM32L4 Series:	STM32L431xx, STM32L432xx, STM32L433xx, STM32L442xx, STM32L443xx, STM32L451xx, STM32L452xx, STM32L462xx, STM32L471xx, STM32L475xx, STM32L476xx, STM32L486xx, STM32L496xx, STM32L4A6xx, STM32L4R5xx, STM32L4R7xx, STM32L4R9xx, STM32L4S5xx, STM32L4S7xx, STM32L4S9xx, STM32L412xx, STM32L422xx, STM32L4P5xx, STM32L4Q5xx, STM32L431xx, STM32L432xx, STM32L433xx, STM32L442xx, STM32L443xx, STM32L451xx, STM32L452xx, STM32L462xx, STM32L471xx, STM32L475xx, STM32L476xx, STM32L486xx, STM32L496xx, STM32L4A6xx, STM32L4R5xx, STM32L4R7xx, STM32L4R9xx, STM32L4S5xx, STM32L4S7xx, STM32L4S9xx, STM32L412xx, STM32L422xx, STM32L4P5xx, STM32L4Q5xx
	STM32L5 Series:	STM32L552xx, STM32L562xx
	STM32WB Series:	STM32WB50xx, STM32WB55xx
	STM32WL Series:	STM32WLE5xx

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1 General information

This document applied to Arm®-based devices.

Note: Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere

2 Related documents

For each supported product (listed in *Table 1*), please refer to the following documents available from *www.st.com*:

- Datasheet or databrief
- Reference manual
- Application Note:
  - AN3154: CAN protocol used in the STM32 bootloader
  - AN3155: USART protocol used in the STM32 bootloader
  - AN3156: USB DFU protocol used in the STM32 bootloader
  - AN4221: I2C protocol used in the STM32 bootloader
  - AN4286: SPI protocol used in the STM32 bootloader
  - AN5405: FDCAN protocol used in the STM32 bootloader

3 Glossary

F0 Series:

STM32F03xxx is used to refer to STM32F030x4, STM32F030x6, STM32F038x6, STM32F030xC, STM32F031x4 and STM32F031x6 devices.

STM32F04xxx is used to refer to STM32F042x4 and STM32F042x6 devices.

STM32F05xxx and STM32F030x8 devices is used to refer to STM32F051x4, STM32F051x6, STM32F051x8, STM32F058x8 and STM32F030x8 devices.

STM32F07xxx is used to refer to STM32F070x6, STM32F070xB, STM32F071xB STM32F072x8 and STM32F072xB devices.

STM32F09xxx is used to refer to STM32F091xx and STM32F098xx devices.

F1 Series:

STM32F10xxx is used to refer to Low-density, Medium-density, High-density, Low-density value line, Medium-density value line and High-density value line devices:

Low-density devices are STM32F101xx, STM32F102xx and STM32F103xx microcontrollers where the Flash memory density ranges between 16 and 32 Kbyte.

Medium-density devices are STM32F101xx, STM32F102xx and STM32F103xx microcontrollers where the Flash memory density ranges between 64 and 128 Kbyte.

High-density devices are STM32F101xx and STM32F103xx microcontrollers where the Flash memory density ranges between 256 and 512 Kbyte.

Low-density value line devices are STM32F100xx microcontrollers where the Flash memory density ranges between 16 and 32 Kbyte.

Medium-density value line devices are STM32F100xx microcontrollers where the Flash memory density ranges between 64 and 128 Kbyte.

High-density value line devices are STM32F100xx microcontrollers where the Flash memory density ranges between 256 and 5128 Kbyte.

STM32F105xx/107xx is used to refer to STM32F105xx and STM32F107xx devices.

STM32F10xxx XL-density is used to refer to STM32F101xx and STM32F103xx devices where the Flash memory density ranges between 768 Kbyte and 1 Mbyte.

F2 Series:

STM32F2xxxx is used to refer to STM32F215xx, STM32F205xx, STM32F207xx and SMT32F217xx devices.

F3 Series:

STM32F301xx/302x4(6/8) is used to refer to STM32F301x4, STM32F301x6, STM32F301x8, STM32F302x4, STM32F302x6 and STM32F302x8 devices.

STM32F302xB(C)/303xB(C) is used to refer to STM32F302xB, STM32F302xC, STM32F303xB and STM32F303xC devices.

STM32F302xD(E)/303xD(E) is used to refer to STM32F302xD, STM32F302xE, STM32F303xD and STM32F303xE devices.

STM32F303x4(6/8)/334xx/328xx is used to refer to STM32F303x4, STM32F303x6, STM32F303x8, STM32F334x4, STM32F334x6, STM32F334x8, and STM32F328x8 devices.

STM32F318xx is used to refer to STM32F318x8 devices.

STM32F358xx is used to refer to STM32F358xC devices.

STM32F373xx is used to refer to STM32F373x8, STM32F373xB and STM32F373xC devices.

STM32F378xx is used to refer to STM32F378xC devices.

STM32F398xx is used to refer to STM32F398xE devices.

F4 Series:

STM32F40xxx/41xxx is used to refer to STM32F405xx, STM32F407xx, STM32F415xx and SMT32F417xx devices.

STM32F401xB(C) is used to refer to STM32F401xB and STM32F401xC devices.

STM32F401xD(E) is used to refer to STM32F401xD and STM32F401xE devices.

STM32F410xx is used to refer to STM32F410x8 and STM32F410xB devices.

STM32F411xx is used to refer to STM32F411xD and STM32F411xE devices.

STM32F412xx is used to refer to STM32F412Cx, STM32F412Rx, STM32F412Vx and STM32F412Zx devices.

STM32F413xx/423xx is used to refer to STM32F413xG, STM32F413xH and STM32F423xH devices.

STM32F42xxx/43xxx is used to refer to STM32F427xx, STM32F429xx, STM32F437xx and STM32F439xx devices

STM32F446xx is used to refer to STM32F446xE and STM32F446xC devices

STM32F469xx/479xx is used to refer to STM32F469xE, STM32F469xG, STM32F469xI, STM32F479xG and STM32F479xI devices.

F7 Series:

STM32F72xxx/73xxx is used to refer to STM32F722xx, STM32F723xx, STM32F732xx and STM32F733xx devices.

STM32F74xxx/75xxx is used to refer to STM32F745xx, STM32F746xx and STM32F756xx devices.

STM32F76xxx/77xxx is used to refer to STM32F765xx, STM32F767xx, STM32F769xx, STM32F777xx and STM32F779xx devices.

G0 Series:

STM32G03xxx/04xxx is used to refer to STM32G03xxx and STM32G04xxx devices.

STM32G07xxx/08xxx is used to refer to STM32G07xxx and STM32G08xxx devices.

G4 Series:

STM32G431xx is used to refer to STM32G431xx devices.

STM32G441xx is used to refer to STM32G441xx devices.

STM32G47xxx is used to refer to STM32G471xx, STM32G473xx and STM32G474xx devices.

STM32G48xxx is used to refer to STM32G483xx and STM32G484xx devices.

H7 Series:

STM32H74xxx/75xxx is used to refer to STM32H74xxx and STM32H75xxx devices.

STM32H7A3xx/7B3xx *is used to refer to STM32H7A3xx/ STM32H7B3xx devices.*

L0 Series:

STM32L01xxx/02xxx is used to refer to STM32L011xx and STM32L021xx devices.

STM32L031xx/041xx is used to refer to STM32L031xx and STM32L041xx devices.

STM32L05xxx/06xxx is used to refer to STM32L051xx, STM32L052xx, STM32L053xx, STM32L062xx and STM32L063xx ultralow power devices.

STM32L07xxx/08xxx is used to refer to STM32L071xx, STM32L072xx, STM32L073xx, STM32L081xx, STM32L082xx and STM32L083xx devices

L1 Series:

STM32L1xxx6(8/B) is used to refer to STM32L1xxV6T6, STM32L1xxV6H6, STM32L1xxR6T6, STM32L1xxR6H6, STM32L1xxC6T6, STM32L1xxC6H6, STM32L1xxV8T6, STM32L1xxV8H6, STM32L1xxR8T6, STM32L1xxR8H6, STM32L1xxC8T6, STM32L1xxC8H6, STM32L1xxVBT6, STM32L1xxVBH6, STM32L1xxRBT6, STM32L1xxRBH6, STM32L1xxCBT6 and STM32L1xxCBH6 ultralow power devices.

STM32L1xxx6(8/B)A is used to refer to STM32L1xxV6T6-A, STM32L1xxV6H6-A, STM32L1xxR6T6-A, STM32L1xxR6H6-A, STM32L1xxC6T6-A, STM32L1xxC6H6-A, STM32L1xxV8T6-A, STM32L1xxV8H6-A, STM32L1xxR8T6-A, STM32L1xxR8H6-A, STM32L1xxC8T6-A, STM32L1xxC8H6-A, STM32L1xxVBT6-A, STM32L1xxVBH6-A, STM32L1xxRBT6-A, STM32L1xxRBH6-A, STM32L1xxCBT6-A and STM32L1xxCBH6-A ultralow power devices.

STM32L1xxxC is used to refer to STM32L1xxVCT6, STM32L1xxVCH6 , STM32L1xxRCT6, STM32L1xxUCY6, STM32L1xxCCT6 and STM32L1xxCCU6 ultralow power devices.

STM32L1xxxD is used to refer to STM32L1xxZDT6, STM32L1xxQDH6, STM32L1xxVDT6, STM32L1xxRDY6, STM32L1xxRDT6, STM32L1xxZCT6, STM32L1xxQCH6, STM32L1xxRCY6, STM32L1xxVCT6-A and STM32L1xxRCT6-A ultralow power devices.

STM32L1xxxE is used to refer to STM32L1xxZET6, STM32L1xxQEH6, STM32L1xxVET6, STM32L1xxVEY6, and STM32L1xxRET6 ultralow power devices.

L4 Series:

STM32L412xx/422xx is used to refer to STM32L412xB, STM32L412x8, STM32L422xB devices.

STM32L43xxx/44xxx is used to refer to STM32L431xx, STM32L432xx, STM32L433xx and STM32L442xx and STM32L443xx devices.

STM32L45xxx/46xxx is used to refer to STM32L451xx, STM32L452xx and STM32L462xx devices.

STM32L47xxx/48xxx is used to refer to STM32L471xx, STM32L475xx, STM32L476xx and STM32L486xx devices.

STM32L496xx/4A6xx is used to refer to STM32L496xE, STM32L496xG and STM32L4A6xG devices.

STM32L4Rxxx/4Sxxx is used to refer to STM32L4R5xx, STM32L4R7xx, STM32L4R9xx, STM32L4S5xx, STM32L4S7xx and STM32L4S9xx devices.

STM32L4P5xx/4Q5xx is used to refer to STM32L4P5xx/STM32L4Q5xx devices.

L5 Series:

STM32L552xx is used to refer to STM32L552xx devices.

STM32L562xx is used to refer to STM32L562xx devices.

WB Series:

STM32WB50xx is used to refer to STM32WB50xx devices.

STM32WB55xx is used to refer to STM32WB55Cx, STM32WB55Rx, STM32WB55Vx devices.

WL Series:

STM32WLE5xx is used to refer to STM32WLE5JC, STM32WLE5JB and STM32WLE5J8 devices.

Note: *BL_USART_Loop refers to the USART bootloader execution loop.*
BL_CAN_Loop refers to the CAN bootloader execution loop.
BL_I2C_Loop refers to the I2C bootloader execution loop.
BL_SPI_Loop refers to the SPI bootloader execution loop.

4 General bootloader description

4.1 Bootloader activation

The bootloader is activated by applying one of the patterns described in *Table 2: Bootloader activation patterns*.

If Boot From Bank2 option is activated (for products supporting this feature), bootloader executes Dual Boot mechanism as described in figures "Dual Bank Boot Implementation for STM32xxxx" where STM32xxxx is the relative STM32 product.

Otherwise, bootloader selection protocol is executed as described in figures "Bootloader VY.x selection for STM32xxxx" where STM32xxxx is the relative STM32 product.

When readout protection Level2 is activated, STM32 does not boot on system memory in any case and bootloader can't be executed (unless jumping to it from Flash user code, all commands are not accessible except Get, GetID, and GetVersion).

Table 2. Bootloader activation patterns

Patterns	Condition
Pattern1	Boot0(pin) = 1 and Boot1(pin) = 0
Pattern2	Boot0(pin) = 1 and nBoot1(bit) = 1
Pattern3	Boot0(pin) = 1, Boot1(pin) = 0 and BFB2(bit) = 1
	Boot0(pin) = 0, BFB2(bit) = 0 and both banks don't contain valid code
	Boot0(pin) = 1, Boot1(pin) = 0, BFB2(bit) = 0 and both banks don't contain valid code
Pattern4	Boot0(pin) = 1, Boot1(pin) = 0 and BFB2(bit) = 1
	Boot0(pin) = 0, BFB2(bit) = 0 and both banks don't contain valid code
	Boot0(pin) = 1, Boot1(pin) = 0 and BFB2(bit) = 0
Pattern5	Boot0(pin) = 1, Boot1(pin) = 0 and BFB2(bit) = 0
	Boot0(pin) = 0, BFB2(bit) = 1 and both banks don't contain valid code
	Boot0(pin) = 1, Boot1(pin) = 0 and BFB2 (bit) = 1
Pattern6	Boot0(pin) = 1, nBoot1(bit) = 1 and nBoot0_SW(bit) = 1
	nBoot0(bit) = 0, nBoot1(bit) = 1 and nBoot0_SW(bit) = 0
	Boot0(pin) = 0, nBoot0_SW(bit) = 1 and main flash empty
	nBoot0(bit) = 1, nBoot0_SW(bit)=0 and main flash empty
Pattern7	Boot0(pin) = 1, nBoot1(bit) = 1 and BFB2(bit) = 0
	Boot0(pin) = 0, BFB2(bit) = 1 and both banks don't contain valid code
	Boot0(pin) = 1, nBoot1(bit) = 1 and BFB2(bit) = 1
Pattern8	Boot(pin) = 0 and BOOT_ADD0(optionbyte) = 0x0040
	Boot(pin) = 1 and BOOT_ADD1(optionbyte) = 0x0040

Table 2. Bootloader activation patterns (continued)

Patterns	Condition
Pattern9	nDBANK(bit) = 1, Boot(pin) = 0 and BOOT_ADD0(optionbyte) = 0x0040
	nDBANK(bit) = 1, Boot(pin) = 1 and BOOT_ADD1(optionbyte) = 0x0040
	nDBANK(bit) = 0, nDBOOT(bit) = 1, Boot(pin) = 0 and BOOT_ADD0(optionbyte) = 0x0040
	nDBANK(bit) = 0, nDBOOT(bit) = 1, Boot(pin) = 1 and BOOT_ADD1(optionbyte) = 0x0040
	nDBANK(bit) = 0, nDBOOT(bit) = 0, BOOT_ADDx(optionbyte) out of memory range or in ICP memory range
	nDBANK(bit) = 0, nDBOOT(bit) = 0, BOOT_ADDx(optionbyte) in Flash memory range and both banks don't contain valid code
Pattern10	Boot(pin) = 0 and BOOT_ADD0(optionbyte) = 0x1FF0
	Boot(pin) = 1 and BOOT_ADD1(optionbyte) = 0x1FF0
Pattern 11	nBoot0(bit) = 0, nBoot1(bit) = 1, nBOOT0_SEL(bit) = 1 and BOOT_LOCK(bit) = 0
	Boot0(pin) = 1, nBoot1(bit) = 1 and nBOOT0_SEL (bit) = 1
	nBoot0(bit) = 1, nBOOT0_SEL(bit) = 1, BOOT_LOCK(bit) = 0 and main Flash memory empty
	Boot0(pin) = 0, nBOOT0_SEL(bit) = 0, BOOT_LOCK(bit) = 0 and main Flash memory empty
	BOOT_LOCK(bit) = 1 and main flash empty
Pattern 12	TZen = 0, Boot0(pin) = 0, nSWBoot0(bit) = 1 and NSBOOTADD0 [24:0] = 0x017F200
	TZen = 0, Boot0(pin) = 1, nSWBoot0 (bit) = 1 and NSBOOTADD1 [24:0] = 0x017F200
	TZen = 0, nBoot0(bit) = 0, nSWBoot0 (bit) = 0 and NSBOOTADD1 [24:0] = 0x017F200
	TZen = 0, nBoot0(bit) = 1, nSWBoot0 (bit) = 0 and NSBOOTADD0 [24:0] = 0x017F200
	TZen = 1, Boot0(pin) = 0, nSWBoot0 (bit) = 1 and SECBOOTADD0 [24:0] = 0x01FF000 & RSSCMD = 0
	TZen = 1, Boot0(pin) = 1, nSWBoot0 (bit) = 1 & RSSCMD = 0, BOOT_LOCK=0 or (BOOT_LOCK = 1 and SECBOOTADD0 [24:0] = 0x01FF000)
	TZen = 1, nBoot0(bit) = 1, nSWBoot0 (bit) = 0 and SECBOOTADD0 [24:0] = 0x01FF000 & RSSCMD = 0, BOOT_LOCK=0 or (BOOT_LOCK = 1 and SECBOOTADD0 [24:0] = 0x01FF000)
	TZen = 1, nBoot0(bit) = 0, nSWBoot0 (bit) = 0 & RSSCMD = 0, BOOT_LOCK=0 or BOOT_LOCK = 1 and SECBOOTADD1 [24:0] = 0x01FF000
	TZen = 1, RSSCMD = 0x1C0, BOOT_LOCK=0 or (BOOT_LOCK = 1 and SECBOOTADD0 [24:0] = 0x01FF000)

Table 2. Bootloader activation patterns (continued)

Patterns	Condition
Pattern13	nBoot0(bit) = 0, nBoot1(bit) = 1 and nSWBoot0(bit) = 0
	nBoot0(bit) = 1, nBoot1(bit) = 1, nSWBoot0(bit) = 0 and user Flash empty
	nBoot1(bit) = 1, nSWBoot0(bit) = 1 and Boot0(pin) = 1
	nBoot1(bit) = 1, nSWBoot0(bit) = 1, Boot0(pin) = 0 and user Flash empty
Pattern14	BOOT_LOCK(bit) = 0, nBoot1(bit) = 1, Boot0(pin) = 1 and nSWBoot0(bit) = 1
	BOOT_LOCK(bit) = 0, nBoot1(bit) = 1, Boot0(pin) = 0 and nSWBoot0(bit) = 0
	BOOT_LOCK(bit) = 0, Boot0(pin) = 0, nSWBoot0(bit) = 1 and both banks don't contain valid code
	BOOT_LOCK(bit) = 0, Boot0(pin) = 1, nSWBoot0(bit) = 0 and both banks don't contain valid code
Pattern15	Boot0(pin) = 1, nBoot1(bit) = 1 and nBoot0_SW(bit) = 1
	nBoot0(bit) = 0, nBoot1(bit) = 1 and nBoot0_SW(bit) = 0

In addition to patterns described above, user can execute bootloader by performing a jump to system memory from user code. Before jumping to bootloader user must:

- Disable all peripheral clocks
- Disable used PLL
- Disable interrupts
- Clear pending interrupts

System memory boot mode can be exited by getting out from bootloader activation condition and generating hardware reset or using Go command to execute user code.

Note: If you choose to execute the Go command, the peripheral registers used by the bootloader are not initialized to their default reset values before jumping to the user application. They should be reconfigured in the user application if they are used. So, if the IWDG is being used in the application, the IWDG prescaler value has to be adapted to meet the requirements of the application (since the prescaler was set to its maximum value). For some products, not all reset values are set. For more information please refer to the known limitations detailed for each product's bootloader versions.

Note: For STM32 devices having the Dual Bank Boot feature, in order to jump to system memory from user code, the user has first to remap the System Memory bootloader at address 0x00000000 using SYSCFG register (except for STM32F7 series), then jump to bootloader. For STM32F7 series, the user has to disable nDBOOT and/or nDBANK features (in option bytes), then jump to bootloader.

Note: For STM32 devices embedding bootloader using the DFU/CAN interface in which the external clock source (HSE) is required for DFU/CAN operations, the detection of the HSE value is done dynamically by the bootloader firmware and is based on the internal oscillator clock (HSI, MSI).
Thus, when due to temperature or other conditions, the internal oscillator precision is altered above the tolerance band (1% around the theoretical value), the bootloader might calculate a wrong HSE frequency value.
In this case, the bootloader DFU/CAN interfaces might dysfunction or might not work at all.

4.2 Bootloader identification

Depending on the STM32 device used, the bootloader may support one or more embedded serial peripherals used to download the code to the internal Flash memory. The bootloader identifier (ID) provides information about the supported serial peripherals.

For a given STM32 device, the bootloader is identified by means of the:

1. **Bootloader (protocol) version**: version of the serial peripheral (USART, CAN, USB, etc.) communication protocol used in the bootloader. This version can be retrieved using the bootloader Get Version command.
2. **Bootloader identifier (ID)**: version of the STM32 device bootloader, coded on one byte in the **0xXY** format**,** where:
   - **X** specifies the embedded serial peripheral(s) used by the device bootloader:
     X = 1: one USART is used
     X = 2: two USARTs are used
     X = 3: USART, CAN and DFU are used
     X = 4: USART and DFU are used
     X = 5: USART and I^2C are used
     X = 6: I^2C is used
     X = 7: USART, CAN, DFU and I^2C are used
     X = 8: I^2C and SPI are used
     X = 9: USART, CAN (or FDCAN), DFU, I^2C and SPI are used
     X = 10: USART, DFU and I^2C are used
     X = 11: USART, I^2C and SPI are used
     X = 12: USART and SPI are used
     X = 13: USART, DFU, I^2C and SPI are used
   - **Y** specifies the device bootloader version
     Let us take the example of a bootloader ID equal to 0x10. This means that it is the first version of the device bootloader that uses only one USART.
     The bootloader ID is programmed in the last byte address - 1 of the device system memory and can be read by using the bootloader “Read memory” command or by direct access to the system memory via JTAG/SWD.

Note: The bootloader ID format is applied to all STM32 devices families except the STM32F1xx family. The bootloader version for the STM32F1xx applies only to the embedded device’s bootloader version and not to its supported protocols.

The table below provides identification information about the bootloaders embedded in STM32 devices.

Table 3. Embedded bootloaders

STM32 series	Device		Supported serial peripherals	Bootloader ID		Bootloader (protocol) version
				ID	Memory location	
F0	STM32F05xxx/STM32F030x8 devices		USART1/USART2	0x21	0x1FFFF7A6	USART (V3.1)
	STM32F03xx4/6		USART1	0x10	0x1FFFF7A6	USART (V3.1)
	STM32F030xC		USART1/I2C1	0x52	0x1FFFF796	USART (V3.1) I2C1(V1.0)
	STM32F04xxx		USART1/USART2/ I2C1/ DFU (USB Device FS)	0xA1	0x1FFFF6A6	USART (V3.1) DFU (V2.2) I2C (V1.0)
	STM32F071xx/072xx		USART1/USART2/ I2C1/ DFU (USB Device FS)	0xA1	0x1FFFF6A6	USART (V3.1) DFU (V2.2) I2C (V1.0)
F0	STM32F070x6		USART1/USART2/ DFU (USB Device FS)/I2C1	0xA2	0x1FFFF6A6	USART (V3.1) DFU (V2.2) I2C (V1.0)
	STM32F070xB		USART1/USART2/ DFU (USB Device FS)/I2C1	0xA3	0x1FFFF6A6	USART (V3.1) DFU (V2.2) I2C (V1.0)
	STM32F09xxx		USART1/USART2/ I2C1	0x50	0x1FFFF796	USART (V3.1) I2C (V1.0)
F1	STM32F10xxx	Low-density	USART1	NA	NA	USART (V2.2)
		Medium-density	USART1	NA	NA	USART (V2.2)
		High-density	USART1	NA	NA	USART (V2.2)
		Medium-density value line	USART1	0x10	0x1FFFF7D6	USART (V2.2)
		High-density value line	USART1	0x10	0x1FFFF7D6	USART (V2.2)
	STM32F105xx/107xx		USART1 / USART2 (remapped) / CAN2 (remapped) / DFU (USB Device)	NA	NA	USART (V2.2[1]) CAN (V2.0) DFU(V2.2)
	STM32F10xxx XL-density		USART1/USART2 (remapped)	0x21	0x1FFFF7D6	USART (V3.0)
F2	STM32F2xxxx		USART1/USART3	0x20	0x1FFF77DE	USART (V3.0)
			USART1/USART3/ CAN2/ DFU (USB Device FS)	0x33	0x1FFF77DE	USART (V3.1) CAN (V2.0) DFU (V2.2)

Table 3. Embedded bootloaders (continued)

STM32 series	Device	Supported serial peripherals	Bootloader ID		Bootloader (protocol) version
			ID	Memory location	
F3	STM32F373xx	USART1/USART2/ DFU (USB Device FS)	0x41	0x1FFFF7A6	USART (V3.1) DFU (V2.2)
	STM32F378xx	USART1/USART2/ I2C1	0x50	0x1FFFF7A6	USART (V3.1) I2C (V1.0)
	STM32F302xB(C)/303xB(C)	USART1/USART2/ DFU (USB Device FS)	0x41	0x1FFFF796	USART (V3.1) DFU (V2.2)
	STM32F358xx	USART1/USART2/ I2C1	0x50	0x1FFFF796	USART (V3.1) I2C (V1.0)
	STM32F301xx/302x4(6/8)	USART1/USART2/ DFU (USB Device FS)	0x40	0x1FFFF796	USART (V3.1) DFU (V2.2)
	STM32F318xx	USART1/USART2/ I2C1/ I2C3	0x50	0x1FFFF796	USART (V3.1) I2C (V1.0)
	STM32F302xD(E)/303xD(E)	USART1/USART2/ DFU (USB Device FS)	0x40	0x1FFFF796	USART (V3.1) DFU (V2.2)
	STM32F303x4(6/8)/334xx/328xx	USART1/USART2/ I2C1	0x50	0x1FFFF796	USART (V3.1) I2C (V1.0)
	STM32F398xx	USART1/USART2/ I2C1/I2C3	0x50	0x1FFFF796	USART (V3.1) I2C (V1.0)

Table 3. Embedded bootloaders (continued)

STM32 series	Device	Supported serial peripherals	Bootloader ID		Bootloader (protocol) version
			ID	Memory location	
F4	STM32F40xxx/41xxx	USART1/USART3/ CAN2/ DFU (USB Device FS)	0x31	0x1FFF77DE	USART (V3.1) CAN (V2.0) DFU (V2.2)
		USART1/USART3/ CAN2 / DFU (USB Device FS) /I2C1/I2C2/I2C3/SPI1/SPI2	0x90	0x1FFF77DE	USART (V3.1) CAN (V2.0) DFU (V2.2) SPI(V1.1) I2C (V1.0)
	STM32F42xxx/43xxx	USART1/USART3/ CAN2 /DFU (USB Device FS) / I2C1	0x70	0x1FFF76DE	USART (V3.1) CAN (V2.0) DFU (V2.2) I2C (V1.0)
		USART1/USART3/ CAN2 / DFU (USB Device FS) / I2C1/I2C2/I2C3/SPI1/ SPI2/ SPI4	0x91	0x1FFF76DE	USART (V3.1) CAN (V2.0) DFU (V2.2) SPI(V1.1) I2C (V1.0)
	STM32F401xB(C)	USART1/USART2/ DFU (USB Device FS)/ I2C1/I2C2/I2C3/ SPI1/SPI2/ SPI3	0xD1	0x1FFF76DE	USART (V3.1) DFU (V2.2) SPI(V1.1) I2C (V1.0)
	STM32F401xD(E)	USART1/USART2/ DFU (USB Device FS)/ I2C1/I2C2/I2C3/ SPI1/SPI2/ SPI3	0xD1	0x1FFF76DE	USART (V3.1) DFU (V2.2) SPI(V1.1) I2C (V1.1)
	STM32F410xx	USART1/USART2/ I2C1/I2C2/I2C4 SPI1/SPI2	0xB1	0x1FFF76DE	USART (V3.1) I2C (V1.2) SPI (V1.1)
	STM32F411xx	USART1/USART2/ DFU (USB Device FS)/ I2C1/I2C2/I2C3/ SPI1/SPI2/ SPI3	0xD0	0x1FFF76DE	USART (V3.1) DFU (V2.2) SPI(V1.1) I2C (V1.1)
	STM32F412xx	USART1/USART2/ USART3/CAN2/ DFU (USB Device FS)/ I2C1/I2C2/I2C3/I2C4/ SPI1/SPI3/SPI4	0x91	0x1FFF76DE	USART (V3.1) CAN (V2.0) DFU (V2.2) SPI (V1.1) I2C (V1.2)
	STM32F413xx/423xx	USART1/USART2/ USART3/CAN2/ DFU (USB Device FS)/ I2C1/I2C2/I2C3/I2C4/ SPI1/SPI3/SPI4	0x90	0x1FFF76DE	USART (V3.1) CAN (V2.0) DFU (V2.2) I2C (V1.2) SPI (V1.1)
	STM32F446xx	USART1/USART3/ CAN2 / DFU (USB Device FS) / I2C1/I2C2/I2C3/SPI1/ SPI2/ SPI4	0x90	0x1FFF76DE	USART (V3.1) CAN (V2.0) DFU (V2.2) SPI(V1.1) I2C (V1.2)

Table 3. Embedded bootloaders (continued)

STM32 series	Device	Supported serial peripherals	Bootloader ID		Bootloader (protocol) version
			ID	Memory location	
F4	STM32F469xx/479xx	USART1/USART3/ I2C1/I2C2/I2C3/ CAN2/ DFU (USB Device FS)/ SPI1/ SPI2/ SPI4	0x90	0x1FFF76DE	USART (V3.1) I2C (V1.2) CAN (V2.0) DFU (V2.2) SPI (V1.1)
F7	STM32F72xxx/73xxx	USART1/USART3/ CAN1/ DFU (USB Device FS)/ I2C1/I2C2/I2C3/ SPI1/SPI2/SPI4	0x90	0x1FF0EDBE	USART (V3.1) CAN (V2.0) DFU (V2.2) I2C (V1.2) SPI (V1.2)
	STM32F74xxx/75xxx	USART1/USART3/ I2C1/I2C2/I2C3/ CAN2/ DFU (USB Device FS)	0x70	0x1FF0EDBE	USART (V3.1) I2C (V1.2) CAN (V2.0) DFU (V2.2)
		USART1/USART3/ I2C1/I2C2/I2C3/ CAN2/ DFU (USB Device FS)/ SPI1/SPI2/SPI4	0x90	0x1FF0EDBE	USART (V3.1) I2C (V1.2) CAN (V2.0) DFU (V2.2) SPI (V1.2)
	STM32F76xxx/77xxx	USART1/USART3/ CAN2/ DFU (USB Device FS)/ I2C1/I2C2/I2C3/ SPI1/SPI2/SPI4	0x93	0x1FF0EDBE	USART (V3.1) CAN (V2.0) DFU (V2.2) I2C (V1.2) SPI (V1.2)
G0	STM32G07xxx/08xxx	USART1/USART2/ USART3/I2C1/I2C2/ SPI1/SPI2	0xB2	0x1FFF6FFE	USART (V3.1) I2C (V1.2) SPI (V1.1)
	STM32G03xxx/04xxx	USART1/USART2/ I2C1\I2C2	0x53	0x1FFF1FFE	USART (V3.1) I2C (V1.2)
G4	STM32G431xx/441xx	USART1/USART2/USART3 I2C2/I2C3 SPI1/SPI2 DFU (USB Device FS)	0xD3	0x1FFF6FFE	USART (V3.1) I2C (V1.2) SPI (V1.1) DFU (V2.2)
	STM32G47xxx/48xxx	USART1/USART2/USART3 I2C2/I2C3/I2C4 SPI1/SPI2 DFU (USB Device FS)	0xD4	0x1FFF6FFE	USART (V3.1) I2C (V1.2) SPI (V1.1) DFU (V2.2)

Table 3. Embedded bootloaders (continued)

STM32 series	Device	Supported serial peripherals	Bootloader ID		Bootloader (protocol) version
			ID	Memory location	
H7	STM32H74xxx/75xxx	USART1/USART2/ USART3 I2C1/I2C2/I2C3/ DFU (USB Device FS)/ SPI1/SPI2/SPI3/SPI4/ FDCAN1	0x90	0x1FF1E7FE	USART (V3.1) I2C (V1.1) DFU (V2.2) SPI (V1.2) FDCAN (V1.0)
	STM32H7A3xx/B3xx	USART1/USART2/ USART3 I2C1/I2C2/I2C3/ DFU (USB Device FS)/ SPI1/SPI2/SPI3/SPI4/ FDCAN1	0x90	0x1FF13FFE	USART (V3.1) I2C (V1.1) DFU (V2.2) SPI (V1.2) FDCAN (V1.0)
L0	STM32L01xxx/02xxx	USART2/SPI1	0xC3	0x1FF00FFE	USART (V3.1) SPI (V1.1)
	STM32L031xx/041xx	USART2/SPI1	0xC0	0x1FF00FFE	USART (V3.1) SPI (V1.1)
	STM32L05xxx/06xxx	USART1/USART2/SPI1/ SPI2	0xC0	0x1FF00FFE	USART (V3.1) SPI (V1.1)
	STM32L07xxx/08xxx	USART1/USART2/ DFU (USB Device FS)	0x41	0x1FF01FFE	USART (V3.1) DFU (V2.2)
		USART1/USART2/ SPI1/SPI2/ I2C1/I2C2	0xB2	0x1FF01FFE	USART (V3.1) SPI (V1.1) I2C (V1.2)
L1	STM32L1xxx6(8/B)	USART1/USART2	0x20	0x1FF00FFE	USART (V3.0)
	STM32L1xxx6(8/B)A	USART1/USART2	0x20	0x1FF00FFE	USART (V3.1)
	STM32L1xxxC	USART1/USART2/ DFU (USB Device FS)	0x40	0x1FF01FFE	USART (V3.1) DFU (V2.2)
	STM32L1xxxD	USART1/USART2/ DFU (USB Device FS)	0x45	0x1FF01FFE	USART (V3.1) DFU (V2.2)
	STM32L1xxxE	USART1/USART2/ DFU (USB Device FS)	0x40	0x1FF01FFE	USART (V3.1) DFU (V2.2)

Table 3. Embedded bootloaders (continued)

STM32 series	Device	Supported serial peripherals	Bootloader ID		Bootloader (protocol) version
			ID	Memory location	
L4	STM32L412xx/422xx	USART1/USART2/USART3 I2C1/I2C2/I2C3/ DFU (USB Device FS)/ SPI1/SPI2	0xD1	0x1FFF6FFE	USART (V3.1) I2C (V1.2) DFU (V2.2) SPI (V1.1)
	STM32L43xxx/44xxx	USART1/USART2/USART3/ I2C1/I2C2/I2C3/ CAN1/ DFU (USB Device FS)/ SPI1/SPI2	0x91	0x1FFF6FFE	USART (V3.1) I2C (V1.2) CAN (V2.0) DFU (V2.2) SPI (V1.1)
	STM32L45xxx/46xxx	USART1/USART2/USART3/ I2C1/I2C2/I2C3/ CAN1/ DFU (USB Device FS)/ SPI1/SPI2	0x92	0x1FFF6FFE	USART (V3.1) I2C (V1.2) CAN (V2.0) DFU (V2.2) SPI (V1.1)
	STM32L47xxx/48xxx	USART1/USART2/ USART3/ I2C1/I2C2/I2C3/ DFU (USB Device FS)	0xA3	0x1FFF6FFE	USART (V3.1) I2C (V1.2) DFU (V2.2)
		USART1/USART2/ USART3/ I2C/I2C2/I2C3/ SPI1/SPI2/CAN1/ DFU (USB Device FS)	0x92	0x1FFF6FFE	USART (V3.1) I2C (V1.2) SPI (V1.1) CAN(V2.0) DFU(V2.2)
	STM32L496xx/4A6xx	USART1/USART2/USART3/ I2C1/I2C2/I2C3/ CAN1/ DFU (USB Device FS)/ SPI1/SPI2	0x93	0x1FFF6FFE	USART (V3.1) I2C (V1.2) CAN (V2.0) DFU (V2.2) SPI (V1.1)
	STM32L4Rxxx/STM32L4Sxxx	USART1/USART2/USART3/ I2C1/I2C2/I2C3/ CAN1/ DFU (USB Device FS)/ SPI1/SPI2	0x95	0x1FFF6FFE	USART (V3.1) I2C (V1.2) CAN (V2.0) DFU (V2.2) SPI (V1.1)
	STM32L4P5xx /Q5xx	USART1/USART2/USART3 I2C1/I2C2/I2C3/ CAN1/ DFU (USB Device FS)/ SPI1/SPI2	0x90	0x1FFF6FFE	USART (V3.1) I2C (V1.2) CAN (V2.0) DFU (V2.2) SPI (V1.1)
L5	STM32L552xx/562xx	USART1/USART2/USART3 I2C1/I2C2/I2C3 SPI1/SPI2/SPI3 DFU (USB Device FS) FDCAN1	0x92	0x0BF97FFE	USART (V3.1) I2C (V1.2) SPI (V1.1) DFU (V2.2) FDCAN (V1.0)

Table 3. Embedded bootloaders (continued)

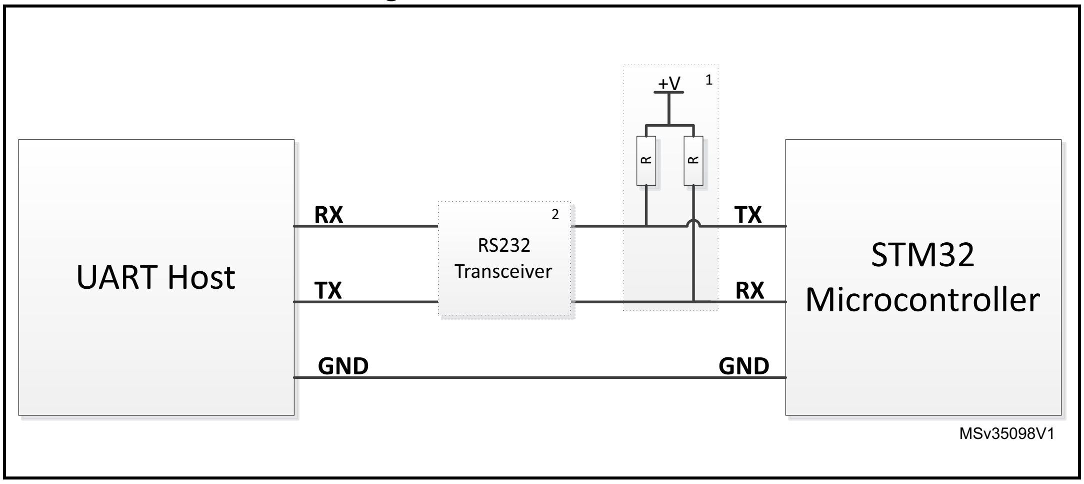
STM32 series	Device	Supported serial peripherals	Bootloader ID		Bootloader (protocol) version
			ID	Memory location	
WB	STM32WB50xx/55xx	USART1/ I2C1/I2C3 SPI1/SPI2 DFU (USB Device FS)	0xD5	0x1FFF6FFE	USART (V3.2) I2C (V1.2) SPI (V1.1) DFU (V2.2)
WL	STM32WLE5xx	USART1/USART2 SPI1/SPI2	0xC2	0x1FF36EFE	USART (V3.1) SPI (V1.1)

1. For connectivity line devices, the USART bootloader returns V2.0 instead of V2.2 for the protocol version. For more details please refer to the “STM32F105xx and STM32F107xx revision Z” errata sheet available from *http://www.st.com*.

4.3 Hardware connection requirements

To use the USART bootloader, the host has to be connected to the (RX) and (TX) pins of the desired USARTx interface via a serial cable.

Figure 1. USART Connection

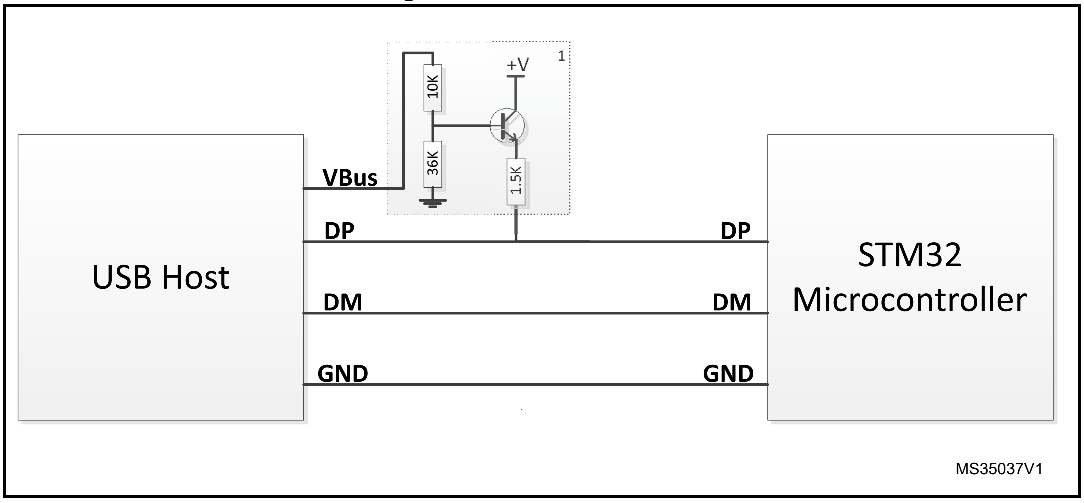


1. A Pull-UP resistor should be added, if pull-up resistor are not connected in host side.
2. An RS232 transceiver must be connected to adapt voltage level (3.3V - 12V) between STM32 device and host.

Note: +V typically 3.3 V and R value typically 100KOhm.This value depend on the application and the used hardware.

To use the DFU, connect the microcontroller's USB interface to a USB host (i.e. PC).

Figure 2. USB Connection

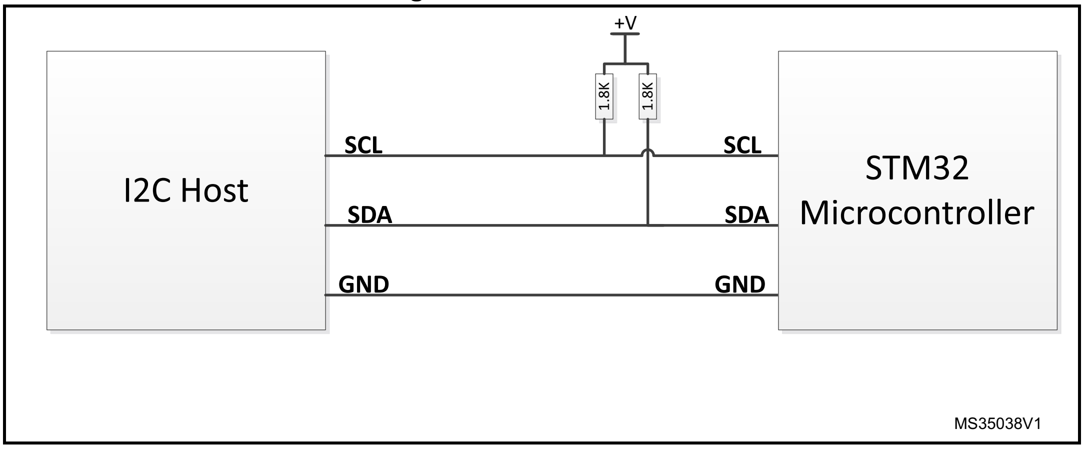


1. This additional circuit permits to connect a Pull-Up resistor to (DP) pin using VBus when needed. Refer to product section (Table which describes STM32 Configuration in system memory boot mode) to know if an external pull-up resistor must be connected to (DP) pin.

Note: +V typically 3.3 V.This value depends on the application and the used hardware.

To use the I2C bootloader, connect the host (master) and the desired I2Cx interface (slave) together via the data (SDA) and clock (SCL) pins. A 1.8 KOhm pull-up resistor has to be connected to both (SDA) and (SCL) lines.

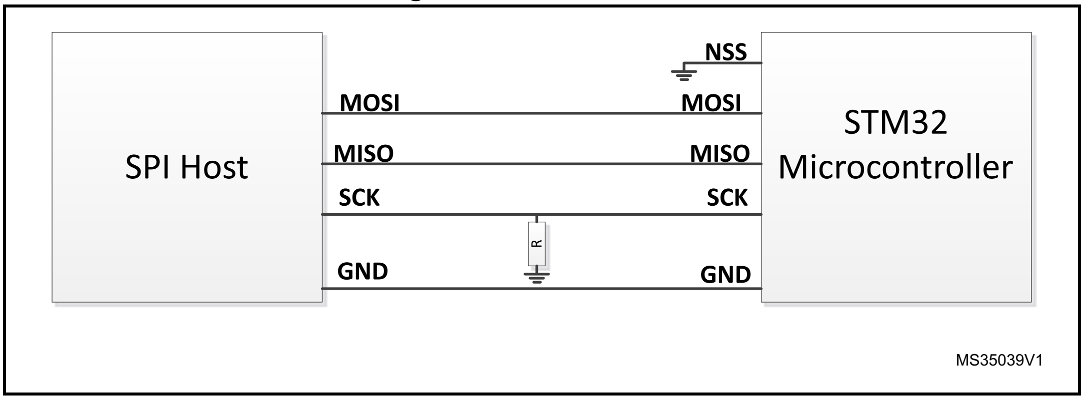
Figure 3. I2C Connection



Note: *+V typically 3.3 V.This value depends on the application and the used hardware.*

To use the SPI bootloader, connect the host (master) and the desired SPIx interface (slave) together via the (MOSI), (MISO) and (SCK) pins. The (NSS) pin must be connected to (GND). A pull-down resistor should be connected to the (SCK) line.

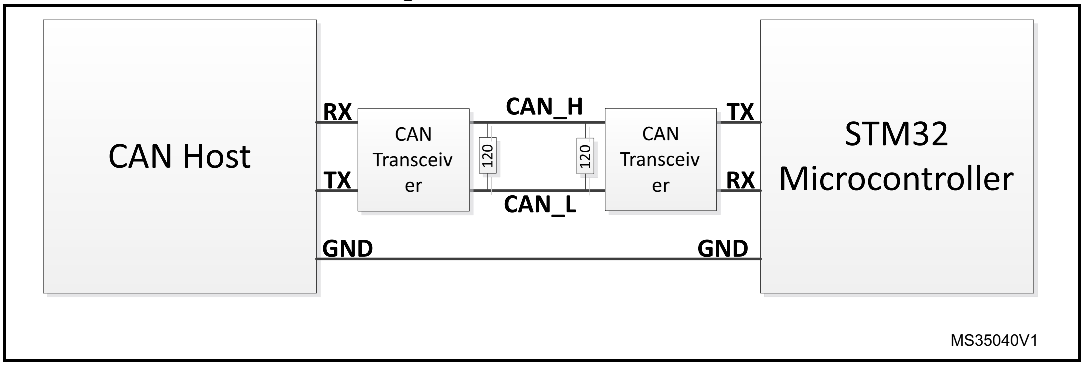
Figure 4. SPI Connection



Note: *R value typically 10KOhm. This value depends on the application and the used hardware.*

To use the CAN interface, the host has to be connected to the (RX) and (TX) pins of the desired CANx interface via CAN transceiver and a serial cable. A 120 Ohm resistor should be added as terminating resistor.

Figure 5. CAN Connection



Note: When a bootloader firmware supports DFU, it is mandatory that no USB Host is connected to the USB peripheral during the selection phase of the other interfaces. After selection phase, the user can plug a USB cable without impacting the selected bootloader execution except commands which generate a system reset.

It is recommended to keep the RX pins of unused bootloader interfaces (USART_RX, SPI_MOSI, CAN_RX and USB D+/D- lines if present) at a known (low or high) level at the startup of the bootloader (detection phase). Leaving these pins floating during the detection phase might lead to activating unused interface.

4.4 Bootloader memory management

All write operations using bootloader commands must only be Word-aligned (the address should be a multiple of 4). The number of data to be written must also be a multiple of 4 (non-aligned half page write addresses are accepted).

Some Products embed bootloader that has some specific features:

- Some products don't support Mass erase operation. To perform a mass erase operation using bootloader, two options are available:
  - Erase all sectors one by one using the Erase command
  - Set protection level to Level 1. Then, set it to Level 0 (using the Read protect command and then the Read Unprotect command). This operation results in a mass erase of the internal Flash memory.
- Bootloader firmware of STM32 L1 and L0 series supports Data Memory in addition to standard memories (internal Flash, internal SRAM, option bytes and System memory). The start address and the size of this area depends on product, please refer to product reference manual for more information. Data memory can be read and written but cannot be erased using the Erase Command. When writing in a Data memory location, the bootloader firmware manages the erase operation of this location before any write. A write to Data memory must be Word-aligned (address to be written should be a multiple of 4) and the number of data must also be a multiple of 4. To erase a Data memory location, you can write zeros at this location.
- Bootloader firmware of STM32 F2, F4, F7 and L4 series supports OTP memory in addition to standard memories (internal Flash, internal SRAM, option bytes and System memory). The start address and the size of this area depends on product, please refer to product reference manual for more information. OTP memory can be read and

written but cannot be erased using Erase command. When writing in an OTP memory location, make sure that the relative protection bit is not reset.

- For STM32 F2, F4 and F7 series the internal flash write operation format depends on voltage Range. By default write operation are allowed by one byte format (Half-Word, Word and Double-Word operations are not allowed). to increase the speed of write operation, the user should apply the adequate voltage range that allows write operation by Half-Word, Word or Double-Word and update this configuration on the fly by the bootloader software through a virtual memory location. This memory location is not physical but can be read and written using usual bootloader read/write operations according to the protocol in use. This memory location contains 4 bytes which are described in table below. It can be accessed by 1, 2, 3 or 4 bytes. However, reserved bytes should remain at their default values (0xFF), otherwise the request will be NACKed.

Table 4. STM32 F2, F4 and F7 Voltage Range configuration using bootloader

Address	Size	Description
0xFFFF0000	1 byte	This byte controls the current value of the voltage range. 0x00: voltage range [1.8 V, 2.1 V] 0x01: voltage range [2.1 V, 2.4 V] 0x02: voltage range [2.4 V, 2.7 V] 0x03: voltage range [2.7 V, 3.6 V] 0x04: voltage range [2.7 V, 3.6 V] and double word write/erase operation is used. In this case it is mandatory to supply 9 V through the VPP pin (refer to the product reference manual for more details about the double-word write procedure). Other: all other values are not supported and will be NACKed.
0xFFFF0001	1 byte	Reserved. 0xFF: default value. Other: all other values are not supported and will be NACKed.
0xFFFF0002	1 byte	Reserved. 0xFF: default value. Other: all other values are not supported and will be NACKed.
0xFFFF0003	1 byte	Reserved. 0xFF: default value. Other: all other values are not supported and will be NACKed.

The table below lists the valid memory area depending on the bootloader commands.

Table 5. Supported memory area by Write, Read, Erase and Go Commands

Memory Area	Write command	Read command	Erase command	Go command
Flash	Supported	Supported	Supported	Supported
RAM	Supported	Supported	Not supported	Supported
System Memory	Not supported	Supported	Not supported	Not supported
Data Memory	Supported	Supported	Not supported	Not supported
OTP Memory	Supported	Supported	Not supported	Not supported

4.5 Bootloader UART baudrate detection

For the UART interface baudrate detection, there are two types of mechanisms implemented on different STM32 devices:

- Software baudrate detection using internal HSI and timer (use GPIO as input, detect falling edge and rising edge as explained in AN3155).
  The devices using this mechanism are subject to software jitter (variable error of baudrate calculation) that can reach up to +/-5%.
  So, in that case, the host connecting to the STM32 bootloader UART interface shall support a deviation in baudrate equivalent to +/-5%.
  The software jitter value is variable and is different at each retry, so it is possible to use multiple retry connections in order to overcome the software jitter (connect and check for correct bootloader answer, if answer is not correct, reset the device and retry connection till correct answer received. Once correct answer received the rest of the communication not be impacted by software jitter).
  It is also possible to reduce software jitter by reducing baudrate value (ie. use 56000bps instead of 115200).
  Table 6 below provides the maximum software jitter value for the baudrate 115200bps. The lower the baudrate the lower will be the software jitter.
- Baudrate detection using UART auto-baudrate feature.The devices using this mechanism do not present any software jitter.

Table 6. Jitter software calculation on bootloader USART detection

Series	Baudrate detection methos	Maximum software jitter for 115200bps
STM32F0	Software Baudrate detection	-1%
STM32F1	Software Baudrate detection	-3%
STM32F2	Software Baudrate detection	-5%
STM32F3	Software Baudrate detection	-2%
STM32F4	Software Baudrate detection	-6%
STM32F7	Software Baudrate detection	-6%
STM32L0	Software Baudrate detection	-2%
STM32L1	Software Baudrate detection	-3%
STM32L4	Software Baudrate detection	-5%
STM32G07x/8x UART3 STM32G03x/4x UART2	Software Baudrate detection	-4%
STM32G07x/8x UART1/UART2 STM32G03x/4x UART1	Auto-baudrate	N/A
STM32G4	Auto-baudrate	N/A
STM32H7	Auto-baudrate	N/A
STM32WB	Auto-baudrate	N/A
STM32WL	Auto-baudrate	N/A

4.6 Flash Programming constraints:

When using bootloader interface to write in the flash memory, alignment on the programmed address shall be respected as following table.

If the address to which the write operation is not aligned, then it will fail and all program operations that are processed after it will also fail.

Table 7. Flash memory alignment constraints on STM32 products

Series	Alignment
STM32F0	4 bytes
STM32F1	4 bytes
STM32F2	4 bytes
STM32F3	4 bytes
STM32F4	4 bytes
STM32F7	8 bytes
STM32L0	8 bytes
STM32L1	8 bytes
STM32L4	8 bytes
STM32G0	4 bytes
STM32G4	4 bytes
STM32H7	8 bytes
STM32WB	8 bytes
STM32WL	8 bytes

Example of alignment:

4 Bytes: 0x08000014 is aligned and will pass, 0x08000012 is not aligned and will fail

8 Bytes: 0x08000010 is aligned and will pass, 0x08000014 is not aligned and will fail

Note: On some products (STM32F4 and STM32F7 only), it is possible to change the alignment constraint by writing in the device feature space.

4.7 "ExitSecureMemory" feature

The securable memory area is used to isolate secure boot code/data, which manipulate sensitive information (secrets) from application code:

- Access is controlled by a securable memory bit SEC_PROT (write once), in the FLASH_CR register
- Executed once at boot then locked by writing the securable memory bit
  - The code protected: in the securable memory area is hidden until the next reset that unlocks the SEC_PROT bit
- Width (number of Flash memory pages) is defined through an option byte, SEC_SIZE, in the Flash memory FLASH_SEC_R register

The ExitSecureMemory is a software developed and hosted on the system memory. When the user boot code jump to it, the software allows setting the SEC_PROT bit to “1” and then jumping to the application code. The SEC_SIZE must be set to the needed value before jumping to the ExitSecureMemory function.

As shown in figure xx, two jump methods can be used by the customer:

Jump to the secure memory function without parameter

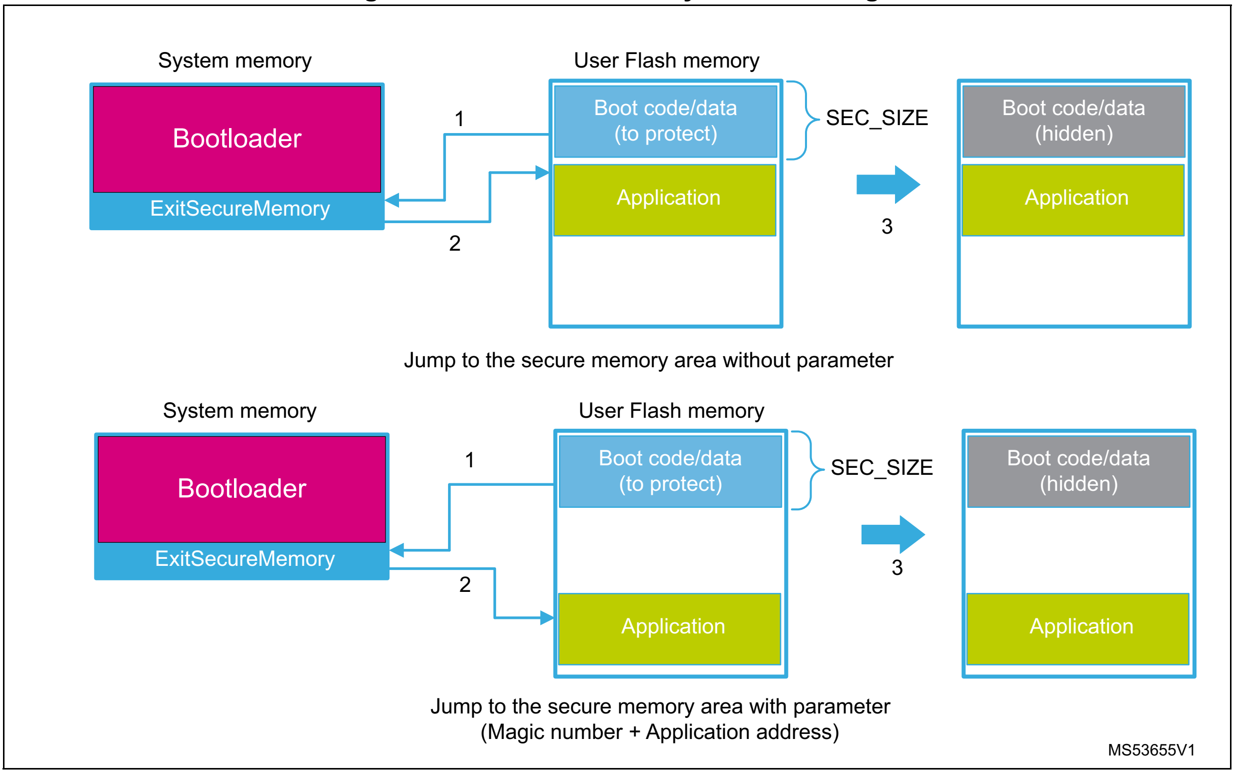
In this case the application must be loaded just after the secure memory defined.

Jump to the secure memory function using two parameters

1. Magic number
   - 0x08192A3C
     – Used to secure boot code/data in Flash and jump in case of a single bank product
     – Used to secure boot code/data in Bank1 and jump in case of a dual bank product
   - 0x08192A3D
     – Used to secure boot code/data and jump to application in Bank2 in case of a dual bank product
2. User address = Application address

- In this case the application can be loaded to any address we want (as per User address defined)

Figure 6. ExitSecureMemory function usage



Note: For more information regarding the option bytes configuration, refer to the used STM32 reference manual.

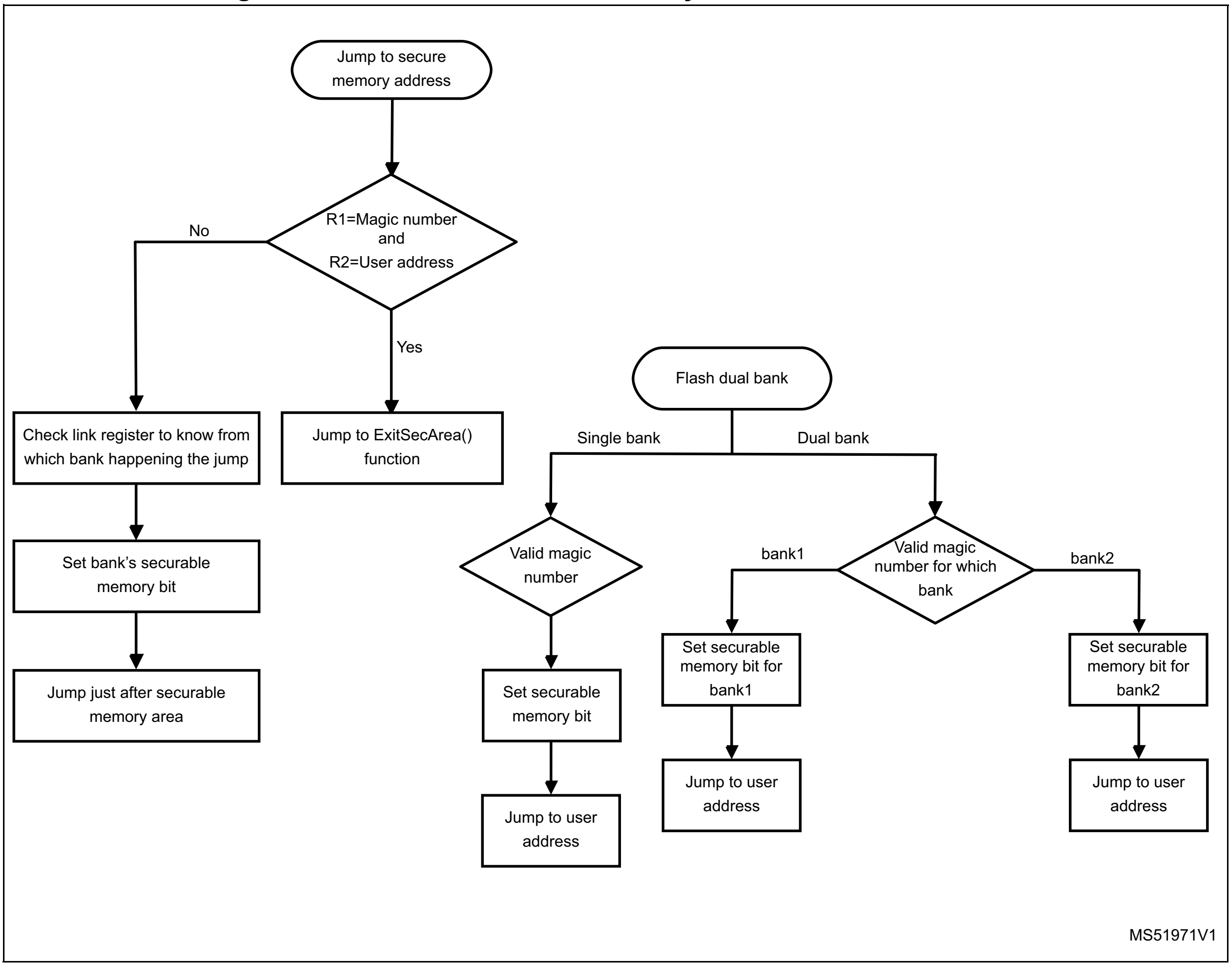
Note: An example of a function that can be used to call the "ExitSecureMemory" is added on the Appendix

Table 8. ExitSecureMemory entry address

STM32		ExitSecureMemory address
STM32G0	STM32G07xxx/08xxx	0x1FFF6800
	STM32G03xxx/04xxx	0x1FFF6800
STM32G4	STM32G47xxx/48xxx	0x1FFF6800
	STM32G431xx/441xx	0x1FFF6800

For more clarification checks the *Figure 7*.

Figure 7. Access to securable memory area from the bootloader



1. The Bootloader doesn't check on the integrity of the user address, it's up to the user to ensure the validity of the address to jump to.

5 STM32F03xx4/6 devices bootloader

5.1 Bootloader configuration

The STM32F03xx4/6 bootloader is activated by applying pattern2 (described in *Table 2: Bootloader activation patterns*). The following table shows the hardware resources used by this bootloader.

Table 9. STM32F03xx4/6 configuration in system memory boot mode

Bootloader	Feature/Peripheral	State	Comment
Common to all bootloaders	RCC	HSI Enabled	The system clock frequency is 24 MHz (using PLL clocked by HSI). 1 Flash Wait State.
	RAM	-	2 Kbyte starting from address 0x20000000 are used by the bootloader firmware.
	System memory	-	3 Kbyte starting from address 0x1FFFEC00 contain the bootloader firmware.
	IWDG	-	The independent watchdog (IWDG) prescaler is configured to its maximum value. It is periodically refreshed to prevent watchdog reset in case the hardware IWDG option was previously enabled by the user.
USART1 bootloader (on PA10/PA9)	USART1	Enabled	Once initialized, the USART1 configuration is 8 bits, even parity and 1 Stop bit.
	USART1_RX pin	Input	PA10 pin: USART1 in reception mode.
	USART1_TX pin	Output	PA9 pin: USART1 in transmission mode.
USART1 bootloader (on PA14/PA15)	USART1	Enabled	Once initialized, the USART1 configuration is 8 bits, even parity and 1 Stop bit.
	USART1_RX pin	Input	PA15 pin: USART1 in reception mode.
	USART1_TX pin	Output	PA14 pin: USART1 in transmission mode.
USART1 bootloaders	SysTick timer	Enabled	Used to automatically detect the serial baud rate from the host.

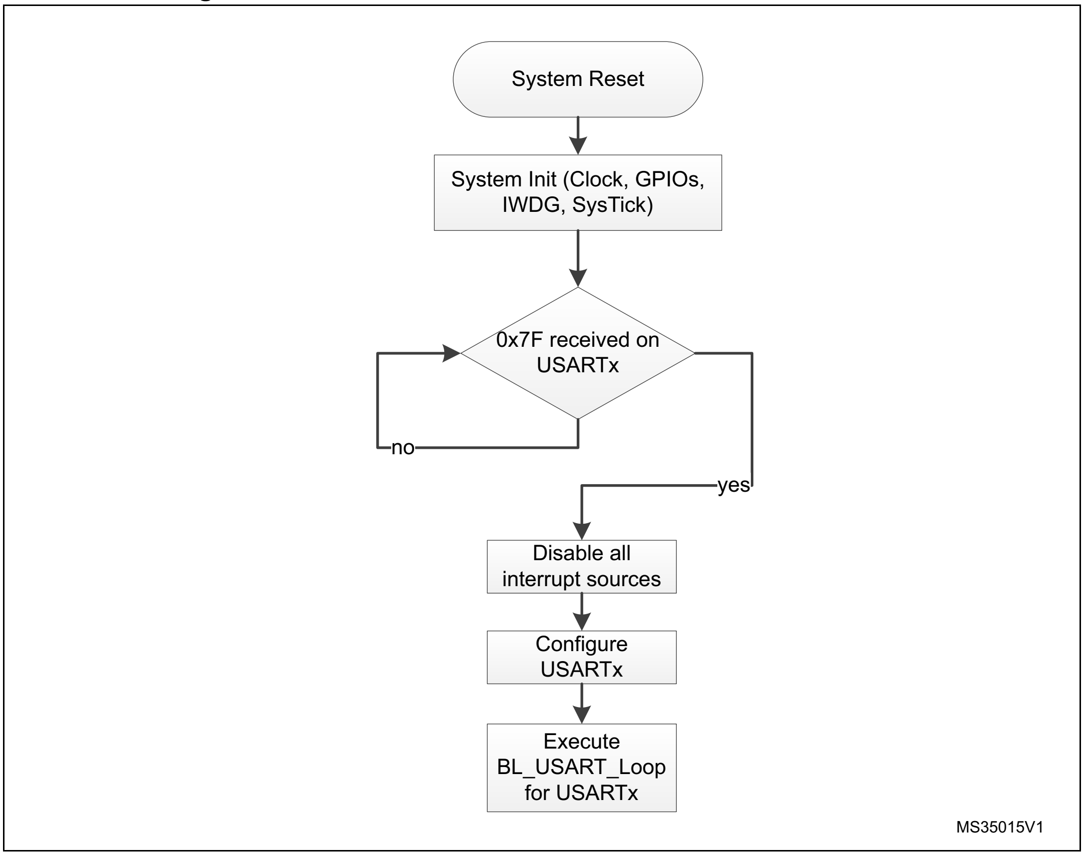
The system clock is derived from the embedded internal high-speed RC, no external quartz is required for the bootloader execution.

Note: After the STM32F03xx4/6 devices has booted in bootloader mode, serial wire debug (SWD) communication is no longer possible until the system is reset. This is because the SWD uses the PA14 pin (SWCLK) which is already used by the bootloader (USART1_TX).

5.2 Bootloader selection

The figure below shows the bootloader selection mechanism.

Figure 8. Bootloader selection for STM32F03xx4/6 devices



5.3 Bootloader version

The following table lists the STM32F03xx4/6 devices bootloader versions.

Table 10. STM32F03xx4/6 bootloader versions

Bootloader version number	Description	Known limitations
V1.0	Initial bootloader version	For the USART interface, two consecutive NACKs instead of 1 NACK are sent when a Read Memory or Write Memory command is sent and the RDP level is active.

6 STM32F030xC devices bootloader

6.1 Bootloader configuration

The STM32F030xC bootloader is activated by applying pattern2 (described in *Table 2: Bootloader activation patterns*). The following table shows the hardware resources used by this bootloader.

Table 11. STM32F030xC configuration in system memory boot mode

Bootloader	Feature/Peripheral	State	Comment
Common to all bootloaders	RCC	HSI enabled	The system clock frequency is 48 MHz with HSI 8 MHz as clock source.
	RAM	-	6 Kbyte starting from address 0x20000000 are used by the bootloader firmware
	System memory	-	8 Kbyte starting from address 0x1FFFD800, contain the bootloader firmware.
USART1 bootloader	USART1	Enabled	Once initialized the USART1 configuration is: 8-bits, even parity and 1 Stop bit
	USART1_RX pin	Input	PA10 pin: USART1 in reception mode
	USART1_TX pin	Output	PA9 pin: USART1 in transmission mode
USART2 bootloader	USART2	Enabled	Once initialized the USART2 configuration is: 8-bits, even parity and 1 Stop bit
	USART2_RX pin	Input	PA15 pin: USART2 in reception mode
	USART2_TX pin	Output	PA14 pin: USART2 in transmission mode
USARTx bootloaders	SysTick timer	Enabled	Used to automatically detect the serial baud rate from the host for USARTx bootloaders.
I2C1 bootloader	I2C1	Enabled	The I2C1 configuration is: I2C speed: up to 400 KHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b1000001x (where x = 0 for write and x = 1 for read)
	I2C1_SCL pin	Input/Output	PB6 pin: clock line is used in open-drain mode.
	I2C1_SDA pin	Input/Output	PB7 pin: data line is used in open-drain mode.

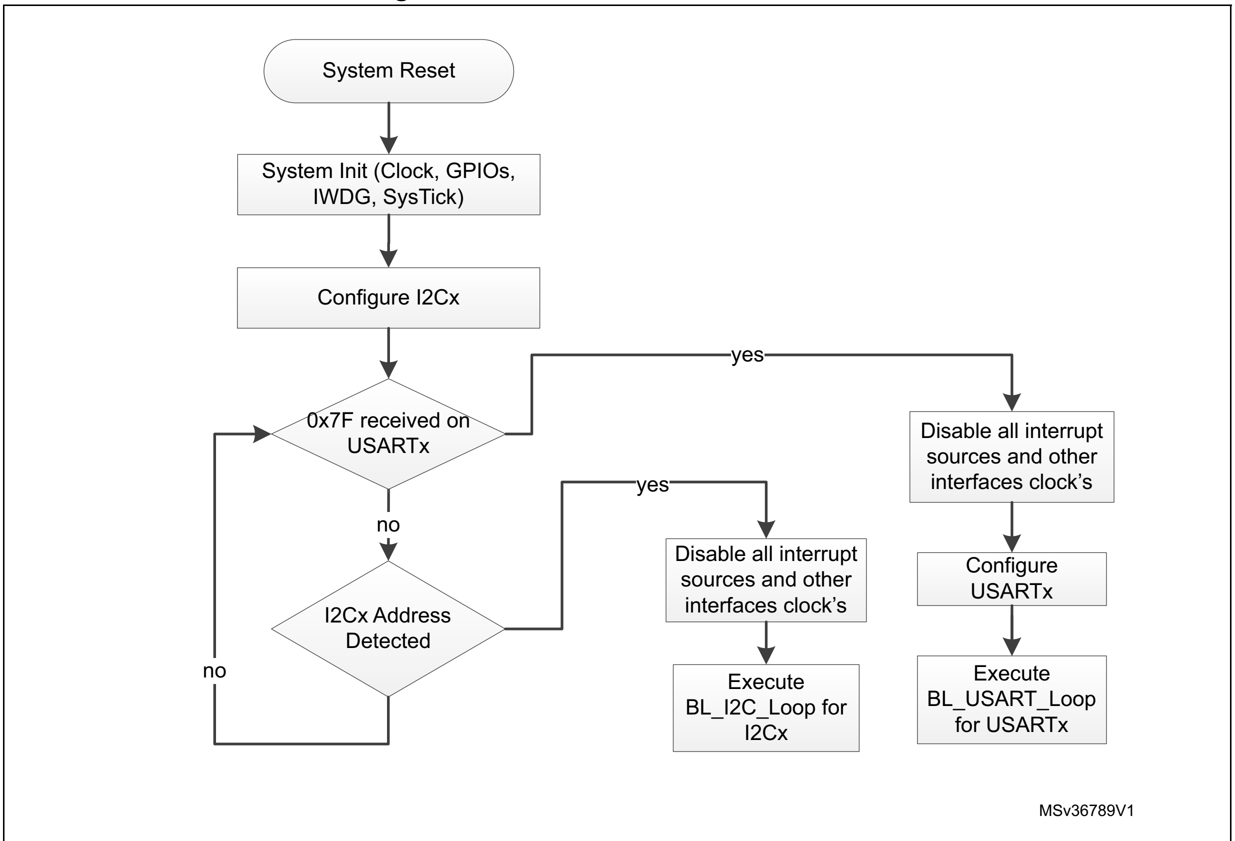
Note: After the STM32F030xC *devices have booted in bootloader mode using USART2, the serial wire debug (SWD) communication is no more possible until the system is reset, because SWD uses PA14 pin (SWCLK) which is already used by the bootloader (USART2_RX).*

The system clock is derived from the embedded internal high-speed RC, no external quartz is required for the bootloader execution.

6.2 Bootloader selection

The figure below shows the bootloader selection mechanism.

Figure 9.Bootloader selection for STM32F030xC



6.3 Bootloader version

The following table lists the STM32F030xC devices bootloader versions.

Table 12. STM32F030xC bootloader versions

Bootloader version number	Description	Known limitations
V5.2	Initial bootloader version	None

7 STM32F05xxx and STM32F030x8 devices bootloader

7.1 Bootloader configuration

The STM32F05xxx and STM32F030x8 devices bootloader is activated by applying pattern2 (described in *Table 2: Bootloader activation patterns*). The following table shows the hardware resources used by this bootloader.

Table 13. STM32F05xxx and STM32F030x8 devices configuration in system memory boot mode

Bootloader	Feature/Peripheral	State	Comment
Common to all bootloaders	RCC	HSI Enabled	The system clock frequency is 24 MHz (using PLL clocked by HSI). 1 Flash Wait State.
	RAM	-	2 Kbyte starting from address 0x20000000 are used by the bootloader firmware.
	System memory	-	3 Kbyte starting from address 0x1FFFEC00, contain the bootloader firmware.
	IWDG	-	The independent watchdog (IWDG) prescaler is configured to its maximum value. It is periodically refreshed to prevent watchdog reset in case the hardware IWDG option was previously enabled by the user.
USART1 bootloader	USART1	Enabled	Once initialized, the USART1 configuration is 8 bits, even parity and 1 Stop bit.
	USART1_RX pin	Input	PA10 pin: USART1 in reception mode.
	USART1_TX pin	Output	PA9 pin: USART1 in transmission mode.
USART2 bootloader	USART2	Enabled	Once initialized, the USART2 configuration is 8 bits, even parity and 1 Stop bit.
	USART2_RX pin	Input	PA15 pin: USART2 in reception mode.
	USART2_TX pin	Output	PA14 pin: USART2 in transmission mode.
USARTx bootloaders	SysTick timer	Enabled	Used to automatically detect the serial baud rate from the host.

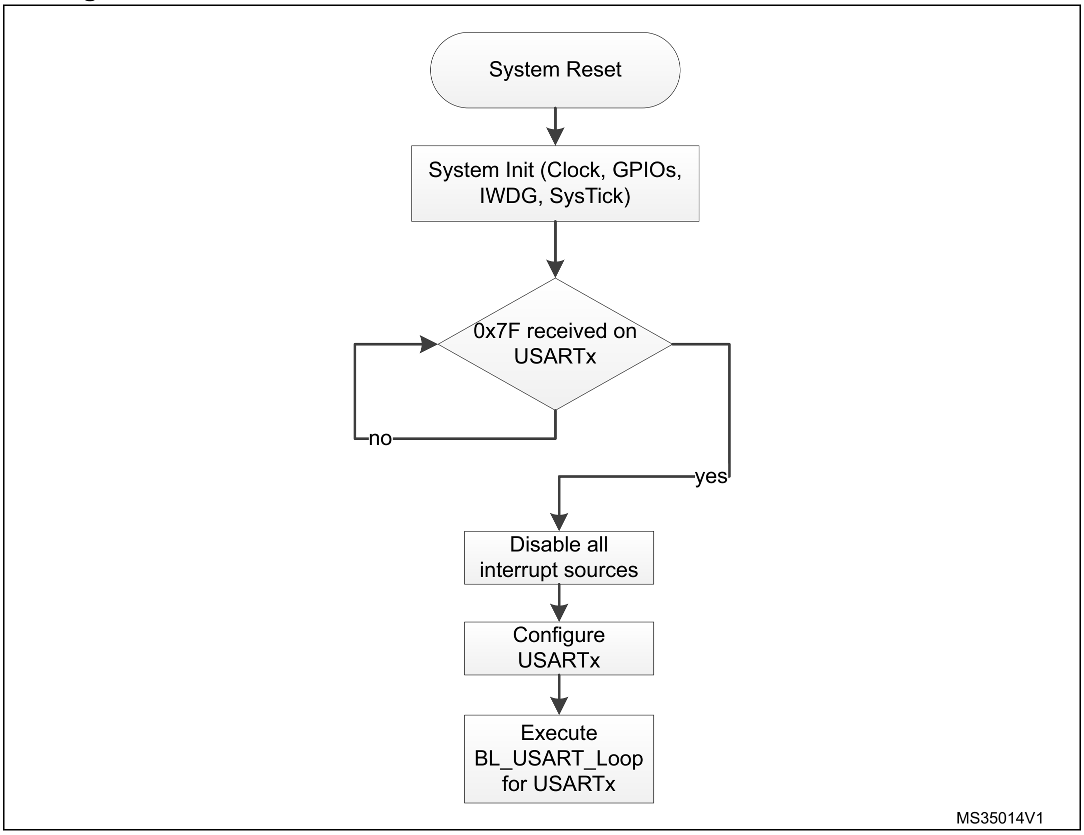
The system clock is derived from the embedded internal high-speed RC, no external quartz is required for the bootloader execution.

Note: After the STM32F05xxx and STM32F030x8 devices have booted in bootloader mode, the serial wire debug (SWD) communication is no more possible until the system is reset, because SWD uses PA14 pin (SWCLK) which is already used by the bootloader (USART2_TX).

7.2 Bootloader selection

The figure below shows the bootloader selection mechanism.

Figure 10. Bootloader selection for STM32F05xxx and STM32F030x8 devices



7.3 Bootloader version

The following table lists the STM32F05xxx and STM32F030x8 devices bootloader versions.

Table 14. STM32F05xxx and STM32F030x8 devices bootloader versions

Bootloader version number	Description	Known limitations
V2.1	Initial bootloader version	– At bootloader startup, the HSITRIM value is set to (0) (in HSITRIM bits on RCC_CR register) instead of default value (16), as consequence a deviation is generated in crystal measurement. For better results, please use the smallest supported crystal value (ie. 4 MHz). – For the USART interface, two consecutive NACKs instead of 1 NACK are sent when a Read Memory or Write Memory command is sent and the RDP level is active.

8 STM32F04xxx devices bootloader

8.1 Bootloader configuration

The STM32F04xxx bootloader is activated by applying pattern6 (described in *Table 2: Bootloader activation patterns*). The following table shows the hardware resources used by this bootloader.

Table 15. STM32F04xxx configuration in system memory boot mode

Bootloader	Feature/Peripheral	State	Comment
Common to all bootloaders	RCC	HSI enabled	The system clock frequency is 48 MHz with HSI48 48 MHz as clock source.
		-	The clock recovery system (CRS) is enabled for the DFU bootloader to allow USB to be clocked by HSI48 48 MHz.
	RAM	-	6 Kbyte starting from address 0x20000000 are used by the bootloader firmware
	System memory	-	13 Kbyte starting from address 0x1FFFC400, contain the bootloader firmware
	IWDG	-	The independent watchdog (IWDG) prescaler is configured to its maximum value. It is periodically refreshed to prevent watchdog reset (in case the hardware IWDG option was previously enabled by the user).
USART1 bootloader	USART1	Enabled	Once initialized the USART1 configuration is: 8-bits, even parity and 1 Stop bit
	USART1_RX pin	Input	PA10 pin: USART1 in reception mode
	USART1_TX pin	Output	PA9 pin: USART1 in transmission mode
USART2 bootloader	USART2	Enabled	Once initialized the USART2 configuration is: 8-bits, even parity and 1 Stop bit
	USART2_RX pin	Input	PA15 pin: USART2 in reception mode
	USART2_TX pin	Output	PA14 pin: USART2 in transmission mode
USARTx bootloaders	SysTick timer	Enabled	Used to automatically detect the serial baud rate from the host for USARTx bootloaders.
I2C1 bootloader	I2C1	Enabled	The I2C1configuration is: I2C speed: up to 400 KHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b0111110x (where x = 0 for write and x = 1 for read).
	I2C1_SCL pin	Input/Output	PB6 pin: clock line is used in open-drain mode.
	I2C1_SDA pin	Input/Output	PB7 pin: data line is used in open-drain mode.

Table 15. STM32F04xxx configuration in system memory boot mode (continued)

Bootloader	Feature/Peripheral	State	Comment
DFU bootloader	USB	Enabled	USB used in FS mode
	USB_DM pin	Input/Output	PA11: USB DM line.
	USB_DP pin		PA12: USB DP line No external pull-up resistor is required.

Note: After the STM32F04xxx devices have booted in bootloader mode using USART2, the serial wire debug (SWD) communication is no more possible until the system is reset, because SWD uses PA14 pin (SWCLK) which is already used by the bootloader (USART2_RX).

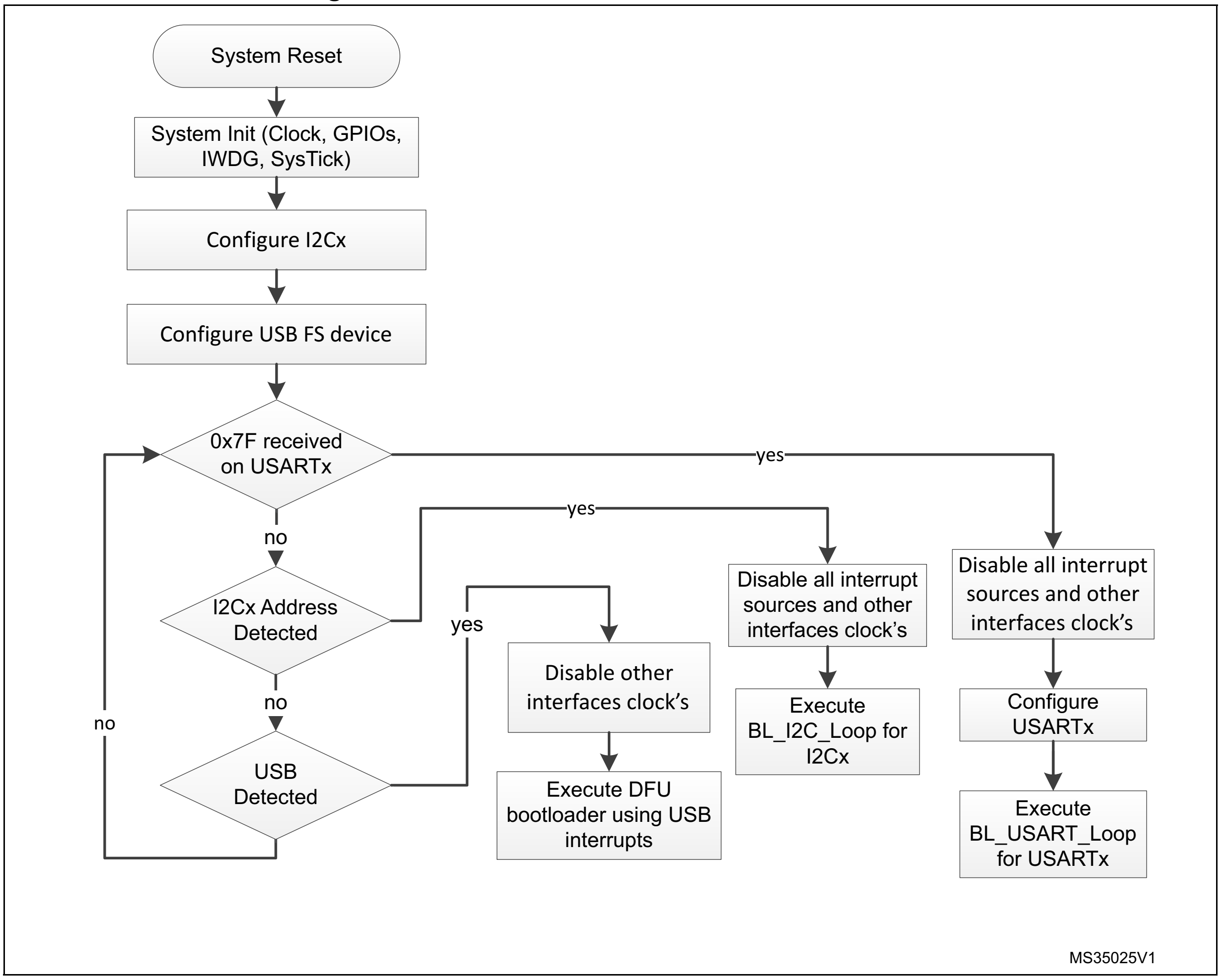
The system clock is derived from the embedded internal high-speed RC, no external quartz is required for the bootloader execution.

Note: Due to empty check mechanism present on this product, it is not possible to jump from user code to system bootloader.
Such jump will result in a jump back to user flash space.
But if the first 4 bytes of User Flash (at 0x0800 0000) are empty at the moment of jump (ie. erase first sector before jump or execute code from SRAM while Flash is empty), then system bootloader will be executed when jumped to.

8.2 Bootloader selection

The figure below shows the bootloader selection mechanism.

Figure 11. Bootloader selection for STM32F04xxx



8.3 Bootloader version

The following table lists the STM32F04xxx devices bootloader versions:

Table 16. STM32F04xxx bootloader versions

Bootloader version number	Description	Known limitations
V10.0	Initial bootloader version	At bootloader startup, the HSITRIM value is set to (0) (in HSITRIM bits on RCC_CR register) instead of default value (16), as consequence a deviation is generated in crystal measurement. For better results, please use the smallest supported crystal value (ie. 4 MHz).
V10.1	Add dynamic support of USART/USB interfaces on PA11/12 IOs for small packages.	

9 STM32F070x6 devices bootloader

9.1 Bootloader configuration

The STM32F070x6 bootloader is activated by applying pattern6 (described in *Table 2: Bootloader activation patterns*). The following table shows the hardware resources used by this bootloader.

Table 17. STM32F070x6 configuration in system memory boot mode

Bootloader	Feature/Peripheral	State	Comment
Common to all bootloaders	RCC	HSI enabled	At startup, the system clock frequency is configured to 48 MHz using the HSI. If an external clock (HSE) is not present, the system is kept clocked from the HSI.
		HSE enabled	The external clock can be used for all bootloader interfaces and should have one of the following values [24, 18, 16, 12, 8, 6, 4] MHz. The PLL is used to generate 48 MHz for USB and system clock.
		-	The Clock Security System (CSS) interrupt is enabled for HSE. Any failure (or removal) of the external clock generates system reset.
	RAM	-	6 Kbyte starting from address 0x20000000 are used by the bootloader firmware
	System memory	-	13 Kbyte starting from address 0x1FFFC400, contain the bootloader firmware.
USART1 bootloader	USART1	Enabled	Once initialized the USART1 configuration is: 8-bits, even parity and 1 Stop bit
	USART1_RX pin	Input	PA10 pin: USART1 in reception mode
	USART1_TX pin	Output	PA9 pin: USART1 in transmission mode
USART2 bootloader	USART2	Enabled	Once initialized the USART2 configuration is: 8-bits, even parity and 1 Stop bit
	USART2_RX pin	Input	PA15 pin: USART2 in reception mode
	USART2_TX pin	Output	PA14 pin: USART2 in transmission mode
USARTx bootloaders	SysTick timer	Enabled	Used to automatically detect the serial baud rate from the host for USARTx bootloaders.
I2C1 bootloader	I2C1	Enabled	The I2C1 configuration is: I2C speed: up to 400 KHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b0111110x where x = 0 for write and x = 1 for read)
	I2C1_SCL pin	Input/Output	PB6 pin: clock line is used in open-drain mode.
	I2C1_SDA pin	Input/Output	PB7 pin: data line is used in open-drain mode.

Table 17. STM32F070x6 configuration in system memory boot mode (continued)

Bootloader	Feature/Peripheral	State	Comment
DFU bootloader	USB	Enabled	USB FS configured in forced device mode. USB FS interrupt vector is enabled and used for USB DFU communications.
	USB_DM pin	Input/Output	PA11 pin: USB FS DM line
	USB_DP pin		PA12 pin: USB FS DP line. No external Pull-up resistor is required.

Note: If HSI deviation exceeds 1% , the bootloader might not function correctly.

Note: After the STM32F070x6 *devices have booted in bootloader mode using USART2, the serial wire debug (SWD) communication is no more possible until the system is reset, because SWD uses PA14 pin (SWCLK) which is already used by the bootloader (USART2_RX).*

The bootloader has two cases of operation depending on the presence of the external clock (HSE) at bootloader startup:

- If HSE is present and has a value of 24, 18, 16, 12, 8, 6, 4 MHz, the system clock is configured to 48 MHz with HSE as clock source. The DFU interface, USART1, USART2 and I2C1 are functional and can be used to communicate with the bootloader device.
- If HSE is not present, the HSI is kept as default clock source and only USART1, USART2 and I2C1 are functional.

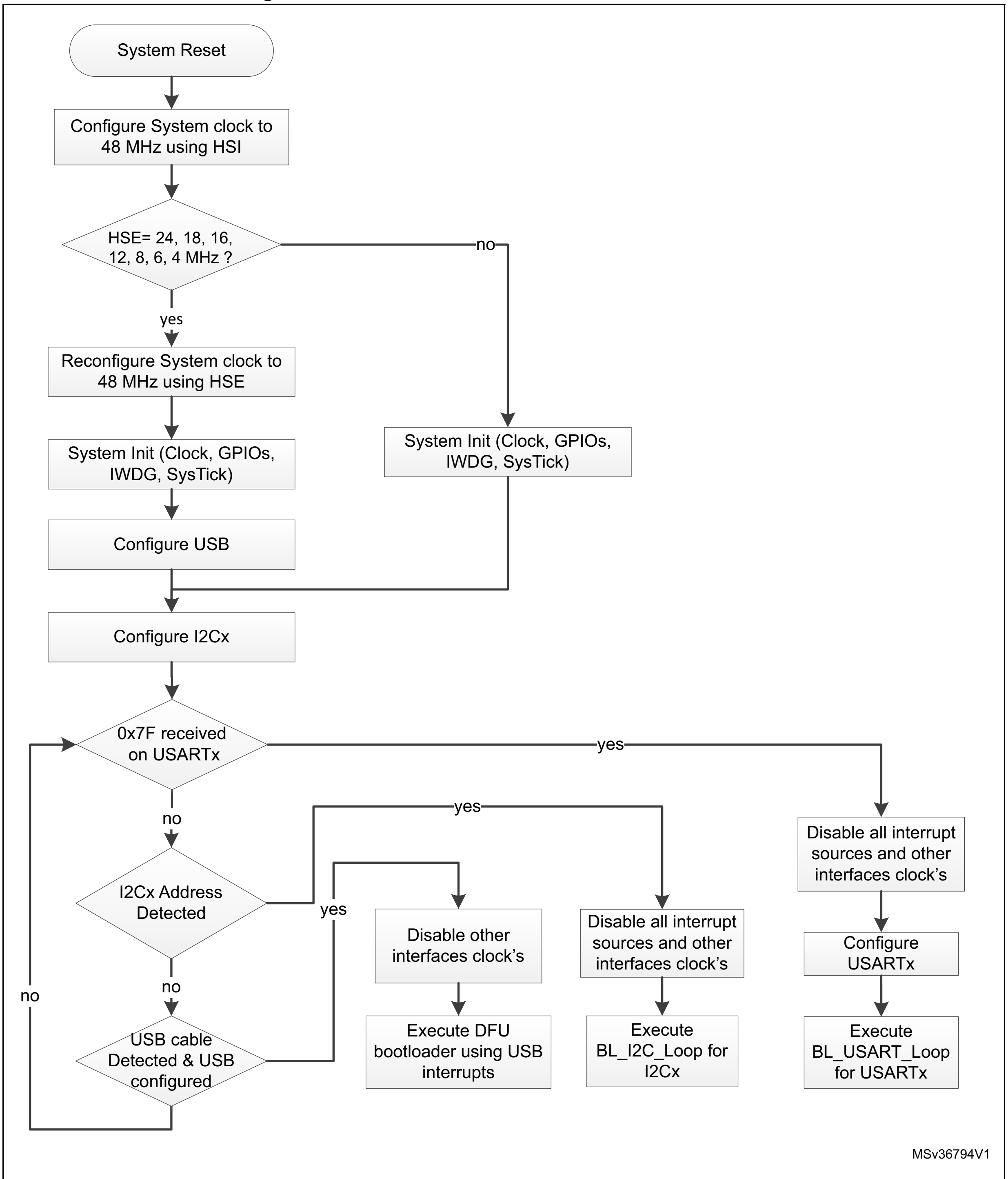
The external clock (HSE) must be kept if it’s connected at bootloader startup because it will be used as system clock source.

Note: Due to empty check mechanism present on this product, it is not possible to jump from user code to system bootloader.
Such jump will result in a jump back to user flash space.
But if the first 4 bytes of User Flash (at 0x0800 0000) are empty at the moment of jump (ie. erase first sector before jump or execute code from SRAM while Flash is empty), then system bootloader will be executed when jumped to.

9.2 Bootloader selection

The figure below shows the bootloader selection mechanism.

Figure 12. Bootloader selection for STM32F070x6



9.3 Bootloader version

The following table lists the STM32F070x6 devices bootloader versions.

Table 18. STM32F070x6 bootloader versions

<table>
<tr><th>Bootloader version number</th><th>Description</th><th>Known limitations</th></tr>
<tr><td>V10.2</td><td>Initial bootloader version</td><td rowspan="2">At bootloader startup, the HSITRIM value is set to (0) (in HSITRIM bits on RCC_CR register) instead of default value (16), as consequence a deviation is generated in crystal measurement. For better results, please use the smallest supported crystal value (ie. 4 MHz).</td></tr>
<tr><td>V10.3</td><td>Clock configuration fixed to HSI 8 MHz</td></tr>
</table>

10 STM32F070xB devices bootloader

10.1 Bootloader configuration

The STM32F070xB bootloader is activated by applying pattern2 (described in *Table 2: Bootloader activation patterns*). The following table shows the hardware resources used by this bootloader.

Table 19. STM32F070xB configuration in system memory boot mode

<table>
<tr><th>Bootloader</th><th>Feature/Peripheral</th><th>State</th><th>Comment</th></tr>
<tr><td rowspan="5">Common to all bootloaders</td><td rowspan="3">RCC</td><td>HSI enabled</td><td>At startup, the system clock frequency is configured to 48 MHz using the HSI. If an external clock (HSE) is not present, the system is kept clocked from the HSI.</td></tr>
<tr><td>HSE enabled</td><td>The external clock can be used for all bootloader interfaces and should have one of the following values [24, 18, 16, 12, 8, 6, 4] MHz. The PLL is used to generate 48 MHz for USB and system clock.</td></tr>
<tr><td>-</td><td>The Clock Security System (CSS) interrupt is enabled for HSE. Any failure (or removal) of the external clock generates system reset.</td></tr>
<tr><td>RAM</td><td>-</td><td>6 Kbyte starting from address 0x20000000 are used by the bootloader firmware</td></tr>
<tr><td>System memory</td><td>-</td><td>12 Kbyte starting from address 0x1FFFC800, contain the bootloader firmware.</td></tr>
<tr><td rowspan="3">USART1 bootloader</td><td>USART1</td><td>Enabled</td><td>Once initialized the USART1 configuration is: 8-bits, even parity and 1 Stop bit</td></tr>
<tr><td>USART1_RX pin</td><td>Input</td><td>PA10 pin: USART1 in reception mode</td></tr>
<tr><td>USART1_TX pin</td><td>Output</td><td>PA9 pin: USART1 in transmission mode</td></tr>
<tr><td rowspan="3">USART2 bootloader</td><td>USART2</td><td>Enabled</td><td>Once initialized the USART2 configuration is: 8-bits, even parity and 1 Stop bit</td></tr>
<tr><td>USART2_RX pin</td><td>Input</td><td>PA15 pin: USART2 in reception mode</td></tr>
<tr><td>USART2_TX pin</td><td>Output</td><td>PA14 pin: USART2 in transmission mode</td></tr>
<tr><td>USARTx bootloaders</td><td>SysTick timer</td><td>Enabled</td><td>Used to automatically detect the serial baud rate from the host for USARTx bootloaders.</td></tr>
<tr><td rowspan="3">I2C1 bootloader</td><td>I2C1</td><td>Enabled</td><td>The I2C1 configuration is:
I2C speed: up to 400 KHz, 7-bit address, slave mode, analog filter ON.
Slave 7-bit address: 0b0111011x
(where x = 0 for write and x = 1 for read)</td></tr>
<tr><td>I2C1_SCL pin</td><td>Input/Output</td><td>PB6 pin: clock line is used in open-drain mode.</td></tr>
<tr><td>I2C1_SDA pin</td><td>Input/Output</td><td>PB7 pin: data line is used in open-drain mode.</td></tr>
</table>

Table 19. STM32F070xB configuration in system memory boot mode (continued)

Bootloader	Feature/Peripheral	State	Comment
DFU bootloader	USB	Enabled	USB FS configured in forced device mode. USB FS interrupt vector is enabled and used for USB DFU communications.
	USB_DM pin	Input/Output	PA11 pin: USB FS DM line
	USB_DP pin		PA12 pin: USB FS DP line. No external Pull-up resistor is required.

Note: If HSI deviation exceeds 1% , the bootloader might not function correctly.

Note: After the STM32F070xB *devices have booted in bootloader mode using USART2, the serial wire debug (SWD) communication is no more possible until the system is reset, because SWD uses PA14 pin (SWCLK) which is already used by the bootloader (USART2_RX).*

The bootloader has two cases of operation depending on the presence of the external clock (HSE) at bootloader startup:

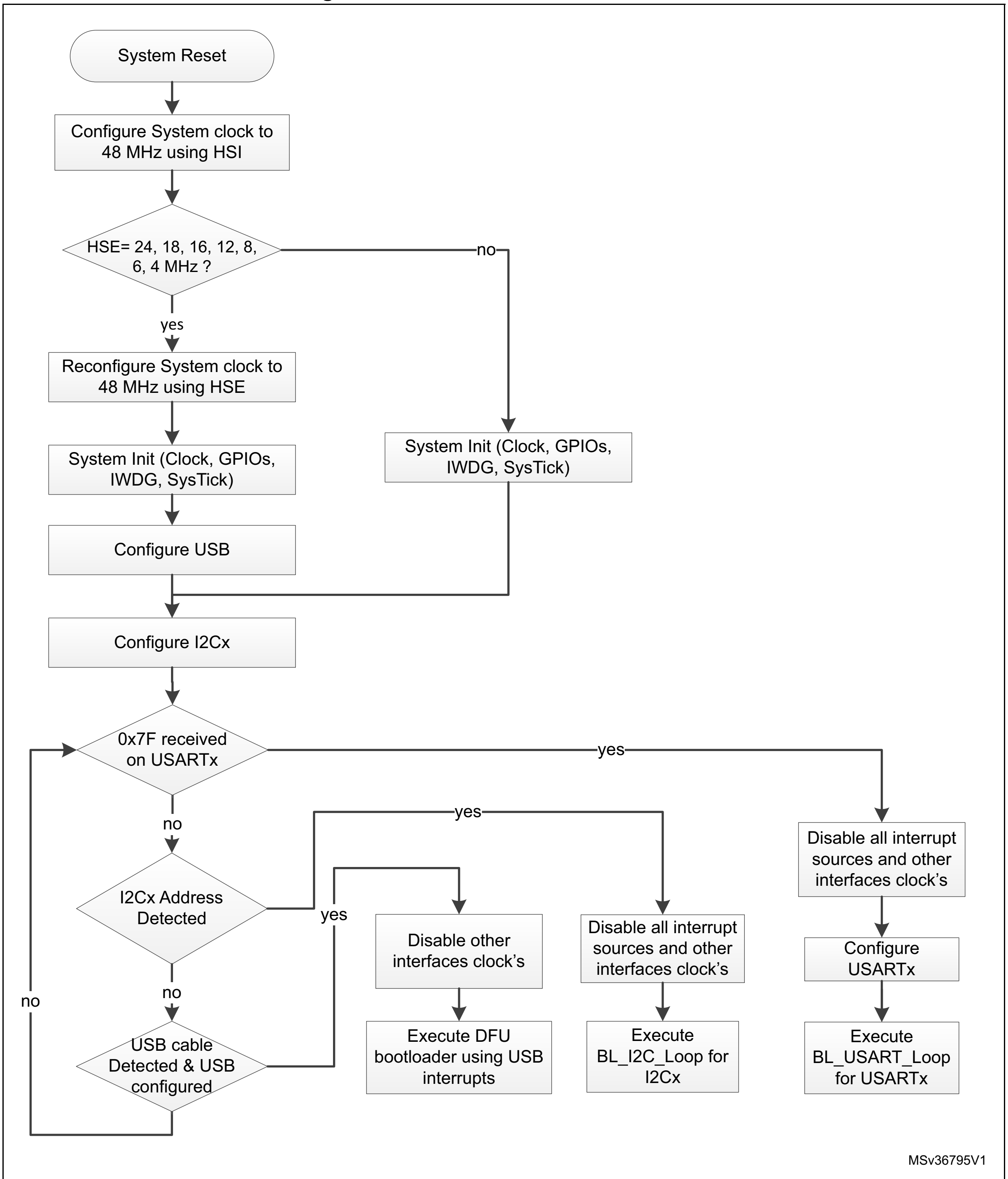
- If HSE is present and has a value of 24, 18, 16, 12, 8, 6, 4 MHz, the system clock is configured to 48 MHz with HSE as clock source. The DFU interface, USART1, USART2 and I2C1 are functional and can be used to communicate with the bootloader device.
- If HSE is not present, the HSI is kept as default clock source and only USART1, USART2 and I2C1 are functional.

The external clock (HSE) must be kept if it’s connected at bootloader startup because it will be used as system clock source.

10.2 Bootloader selection

The figure below shows the bootloader selection mechanism.

Figure 13.Bootloader selection for STM32F070xB



10.3 Bootloader version

The following table lists the STM32F070xB devices bootloader versions.

Table 20. STM32F070xB bootloader versions

Bootloader version number	Description	Known limitations
V10.2	Initial bootloader version	At bootloader startup, the HSITRIM value is set to (0) (in HSITRIM bits on RCC_CR register) instead of default value (16), as consequence a deviation is generated in crystal measurement. For better results, please use the smallest supported crystal value (ie. 4 MHz).
V10.3	Clock configuration fixed to HSI 8 MHz	

11 STM32F071xx/072xx devices bootloader

11.1 Bootloader configuration

The STM32F071xx/072xx bootloader is activated by applying pattern2 (described in *Table 2: Bootloader activation patterns*). The following table shows the hardware resources used by this bootloader.

Table 21. STM32F071xx/072xx configuration in system memory boot mode

Bootloader	Feature/Peripheral	State	Comment
Common to all bootloaders	RCC	HSI enabled	The system clock frequency is 48 MHz with HSI48 48 MHz as clock source.
		-	The clock recovery system (CRS) is enabled for the DFU bootloader to allow USB to be clocked by HSI48 48 MHz.
	RAM	-	6 Kbyte starting from address 0x20000000 are used by the bootloader firmware
	System memory	-	12 Kbyte starting from address 0x1FFFC800, contain the bootloader firmware
	IWDG	-	The independent watchdog (IWDG) prescaler is configured to its maximum value. It is periodically refreshed to prevent watchdog reset (in case the hardware IWDG option was previously enabled by the user).
USART1 bootloader	USART1	Enabled	Once initialized the USART1 configuration is: 8-bits, even parity and 1 Stop bit
	USART1_RX pin	Input	PA10 pin: USART1 in reception mode
	USART1_TX pin	Output	PA9 pin: USART1 in transmission mode
USART2 bootloader	USART2	Enabled	Once initialized the USART2 configuration is: 8-bits, even parity and 1 Stop bit
	USART2_RX pin	Input	PA15 pin: USART2 in reception mode
	USART2_TX pin	Output	PA14 pin: USART2 in transmission mode
USARTx bootloaders	SysTick timer	Enabled	Used to automatically detect the serial baud rate from the host for USARTx bootloaders.
I2C1 bootloader	I2C1	Enabled	The I2C1 configuration is: I2C speed: up to 400 KHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b0111011x (where x = 0 for write and x = 1 for read)
	I2C1_SCL pin	Input/Output	PB6 pin: clock line is used in open-drain mode.
	I2C1_SDA pin	Input/Output	PB7 pin: data line is used in open-drain mode.

Table 21. STM32F071xx/072xx configuration in system memory boot mode (continued)

Bootloader	Feature/Peripheral	State	Comment
DFU bootloader	USB	Enabled	USB used in FS mode
	USB_DM pin	Input/Output	PA11: USB DM line.
	USB_DP pin		PA12: USB DP line No external pull-up resistor is required.

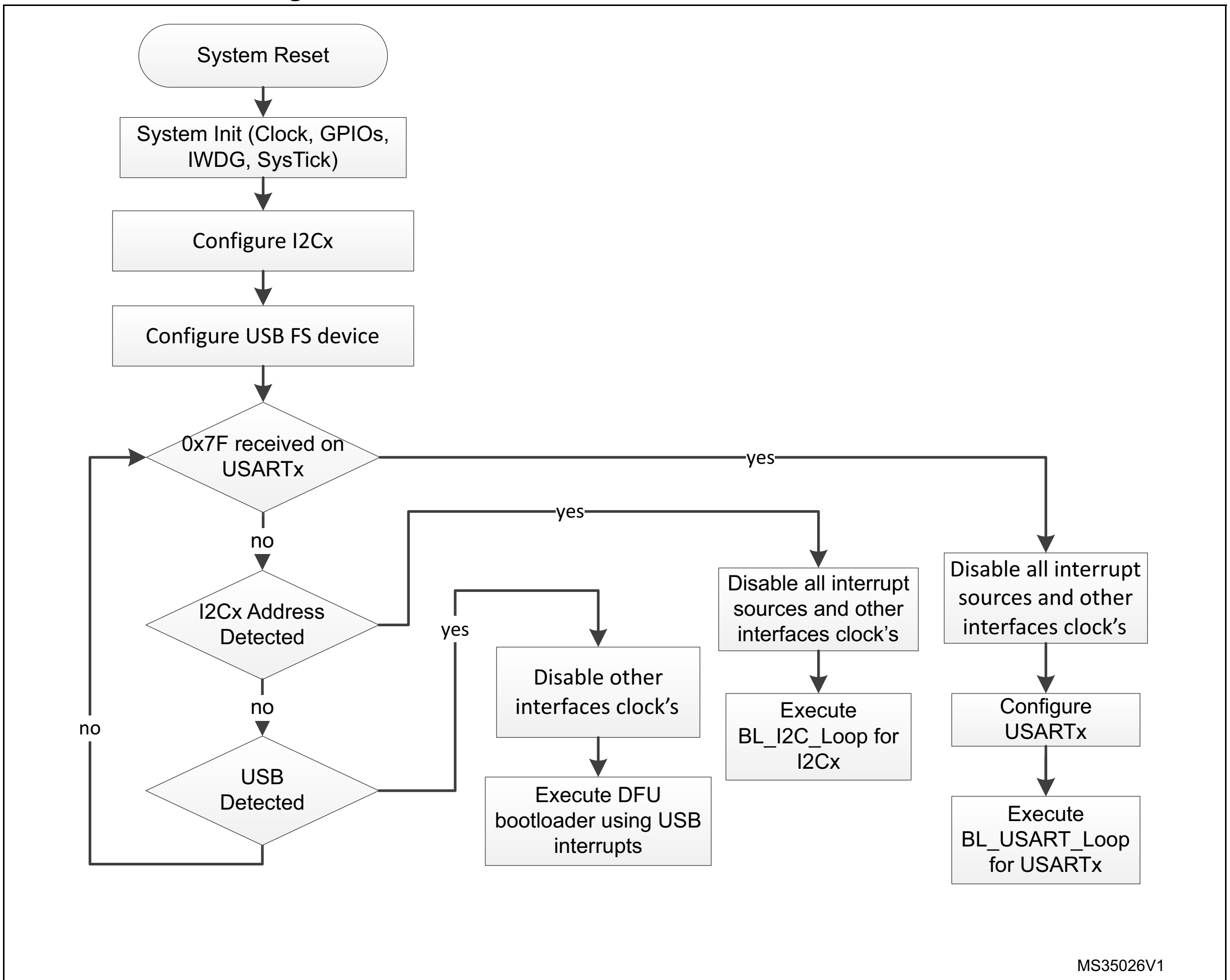
Note: After the STM32F071xx/072xx devices have booted in bootloader mode using USART2, the serial wire debug (SWD) communication is no more possible until the system is reset, because SWD uses PA14 pin (SWCLK) which is already used by the bootloader (USART2_RX).

The system clock is derived from the embedded internal high-speed RC, no external quartz is required for the bootloader execution.

11.2 Bootloader selection

The figure below shows the bootloader selection mechanism.

Figure 14. Bootloader selection for STM32F071xx/072xx



11.3 Bootloader version

The following table lists the STM32F071xx/072xx devices bootloader versions:

Table 22. STM32F071xx/072xx bootloader versions

Bootloader version number	Description	Known limitations
V10.1	Initial bootloader version	At bootloader startup, the HSITRIM value is set to (0) (in HSITRIM bits on RCC_CR register) instead of default value (16), as consequence a deviation is generated in crystal measurement. For better results, please use the smallest supported crystal value (ie. 4 MHz).

12 STM32F09xxx devices bootloader

12.1 Bootloader configuration

The STM32F09xxx bootloader is activated by applying pattern6 (described in *Table 2: Bootloader activation patterns*). The following table shows the hardware resources used by this bootloader.

Table 23. STM32F09xxx configuration in system memory boot mode

Bootloader	Feature/Peripheral	State	Comment
Common to all bootloaders	RCC	HSI enabled	The system clock frequency is 48 MHz with HSI48 48 MHz as clock source.
	RAM	-	6 Kbyte starting from address 0x20000000 are used by the bootloader firmware
	System memory	-	8 Kbyte starting from address 0x1FFFD800, contain the bootloader firmware.
USART1 bootloader	USART1	Enabled	Once initialized the USART1 configuration is: 8-bits, even parity and 1 Stop bit
	USART1_RX pin	Input	PA10 pin: USART1 in reception mode
	USART1_TX pin	Output	PA9 pin: USART1 in transmission mode
USART2 bootloader	USART2	Enabled	Once initialized the USART2 configuration is: 8-bits, even parity and 1 Stop bit
	USART2_RX pin	Input	PA3 pin: USART2 in reception mode
			PA15 pin: USART2 in reception mode
	USART2_TX pin	Output	PA2 pin: USART2 in transmission mode
			PA14 pin: USART2 in transmission mode
USARTx bootloaders	SysTick timer	Enabled	Used to automatically detect the serial baud rate from the host for USARTx bootloaders.
I2C1 bootloader	I2C1	Enabled	The I2C1 configuration is: I2C speed: up to 400 KHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b1000001x (where x = 0 for write and x = 1 for read)
	I2C1_SCL pin	Input/Output	PB6 pin: clock line is used in open-drain mode.
	I2C1_SDA pin	Input/Output	PB7 pin: data line is used in open-drain mode.

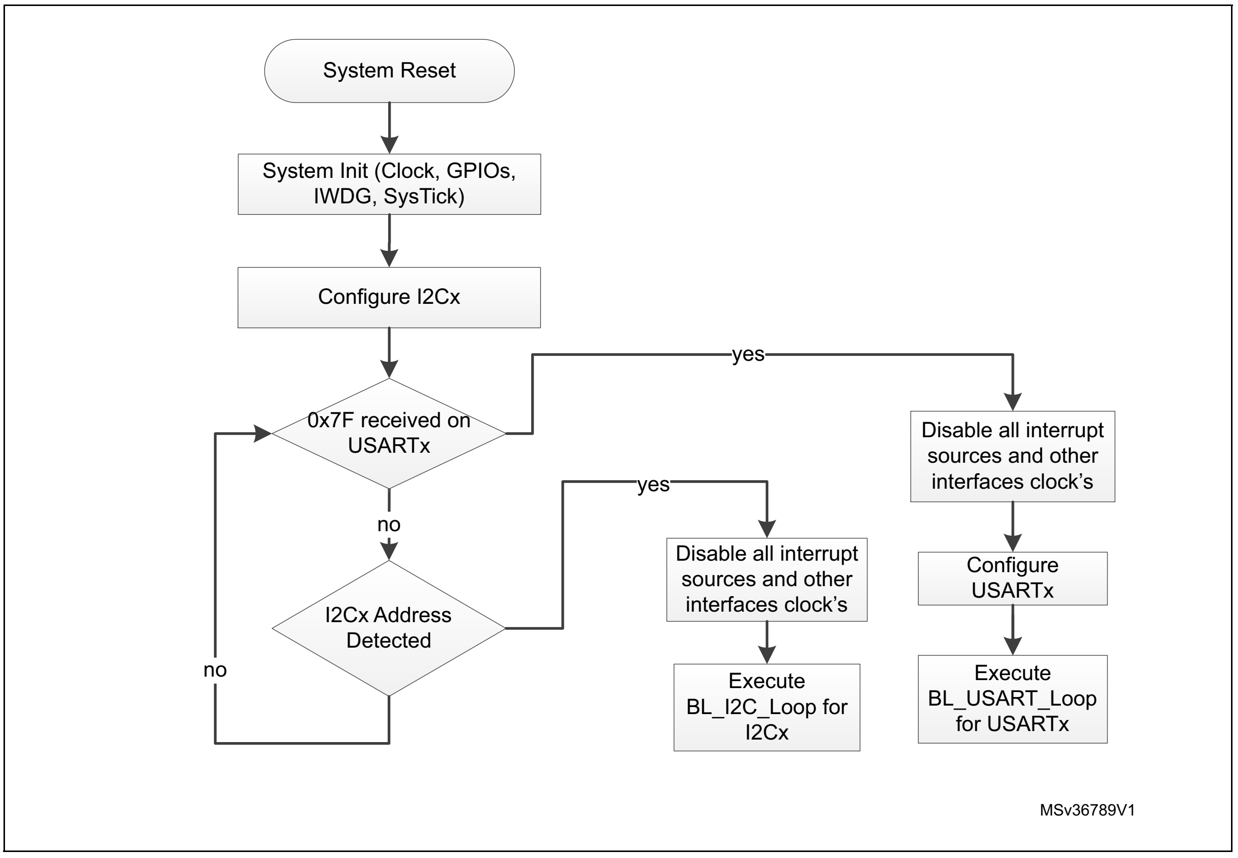
Note: After the STM32F09xxx *devices have booted in bootloader mode using USART2, the serial wire debug (SWD) communication is no more possible until the system is reset, because SWD uses PA14 pin (SWCLK) which is already used by the bootloader (USART2_RX).*

The system clock is derived from the embedded internal high-speed RC, no external quartz is required for the bootloader execution.

12.2 Bootloader selection

The figure below shows the bootloader selection mechanism.

Figure 15. Bootloader selection for STM32F09xxx



12.3 Bootloader version

The following table lists the STM32F09xxx devices bootloader versions.

Table 24. STM32F09xxx bootloader versions

Bootloader version number	Description	Known limitations
V5.0	Initial bootloader version	At bootloader startup, the HSITRIM value is set to (0) (in HSITRIM bits on RCC_CR register) instead of default value (16), as consequence a deviation is generated in crystal measurement. For better results, please use the smallest supported crystal value (ie. 4 MHz).

13 STM32F10xxx devices bootloader

13.1 Bootloader configuration

The STM32F10xxx bootloader is activated by applying pattern1 (described in *Table 2: Bootloader activation patterns*). The following table shows the hardware resources used by this bootloader.

Table 25. STM32F10xxx configuration in system memory boot mode

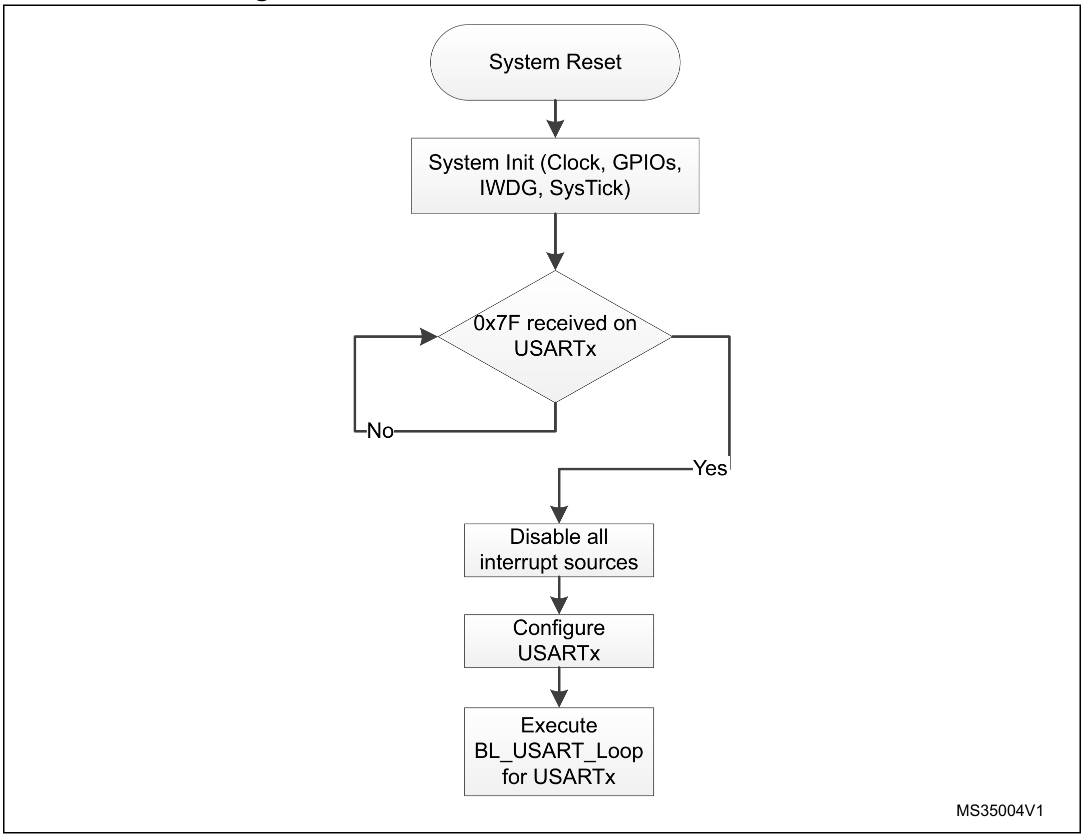
Bootloader	Feature/Peripheral	State	Comment
USART1 bootloader	RCC	HSI enabled	The system clock frequency is 24 MHz using the PLL.
	RAM	-	512 byte starting from address 0x20000000 are used by the bootloader firmware.
	System memory	-	2 Kbyte starting from address 0x1FFFF000 contain the bootloader firmware.
	IWDG	-	The independent watchdog (IWDG) prescaler is configured to its maximum value and is periodically refreshed to prevent watchdog reset (in case the hardware IWDG option was previously enabled by the user).
	USART1	Enabled	Once initialized, the USART1 configuration is: 8 bits, even parity and 1 Stop bit.
	USART1_RX pin	Input	PA10 pin: USART1 in reception mode
	USART1_TX pin	Output push-pull	PA9 pin: USART1 in transmission mode
	SysTick timer	Enabled	Used to automatically detect the serial baud rate from the host.

The system clock is derived from the embedded internal high-speed RC, no external quartz is required for the bootloader execution.

13.2 Bootloader selection

The figure below shows the bootloader selection mechanism.

Figure 16. Bootloader selection for STM32F10xxx



13.3 Bootloader version

The following table lists the STM32F10xxx devices bootloader versions:

Table 26. STM32F10xxx bootloader versions

Bootloader version number	Description
V2.0	Initial bootloader version
V2.1	– Updated Go Command to initialize the main stack pointer – Updated Go command to return NACK when jump address is in the Option byte area or System memory area – Updated Get ID command to return the device ID on two bytes – Update the bootloader version to V2.1
V2.2	– Updated Read Memory, Write Memory and Go commands to deny access with a NACK response to the first 0x200 bytes of RAM memory used by the bootloader – Updated Readout Unprotect command to initialize the whole RAM content to 0x0 before ROP disable operation

Note: The bootloader ID format is applied to all STM32 devices families except the STM32F1xx family. The bootloader version for the STM32F1xx applies only to the embedded device's bootloader version and not to its supported protocols.

14 STM32F105xx/107xx devices bootloader

14.1 Bootloader configuration

The STM32F105xx/107xx bootloader is activated by applying pattern1 (described in *Table 2: Bootloader activation patterns*). The following table shows the hardware resources used by this bootloader.

Table 27. STM32F105xx/107xx configuration in system memory boot mode

Bootloader	Feature/Peripheral	State	Comment
Common to all bootloaders	RCC	HSI enabled	The system clock frequency is 24 MHz using the PLL. This is used only for USARTx bootloaders and during CAN2, USB detection for CAN and DFU bootloaders (once CAN or DFU bootloader is selected, the clock source will be derived from the external crystal).
		HSE enabled	The external clock is mandatory only for DFU and CAN bootloaders and it must provide one of the following frequencies: 8 MHz, 14.7456 MHz or 25 MHz. For CAN bootloader, the PLL is used only to generate 48 MHz when 14.7456 MHz is used as HSE. For DFU bootloader, the PLL is used to generate a 48 MHz system clock from all supported external clock frequencies.
		-	The Clock Security System (CSS) interrupt is enabled for the CAN and DFU bootloaders. Any failure (or removal) of the external clock will generate system reset.
	RAM	-	4 Kbyte starting from address 0x20000000 are used by the bootloader firmware.
	System memory	-	18 Kbyte starting from address 0x1FFFB000 contain the bootloader firmware.
	IWDG	-	The independent watchdog (IWDG) prescaler is configured to its maximum value and is periodically refreshed to prevent watchdog reset (in case the hardware IWDG option was previously enabled by the user).
USART1 bootloader	USART1	Enabled	Once initialized, the USART1 configuration is: 8 bits, even parity and 1 Stop bit.
	USART1_RX pin	Input	PA10 pin: USART1 in reception mode
	USART1_TX pin	Output push-pull	PA9 pin: USART1 in transmission mode

Table 27. STM32F105xx/107xx configuration in system memory boot mode (continued)

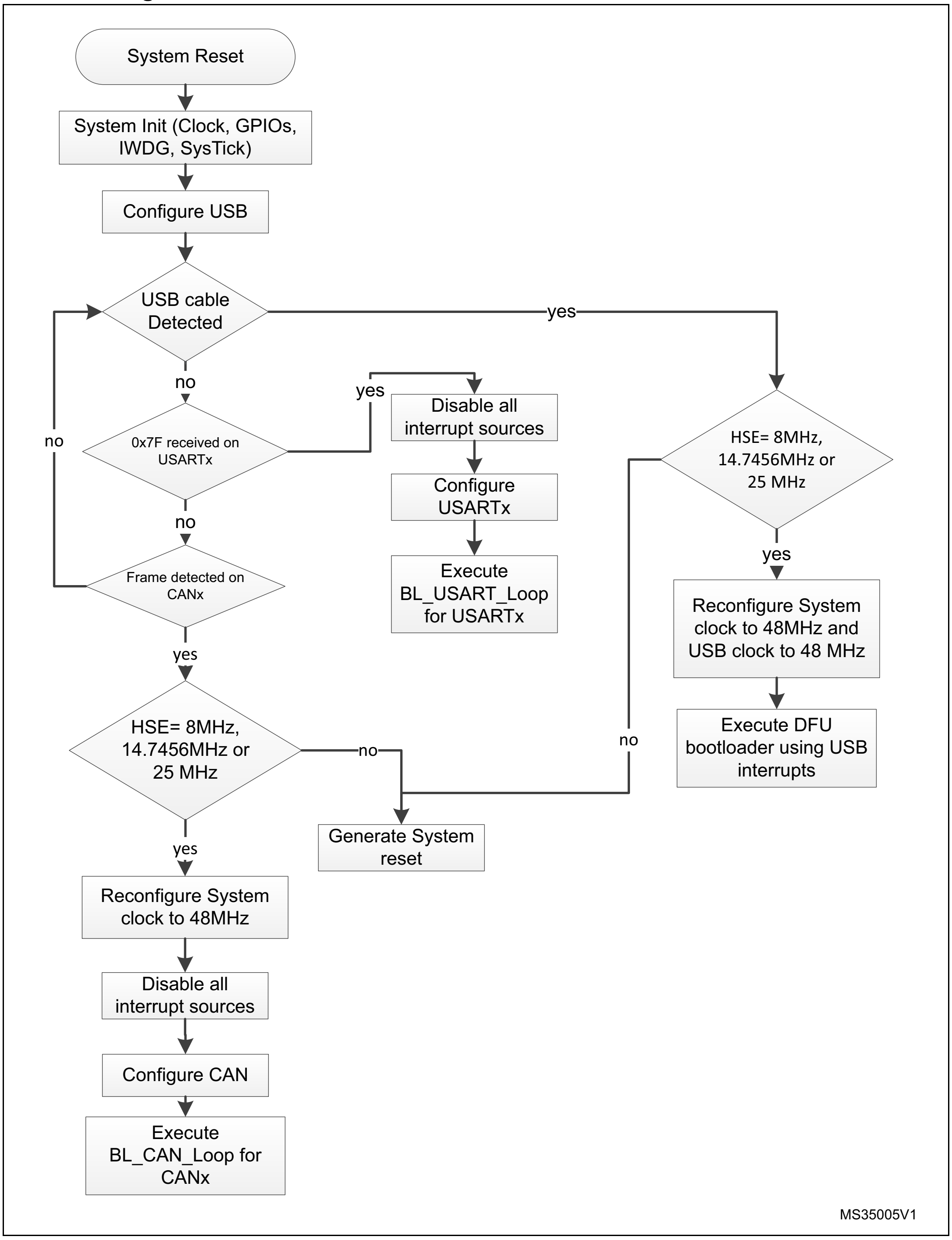
Bootloader	Feature/Peripheral	State	Comment
USART2 bootloader	USART2	Enabled	Once initialized, the USART2 configuration is: 8 bits, even parity and 1 Stop bit. The USART2 uses its remapped pins.
	USART2_RX pin	Input	PD6 pin: USART2 receive (remapped pin)
	USART2_TX pin	Output push-pull	PD5 pin: USART2 transmit (remapped pin)
USARTx bootloaders	SysTick timer	Enabled	Used to automatically detect the serial baud rate from the host for USARTx bootloader.
CAN2 bootloader	CAN2	Enabled	Once initialized, the CAN2 configuration is: Baudrate 125 kbps, 11-bit identifier. **Note:** CAN1 is clocked during the CAN bootloader execution because CAN1 manages the communication between CAN2 and SRAM.
	CAN2_RX pin	Input	PB5 pin: CAN2 receives (remapped pin).
	CAN2_TX pin	Output push-pull	PB6 pin: CAN2 transmits (remapped pin).
DFU bootloader	USB	Enabled	USB OTG FS configured in forced device mode
	USB_VBUS pin	Input	PA9: Power supply voltage line
	USB_DM pin	Input/Output	PA11 pin: USB_DM line
	USB_DP pin		PA12 pin: USB_DP line. No external Pull-up resistor is required

The system clock is derived from the embedded internal high-speed RC for USARTx bootloader. This internal clock is used also for DFU and CAN bootloaders but only for the selection phase. An external clock (8 MHz, 14.7456 MHz or 25 MHz.) is required for DFU and CAN bootloader execution after the selection phase.

14.2 Bootloader selection

The figure below shows the bootloader selection mechanism.

Figure 17. Bootloader selection for STM32F105xx/107xx devices



14.3 Bootloader version

The following table lists the STM32F105xx/107xx devices bootloader versions:

Table 28. STM32F105xx/107xx bootloader versions

Bootloader version number	Description
V1.0	Initial bootloader version
V2.0	– Bootloader detection mechanism updated to fix the issue when GPIOs of unused peripherals in this bootloader are connected to low level or left floating during the detection phase. For more details please refer to *Section 14.3.2*. – Vector table set to 0x1FFFB000 instead of 0x00000000 – Go command updated (for all bootloaders): USART1, USART2, CAN2, GPIOA, GPIOB, GPIOD and SysTick peripheral registers are set to their default reset values – DFU bootloader: USB pending interrupt cleared before executing the Leave DFU command – DFU subprotocol version changed from V1.0 to V1.2 – Bootloader version updated to V2.0
V2.1	– Fixed PA9 excessive consumption described in *Section 14.3.4*. – Get-Version command (defined in AN3155) corrected. It returns 0x22 instead of 0x20 in bootloader V2.0. Refer to *Section 14.3.3* for more details. – Bootloader version updated to V2.1
V2.2	– Fixed DFU option bytes descriptor (set to ‘e’ instead of ‘g’ because it is read/write and not erasable). – Fixed DFU polling timings for Flash Read/Write/Erase operations. – Robustness enhancements for DFU bootloader interface. – Updated bootloader version to V2.2.

Note: The bootloader ID format is applied to all STM32 devices families except the STM32F1xx family. The bootloader version for the STM32F1xx applies only to the embedded device’s bootloader version and not to its supported protocols.

14.3.1 How to identify STM32F105xx/107xx bootloader versions

Bootloader V1.0 is implemented on devices which date code is below 937 (refer to STM32F105xx and STM32F107xx datasheet for where to find the date code on the device marking).

Bootloader V2.0 and V2.1 are implemented on devices with a date code higher or equal to 937.

Bootloader V2.2 is implemented on devices with a date code higher or equal to 227.

There are two ways to distinguish between bootloader versions:

- When using the USART bootloader, the Get-Version command defined in AN2606 and AN3155 has been corrected in V2.1 version. It returns 0x22 instead of 0x20 as in bootloader V2.0.

- The values of the vector table at the beginning of the bootloader code are different. The user software (or via JTAG/SWD) reads 0x1FFFE945 at address 0x1FFFB004 for bootloader V2.0 0x1FFFE9A1 for bootloader V2.1, and 0x1FFFE9C1 for bootloader V2.2.
- The DFU version is the following:
  - V2.1 in bootloader V2.1
  - V2.2 in bootloader V2.2.

  It can be read through the bcdDevice field of the DFU Device Descriptor.

14.3.2 Bootloader unavailability on STM32F105xx/STM32F107xx devices with a date code below 937

Description

The bootloader cannot be used if the USART1_RX (PA10), USART2_RX (PD6, remapped), CAN2_Rx (PB5, remapped), OTG_FS_DM (PA11), and/or OTG_FS_DP (PA12) pin(s) are held low or left floating during the bootloader activation phase.

The bootloader cannot be connected through CAN2 (remapped), DFU (OTG FS in Device mode), USART1 or USART2 (remapped).

On 64-pin packages, the USART2_RX signal remapped PD6 pin is not available and it is internally grounded. In this case, the bootloader cannot be used at all.

Workaround

- For 64-pin packages

  None. The bootloader cannot be used.
- For 100-pin packages

  Depending on the used peripheral, the pins for the unused peripherals have to be kept at a high level during the bootloader activation phase as described below:
  - If USART1 is used to connect to the bootloader, PD6 and PB5 have to be kept at a high level.
  - If USART2 is used to connect to the bootloader, PA10, PB5, PA11 and PA12 have to be kept at a high level.
  - If CAN2 is used to connect to the bootloader, PA10, PD6, PA11 and PA12 have to be kept at a high level.
  - If DFU is used to connect to the bootloader, PA10, PB5 and PD6 have to be kept at a high level.

Note: This limitation applies only to STM32F105xx and STM32F107xx devices with a date code below 937. STM32F105xx and STM32F107xx devices with a date code higher or equal to 937 are not impacted. See STM32F105xx and STM32F107xx datasheets for where to find the date code on the device marking.

14.3.3 USART bootloader Get-Version command returns 0x20 instead of 0x22

Description

In USART mode, the Get-Version command (defined in AN3155) returns 0x20 instead of 0x22.

This limitation is present on bootloader versions V1.0 and V2.0, while it is fixed in bootloader version 2.1.

Workaround

None.

14.3.4 PA9 excessive power consumption when USB cable is plugged in bootloader V2.0

Description

When connecting a USB cable after booting from System-Memory mode, PA9 pin (connected to V_{BUS}=5 V) is also shared with USART TX pin which is configured as alternate push-pull and forced to 0 since the USART peripheral is not yet clocked. As a consequence, a current higher than 25 mA is drained by PA9 I/O and may affect the I/O pad reliability.

This limitation is fixed in bootloader version 2.1 by configuring PA9 as alternate function push-pull when a correct 0x7F is received on RX pin and the USART is clocked. Otherwise, PA9 is configured as alternate input floating.

Workaround

None.

15 STM32F10xxx XL-density devices bootloader

15.1 Bootloader configuration

The STM32F10xxx XL-density bootloader is activated by applying pattern3 (described in *Table 2: Bootloader activation patterns*). The following table shows the hardware resources used by this bootloader:

Table 29. STM32F10xxx XL-density configuration in system memory boot mode

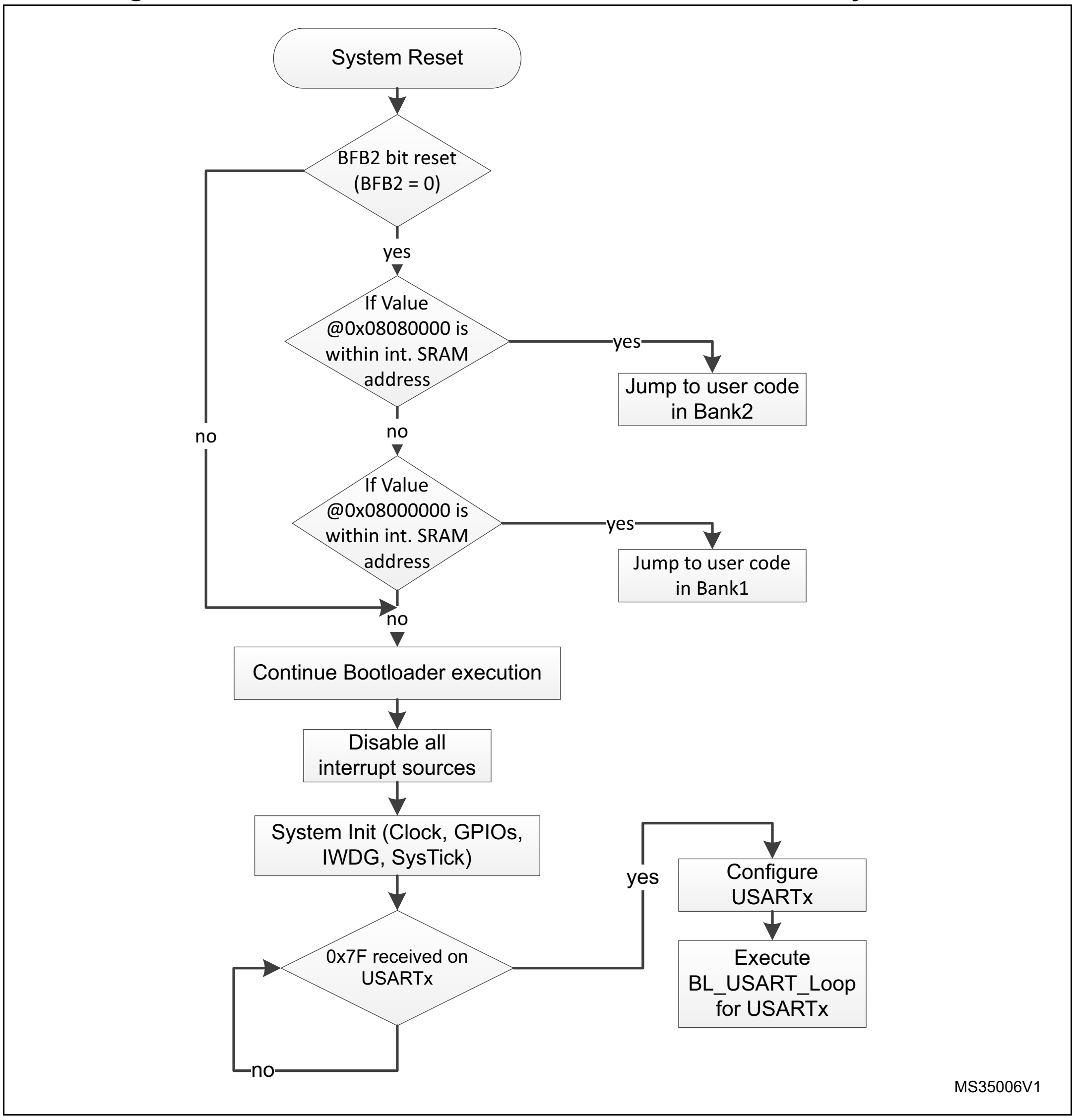
Bootloader	Feature/Peripheral	State	Comment
Common to all bootloaders	RCC	HSI enabled	The system clock frequency is 24 MHz using the PLL.
	RAM	-	2 Kbyte starting from address 0x20000000 are used by the bootloader firmware.
	System memory	-	6 Kbyte starting from address 0x1FFFE000 contain the bootloader firmware.
	IWDG	-	The independent watchdog (IWDG) prescaler is configured to its maximum value and is periodically refreshed to prevent watchdog reset (in case the hardware IWDG option was previously enabled by the user).
USART1 bootloader	USART1	Enabled	Once initialized, the USART1 configuration is: 8 bits, even parity and 1 Stop bit.
	USART1_RX pin	Input	PA10 pin: USART1 in reception mode
	USART1_TX pin	Output push-pull	PA9 pin: USART1 in transmission mode
USART2 bootloader	USART2	Enabled	Once initialized, the USART2 configuration is: 8 bits, even parity and 1 Stop bit.
	USART2_RX pin	Input	PD6 pin: USART2 receives (remapped pins).
	USART2_TX pin	Output push-pull	PD5 pin: USART2 transmits (remapped pins).
USARTx bootloaders	SysTick timer	Enabled	Used to automatically detect the serial baud rate from the host.

The system clock is derived from the embedded internal high-speed RC, no external quartz is required for the bootloader execution.

15.2 Bootloader selection

The figure below shows the bootloader selection mechanism.

Figure 18. Bootloader selection for STM32F10xxx XL-density devices



15.3 Bootloader version

The following table lists the STM32F10xxx XL-density devices bootloader versions:

Table 30. STM32F10xxx XL-density bootloader versions

Bootloader version number	Description
V2.1	Initial bootloader version

Note: The bootloader ID format is applied to all STM32 devices families except the STM32F1xx family. The bootloader version for the STM32F1xx applies only to the embedded device's bootloader version and not to its supported protocols.

16 STM32F2xxxx devices bootloader

Two bootloader versions are available on STM32F2xxxx devices:

- V2.x supporting USART1 and USART3
  This version is embedded in STM32F2xxxx devices revisions A, Z and B.
- V3.x supporting USART1, USART3, CAN2 and DFU (USB FS device)
  This version is embedded in STM32F2xxxx devices all other revisions (Y, X, W, 1, V, 2, 3, and 4).

16.1 Bootloader V2.x

16.1.1 Bootloader configuration

The STM32F2xxxx bootloader is activated by applying pattern1 (described in *Table 2: Bootloader activation patterns*). The following table shows the hardware resources used by this bootloader.

Table 31. STM32F2xxxx configuration in system memory boot mode

Bootloader	Feature/Peripheral	State	Comment
Common to all bootloaders	RCC	HSI enabled	The system clock frequency is 24 MHz.
	RAM	-	8 Kbyte starting from address 0x20000000.
	System memory	-	29 Kbyte starting from address 0x1FFF0000, contain the bootloader firmware.
	IWDG	-	The independent watchdog (IWDG) prescaler is configured to its maximum value and is periodically refreshed to prevent watchdog reset (in case the hardware IWDG option was previously enabled by the user).
	Power	-	Voltage range is set to [1.62 V, 2.1 V]. In this range internal Flash write operations are allowed only in byte format (Half-Word, Word and Double-Word operations are not allowed). The voltage range can be configured in run time using bootloader commands.
USART1 bootloader	USART1	Enabled	Once initialized, the USART1 configuration is: 8 bits, even parity and 1 Stop bit.
	USART1_RX pin	Input	PA10 pin: USART1 in reception mode
	USART1_TX pin	Output	PA9 pin: USART1 in transmission mode

Table 31. STM32F2xxxx configuration in system memory boot mode (continued)

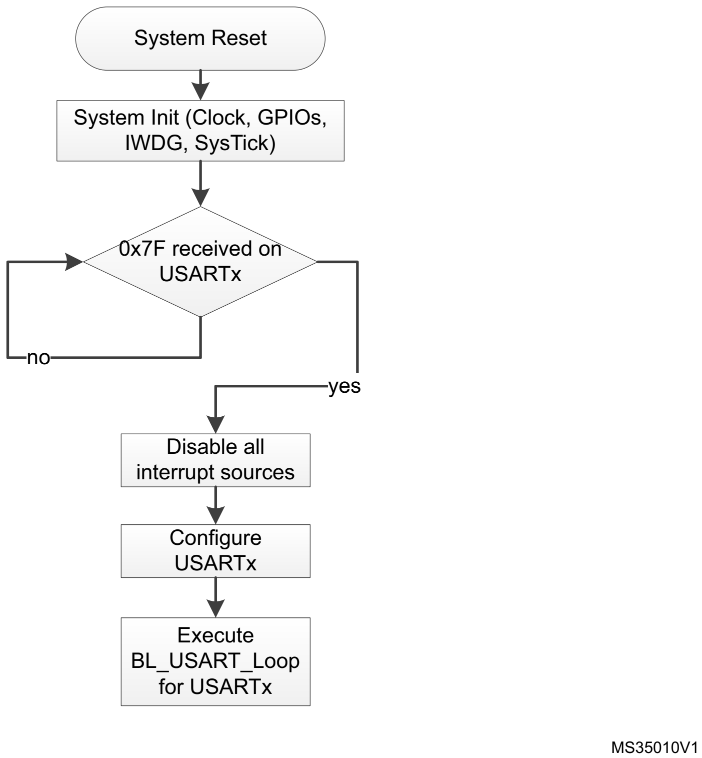
Bootloader	Feature/Peripheral	State	Comment
USART3 bootloader (on PC10/PC11)	USART3	Enabled	Once initialized, the USART3 configuration is: 8 bits, even parity and 1 Stop bit.
	USART3_RX pin	Input	PC11 pin: USART3 in reception mode
	USART3_TX pin	Output	PC10 pin: USART3 in transmission mode
USART3 bootloader (on PB10/PB11)	USART3	Enabled	Once initialized, the USART3 configuration is: 8 bits, even parity and 1 Stop bit
	USART3_RX pin	Input	PB11 pin: USART3 in reception mode
	USART3_TX pin	Output	PB10 pin: USART3 in transmission mode
USARTx bootloaders	SysTick timer	Enabled	Used to automatically detect the serial baud rate from the host.

The system clock is derived from the embedded internal high-speed RC. No external quartz is required for the bootloader code.

16.1.2 Bootloader selection

The figure below shows the bootloader selection mechanism.

Figure 19. Bootloader V2.x selection for STM32F2xxxx devices



16.1.3 Bootloader version

This following table lists the STM32F2xxxx devices V2.x bootloader versions:

Table 32. STM32F2xxxx bootloader V2.x versions

Bootloader version number	Description	Known limitations
V2.0	Initial bootloader version	When a Read Memory command or Write Memory command is issued with an unsupported memory address and a correct address checksum (ie. address 0x6000 0000), the command is aborted by the bootloader device, but the NACK (0x1F) is not sent to the host. As a result, the next 2 bytes (which are the number of bytes to be read/written and its checksum) are considered as a new command and its checksum. For the CAN interface, the Write Unprotect command is not functional. Instead you can use Write Memory command and write directly to the option bytes in order to disable the write protection.(1)

1. If the “number of data - 1” (N-1) to be read/written is not equal to a valid command code (0x00, 0x01, 0x02, 0x11, 0x21, 0x31, 0x43, 0x44, 0x63, 0x73, 0x82 or 0x92), then the limitation is not perceived from the host since the command is NACKed anyway (as an unsupported new command).

16.2 Bootloader V3.x

16.2.1 Bootloader configuration

The STM32F2xxxx bootloader is activated by applying pattern1 (described in *Table 2: Bootloader activation patterns*). The following table shows the hardware resources used by this bootloader.

Table 33. STM32F2xxxx configuration in system memory boot mode

Bootloader	Feature/Peripheral	State	Comment
Common to all bootloaders	RCC	HSI enabled	The system clock frequency is 24 MHz using the PLL. The HSI clock source is used at startup (interface detection phase) and when USARTx interfaces are selected (once CAN or DFU bootloader is selected, the clock source will be derived from the external crystal).
		HSE enabled	The system clock frequency is 60 MHz. The HSE clock source is used only when the CAN or the DFU (USB FS Device) interfaces are selected. The external clock must provide a frequency multiple of 1 MHz and ranging from 4 MHz to 26 MHz.
		-	The Clock Security System (CSS) interrupt is enabled for the CAN and DFU bootloaders. Any failure (or removal) of the external clock generates system reset.
	RAM	-	8 Kbyte starting from address 0x20000000 are used by the bootloader firmware.
	System memory	-	29 Kbyte starting from address 0x1FF00000 contain the bootloader firmware.
	IWDG	-	The independent watchdog (IWDG) prescaler is configured to its maximum value. It is periodically refreshed to prevent watchdog reset (in case the hardware IWDG option was previously enabled by the user).
	Power	-	Voltage range is set to [1.62 V, 2.1 V]. In this range internal Flash write operations are allowed only in byte format (Half-Word, Word and Double-Word operations are not allowed). The voltage range can be configured in run time using bootloader commands.

Table 33. STM32F2xxxx configuration in system memory boot mode (continued)

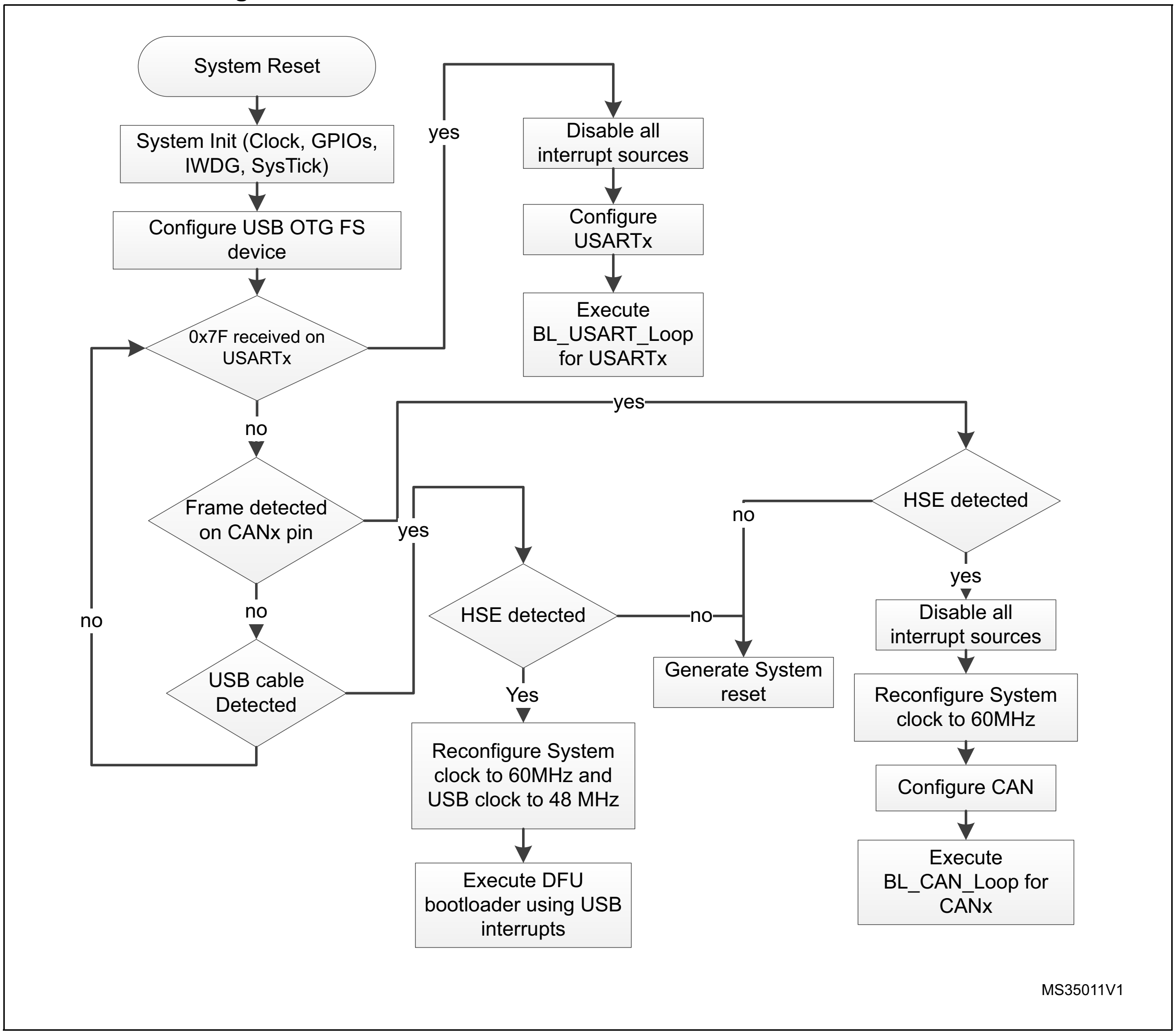
<table>
<tr><th>Bootloader</th><th>Feature/Peripheral</th><th>State</th><th>Comment</th></tr>
<tr><td rowspan="3">USART1 bootloader</td><td>USART1</td><td>Enabled</td><td>Once initialized, the USART1 configuration is: 8 bits, even parity and 1 Stop bit.</td></tr>
<tr><td>USART1_RX pin</td><td>Input</td><td>PA10 pin: USART1 in reception mode</td></tr>
<tr><td>USART1_TX pin</td><td>Output</td><td>PA9 pin: USART1 in transmission mode</td></tr>
<tr><td rowspan="3">USART3 bootloader (on PB10/PB11)</td><td>USART3</td><td>Enabled</td><td>Once initialized, the USART3 configuration is: 8 bits, even parity and 1 Stop bit.</td></tr>
<tr><td>USART3_RX pin</td><td>Input</td><td>PB11 pin: USART3 in reception mode</td></tr>
<tr><td>USART3_TX pin</td><td>Output</td><td>PB10 pin: USART3 in transmission mode</td></tr>
<tr><td rowspan="3">USART3 bootloader (on PC10/PC11)</td><td>USART3</td><td>Enabled</td><td>Once initialized, the USART3 configuration is: 8 bits, even parity and 1 Stop bit.</td></tr>
<tr><td>USART3_RX pin</td><td>Input</td><td>PC11 pin: USART3 in reception mode</td></tr>
<tr><td>USART3_TX pin</td><td>Output</td><td>PC10 pin: USART3 in transmission mode</td></tr>
<tr><td>USARTx bootloaders</td><td>SysTick timer</td><td>Enabled</td><td>Used to automatically detect the serial baud rate from the host for USARTx bootloaders.</td></tr>
<tr><td rowspan="3">CAN2 bootloader</td><td>CAN2</td><td>Enabled</td><td>Once initialized, the CAN2 configuration is: Baudrate 125 kbps, 11-bit identifier.
Note: CAN1 is clocked during CAN2 bootloader execution because CAN1 manages the communication between CAN2 and SRAM.</td></tr>
<tr><td>CAN2_RX pin</td><td>Input</td><td>PB5 pin: CAN2 in reception mode</td></tr>
<tr><td>CAN2_TX pin</td><td>Output</td><td>PB13 pin: CAN2 in transmission mode</td></tr>
<tr><td rowspan="3">DFU bootloader</td><td>USB</td><td>Enabled</td><td>USB OTG FS configured in forced device mode</td></tr>
<tr><td>USB_DM pin</td><td rowspan="2">Input/Output</td><td>PA11: USB DM line.</td></tr>
<tr><td>USB_DP pin</td><td>PA12: USB DP line
No external Pull-up resistor is required</td></tr>
<tr><td>CAN2 and DFU bootloaders</td><td>TIM11</td><td>Enabled</td><td>This timer is used to determine the value of the HSE. Once the HSE frequency is determined, the system clock is configured to 60 MHz using PLL and HSE.</td></tr>
</table>

The system clock is derived from the embedded internal high-speed RC for USARTx bootloaders. This internal clock is also used for CAN and DFU (USB FS Device) but only for the selection phase. An external clock multiple of 1 MHz (between 4 and 26 MHz) is required for CAN and DFU bootloader execution after the selection phase.

16.2.2 Bootloader selection

The figure below shows the bootloader selection mechanism.

Figure 20. Bootloader V3.x selection for STM32F2xxxx devices



16.2.3 Bootloader version

The following table lists the STM32F2xxxx devices V3.x bootloader versions:

Table 34. STM32F2xxxx bootloader V3.x versions

Bootloader version number	Description	Known limitations
V3.2	Initial bootloader version.	– When a Read Memory command or Write Memory command is issued with an unsupported memory address and a correct address checksum (ie. address 0x6000 0000), the command is aborted by the bootloader device, but the NACK (0x1F) is not sent to the host. As a result, the next 2 bytes (which are the number of bytes to be read/written and its checksum) are considered as a new command and its checksum(1). – Option bytes, OTP and Device Feature descriptors (in DFU interface) are set to “g” instead of “e” (not erasable memory areas).
V3.3	Fix V3.2 limitations. DFU interface robustness enhancement.	– For the USART interface, two consecutive NACKs (instead of 1 NACK) are sent when a Read Memory or Write Memory command is sent and the RDP level is active. – For the CAN interface, the Write Unprotect command is not functional. Instead you can use Write Memory command and write directly to the option bytes in order to disable the write protection.

1. If the “number of data - 1” (N-1) to be read/written is not equal to a valid command code (0x00, 0x01, 0x02, 0x11, 0x21, 0x31, 0x43, 0x44, 0x63, 0x73, 0x82 or 0x92), then the limitation is not perceived from the host since the command is NACKed anyway (as an unsupported new command).

17 STM32F301xx/302x4(6/8) devices bootloader

17.1 Bootloader configuration

The STM32F301xx/302x4(6/8) bootloader is activated by applying pattern2 (described in *Table 2: Bootloader activation patterns*). The following table shows the hardware resources used by this bootloader.

Table 35. STM32F301xx/302x4(6/8) configuration in system memory boot mode

Bootloader	Feature/Peripheral	State	Comment
Common to all bootloaders	RCC	HSI enabled	The system clock frequency is 48 MHz with HSI48 48 MHz as clock source.
		HSE enabled	The external clock can be used for all bootloader interfaces and should have one the following values [24,18,16,12,9,8,6,4,3] MHz. The PLL is used to generate the USB48 MHz clock and the 48 MHz clock for the system clock.
		-	The Clock Security System (CSS) interrupt is enabled for the DFU bootloader. Any failure (or removal) of the external clock generates system reset.
	RAM	-	6 Kbyte starting from address 0x20000000 are used by the bootloader firmware
	System memory	-	8 Kbyte starting from address 0x1FFFD800, contain the bootloader firmware
	IWDG	-	The independent watchdog (IWDG) prescaler is configured to its maximum value. It is periodically refreshed to prevent watchdog reset (in case the hardware IWDG option was previously enabled by the user).
USART1 bootloader	USART1	Enabled	Once initialized the USART1 configuration is: 8-bits, even parity and 1 Stop bit
	USART1_RX pin	Input	PA10 pin: USART1 in reception mode
	USART1_TX pin	Output	PA9 pin: USART1 in transmission mode
USART2 bootloader	USART2	Enabled	Once initialized the USART2 configuration is: 8-bits, even parity and 1 Stop bit
	USART2_RX pin	Input	PA3 pin: USART2 in reception mode
	USART2_TX pin	Output	PA2 pin: USART2 in transmission mode
USARTx bootloaders	SysTick timer	Enabled	Used to automatically detect the serial baud rate from the host for USARTx bootloaders.

Table 35. STM32F301xx/302x4(6/8) configuration in system memory boot mode (continued)

Bootloader	Feature/Peripheral	State	Comment
DFU bootloader	USB	Enabled	USB used in FS mode
	USB_DM pin	Input/Output	PA11: USB DM line.
	USB_DP pin		PA12: USB DP line An external pull-up resistor 1.5 KOhm must be connected to USB_DP pin.

The bootloader has two case of operation depending on the presence of the external clock (HSE) at bootloader startup:

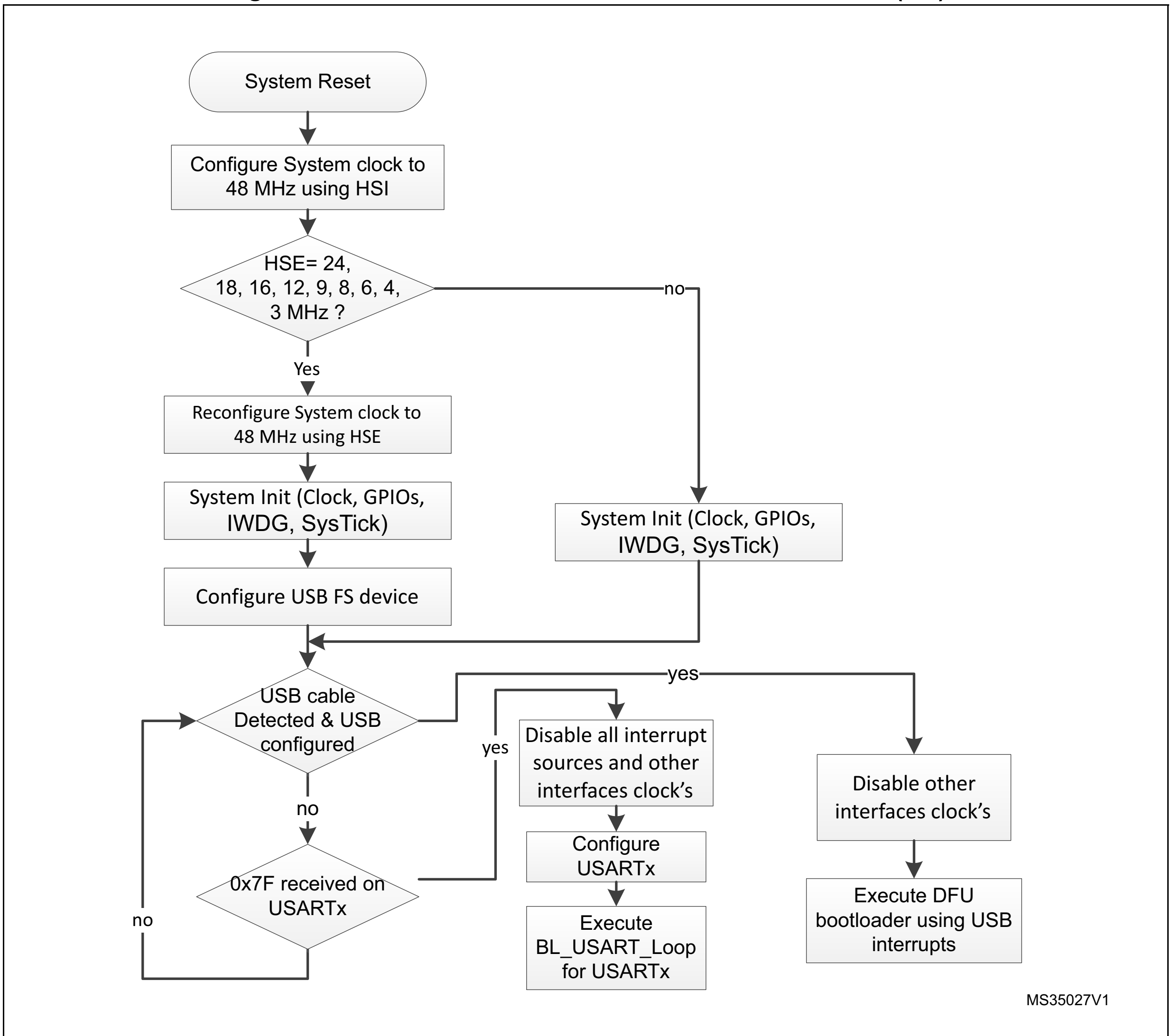
- If HSE is present and has a value of 24, 18, 16, 12, 9, 8, 6, 4 or 3 MHz, the system clock is configured to 48 MHz with HSE as clock source. The DFU interface, USART1 and USART2 are functional and can be used to communicate with the bootloader device.
- If HSE is not present, the HSI is kept as default clock source and only USART1 and USART2 are functional.

The external clock (HSE) must be kept if it's connected at bootloader startup because it will be used as system clock source.

17.2 Bootloader selection

The figure below shows the bootloader selection mechanism.

Figure 21. Bootloader selection for STM32F301xx/302x4(6/8)



17.3 Bootloader version

The following table lists the STM32F301xx/302x4(6/8) devices bootloader versions:

Table 36. STM32F301xx/302x4(6/8) bootloader versions

Bootloader version number	Description	Known limitations
V4.0	Initial bootloader version	None

18 STM32F302xB(C)/303xB(C) devices bootloader

18.1 Bootloader configuration

The STM32F302xB(C)/303xB(C) bootloader is activated by applying pattern2 (described in *Table 2: Bootloader activation patterns*). The following table shows the hardware resources used by this bootloader.

Table 37. STM32F302xB(C)/303xB(C) configuration in system memory boot mode

Bootloader	Feature/Peripheral	State	Comment
Common to all bootloaders	RCC	HSI enabled	At startup, the system clock frequency is configured to 48 MHz using the HSI. If an external clock (HSE) is not present, the system is kept clocked from the HSI.
		HSE enabled	The external clock can be used for all bootloader interfaces and should have one the following values [24, 18,16, 12, 9, 8, 6, 4, 3] MHz. The PLL is used to generate the USB 48 MHz clock and the 48 MHz clock for the system clock.
		-	The Clock Security System (CSS) interrupt is enabled for the DFU bootloader. Any failure (or removal) of the external clock generates system reset.
	RAM	-	5 Kbyte starting from address 0x20000000 are used by the bootloader firmware.
	System memory	-	8 Kbyte starting from address 0x1FFFD800, contains the bootloader firmware.
	IWDG	-	The independent watchdog (IWDG) prescaler is configured to its maximum value and is periodically refreshed to prevent watchdog reset (in case the hardware IWDG option was previously enabled by the user).
USART1 bootloader	USART1	Enabled	Once initialized, the USART1 configuration is: 8 bits, even parity and 1 Stop bit.
	USART1_RX pin	Input	PA10 pin: USART1 in reception mode
	USART1_TX pin	Output	PA9 pin: USART1 in transmission mode
USART2 bootloader	USART2	Enabled	Once initialized, the USART2 configuration is: 8 bits, even parity and 1 Stop bit. The USART2 uses its remapped pins.
	USART2_RX pin	Input	PD6 pin: USART2 in reception mode
	USART2_TX pin	Output	PD5 pin: USART2 in transmission mode
USARTx bootloaders	SysTick timer	Enabled	Used to automatically detect the serial baud rate from the host for USARTx bootloaders.

Table 37. STM32F302xB(C)/303xB(C) configuration in system memory boot mode (continued)

<table>
<tr><th>Bootloader</th><th>Feature/Peripheral</th><th>State</th><th>Comment</th></tr>
<tr><td rowspan="3">DFU bootloader</td><td>USB</td><td>Enabled</td><td>USB used in FS mode</td></tr>
<tr><td>USB_DM pin</td><td rowspan="2">Input/Output</td><td>PA11: USB DM line.</td></tr>
<tr><td>USB_DP pin</td><td>PA12: USB DP line
An external pull-up resistor 1.5 KOhm must be connected to USB_DP pin.</td></tr>
</table>

The bootloader has two case of operation depending on the presence of the external clock (HSE) at bootloader startup:

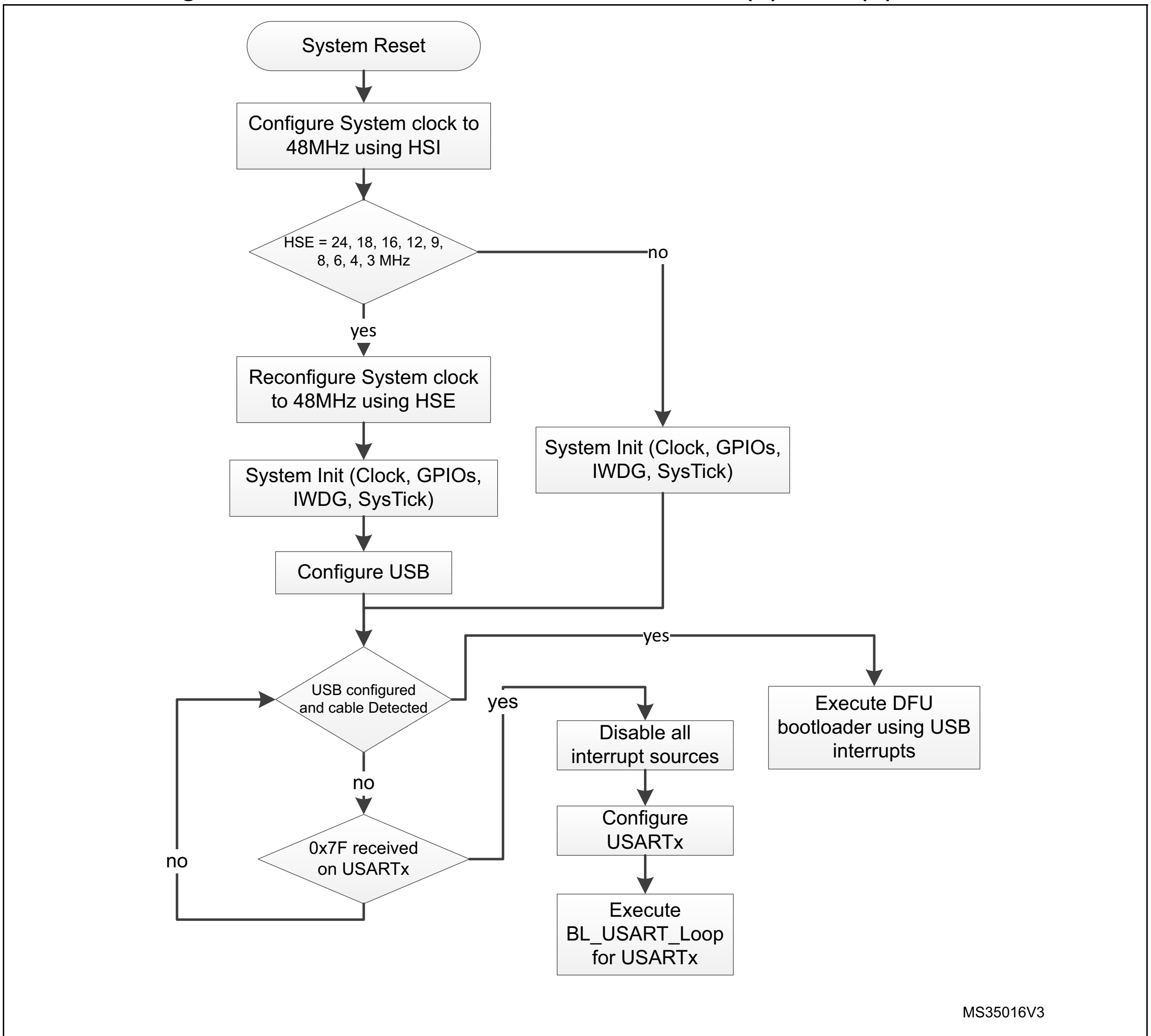
- If HSE is present and has a value of 24, 18, 16, 12, 9, 8, 6, 4 or 3 MHz, the system clock is configured to 48 MHz with HSE as clock source. The DFU interface, USART1 and USART2 are functional and can be used to communicate with the bootloader device.
- If HSE is not present, the HSI is kept as default clock source and only USART1 and USART2 are functional.

The external clock (HSE) must be kept if it’s connected at bootloader startup because it will be used as system clock source.

18.2 Bootloader selection

The figure below shows the bootloader selection mechanism.

Figure 22. Bootloader selection for STM32F302xB(C)/303xB(C) devices



18.3 Bootloader version

The following table lists the STM32F302xB(C)/303xB(C) devices bootloader versions.

Table 38. STM32F302xB(C)/303xB(C) bootloader versions

Bootloader version number	Description	Known limitations
V4.1	Initial bootloader version	None

19 STM32F302xD(E)/303xD(E) devices bootloader

19.1 Bootloader configuration

The STM32F302xD(E)/303xD(E) bootloader is activated by applying pattern2 (described in *Table 2: Bootloader activation patterns*). The following table shows the hardware resources used by this bootloader.

Table 39.STM32F302xD(E)/303xD(E) configuration in system memory boot mode

Bootloader	Feature/Peripheral	State	Comment
Common to all bootloaders	RCC	HSI enabled	The system clock frequency is 48 MHz with HSI48 48 MHz as clock source.
		HSE enabled	The external clock can be used for all bootloader interfaces and should have one the following values [24,18,16, 12, 9, 8, 6, 4, 3] MHz. The PLL is used to generate the USB 48 MHz clock and the 48 MHz clock for the system clock.
		-	The Clock Security System (CSS) interrupt is enabled for the DFU bootloader. Any failure (or removal) of the external clock generates system reset.
	RAM	-	6 Kbyte starting from address 0x20000000 are used by the bootloader firmware
	System memory	-	8 Kbyte starting from address 0x1FFFD800, contain the bootloader firmware
	IWDG	-	The independent watchdog (IWDG) prescaler is configured to its maximum value. It is periodically refreshed to prevent watchdog reset (in case the hardware IWDG option was previously enabled by the user).
USART1 bootloader	USART1	Enabled	Once initialized the USART1 configuration is: 8-bits, even parity and 1 Stop bit
	USART1_RX pin	Input	PA10 pin: USART1 in reception mode
	USART1_TX pin	Output	PA9 pin: USART1 in transmission mode
USART2 bootloader	USART2	Enabled	Once initialized the USART2 configuration is: 8-bits, even parity and 1 Stop bit
	USART2_RX pin	Input	PA3 pin: USART2 in reception mode
	USART2_TX pin	Output	PA2 pin: USART2 in transmission mode
USARTx bootloaders	SysTick timer	Enabled	Used to automatically detect the serial baud rate from the host for USARTx bootloaders.
DFU bootloader	USB	Enabled	USB FS configured in forced device mode. USB FS interrupt vector is enabled and used for USB DFU communications.
	USB_DM pin	Input/Output	PA11 pin: USB FS DM line.
	USB_DP pin		PA12 pin: USB FS DP line. An external pull-up resistor 1.5 KOhm must be connected to USB_DP pin.

The bootloader has two cases of operation depending on the presence of the external clock (HSE) at bootloader startup:

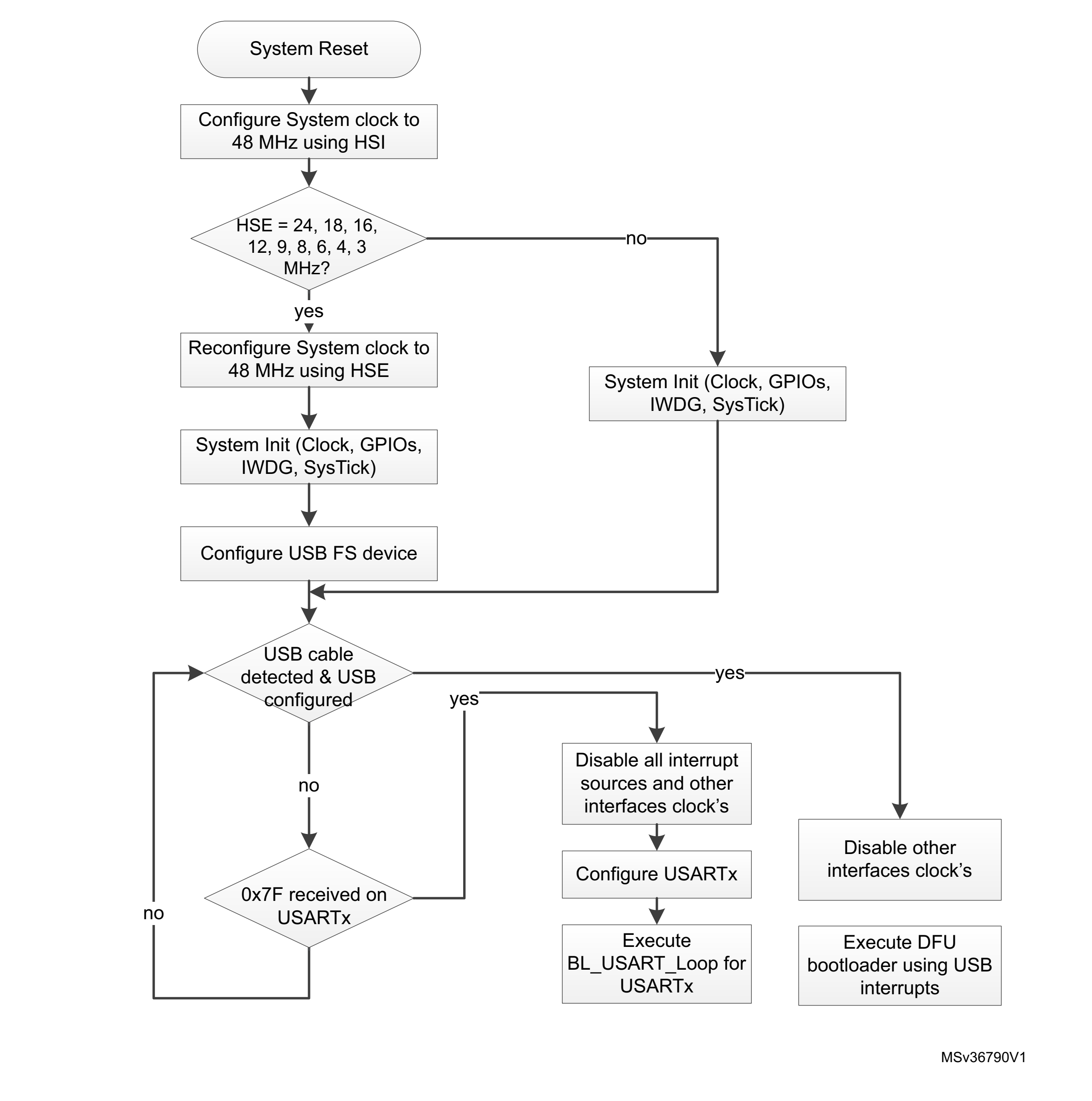
- If HSE is present and has a value of 24, 18, 16, 12, 9, 8, 6, 4 or 3 MHz, the system clock is configured to 48 MHz with HSE as clock source. The DFU interface, USART1 and USART2 are functional and can be used to communicate with the bootloader device.
- If HSE is not present, the HSI is kept as default clock source and only USART1 and USART2 are functional.

The external clock (HSE) must be kept if it’s connected at bootloader startup because it will be used as system clock source.

19.2 Bootloader selection

The figure below shows the bootloader selection mechanism.

Figure 23. Bootloader selection for STM32F302xD(E)/303xD(E)



19.3 Bootloader version

The following table lists the STM32F302xD(E)/303xD(E) devices bootloader versions.

Table 40. STM32F302xD(E)/303xD(E) bootloader versions

Bootloader version number	Description	Known limitations
V4.0	Initial bootloader version	None

20 STM32F303x4(6/8)/334xx/328xx devices bootloader

20.1 Bootloader configuration

The STM32F303x4(6/8)/334xx/328xx bootloader is activated by applying pattern2 (described in *Table 2: Bootloader activation patterns*). The following table shows the hardware resources used by this bootloader.

Table 41. STM32F303x4(6/8)/334xx/328xx configuration in system memory boot mode

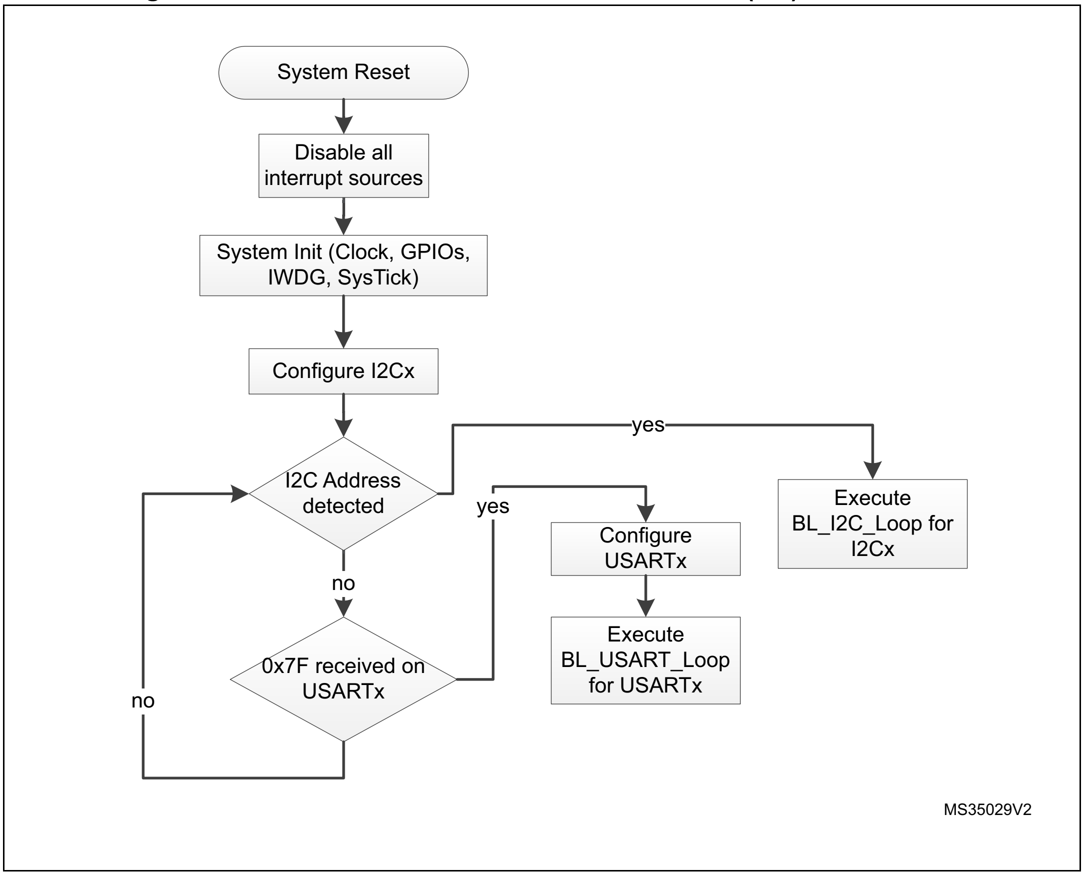
Bootloader	Feature/Peripheral	State	Comment
Common to all bootloaders	RCC	HSI enabled	The system clock frequency is 60 MHz with HSI 8 MHz as clock source.
	RAM	-	6 Kbyte starting from address 0x20000000 are used by the bootloader firmware
	System memory	-	8 Kbyte starting from address 0x1FFFD800, contain the bootloader firmware
	IWDG	-	The independent watchdog (IWDG) prescaler is configured to its maximum value. It is periodically refreshed to prevent watchdog reset (in case the hardware IWDG option was previously enabled by the user).
USART1 bootloader	USART1	Enabled	Once initialized the USART1 configuration is: 8-bits, even parity and 1 Stop bit
	USART1_RX pin	Input	PA10 pin: USART1 in reception mode
	USART1_TX pin	Output	PA9 pin: USART1 in transmission mode
USART2 bootloader	USART2	Enabled	Once initialized the USART2 configuration is: 8-bits, even parity and 1 Stop bit
	USART2_RX pin	Input	PA3 pin: USART2 in reception mode
	USART2_TX pin	Output	PA2 pin: USART2 in transmission mode
USARTx bootloaders	SysTick timer	Enabled	Used to automatically detect the serial baud rate from the host for USARTx bootloaders.
I2C1 bootloader	I2C1	Enabled	The I2C1 configuration is: I2C speed: up to 400 KHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b0111111x (where x = 0 for write and x = 1 for read)
	I2C1_SCL pin	Input/Output	PB6 pin: clock line is used in open-drain mode.
	I2C1_SDA pin	Input/Output	PB7 pin: data line is used in open-drain mode.

The system clock is derived from the embedded internal high-speed RC, no external quartz is required for the bootloader execution.

20.2 Bootloader selection

The figure below shows the bootloader selection mechanism.

Figure 24. Bootloader selection for STM32F303x4(6/8)/334xx/328xx



20.3 Bootloader version

The following table lists the STM32F303x4(6/8)/334xx/328xx devices bootloader versions:

Table 42. STM32F303x4(6/8)/334xx/328xx bootloader versions

Bootloader version number	Description	Known limitations
V5.0	Initial bootloader version	None

21 STM32F318xx devices bootloader

21.1 Bootloader configuration

The STM32F318xx bootloader is activated by applying pattern2 (described in *Table 2: Bootloader activation patterns*). The following table shows the hardware resources used by this bootloader.

Table 43. STM32F318xx configuration in system memory boot mode

Bootloader	Feature/Peripheral	State	Comment
Common to all bootloaders	RCC	HSI enabled	The system clock frequency is 60 MHz with HSI 8 MHz as clock source.
	RAM	-	6 Kbyte starting from address 0x20000000 are used by the bootloader firmware
	System memory	-	8 Kbyte starting from address 0x1FFFD800, contain the bootloader firmware
	IWDG	-	The independent watchdog (IWDG) prescaler is configured to its maximum value. It is periodically refreshed to prevent watchdog reset (in case the hardware IWDG option was previously enabled by the user).
USART1 bootloader	USART1	Enabled	Once initialized the USART1 configuration is: 8-bits, even parity and 1 Stop bit
	USART1_RX pin	Input	PA10 pin: USART1 in reception mode
	USART1_TX pin	Output	PA9 pin: USART1 in transmission mode
USART2 bootloader	USART2	Enabled	Once initialized the USART2 configuration is: 8-bits, even parity and 1 Stop bit
	USART2_RX pin	Input	PA3 pin: USART2 in reception mode
	USART2_TX pin	Output	PA2 pin: USART2 in transmission mode
USARTx bootloaders	SysTick timer	Enabled	Used to automatically detect the serial baud rate from the host for USARTx bootloaders.
I2C1 bootloader	I2C1	Enabled	The I2C1 configuration is: I2C speed: up to 400 KHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b0111101x (where x = 0 for write and x = 1 for read)
	I2C1_SCL pin	Input/Output	PB6 pin: clock line is used in open-drain mode.
	I2C1_SDA pin	Input/Output	PB7 pin: data line is used in open-drain mode.

Table 43. STM32F318xx configuration in system memory boot mode (continued)

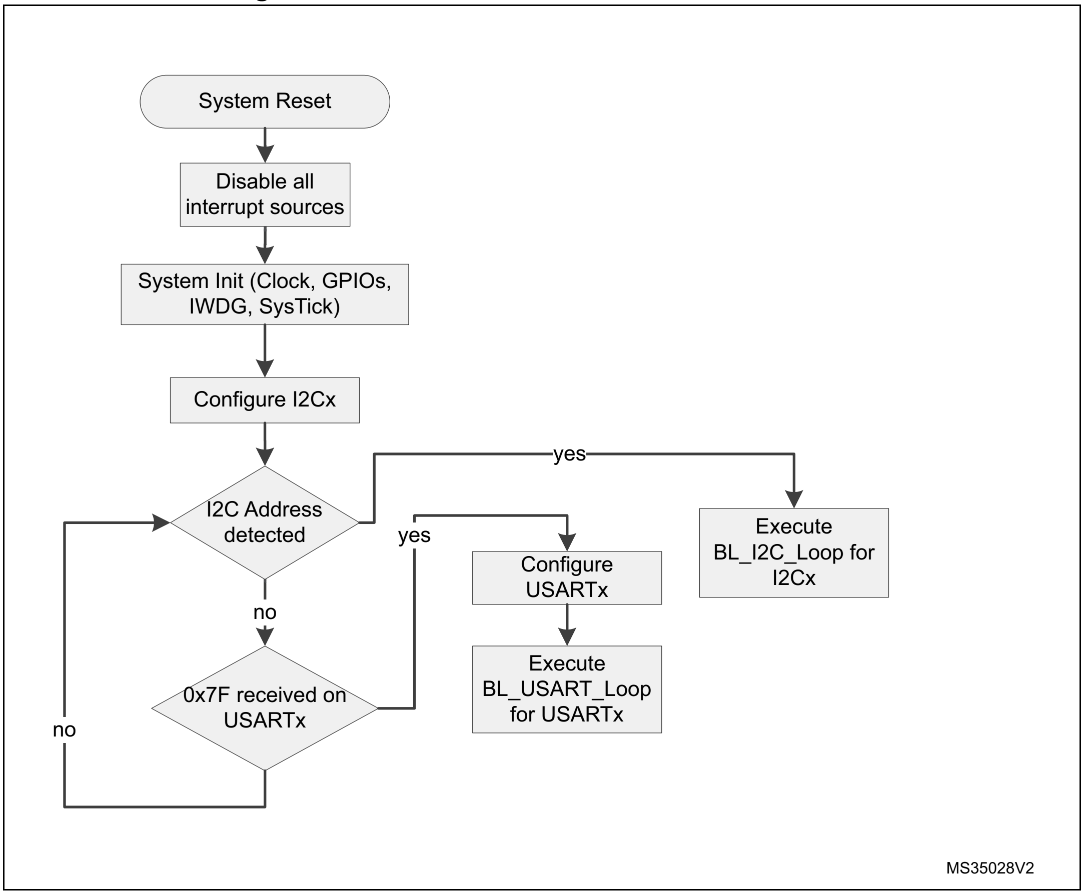
Bootloader	Feature/Peripheral	State	Comment
I2C3 bootloader	I2C3	Enabled	The I2C3 configuration is: I2C speed: up to 400 KHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b0111101x (where x = 0 for write and x = 1 for read) and digital filter disabled.
	I2C3_SCL pin	Input/Output	PA8 pin: clock line is used in open-drain mode.
	I2C3_SDA pin	Input/Output	PB5 pin: data line is used in open-drain mode.

The system clock is derived from the embedded internal high-speed RC, no external quartz is required for the bootloader execution.

21.2 Bootloader selection

The figure below shows the bootloader selection mechanism.

Figure 25. Bootloader selection for STM32F318xx



21.3 Bootloader version

The following table lists the STM32F318xx devices bootloader versions:

Table 44. STM32F318xx bootloader versions

Bootloader version number	Description	Known limitations
V5.0	Initial bootloader version	None

22 STM32F358xx devices bootloader

22.1 Bootloader configuration

The STM32F358xx bootloader is activated by applying pattern2 (described in *Table 2: Bootloader activation patterns*). The following table shows the hardware resources used by this bootloader.

Table 45. STM32F358xx configuration in system memory boot mode

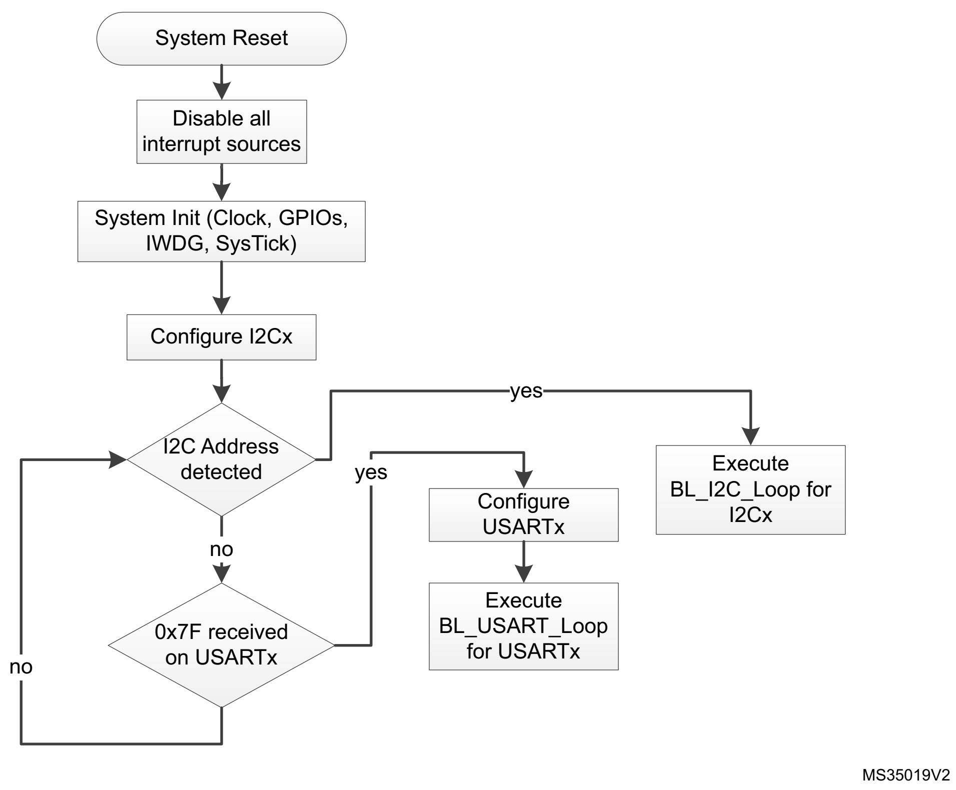
Bootloader	Feature/Peripheral	State	Comment
Common to all bootloaders	RCC	HSI enabled	The system clock frequency is 8 MHz using the HSI.
	RAM	-	5 Kbyte starting from address 0x20000000 are used by the bootloader firmware.
	System memory	-	8 Kbyte starting from address 0x1FFFD800, contains the bootloader firmware.
	IWDG	-	The independent watchdog (IWDG) prescaler is configured to its maximum value and is periodically refreshed to prevent watchdog reset (in case the hardware IWDG option was previously enabled by the user). Window feature is disabled.
USART1 bootloader	USART1	Enabled	Once initialized, the USART1 configuration is: 8 bits, even parity and 1 Stop bit.
	USART1_RX pin	Input	PA10 pin: USART1 in reception mode.
	USART1_TX pin	Output	PA9 pin: USART1 in transmission mode.
USART2 bootloader	USART2	Enabled	Once initialized, the USART2 configuration is: 8 bits, even parity and 1 Stop bit. The USART2 uses its remapped pins.
	USART2_RX pin	Input	PD6 pin: USART2 in reception mode.
	USART2_TX pin	Output	PD5 pin: USART2 in transmission mode.
USARTx bootloaders	SysTick timer	Enabled	Used to automatically detect the serial baud rate from the host for USARTx bootloader.
I2C1 bootloader	I2C1	Enabled	The I2C1 configuration is: I2C speed: up to 400 KHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b0110111x (where x = 0 for write and x = 1 for read)
	I2C1_SCL pin	Input/Output	PB6 pin: clock line is used in open-drain mode.
	I2C1_SDA pin	Input/Output	PB7 pin: data line is used in open-drain mode.

The system clock is derived from the embedded internal high-speed RC, no external quartz is required for the bootloader execution.

22.2 Bootloader selection

The figure below shows the bootloader selection mechanism.

Figure 26. Bootloader selection for STM32F358xx devices



22.3 Bootloader version

The following table lists the STM32F358xx devices bootloader versions.

Table 46. STM32F358xx bootloader versions

Bootloader version number	Description	Known limitations
V5.0	Initial bootloader version	For USART1 and USART2 interfaces, the maximum baudrate supported by the bootloader is 57600 baud.

23 STM32F373xx devices bootloader

23.1 Bootloader configuration

The STM32F373xx bootloader is activated by applying pattern2 (described in *Table 2: Bootloader activation patterns*). The following table shows the hardware resources used by this bootloader.

Table 47. STM32F373xx configuration in system memory boot mode

Bootloader	Feature/Peripheral	State	Comment
Common to all bootloaders	RCC	HSI enabled	At startup, the system clock frequency is configured to 48 MHz using the HSI. If an external clock (HSE) is not present, the system is kept clocked from the HSI.
		HSE enabled	The external clock can be used for all bootloader interfaces and should have one the following values [24,18,16,12,9,8,6,4,3] MHz. The PLL is used to generate the USB 48 MHz clock and the 48 MHz clock for the system clock.
		-	The Clock Security System (CSS) interrupt is enabled for the DFU bootloader. Any failure (or removal) of the external clock generates system reset.
	RAM	-	5 Kbyte starting from address 0x20000000 are used by the bootloader firmware.
	System memory	-	8 Kbyte starting from address 0x1FFFD800, contains the bootloader firmware
	IWDG	-	The independent watchdog (IWDG) prescaler is configured to its maximum value and is periodically refreshed to prevent watchdog reset (in case the hardware IWDG option was previously enabled by the user).
USART1 bootloader	USART1	Enabled	Once initialized, the USART1 configuration is: 8 bits, even parity and 1 Stop bit.
	USART1_RX pin	Input	PA10 pin: USART1 in reception mode
	USART1_TX pin	Output	PA9 pin: USART1 in transmission mode
USART2 bootloader	USART2	Enabled	Once initialized, the USART2 configuration is: 8 bits, even parity and 1 Stop bit. The USART2 uses its remapped pins.
	USART2_RX pin	Input	PD6 pin: USART2 in reception mode
	USART2_TX pin	Output	PD5 pin: USART2 in transmission mode
USARTx bootloaders	SysTick timer	Enabled	Used to automatically detect the serial baud rate from the host for USARTx bootloaders.

Table 47. STM32F373xx configuration in system memory boot mode (continued)

Bootloader	Feature/Peripheral	State	Comment
DFU bootloader	USB	Enabled	USB used in FS mode
	USB_DM pin	Input/Output	PA11: USB DM line.
	USB_DP pin		PA12: USB DP line An external pull-up resistor 1.5 KOhm must be connected to USB_DP pin.

The bootloader has two case of operation depending on the presence of the external clock (HSE) at bootloader startup:

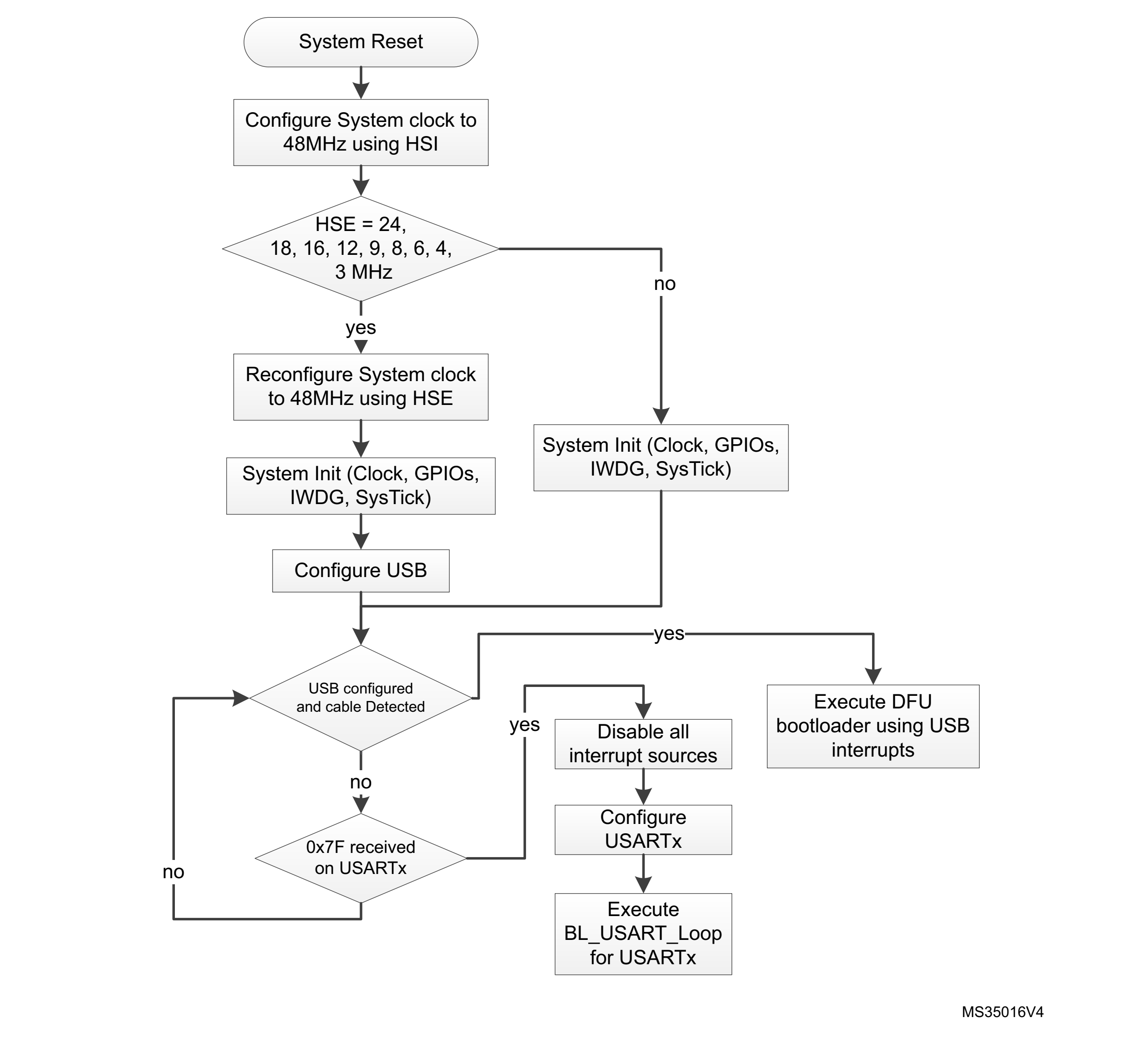
- If HSE is present and has a value of 24, 18, 16, 12, 9, 8, 6, 4 or 3 MHz, the system clock is configured to 48 MHz with HSE as clock source. The DFU interface, USART1 and USART2 are functional and can be used to communicate with the bootloader device.
- If HSE is not present, the HSI is kept as default clock source and only USART1 and USART2 are functional.

Note: The external clock (HSE) must be kept if it’s connected at bootloader startup because it will be used as system clock source.

23.2 Bootloader selection

The figure below shows the bootloader selection mechanism.

Figure 27. Bootloader selection for STM32F373xx devices



23.3 Bootloader version

The following table lists the STM32F373xx devices bootloader versions.

Table 48. STM32F373xx bootloader versions

Bootloader version number	Description	Known limitations
V4.1	Initial bootloader version	None

24 STM32F378xx devices bootloader

24.1 Bootloader configuration

The STM32F378xx bootloader is activated by applying pattern2 (described in *Table 2: Bootloader activation patterns*). The following table shows the hardware resources used by this bootloader.

Table 49. STM32F378xx configuration in system memory boot mode

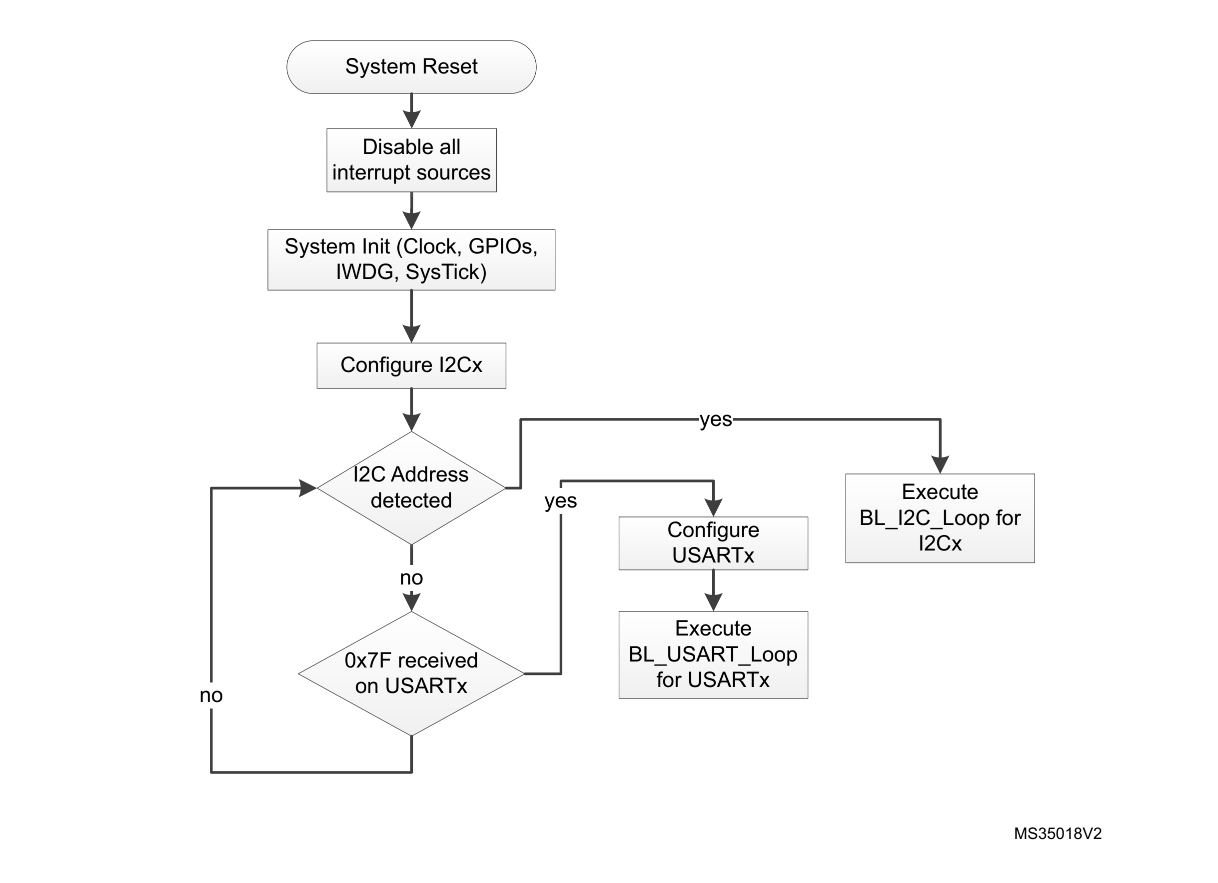
Bootloader	Feature/Peripheral	State	Comment
Common to all bootloaders	RCC	HSI enabled	The system clock frequency is 8 MHz using the HSI.
	RAM	-	4 Kbyte starting from address 0x20000000 are used by the bootloader firmware.
	System memory	-	8 Kbyte starting from address 0x1FFFD800, contains the bootloader firmware
	IWDG	-	The independent watchdog (IWDG) prescaler is configured to its maximum value and is periodically refreshed to prevent watchdog reset (in case the hardware IWDG option was previously enabled by the user). Window feature is disabled.
USART1 bootloader	USART1	Enabled	Once initialized, the USART1 configuration is: 8 bits, even parity and 1 Stop bit
	USART1_RX pin	Input	PA10 pin: USART1 in reception mode.
	USART1_TX pin	Output	PA9 pin: USART1 in transmission mode.
USART2 bootloader	USART2	Enabled	Once initialized, the USART2 configuration is: 8 bits, even parity and 1 Stop bit. The USART2 uses its remapped pins.
	USART2_RX pin	Input	PD6 pin: USART2 in reception mode.
	USART2_TX pin	Output	PD5 pin: USART2 in transmission mode.
USARTx bootloaders	SysTick timer	Enabled	Used to automatically detect the serial baud rate from the host for USARTx bootloader.
I2C1 bootloader	I2C1	Enabled	The I2C1 configuration is: I2C speed: up to 400 KHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b0110111x (where x = 0 for write and x = 1 for read).
	I2C1_SCL pin	Input/Output	PB6 pin: clock line is used in open-drain mode.
	I2C1_SDA pin	Input/Output	PB7 pin: data line is used in open-drain mode.

The system clock is derived from the embedded internal high-speed RC, no external quartz is required for the bootloader execution.

24.2 Bootloader selection

The figure below shows the bootloader selection mechanism.

Figure 28. Bootloader selection for STM32F378xx devices



24.3 Bootloader version

The following table lists the STM32F378xx devices bootloader versions.

Table 50. STM32F378xx bootloader versions

Bootloader version number	Description	Known limitations
V5.0	Initial bootloader version	For USART1 and USART2 interfaces, the maximum baudrate supported by the bootloader is 57600 baud.

25 STM32F398xx devices bootloader

25.1 Bootloader configuration

The STM32F398xx bootloader is activated by applying pattern2 (described in *Table 2: Bootloader activation patterns*). The following table shows the hardware resources used by this bootloader.

Table 51.STM32F398xx configuration in system memory boot mode

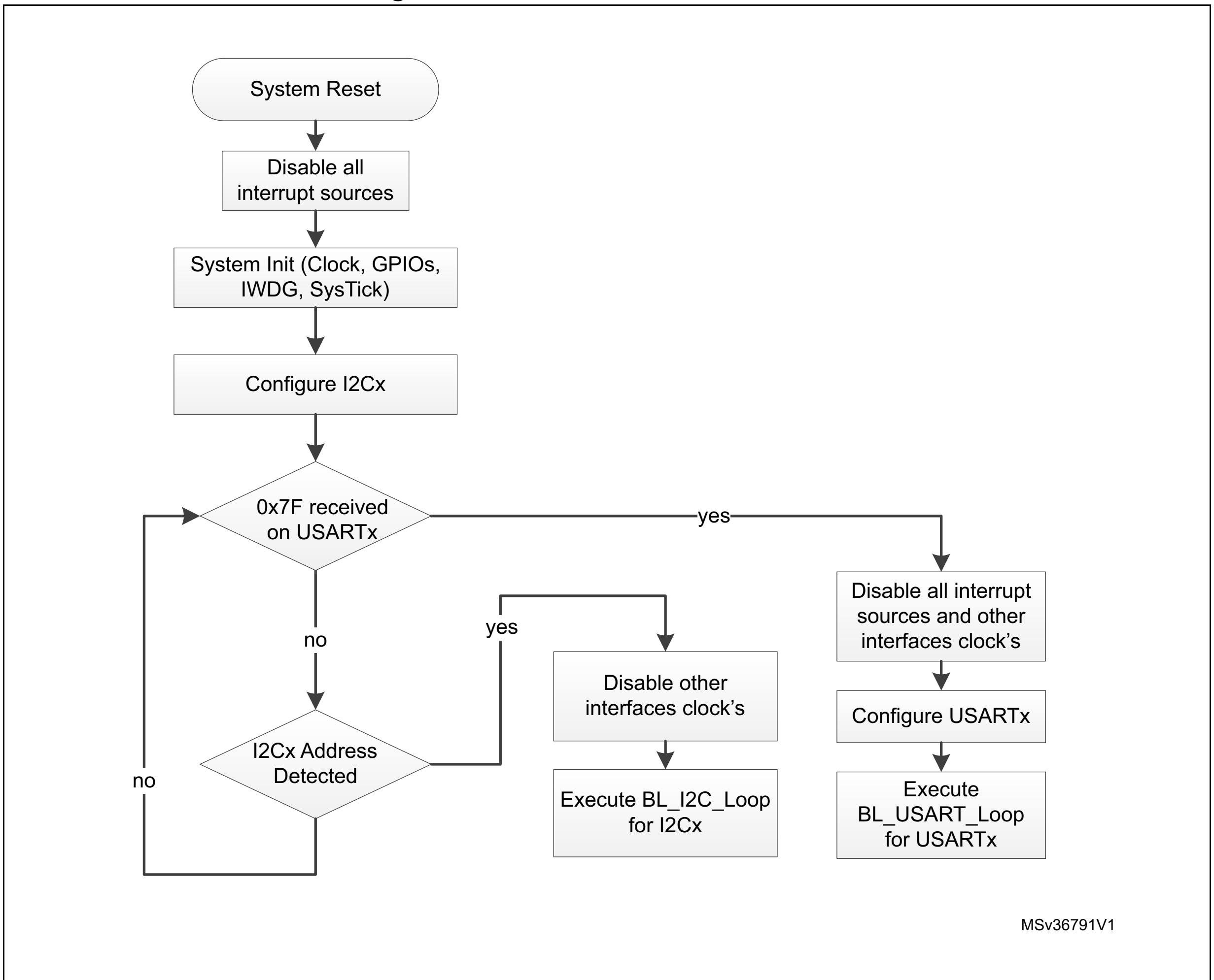
Bootloader	Feature/Peripheral	State	Comment
Common to all bootloaders	RCC	HSI enabled	The system clock frequency is 60 MHz with HSI 8 MHz as clock source.
	RAM	-	6 Kbyte starting from address 0x20000000 are used by the bootloader firmware
	System memory	-	7 Kbyte starting from address 0x1FFFD800, contain the bootloader firmware
	IWDG	-	The independent watchdog (IWDG) prescaler is configured to its maximum value. It is periodically refreshed to prevent watchdog reset (in case the hardware IWDG option was previously enabled by the user).
USART1 bootloader	USART1	Enabled	Once initialized the USART1 configuration is: 8-bits, even parity and 1 Stop bit
	USART1_RX pin	Input	PA10 pin: USART1 in reception mode
	USART1_TX pin	Output	PA9 pin: USART1 in transmission mode
USART2 bootloader	USART2	Enabled	Once initialized the USART2 configuration is: 8-bits, even parity and 1 Stop bit
	USART2_RX pin	Input	PA3 pin: USART2 in reception mode
	USART2_TX pin	Output	PA2 pin: USART2 in transmission mode
USARTx bootloaders	SysTick timer	Enabled	Used to automatically detect the serial baud rate from the host for USARTx bootloaders.
I2C1 bootloader	I2C1	Enabled	The I2C1 configuration is: I2C speed: up to 400 KHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b1000000x (where x = 0 for write and x = 1 for read).
	I2C1_SCL pin	Input/Output	PB6 pin: clock line is used in open-drain mode.
	I2C1_SDA pin	Input/Output	PB7 pin: data line is used in open-drain mode.
I2C3 bootloader	I2C3	Enabled	The I2C3 configuration is: I2C speed: up to 400 KHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b1000000x (where x = 0 for write and x = 1 for read).
	I2C3_SCL pin	Input/Output	PA8 pin: clock line is used in open-drain mode.
	I2C3_SDA pin	Input/Output	PB5 pin: data line is used in open-drain mode.

The system clock is derived from the embedded internal high-speed RC for all bootloader interfaces. No external quartz is required for bootloader operations.

25.2 Bootloader selection

The figure below shows the bootloader selection mechanism.

Figure 29.Bootloader selection for STM32F398xx



25.3 Bootloader version

The following table lists the STM32F398xx devices bootloader versions.

Table 52. STM32F398xx bootloader versions

Bootloader version number	Description	Known limitations
V5.0	Initial bootloader version	None

26 STM32F40xxx/41xxx devices bootloader

26.1 Bootloader V3.x

26.1.1 Bootloader configuration

The STM32F40xxx/41xxx bootloader is activated by applying pattern1 (described in *Table 2: Bootloader activation patterns*). The following table shows the hardware resources used by this bootloader.

Table 53. STM32F40xxx/41xxx configuration in system memory boot mode

Bootloader	Feature/Peripheral	State	Comment
Common to all bootloaders	RCC	HSI enabled	The system clock frequency is 24 MHz using the PLL. The HSI clock source is used at startup (interface detection phase) and when USARTx interfaces are selected (once CAN or DFU bootloader is selected, the clock source will be derived from the external crystal).
		HSE enabled	The system clock frequency is 60 MHz. The HSE clock source is used only when the CAN or the DFU (USB FS Device) interfaces are selected. The external clock must provide a frequency multiple of 1 MHz and ranging from 4 MHz to 26 MHz.
		-	The Clock Security System (CSS) interrupt is enabled for the CAN and DFU bootloaders. Any failure (or removal) of the external clock generates system reset.
	RAM	-	8 Kbyte starting from address 0x20000000 are used by the bootloader firmware.
	System memory	-	29 Kbyte starting from address 0x1FFF 0000 contain the bootloader firmware.
	IWDG	-	The independent watchdog (IWDG) prescaler is configured to its maximum value. It is periodically refreshed to prevent watchdog reset (in case the hardware IWDG option was previously enabled by the user).
	Power	-	Voltage range is set to [1.62 V, 2.1 V]. In this range internal Flash write operations are allowed only in byte format (Half-Word, Word and Double-Word operations are not allowed). The voltage range can be configured in run time using bootloader commands.

Table 53. STM32F40xxx/41xxx configuration in system memory boot mode (continued)

Bootloader	Feature/Peripheral	State	Comment
USART1 bootloader	USART1	Enabled	Once initialized, the USART1 configuration is: 8 bits, even parity and 1 Stop bit.
	USART1_RX pin	Input	PA10 pin: USART1 in reception mode
	USART1_TX pin	Output	PA9 pin: USART1 in transmission mode
USART3 bootloader (on PB10/PB11)	USART3	Enabled	Once initialized, the USART3 configuration is: 8 bits, even parity and 1 Stop bit.
	USART3_RX pin	Input	PB11 pin: USART3 in reception mode
	USART3_TX pin	Output	PB10 pin: USART3 in transmission mode
USART3 bootloader (on PC10/PC11)	USART3	Enabled	Once initialized, the USART3 configuration is: 8 bits, even parity and 1 Stop bit.
	USART3_RX pin	Input	PC11 pin: USART3 in reception mode
	USART3_TX pin	Output	PC10 pin: USART3 in transmission mode
USARTx bootloaders	SysTick timer	Enabled	Used to automatically detect the serial baud rate from the host for USARTx bootloaders.
CAN2 bootloader	CAN2	Enabled	Once initialized, the CAN2 configuration is: Baudrate 125 kbps, 11-bit identifier. **Note:** CAN1 is clocked during CAN2 bootloader execution because CAN1 manages the communication between CAN2 and SRAM.
	CAN2_RX pin	Input	PB5 pin: CAN2 in reception mode
	CAN2_TX pin	Output	PB13 pin: CAN2 in transmission mode
DFU bootloader	USB	Enabled	USB OTG FS configured in forced device mode
	USB_DM pin	Input/Output	PA11: USB DM line.
	USB_DP pin		PA12: USB DP line No external Pull-up resistor is required
CAN2 and DFU bootloaders	TIM11	Enabled	This timer is used to determine the value of the HSE. Once the HSE frequency is determined, the system clock is configured to 60 MHz using PLL and HSE.

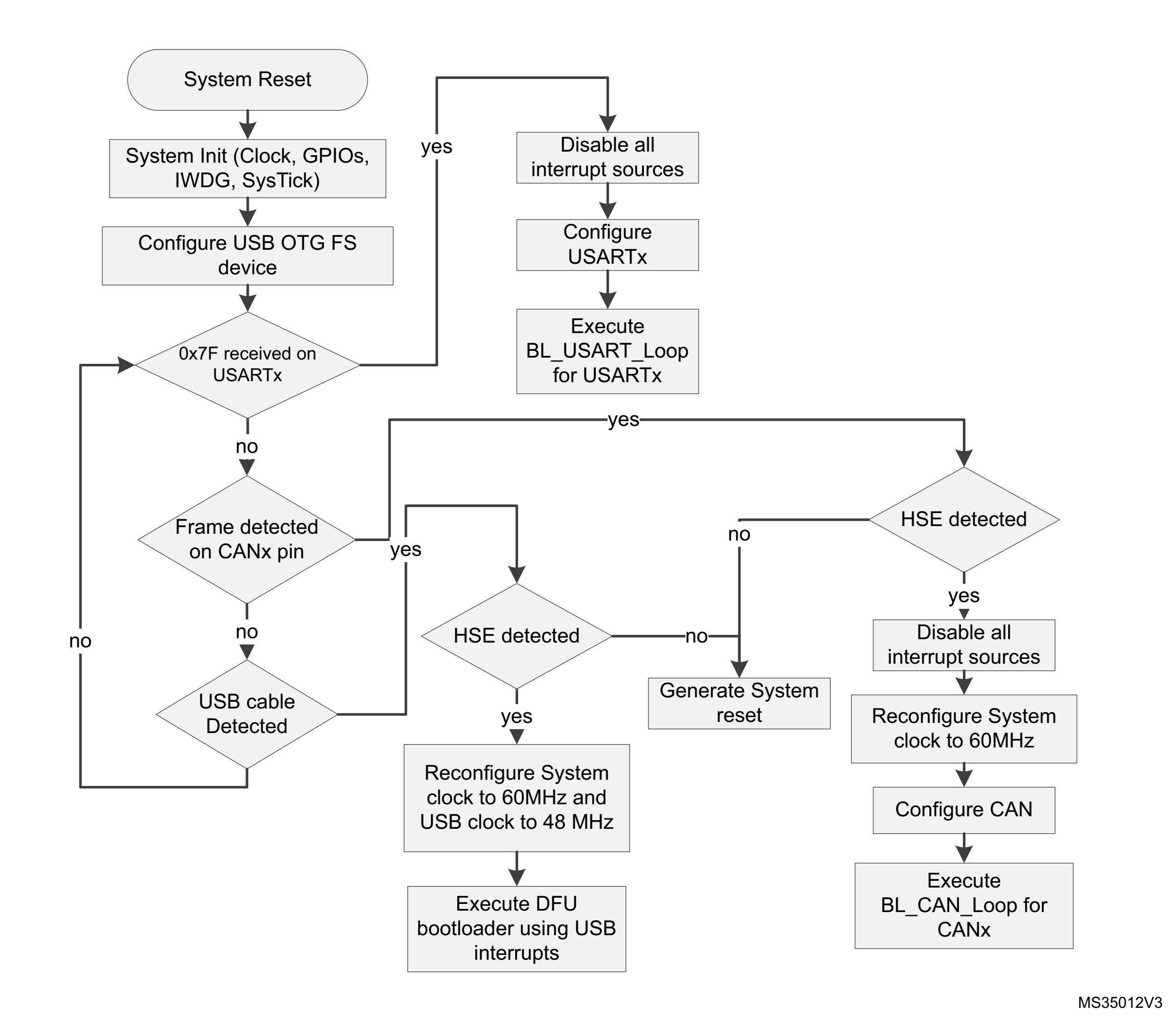
The system clock is derived from the embedded internal high-speed RC for USARTx bootloaders. This internal clock is also used for CAN and DFU (USB FS Device) but only for the selection phase. An external clock multiple of 1 MHz (between 4 and 26 MHz) is required for CAN and DFU bootloader execution after the selection phase.

Note: Due to HSI deviation and since HSI is used to detect HSE value, the user must use low frequency HSE crystal values rather than high frequency values.
Low frequency values are better detected due to larger error margin. For example, it is better to use 8 MHz instead of 25 MHz.

26.1.2 Bootloader selection

The figure below shows the bootloader selection mechanism.

Figure 30. Bootloader V3.x selection for STM32F40xxx/41xxx devices



26.1.3 Bootloader version

The following table lists the STM32F40xxx/41xxx devices V3.x bootloader versions:

Table 54. STM32F40xxx/41xxx bootloader V3.x versions

Bootloader version number	Description	Known limitations
V3.0	Initial bootloader version	– When a Read Memory command or Write Memory command is issued with an unsupported memory address and a correct address checksum (ie. address 0x6000 0000), the command is aborted by the bootloader device, but the NACK (0x1F) is not sent to the host. As a result, the next 2 bytes (which are the number of bytes to be read/written and its checksum) are considered as a new command and its checksum[(1)]. – Option bytes, OTP and Device Feature descriptors (in DFU interface) are set to “g” instead of “e” (not erasable memory areas). After executing Go command (jump to user code) the bootloader resets AHB1ENR value to 0x0000 0000 and thus CCM RAM, when present, is not active (shall be re-enabled by user code at startup)
V3.1	Fix V3.0 limitations. DFU interface robustness enhancement.	– For the USART interface, two consecutive NACKs (instead of 1 NACK) are sent when a Read Memory or Write Memory command is sent and the RDP level is active. – For the CAN interface, the Write Unprotect command is not functional. Instead you can use Write Memory command and write directly to the option bytes in order to disable the write protection. After executing Go command (jump to user code) the bootloader resets AHB1ENR value to 0x0000 0000 and thus CCM RAM, when present, is not active (shall be re-enabled by user code at startup)

1. If the “number of data - 1” (N-1) to be read/written is not equal to a valid command code (0x00, 0x01, 0x02, 0x11, 0x21, 0x31, 0x43, 0x44, 0x63, 0x73, 0x82 or 0x92), then the limitation is not perceived from the host since the command is NACKed anyway (as an unsupported new command).

26.2 Bootloader V9.x

26.2.1 Bootloader configuration

The STM32F40xxx/41xxx bootloader is activated by applying pattern1 (described in *Table 2: Bootloader activation patterns*). The following table shows the hardware resources used by this bootloader.

Note: The bootloader version V9.x is only embedded in STM32F405xx/415xx WCSP90 package devices.

Table 55. STM32F40xxx/41xxx configuration in system memory boot mode

Bootloader	Feature/Peripheral	State	Comment
Common to all bootloaders	RCC	HSI enabled	The system clock frequency is 60 MHz using the PLL. The HSI clock source is used at startup (interface detection phase) and when USART or SPI or I2C interfaces are selected (once CAN or DFU bootloader is selected, the clock source will be derived from the external crystal).
		HSE enabled	The system clock frequency is 60 MHz. The HSE clock source is used only when the CAN or the DFU (USB FS Device) interfaces are selected. The external clock must provide a frequency multiple of 1 MHz and ranging from 4 MHz to 26 MHz.
		-	The Clock Security System (CSS) interrupt is enabled for the CAN and DFU bootloaders. Any failure (or removal) of the external clock generates system reset.
	RAM	-	12 Kbyte starting from address 0x20000000 are used by the bootloader firmware
	System memory	-	29 Kbyte starting from address 0x1FFF0000, contain the bootloader firmware
	IWDG	-	The independent watchdog (IWDG) prescaler is configured to its maximum value. It is periodically refreshed to prevent watchdog reset (in case the hardware IWDG option was previously enabled by the user).
	Power	-	Voltage range is set to [1.62 V, 2.1 V]. In this range internal Flash write operations are allowed only in byte format (Half-Word, Word and Double-Word operations are not allowed). The voltage range can be configured in run time using bootloader commands.

Table 55. STM32F40xxx/41xxx configuration in system memory boot mode (continued)

Bootloader	Feature/Peripheral	State	Comment
USART1 bootloader	USART1	Enabled	Once initialized the USART1 configuration is: 8-bits, even parity and 1 Stop bit
	USART1_RX pin	Input	PA10 pin: USART1 in reception mode
	USART1_TX pin	Output	PA9 pin: USART1 in transmission mode
USART3 bootloader (on PB10/PB11)	USART3	Enabled	Once initialized the USART3 configuration is: 8-bits, even parity and 1 Stop bit
	USART3_RX pin	Input	PB11 pin: USART3 in reception mode
	USART3_TX pin	Output	PB10 pin: USART3 in transmission mode
USART3 bootloader (on PC10/PC11)	USART3	Enabled	Once initialized the USART3 configuration is: 8-bits, even parity and 1 Stop bit
	USART3_RX pin	Input	PC11 pin: USART3 in reception mode
	USART3_TX pin	Output	PC10 pin: USART3 in transmission mode
USARTx bootloaders	SysTick timer	Enabled	Used to automatically detect the serial baud rate from the host for USARTx bootloaders.
CAN2 bootloader	CAN2	Enabled	Once initialized the CAN2 configuration is: Baudrate 125 kbps, 11-bit identifier. **Note:** CAN1 is clocked during CAN2 bootloader execution because CAN1 manages the communication between CAN2 and SRAM.
	CAN2_RX pin	Input	PB5 pin: CAN2 in reception mode
	CAN2_TX pin	Output	PB13 pin: CAN2 in transmission mode
I2C1 bootloader	I2C1	Enabled	The I2C1 configuration is: I2C speed: up to 400 KHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b0111010x (where x = 0 for write and x = 1 for read).
	I2C1_SCL pin	Input/Output	PB6 pin: clock line is used in open-drain mode.
	I2C1_SDA pin	Input/Output	PB7 pin: data line is used in open-drain mode.
I2C2 bootloader	I2C2	Enabled	The I2C2 configuration is: I2C speed: up to 400 KHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b0111010x (where x = 0 for write and x = 1 for read).
	I2C2_SCL pin	Input/Output	PF1 pin: clock line is used in open-drain mode.
	I2C2_SDA pin	Input/Output	PF0 pin: data line is used in open-drain mode.

Table 55. STM32F40xxx/41xxx configuration in system memory boot mode (continued)

Bootloader	Feature/Peripheral	State	Comment
I2C3 bootloader	I2C3	Enabled	The I2C3 configuration is: I2C speed: up to 400 KHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b0111010x (where x = 0 for write and x = 1 for read).
	I2C3_SCL pin	Input/Output	PA8 pin: clock line is used in open-drain mode.
	I2C3_SDA pin	Input/Output	PC9 pin: data line is used in open-drain mode.
SPI1 bootloader	SPI1	Enabled	The SPI1 configuration is: slave mode, Full Duplex, 8-bit MSB, Speed up to 8 MHz, Polarity: CPOL Low, CPHA Low, NSS hardware.
	SPI1_MOSI pin	Input	PA7 pin: Slave data Input line, used in push-pull pull-down mode
	SPI1_MISO pin	Output	PA6 pin: Slave data output line, used in push-pull pull-down mode
	SPI1_SCK pin	Input	PA5 pin: Slave clock line, used in push-pull pull-down mode
	SPI1_NSS pin	Input	PA4 pin: slave chip select pin used in push-pull pull-down mode.
SPI2 bootloader	SPI2	Enabled	The SPI2 configuration is: Slave mode, Full Duplex, 8-bit MSB, Speed up to 8 MHz, Polarity: CPOL Low, CPHA Low, NSS hardware.
	SPI2_MOSI pin	Input	PI3 pin: Slave data Input line, used in push-pull pull-down mode
	SPI2_MISO pin	Output	PI2 pin: Slave data output line, used in push-pull pull-down mode
	SPI2_SCK pin	Input	PI1 pin: Slave clock line, used in push-pull pull-down mode
	SPI2_NSS pin	Input	PI0 pin: slave chip select pin used in push-pull pull-down mode.
DFU bootloader	USB	Enabled	USB OTG FS configured in forced device mode
	USB_DM pin	Input/Output	PA11: USB DM line.
	USB_DP pin		PA12: USB DP line No external Pull-up resistor is required
CAN2 and DFU bootloaders	TIM11	Enabled	This timer is used to determine the value of the HSE. Once the HSE frequency is determined, the system clock is configured to 60 MHz using PLL and HSE.

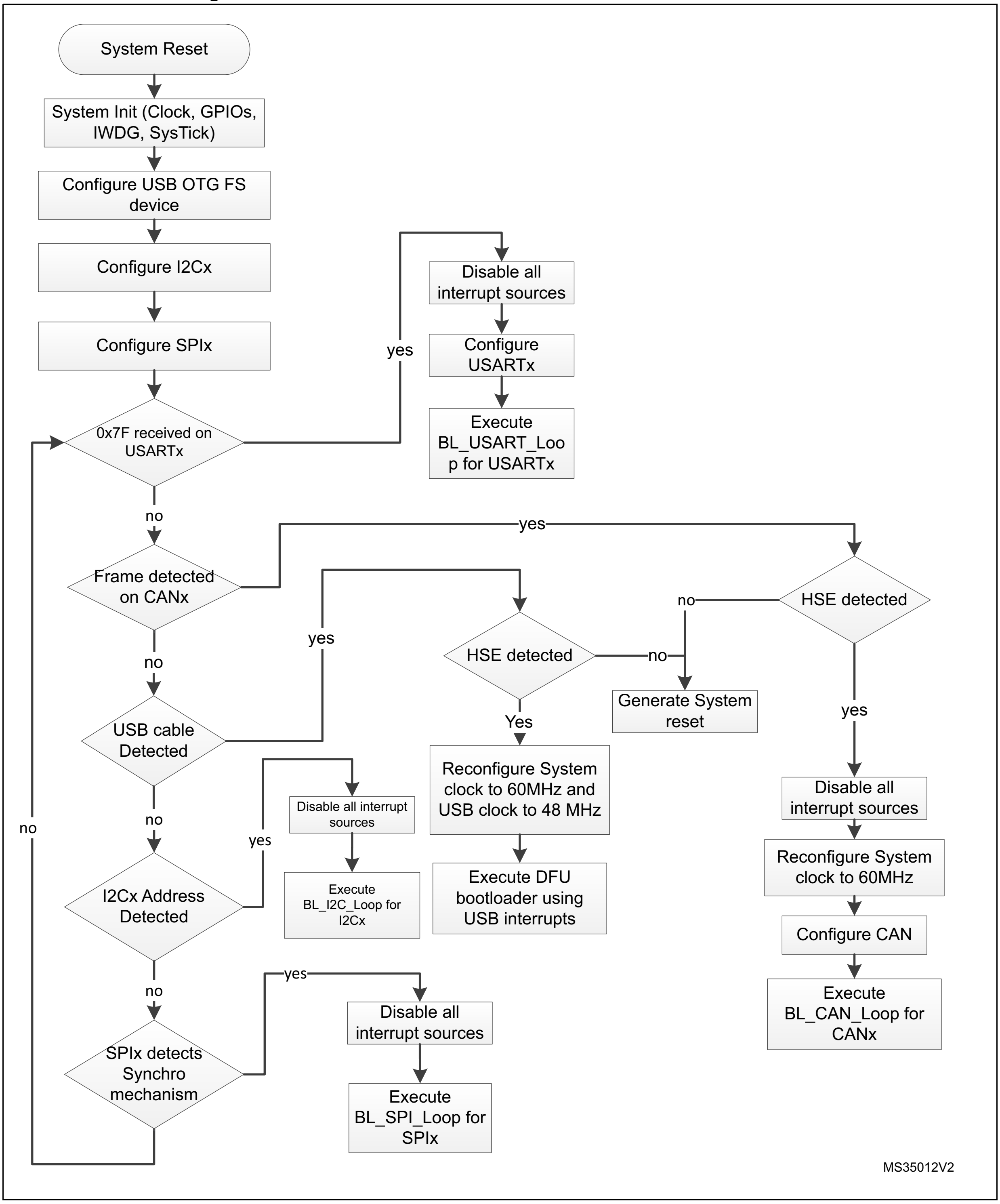
The system clock is derived from the embedded internal high-speed RC for USARTx, I2Cx and SPIx bootloaders. This internal clock is also used for CAN and DFU (USB FS Device) but only for the selection phase. An external clock multiple of 1 MHz (between 4 and 26 MHz) is required for CAN and DFU bootloader execution after the selection phase.

Note: Due to HSI deviation and since HSI is used to detect HSE value, the user must use low frequency HSE crystal values rather than high frequency values.
Low frequency values are better detected due to larger error margin. For example, it is better to use 8 MHz instead of 25 MHz.

26.2.2 Bootloader selection

The figure below shows the bootloader selection mechanism.

Figure 31. Bootloader V9.x selection for STM32F40xxx/41xxx



26.2.3 Bootloader version

The following table lists the STM32F40xxx/41xxx devices V9.x bootloader versions.

Table 56. STM32F40xxx/41xxx bootloader V9.x versions

Bootloader version number	Description	Known limitations
V9.0	This bootloader is an updated version of bootloader v3.1. This new version of bootloader supports I2C1, I2C2, I2C3, SPI1 and SPI2 interfaces. The RAM used by this bootloader is increased from 8Kb to 12Kb. The ID of this bootloader is 0x90. The connection time is increased.	– For the USART interface, two consecutive NACKs (instead of 1 NACK) are sent when a Read Memory or Write Memory command is sent and the RDP level is active. – For the CAN interface, the Write Unprotect command is not functional. Instead you can use Write Memory command and write directly to the option bytes in order to disable the write protection. After executing Go command (jump to user code) the bootloader resets AHB1ENR value to 0x0000 0000 and thus CCM RAM, when present, is not active (shall be re-enabled by user code at startup)

27 STM32F401xB(C) devices bootloader

27.1 Bootloader configuration

The STM32F401xB(C) bootloader is activated by applying pattern1 (described in *Table 2: Bootloader activation patterns*). The following table shows the hardware resources used by this bootloader.

Table 57. STM32F401xB(C) configuration in system memory boot mode

Bootloader	Feature/Peripheral	State	Comment
Common to all bootloaders	RCC	HSI enabled	The system clock frequency is 60 MHz using the PLL. The HSI clock source is used at startup (interface detection phase) and when USART or SPI or I2C interface is selected (once DFU bootloader is selected, the clock source will be derived from the external crystal).
		HSE enabled	The system clock frequency is 60 MHz. The HSE clock source is used only when the DFU (USB FS Device) interface is selected. The external clock must provide a frequency multiple of 1 MHz and ranging from 4 MHz to 26 MHz.
		-	The Clock Security System (CSS) interrupt is enabled for the CAN and DFU bootloaders. Any failure (or removal) of the external clock generates system reset.
	RAM	-	12 Kbyte starting from address 0x20000000 are used by the bootloader firmware
	System memory	-	29 Kbyte starting from address 0x1FFF0000, contain the bootloader firmware
	IWDG	-	The independent watchdog (IWDG) prescaler is configured to its maximum value. It is periodically refreshed to prevent watchdog reset (in case the hardware IWDG option was previously enabled by the user).
	Power	-	Voltage range is set to [1.62 V, 2.1 V]. In this range internal Flash write operations are allowed only in byte format (Half-Word, Word and Double-Word operations are not allowed). The voltage range can be configured in run time using bootloader commands.

Table 57. STM32F401xB(C) configuration in system memory boot mode (continued)

Bootloader	Feature/Peripheral	State	Comment
USART1 bootloader	USART1	Enabled	Once initialized the USART1 configuration is: 8-bits, even parity and 1 Stop bit
	USART1_RX pin	Input	PA10 pin: USART1 in reception mode
	USART1_TX pin	Output	PA9 pin: USART1 in transmission mode
USART2 bootloader	USART2	Enabled	Once initialized the USART2 configuration is: 8-bits, even parity and 1 Stop bit
	USART2_RX pin	Input	PD6 pin: USART2 in reception mode
	USART2_TX pin	Output	PD5 pin: USART2 in transmission mode
USARTx bootloaders	SysTick timer	Enabled	Used to automatically detect the serial baud rate from the host for USARTx bootloaders.
I2C1 bootloader	I2C1	Enabled	The I2C1 configuration is: I2C speed: up to 400 KHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b0111001x (where x = 0 for write and x = 1 for read)
	I2C1_SCL pin	Input/Output	PB6 pin: clock line is used in open-drain mode.
	I2C1_SDA pin	Input/Output	PB7 pin: data line is used in open-drain mode.
I2C2 bootloader	I2C2	Enabled	The I2C2 configuration is: I2C speed: up to 400 KHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b0111001x (where x = 0 for write and x = 1 for read)
	I2C2_SCL pin	Input/Output	PB10 pin: clock line is used in open-drain mode.
	I2C2_SDA pin	Input/Output	PB3 pin: data line is used in open-drain mode.
I2C3 bootloader	I2C3	Enabled	The I2C3 configuration is: I2C speed: up to 400 KHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b0111001x (where x = 0 for write and x = 1 for read)
	I2C3_SCL pin	Input/Output	PA8 pin: clock line is used in open-drain mode.
	I2C3_SDA pin	Input/Output	PB4 pin: data line is used in open-drain mode.

Table 57. STM32F401xB(C) configuration in system memory boot mode (continued)

Bootloader	Feature/Peripheral	State	Comment
SPI1 bootloader	SPI1	Enabled	The SPI1 configuration is: Slave mode, Full Duplex, 8-bit MSB, Speed up to 8 MHz, Polarity: CPOL Low, CPHA Low, NSS hardware.
	SPI1_MOSI pin	Input	PA7 pin: Slave data Input line, used in push-pull pull-down mode
	SPI1_MISO pin	Output	PA6 pin: Slave data output line, used in push-pull pull-down mode
	SPI1_SCK pin	Input	PA5 pin: Slave clock line, used in push-pull pull-down mode
	SPI1_NSS pin	Input	PA4 pin: slave chip select pin used in push-pull pull-down mode.
SPI2 bootloader	SPI2	Enabled	The SPI2 configuration is: Slave mode, Full Duplex, 8-bit MSB, Speed up to 8 MHz, Polarity: CPOL Low, CPHA Low, NSS hardware.
	SPI2_MOSI pin	Input	PB15 pin: Slave data Input line, used in push-pull pull-down mode
	SPI2_MISO pin	Output	PB14 pin: Slave data output line, used in push-pull pull-down mode
	SPI2_SCK pin	Input	PB13 pin: Slave clock line, used in push-pull pull-down mode
	SPI2_NSS pin	Input	PB12 pin: slave chip select pin used in push-pull pull-down mode.
SPI3 bootloader	SPI3	Enabled	The SPI3 configuration is: Slave mode, Full Duplex, 8-bit MSB, Speed up to 8 MHz, Polarity: CPOL Low, CPHA Low, NSS hardware.
	SPI3_MOSI pin	Input	PC12 pin: Slave data Input line, used in push-pull pull-down mode
	SPI3_MISO pin	Output	PC11 pin: Slave data output line, used in push-pull pull-down mode
	SPI3_SCK pin	Input	PC10 pin: Slave clock line, used in push-pull pull-down mode
	SPI3_NSS pin	Input	PA15 pin: slave chip select pin used in push-pull pull-down mode.

Table 57. STM32F401xB(C) configuration in system memory boot mode (continued)

Bootloader	Feature/Peripheral	State	Comment
DFU bootloader	USB	Enabled	USB OTG FS configured in forced device mode
	USB_DM pin	Input/Output	PA11: USB DM line.
	USB_DP pin		PA12: USB DP line No external Pull-up resistor is required
	TIM11	Enabled	This timer is used to determine the value of the HSE. Once the HSE frequency is determined, the system clock is configured to 60 MHz using PLL and HSE.

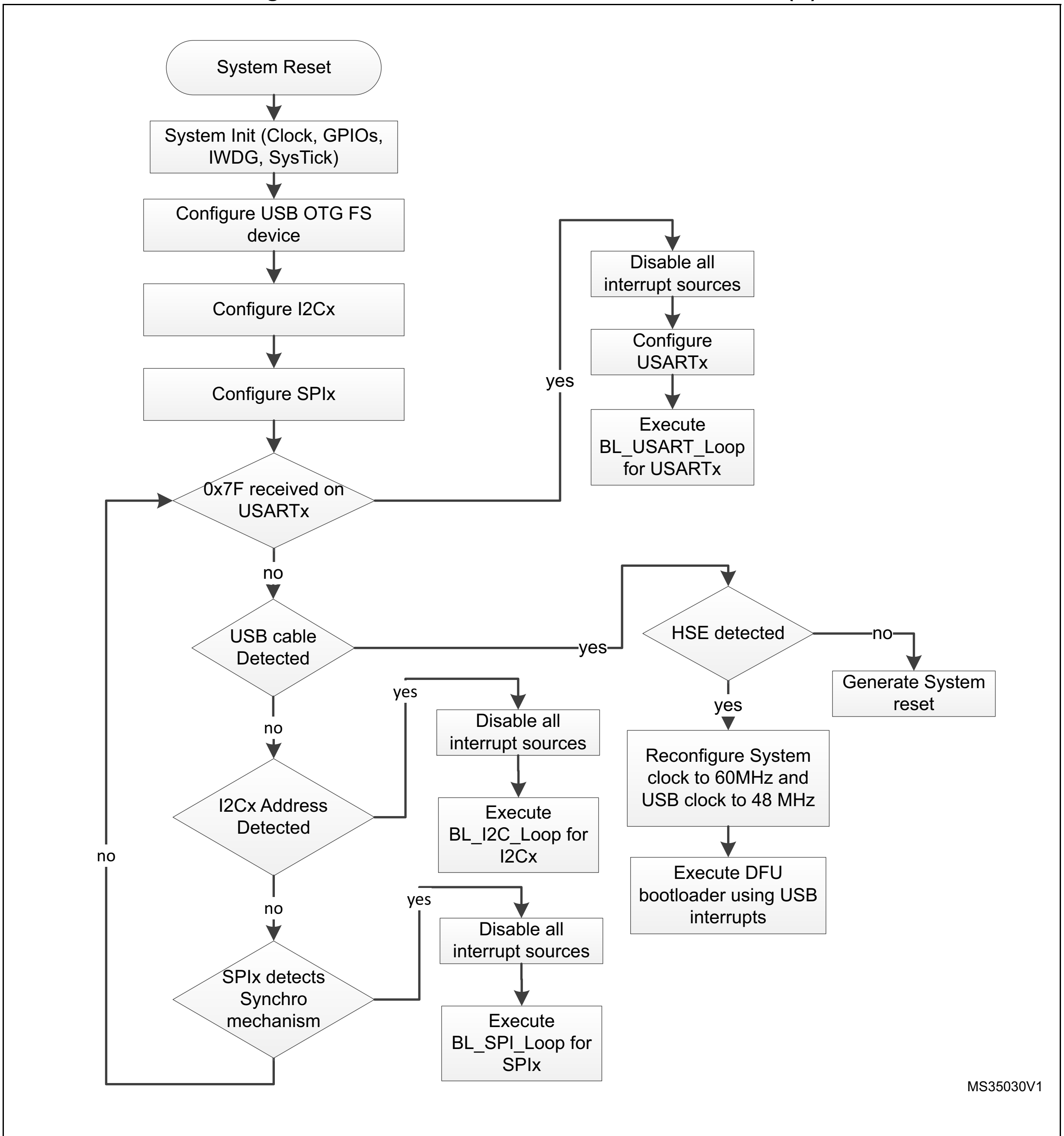
The system clock is derived from the embedded internal high-speed RC for USARTx, I2Cx and SPIx bootloaders. This internal clock is also used for CAN and DFU (USB FS Device) but only for the selection phase. An external clock multiple of 1 MHz (between 4 and 26 MHz) is required for CAN and DFU bootloader execution after the selection phase.

Note: Due to HSI deviation and since HSI is used to detect HSE value, the user must use low frequency HSE crystal values rather than high frequency values.
Low frequency values are better detected due to larger error margin. For example, it is better to use 8 MHz instead of 25 MHz.

27.2 Bootloader selection

The figure below shows the bootloader selection mechanism.

Figure 32. Bootloader selection for STM32F401xB(C)



27.3 Bootloader version

The following table lists the STM32F401xB(C) devices bootloader version.

Table 58. STM32F401xB(C) bootloader versions

Bootloader version number	Description	Known limitations
V13.0	Initial bootloader version	After executing Go command (jump to user code) the bootloader resets AHB1ENR value to 0x0000 0000 and thus CCM RAM, when present, is not active (shall be re-enabled by user code at startup)

28 STM32F401xD(E) devices bootloader

28.1 Bootloader configuration

The STM32F401xD(E) bootloader is activated by applying pattern1 (described in *Table 2: Bootloader activation patterns*). The following table shows the hardware resources used by this bootloader.

Table 59. STM32F401xD(E) configuration in system memory boot mode

Bootloader	Feature/Peripheral	State	Comment
Common to all bootloaders	RCC	HSI enabled	The system clock frequency is 60 MHz using the PLL. The HSI clock source is used at startup (interface detection phase) and when USART or SPI or I2C interface is selected (once DFU bootloader is selected, the clock source will be derived from the external crystal).
		HSE enabled	The system clock frequency is 60 MHz. The HSE clock source is used only when the DFU (USB FS Device) interface is selected. The external clock must provide a frequency multiple of 1 MHz and ranging from 4 MHz to 26 MHz.
		-	The Clock Security System (CSS) interrupt is enabled for the DFU bootloader. Any failure (or removal) of the external clock generates system reset.
	RAM	-	12 Kbyte starting from address 0x20000000 are used by the bootloader firmware
	System memory	-	29 Kbyte starting from address 0x1FFF0000, contain the bootloader firmware
	IWDG	-	The independent watchdog (IWDG) prescaler is configured to its maximum value. It is periodically refreshed to prevent watchdog reset (in case the hardware IWDG option was previously enabled by the user).
	Power	-	Voltage range is set to [1.62 V, 2.1 V]. In this range internal Flash write operations are allowed only in byte format (Half-Word, Word and Double-Word operations are not allowed). The voltage range can be configured in run time using bootloader commands.

Table 59. STM32F401xD(E) configuration in system memory boot mode (continued)

Bootloader	Feature/Peripheral	State	Comment
USART1 bootloader	USART1	Enabled	Once initialized the USART1 configuration is: 8-bits, even parity and 1 Stop bit
	USART1_RX pin	Input	PA10 pin: USART1 in reception mode
	USART1_TX pin	Output	PA9 pin: USART1 in transmission mode
USART2 bootloader	USART2	Enabled	Once initialized the USART2 configuration is: 8-bits, even parity and 1 Stop bit
	USART2_RX pin	Input	PD6 pin: USART2 in reception mode
	USART2_TX pin	Output	PD5 pin: USART2 in transmission mode
USARTx bootloaders	SysTick timer	Enabled	Used to automatically detect the serial baud rate from the host for USARTx bootloaders.
I2C1 bootloader	I2C1	Enabled	The I2C1 configuration is: I2C speed: up to 400 KHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b0111001x (where x = 0 for write and x = 1 for read)
	I2C1_SCL pin	Input/Output	PB6 pin: clock line is used in open-drain mode.
	I2C1_SDA pin	Input/Output	PB7 pin: data line is used in open-drain mode.
I2C2 bootloader	I2C2	Enabled	The I2C2 configuration is: I2C speed: up to 400 KHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b0111001x (where x = 0 for write and x = 1 for read)
	I2C2_SCL pin	Input/Output	PB10 pin: clock line is used in open-drain mode.
	I2C2_SDA pin	Input/Output	PB3 pin: data line is used in open-drain mode.
I2C3 bootloader	I2C3	Enabled	The I2C3 configuration is: I2C speed: up to 400 KHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b0111001x (where x = 0 for write and x = 1 for read)
	I2C3_SCL pin	Input/Output	PA8 pin: clock line is used in open-drain mode.
	I2C3_SDA pin	Input/Output	PB4 pin: data line is used in open-drain mode.

Table 59. STM32F401xD(E) configuration in system memory boot mode (continued)

Bootloader	Feature/Peripheral	State	Comment
SPI1 bootloader	SPI1	Enabled	The SPI1 configuration is: Slave mode, Full Duplex, 8-bit MSB, Speed up to 8 MHz, Polarity: CPOL Low, CPHA Low, NSS hardware.
	SPI1_MOSI pin	Input	PA7 pin: Slave data Input line, used in push-pull pull-down mode
	SPI1_MISO pin	Output	PA6 pin: Slave data output line, used in push-pull pull-down mode
	SPI1_SCK pin	Input	PA5 pin: Slave clock line, used in push-pull pull-down mode
	SPI1_NSS pin	Input	PA4 pin: slave chip select pin used in push-pull pull-down mode.
SPI2 bootloader	SPI2	Enabled	The SPI2 configuration is: Slave mode, Full Duplex, 8-bit MSB, Speed up to 8 MHz, Polarity: CPOL Low, CPHA Low, NSS hardware.
	SPI2_MOSI pin	Input	PB15 pin: Slave data Input line, used in push-pull pull-down mode
	SPI2_MISO pin	Output	PB14 pin: Slave data output line, used in push-pull pull-down mode
	SPI2_SCK pin	Input	PB13 pin: Slave clock line, used in push-pull pull-down mode
	SPI2_NSS pin	Input	PB12 pin: slave chip select pin used in push-pull pull-down mode.
SPI3 bootloader	SPI3	Enabled	The SPI3 configuration is: Slave mode, Full Duplex, 8-bit MSB, Speed up to 8 MHz, Polarity: CPOL Low, CPHA Low, NSS hardware.
	SPI3_MOSI pin	Input	PC12 pin: Slave data Input line, used in push-pull pull-down mode
	SPI3_MISO pin	Output	PC11 pin: Slave data output line, used in push-pull pull-down mode
	SPI3_SCK pin	Input	PC10 pin: Slave clock line, used in push-pull pull-down mode
	SPI3_NSS pin	Input	PA15 pin: slave chip select pin used in push-pull pull-down mode.
DFU bootloader	USB	Enabled	USB OTG FS configured in forced device mode
	USB_DM pin	Input/Output	PA11: USB DM line.
	USB_DP pin		PA12: USB DP line No external Pull-up resistor is required
	TIM11	Enabled	This timer is used to determine the value of the HSE. Once the HSE frequency is determined, the system clock is configured to 60 MHz using PLL and HSE.

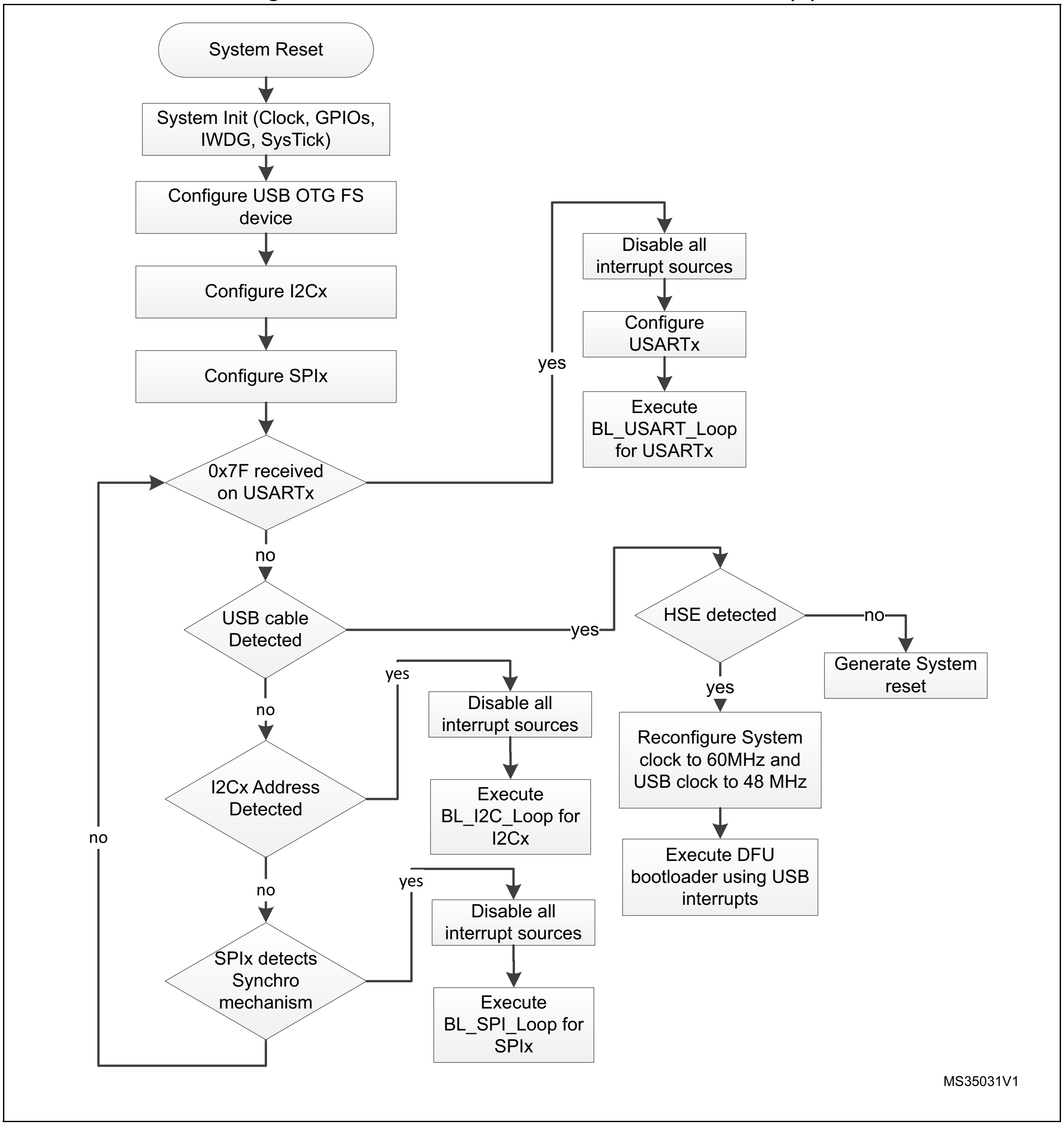
The system clock is derived from the embedded internal high-speed RC for USARTx, I2Cx and SPIx bootloaders. This internal clock is also used for DFU (USB FS Device) but only for the selection phase. An external clock multiple of 1 MHz (between 4 and 26 MHz) is required for DFU bootloader execution after the selection phase.

Note: Due to HSI deviation and since HSI is used to detect HSE value, the user must use low frequency HSE crystal values rather than high frequency values.
Low frequency values are better detected due to larger error margin. For example, it is better to use 8 MHz instead of 25 MHz.

28.2 Bootloader selection

The figure below shows the bootloader selection mechanism.

Figure 33. Bootloader selection for STM32F401xD(E)



28.3 Bootloader version

The following table lists the STM32F401xD(E) devices bootloader version.

Table 60. STM32F401xD(E) bootloader versions

Bootloader version number	Description	Known limitations
V13.1	Initial bootloader version	After executing Go command (jump to user code) the bootloader resets AHB1ENR value to 0x0000 0000 and thus CCM RAM, when present, is not active (shall be re-enabled by user code at startup)

29 STM32F410xx devices bootloader

29.1 Bootloader configuration

The STM32F410xx bootloader is activated by applying pattern1 (described in *Table 2: Bootloader activation patterns*). The following table shows the hardware resources used by this bootloader.

Table 61. STM32F410xx configuration in system memory boot mode

Bootloader	Feature/Peripheral	State	Comment
Common to all bootloaders	RCC	HSI enabled	The HSI is used at startup as clock source for system clock configured to 60 MHz and for USART and I2C bootloader operation.
	RAM	-	5 Kbyte starting from address 0x20000000 are used by the bootloader firmware
	System memory	-	29 Kbyte starting from address 0x1FFF0000, contain the bootloader firmware
	IWDG	-	The independent watchdog (IWDG) prescaler is configured to its maximum value. It is periodically refreshed to prevent watchdog reset (in case the hardware IWDG option was previously enabled by the user).
	Power	-	The voltage range is [1.8V, 3.6V] In this range: - Flash wait states 3. - System clock Frequency 60 MHz. - ART Accelerator enabled. - Flash write operation by byte (refer to bootloader memory management section for more information).
USART1 bootloader	USART1	Enabled	Once initialized the USART1 configuration is: 8-bits, even parity and 1 Stop bit
	USART1_RX pin	Input	PA10 pin: USART1 in reception mode
	USART1_TX pin	Output	PA9 pin: USART1 in transmission mode
USART2 bootloader	USART2	Enabled	Once initialized the USART2 configuration is: 8-bits, even parity and 1 Stop bit
	USART2_RX pin	Input	PA3 pin: USART2 in reception mode
	USART2_TX pin	Output	PA2 pin: USART2 in transmission mode
USARTx bootloaders	SysTick timer	Enabled	Used to automatically detect the serial baud rate from the host for USARTx bootloaders.

Table 61. STM32F410xx configuration in system memory boot mode (continued)

Bootloader	Feature/Peripheral	State	Comment
I2C1 bootloader	I2C1	Enabled	The I2C1 configuration is: I2C speed: up to 400 KHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b1000111x (where x = 0 for write and x = 1 for read)
	I2C1_SCL pin	Input/Output	PB6 pin: clock line is used in open-drain mode.
	I2C1_SDA pin	Input/Output	PB7 pin: data line is used in open-drain mode.
I2C2 bootloader	I2C2	Enabled	The I2C2 configuration is: I2C speed: up to 400 KHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b1000111x (where x = 0 for write and x = 1 for read)
	I2C2_SCL pin	Input/Output	PB10 pin: clock line is used in open-drain mode.
	I2C2_SDA pin	Input/Output	PB11 pin: data line is used in open-drain mode.
I2C4 bootloader	I2C4	Enabled	The I2C4 configuration is: I2C speed: up to 1 MHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b1000111x (where x = 0 for write and x = 1 for read)
	I2C4_SCL pin	Input/Output	PB15 pin: clock line is used in open-drain mode for STM32F410Cx/Rx devices. PB10 pin: clock line is used in open-drain mode for STM32F410Tx devices.
	I2C4_SDA pin	Input/Output	PB14 pin: data line is used in open-drain mode for STM32F410Cx/Rx devices. PB3 pin: data line is used in open-drain mode for STM32F410Tx devices.

Table 61. STM32F410xx configuration in system memory boot mode (continued)

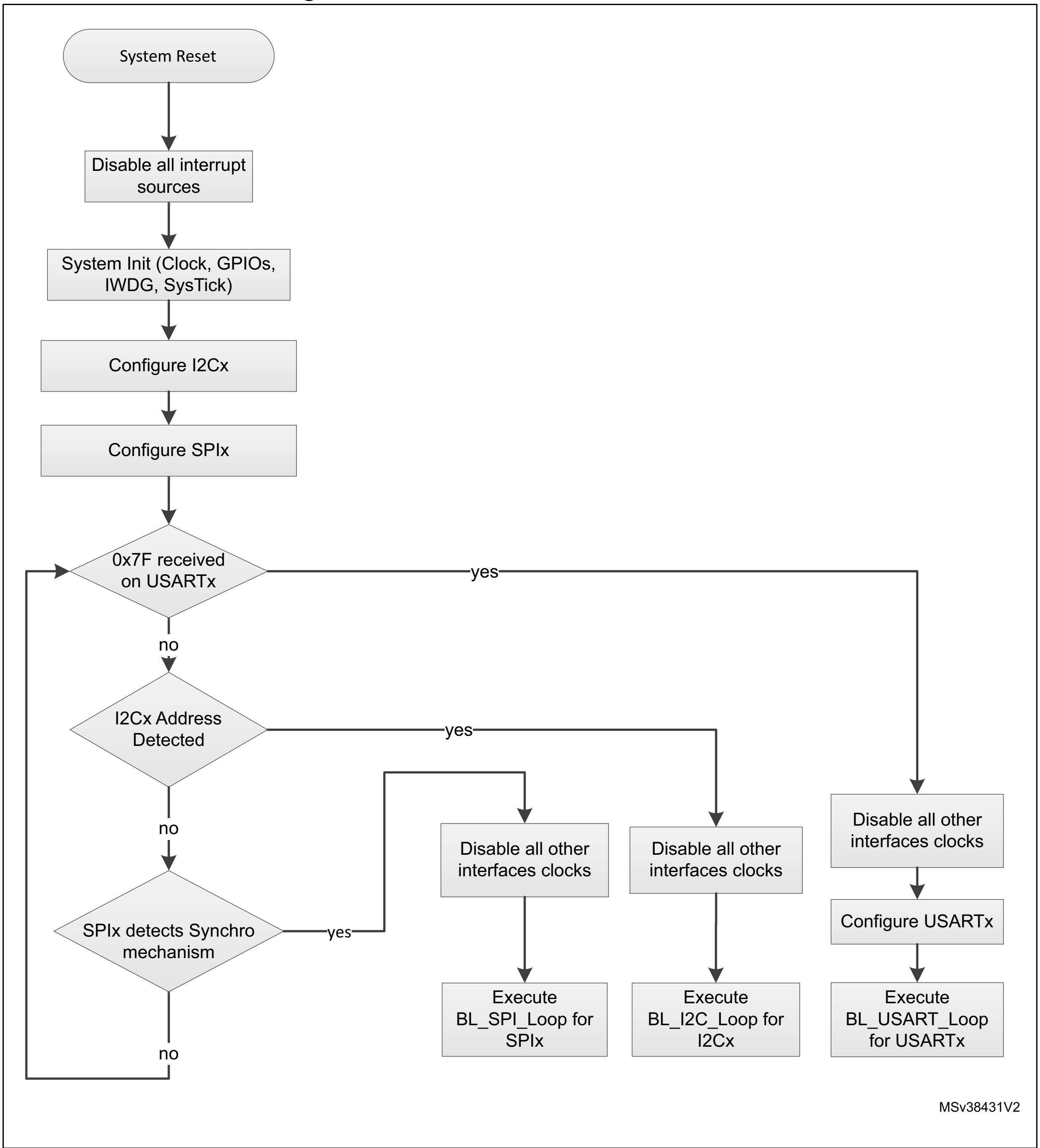
Bootloader	Feature/Peripheral	State	Comment
SPI1 bootloader	SPI1	Enabled	The SPI1 configuration is: Slave mode, Full Duplex, 8-bit MSB, Speed up to 8MHz, Polarity: CPOL Low, CPHA Low, NSS hardware.
	SPI1_MOSI pin	Input	PA7 pin: Slave data Input line, used in push-pull pull-down mode for STM32F410Cx/Rx devices. PB5 pin: Slave data Input line, used in push-pull pull-down mode for STM32F410Tx devices.
	SPI1_MISO pin	Output	PA6 pin: Slave data output line, used in push-pull pull-down mode for STM32F410Cx/Rx devices. PB4 pin: Slave data output line, used in push-pull pull-down mode for STM32F410Tx devices.
	SPI1_SCK pin	Input	PA5 pin: Slave clock line, used in push-pull pull-down mode.
	SPI1_NSS pin	Input	PA4 pin: slave chip select pin used in push-pull pull-up mode for STM32F410Cx/Rx devices. PA15 pin: slave chip select pin used in push-pull pull-up mode for STM32F410Tx devices.
SPI2 bootloader	SPI2	Enabled	The SPI2 configuration is: Slave mode, Full Duplex, 8-bit MSB, Speed up to 8MHz, Polarity: CPOL Low, CPHA Low, NSS hardware.
	SPI2_MOSI pin	Input	PC3 pin: Slave data Input line, used in push-pull pull-down mode
	SPI2_MISO pin	Output	PC2 pin: Slave data output line, used in push-pull pull-down mode
	SPI2_SCK pin	Input	PB13 pin: Slave clock line, used in push-pull pull-down mode
	SPI2_NSS pin	Input	PB12 pin: slave chip select pin used in push-pull pull-up mode.

The system clock is derived from the embedded internal high-speed RC for all bootloader interfaces. No external quartz is required for bootloader operations.

29.2 Bootloader selection

The *Figure 34* shows the bootloader selection mechanism.

Figure 34.Bootloader V11.x selection for STM32F410xx



29.3 Bootloader version

The following table lists the STM32F410xx devices bootloader V11.x versions.

Table 62. STM32F410xx bootloader V11.x versions

Bootloader version number	Description	Known limitations
V11.0	Initial bootloader version	After executing Go command (jump to user code) the bootloader resets AHB1ENR value to 0x0000 0000 and thus CCM RAM, when present, is not active (shall be re-enabled by user code at startup)
V11.1	Support I2C4 and SPI1 for STM32F410Tx devices.	After executing Go command (jump to user code) the bootloader resets AHB1ENR value to 0x0000 0000 and thus CCM RAM, when present, is not active (shall be re-enabled by user code at startup)

30 STM32F411xx devices bootloader

30.1 Bootloader configuration

The STM32F411xx bootloader is activated by applying pattern1 (described in *Table 2: Bootloader activation patterns*). The following table shows the hardware resources used by this bootloader.

Table 63. STM32F411xx configuration in system memory boot mode

Bootloader	Feature/Peripheral	State	Comment
Common to all bootloaders	RCC	HSI enabled	The system clock frequency is 60 MHz using the PLL. The HSI clock source is used at startup (interface detection phase) and when USART or SPI or I2C interface is selected (once DFU bootloader is selected, the clock source will be derived from the external crystal).
		HSE enabled	The system clock frequency is 60 MHz. The HSE clock source is used only when the DFU (USB FS Device) interface is selected. The external clock must provide a frequency multiple of 1 MHz and ranging from 4 MHz to 26 MHz.
		-	The Clock Security System (CSS) interrupt is enabled for the DFU bootloader. Any failure (or removal) of the external clock generates system reset.
	RAM	-	12 Kbyte starting from address 0x20000000 are used by the bootloader firmware
	System memory	-	29 Kbyte starting from address 0x1FFF0000, contain the bootloader firmware
	IWDG	-	The independent watchdog (IWDG) prescaler is configured to its maximum value. It is periodically refreshed to prevent watchdog reset (in case the hardware IWDG option was previously enabled by the user).
	Power	-	Voltage range is set to [1.62 V, 2.1 V]. In this range internal Flash write operations are allowed only in byte format (Half-Word, Word and Double-Word operations are not allowed). The voltage range can be configured in run time using bootloader commands.

Table 63. STM32F411xx configuration in system memory boot mode (continued)

Bootloader	Feature/Peripheral	State	Comment
USART1 bootloader	USART1	Enabled	Once initialized the USART1 configuration is: 8-bits, even parity and 1 Stop bit
	USART1_RX pin	Input	PA10 pin: USART1 in reception mode
	USART1_TX pin	Output	PA9 pin: USART1 in transmission mode
USART2 bootloader	USART2	Enabled	Once initialized the USART2 configuration is: 8-bits, even parity and 1 Stop bit
	USART2_RX pin	Input	PD6 pin: USART2 in reception mode
	USART2_TX pin	Output	PD5 pin: USART2 in transmission mode
USARTx bootloaders	SysTick timer	Enabled	Used to automatically detect the serial baud rate from the host for USARTx bootloaders.
I2C1 bootloader	I2C1	Enabled	The I2C1 configuration is: I2C speed: up to 400 KHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b0111001x (where x = 0 for write and x = 1 for read)
	I2C1_SCL pin	Input/Output	PB6 pin: clock line is used in open-drain mode.
	I2C1_SDA pin	Input/Output	PB7 pin: data line is used in open-drain mode.
I2C2 bootloader	I2C2	Enabled	The I2C2 configuration is: I2C speed: up to 400 KHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b0111001x (where x = 0 for write and x = 1 for read)
	I2C2_SCL pin	Input/Output	PB10 pin: clock line is used in open-drain mode.
	I2C2_SDA pin	Input/Output	PB3 pin: data line is used in open-drain mode.
I2C3 bootloader	I2C3	Enabled	The I2C3 configuration is: I2C speed: up to 400 KHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b0111001x (where x = 0 for write and x = 1 for read)
	I2C3_SCL pin	Input/Output	PA8 pin: clock line is used in open-drain mode.
	I2C3_SDA pin	Input/Output	PB4 pin: data line is used in open-drain mode.

Table 63. STM32F411xx configuration in system memory boot mode (continued)

Bootloader	Feature/Peripheral	State	Comment
SPI1 bootloader	SPI1	Enabled	The SPI1 configuration is: Slave mode, Full Duplex, 8-bit MSB, Speed up to 8 MHz, Polarity: CPOL Low, CPHA Low, NSS hardware.
	SPI1_MOSI pin	Input	PA7 pin: Slave data Input line, used in push-pull pull-down mode
	SPI1_MISO pin	Output	PA6 pin: Slave data output line, used in push-pull pull-down mode
	SPI1_SCK pin	Input	PA5 pin: Slave clock line, used in push-pull pull-down mode
	SPI1_NSS pin	Input	PA4 pin: slave chip select pin used in push-pull pull-down mode.
SPI2 bootloader	SPI2	Enabled	The SPI2 configuration is: Slave mode, Full Duplex, 8-bit MSB, Speed up to 8 MHz, Polarity: CPOL Low, CPHA Low, NSS hardware.
	SPI2_MOSI pin	Input	PB15 pin: Slave data Input line, used in push-pull pull-down mode
	SPI2_MISO pin	Output	PB14 pin: Slave data output line, used in push-pull pull-down mode
	SPI2_SCK pin	Input	PB13 pin: Slave clock line, used in push-pull pull-down mode
	SPI2_NSS pin	Input	PB12 pin: slave chip select pin used in push-pull pull-down mode.
SPI3 bootloader	SPI3	Enabled	The SPI3 configuration is: Slave mode, Full Duplex, 8-bit MSB, Speed up to 8 MHz, Polarity: CPOL Low, CPHA Low, NSS hardware.
	SPI3_MOSI pin	Input	PC12 pin: Slave data Input line, used in push-pull pull-down mode
	SPI3_MISO pin	Output	PC11 pin: Slave data output line, used in push-pull pull-down mode
	SPI3_SCK pin	Input	PC10 pin: Slave clock line, used in push-pull pull-down mode
	SPI3_NSS pin	Input	PA15 pin: slave chip select pin used in push-pull pull-down mode.

Table 63. STM32F411xx configuration in system memory boot mode (continued)

Bootloader	Feature/Peripheral	State	Comment
DFU bootloader	USB	Enabled	USB OTG FS configured in forced device mode
	USB_DM pin	Input/Output	PA11: USB DM line.
	USB_DP pin		PA12: USB DP line No external Pull-up resistor is required
	TIM11	Enabled	This timer is used to determine the value of the HSE. Once the HSE frequency is determined, the system clock is configured to 60 MHz using PLL and HSE.

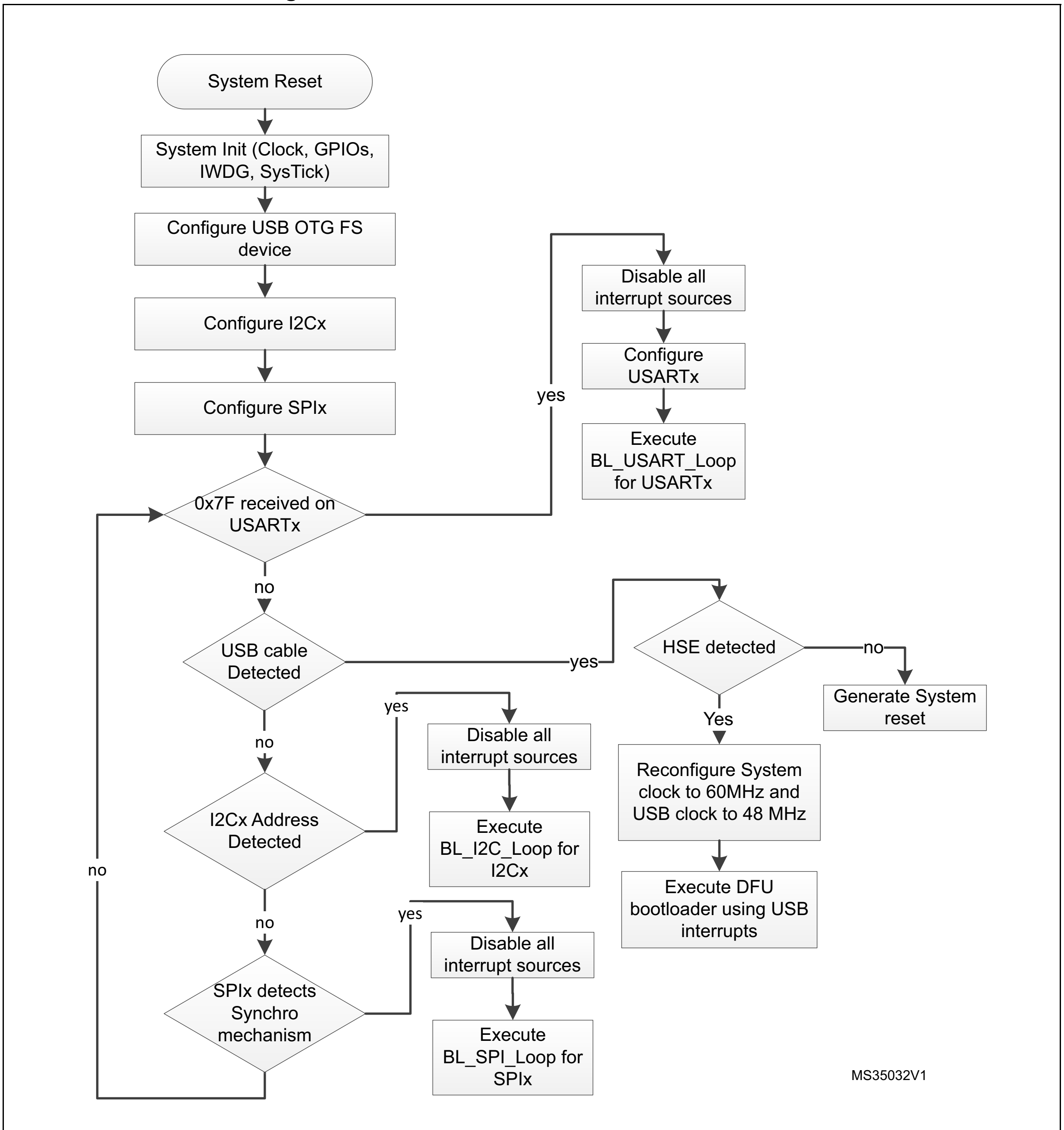
The system clock is derived from the embedded internal high-speed RC for USARTx, I2Cx and SPIx bootloaders. This internal clock is also used for DFU (USB FS Device) but only for the selection phase. An external clock multiple of 1 MHz (between 4 and 26 MHz) is required for DFU bootloader execution after the selection phase.

Note: Due to HSI deviation and since HSI is used to detect HSE value, the user must use low frequency HSE crystal values rather than high frequency values.
Low frequency values are better detected due to larger error margin. For example, it is better to use 8 MHz instead of 25 MHz.

30.2 Bootloader selection

The figure below shows the bootloader selection mechanism.

Figure 35. Bootloader selection for STM32F411xx



30.3 Bootloader version

The following table lists the STM32F411xx devices bootloader version.

Table 64. STM32F411xx bootloader versions

Bootloader version number	Description	Known limitations
V13.0	Initial bootloader version	After executing Go command (jump to user code) the bootloader resets AHB1ENR value to 0x0000 0000 and thus CCM RAM, when present, is not active (shall be re-enabled by user code at startup)

31 STM32F412xx devices bootloader

31.1 Bootloader configuration

The STM32F412xx bootloader is activated by applying pattern1 (described in *Table 2: Bootloader activation patterns*). The table shows the hardware resources used by this bootloader.

Table 65.STM32F412xx configuration in system memory boot mode

Bootloader	Feature/Peripheral	State	Comment
Common to all bootloaders	RCC	HSI enabled	The HSI is used at startup as clock source for system clock configured to 60 MHz and for USART and I2C bootloader operation.
		HSE enabled	The HSE is used only when the CAN or the DFU (USB FS Device) interfaces are selected. In this case the system clock configured to 60 MHz with HSE as clock source. The HSE frequency must be multiple of 1 MHz and ranging from 4 MHz to 26 MHz.
		-	The Clock Security System (CSS) interrupt is enabled for the CAN and DFU bootloaders. Any failure (or removal) of the external clock generates system reset.
	RAM	-	16 Kbyte starting from address 0x20000000 are used by the bootloader firmware
	System memory	-	29 Kbyte starting from address 0x1FFF0000, contain the bootloader firmware
	IWDG	-	The independent watchdog (IWDG) prescaler is configured to its maximum value. It is periodically refreshed to prevent watchdog reset (in case the hardware IWDG option was previously enabled by the user).
	Power	-	The voltage range is [1.8V, 3.6V] In this range: - Flash wait states 3. - System clock Frequency 60 MHz. - ART Accelerator enabled. - Flash write operation by byte (refer to bootloader memory management section for more information).

Table 65.STM32F412xx configuration in system memory boot mode (continued)

Bootloader	Feature/Peripheral	State	Comment
USART1 bootloader	USART1	Enabled	Once initialized the USART1 configuration is: 8-bits, even parity and 1 Stop bit
	USART1_RX pin	Input	PA10 pin: USART1 in reception mode
	USART1_TX pin	Output	PA9 pin: USART1 in transmission mode
USART2 bootloader	USART2	Enabled	Once initialized the USART2 configuration is: 8-bits, even parity and 1 Stop bit
	USART2_RX pin	Input	PD6 pin: USART2 in reception mode
	USART2_TX pin	Output	PD5 pin: USART2 in transmission mode
USART3 bootloader	USART3	Enabled	Once initialized the USART3 configuration is: 8-bits, even parity and 1 Stop bit
	USART3_RX pin	Input	PB11 pin: USART3 in reception mode
	USART3_TX pin	Output	PB10 pin: USART3 in transmission mode
USARTx bootloaders	SysTick timer	Enabled	Used to automatically detect the serial baud rate from the host for USARTx bootloaders.
CAN2 bootloader	CAN2	Enabled	Once initialized the CAN2 configuration is: Baudrate 125 kbps, 11-bit identifier. **Note:** CAN1 is clocked during CAN2 bootloader execution because CAN1 manages the communication between CAN2 and SRAM.
	CAN2_RX pin	Input	PB5 pin: CAN2 in reception mode
	CAN2_TX pin	Output	PB13 pin: CAN2 in transmission mode
I2C1 bootloader	I2C1	Enabled	The I2C1 configuration is: I2C speed: up to 400 KHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b1000110x (where x = 0 for write and x = 1 for read)
	I2C1_SCL pin	Input/Output	PB6 pin: clock line is used in open-drain mode.
	I2C1_SDA pin	Input/Output	PB7 pin: data line is used in open-drain mode.
I2C2 bootloader	I2C2	Enabled	The I2C2 configuration is: I2C speed: up to 400 KHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b1000110x (where x = 0 for write and x = 1 for read)
	I2C2_SCL pin	Input/Output	PF1 pin: clock line is used in open-drain mode.
	I2C2_SDA pin	Input/Output	PF0 pin: data line is used in open-drain mode.

Table 65.STM32F412xx configuration in system memory boot mode (continued)

Bootloader	Feature/Peripheral	State	Comment
I2C3 bootloader	I2C3	Enabled	The I2C3 configuration is: I2C speed: up to 400 KHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b1000110x (where x = 0 for write and x = 1 for read)
	I2C3_SCL pin	Input/Output	PA8 pin: clock line is used in open-drain mode.
	I2C3_SDA pin	Input/Output	PB4 pin: data line is used in open-drain mode.
I2C4 bootloader	I2C4	Enabled	The I2C4 configuration is: I2C speed: up to 1 MHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b1000110x (where x = 0 for write and x = 1 for read)
	I2C4_SCL pin	Input/Output	PB15 pin: clock line is used in open-drain mode.
	I2C4_SDA pin	Input/Output	PB14 pin: data line is used in open-drain mode.
SPI1 bootloader	SPI1	Enabled	The SPI1 configuration is: Slave mode, Full Duplex, 8-bit MSB, Speed up to 8MHz, Polarity: CPOL Low, CPHA Low, NSS hardware.
	SPI1_MOSI pin	Input	PA7 pin: Slave data Input line, used in push-pull pull-down mode
	SPI1_MISO pin	Output	PA6 pin: Slave data output line, used in push-pull pull-down mode
	SPI1_SCK pin	Input	PA5 pin: Slave clock line, used in push-pull pull-down mode
	SPI1_NSS pin	Input	PA4 pin: slave chip select pin used in push-pull pull-up mode.
SPI3 bootloader	SPI3	Enabled	The SPI3 configuration is: Slave mode, Full Duplex, 8-bit MSB, Speed up to 8MHz, Polarity: CPOL Low, CPHA Low, NSS hardware.
	SPI3_MOSI pin	Input	PC12 pin: Slave data Input line, used in push-pull pull-down mode
	SPI3_MISO pin	Output	PC11 pin: Slave data output line, used in push-pull pull-down mode
	SPI3_SCK pin	Input	PC10 pin: Slave clock line, used in push-pull pull-down mode
	SPI3_NSS pin	Input	PA15 pin: slave chip select pin used in push-pull pull-up mode.

Table 65.STM32F412xx configuration in system memory boot mode (continued)

Bootloader	Feature/Peripheral	State	Comment
SPI4 bootloader	SPI4	Enabled	The SPI4 configuration is: Slave mode, Full Duplex, 8-bit MSB, Speed up to 8MHz, Polarity: CPOL Low, CPHA Low, NSS hardware.
	SPI4_MOSI pin	Input	PE14 pin: Slave data Input line, used in push-pull pull-down mode
	SPI4_MISO pin	Output	PE13 pin: Slave data output line, used in push-pull pull-down mode
	SP4_SCK pin	Input	PE12 pin: Slave clock line, used in push-pull pull-down mode
	SPI4_NSS pin	Input	PE11 pin: slave chip select pin used in push-pull pull-up mode.
DFU bootloader	USB	Enabled	USB OTG FS configured in forced device mode
	USB_DM pin	Input/Output	PA11 pin: USB DM line.
	USB_DP pin		PA12 pin: USB DP line No external Pull-Up resistor is required.
CAN2 and DFU bootloaders	TIM11	Enabled	This timer is used to determine the value of the HSE. Once HSE frequency is determined, the system clock is configured to 60 MHz using PLL and HSE.

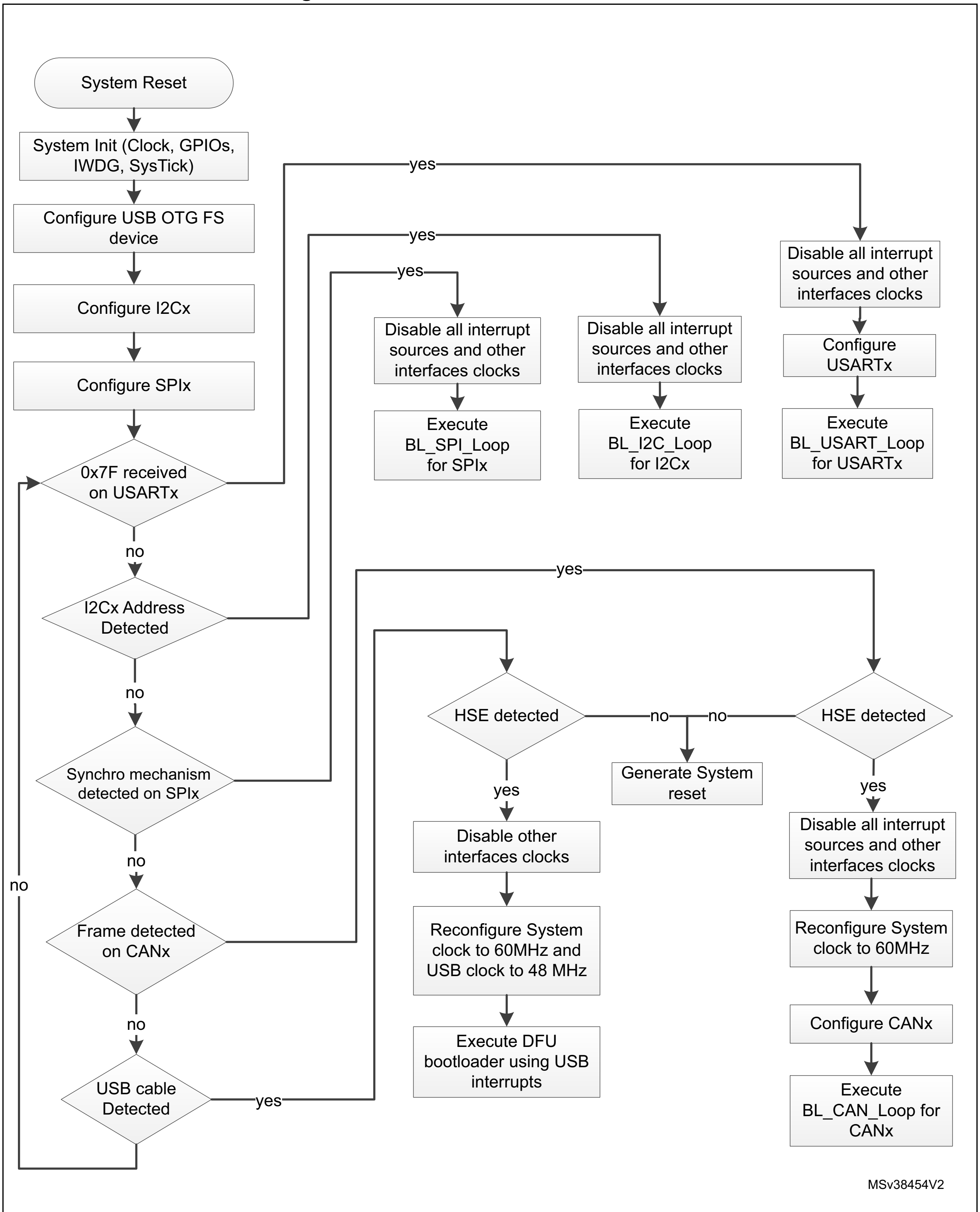
The system clock is derived from the embedded internal high-speed RC for USARTx and I2Cx bootloaders. This internal clock is also used for CAN and DFU (USB FS Device) but only for the selection phase. An external clock multiple of 1 MHz (between 4 and 26 MHz) is required for CAN and DFU bootloader execution after the selection phase.

Note: *Due to HSI deviation and since HSI is used to detect HSE value, the user must use low frequency HSE crystal values rather than high frequency values.*
Low frequency values are better detected due to larger error margin. For example, it is better to use 8 MHz instead of 25 MHz.

31.2 Bootloader selection

The *Figure 36* shows the bootloader selection mechanism.

Figure 36.Bootloader V9.x selection for STM32F412xx



31.3 Bootloader version

The following table lists the STM32F412xx devices bootloader V9.x versions.

Table 66. STM32F412xx bootloader V9.x versions

Bootloader version number	Description	Known limitations
V9.0	Initial bootloader version	After executing Go command (jump to user code) the bootloader resets AHB1ENR value to 0x0000 0000 and thus CCM RAM, when present, is not active (shall be re-enabled by user code at startup)
V9.1	Fix USART3 interface pinout	After executing Go command (jump to user code) the bootloader resets AHB1ENR value to 0x0000 0000 and thus CCM RAM, when present, is not active (shall be re-enabled by user code at startup)

32 STM32F413xx/423xx devices bootloader

32.1 Bootloader configuration

The STM32F413xx/423xx bootloader is activated by applying pattern1 (described in *Table 2: Bootloader activation patterns*). The following table shows the hardware resources used by this bootloader.

Table 67. STM32F413xx/423xx configuration in system memory boot mode

Bootloader	Feature/Peripheral	State	Comment
Common to all bootloaders	RCC	HSI enabled	The HSI is used at startup as clock source for system clock configured to 60 MHz and for USART and I2C bootloader operation.
		HSE enabled	The HSE is used only when the CAN or the DFU (USB FS Device) interfaces are selected. In this case the system clock configured to 60 MHz with HSE as clock source. The HSE frequency must be multiple of 1 MHz and ranging from 4 MHz to 26 MHz.
		-	The Clock Security System (CSS) interrupt is enabled for the CAN and DFU bootloaders. Any failure (or removal) of the external clock generates system reset.
	RAM	-	16 Kbyte starting from address 0x20000000 are used by the bootloader firmware
	System memory	-	60 Kbyte starting from address 0x1FF00000, contain the bootloader firmware
	IWDG	-	The independent watchdog (IWDG) prescaler is configured to its maximum value. It is periodically refreshed to prevent watchdog reset (in case the hardware IWDG option was previously enabled by the user).
	Power	-	The voltage range is [1.8V, 3.6V] In this range: – Flash wait states 4. – System clock Frequency 60 MHz. – ART Accelerator enabled. – Flash write operation by byte (refer to *Bootloader memory management* for more information).

Table 67. STM32F413xx/423xx configuration in system memory boot mode (continued)

Bootloader	Feature/Peripheral	State	Comment
USART1 bootloader	USART1	Enabled	Once initialized the USART1 configuration is: 8-bits, even parity and 1 Stop bit
	USART1_RX pin	Input	PA10 pin: USART1 in reception mode
	USART1_TX pin	Output	PA9 pin: USART1 in transmission mode
USART2 bootloader	USART2	Enabled	Once initialized the USART2 configuration is: 8-bits, even parity and 1 Stop bit
	USART2_RX pin	Input	PD6 pin: USART2 in reception mode
	USART2_TX pin	Output	PD5 pin: USART2 in transmission mode
USART3 bootloader	USART3	Enabled	Once initialized the USART3 configuration is: 8-bits, even parity and 1 Stop bit
	USART3_RX pin	Input	PB11 pin: USART3 in reception mode
	USART3_TX pin	Output	PB10 pin: USART3 in transmission mode
USARTx bootloaders	SysTick timer	Enabled	Used to automatically detect the serial baud rate from the host for USARTx bootloaders.
CAN2 bootloader	CAN2	Enabled	Once initialized the CAN2 configuration is: Baudrate 125 kbps, 11-bit identifier. **Note**: CAN1 is clocked during CAN2 bootloader execution because CAN1 manages the communication between CAN2 and SRAM.
	CAN2_RX pin	Input	PB5 pin: CAN2 in reception mode
	CAN2_TX pin	Output	PB13 pin: CAN2 in transmission mode
I2C1 bootloader	I2C1	Enabled	The I2C1 configuration is: I2C speed: up to 400 KHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b1001011x (where x = 0 for write and x = 1 for read)
	I2C1_SCL pin	Input/Output	PB6 pin: clock line is used in open-drain mode.
	I2C1_SDA pin	Input/Output	PB7 pin: data line is used in open-drain mode.

Table 67. STM32F413xx/423xx configuration in system memory boot mode (continued)

Bootloader	Feature/Peripheral	State	Comment
I2C2 bootloader	I2C2	Enabled	The I2C2 configuration is: I2C speed: up to 400 KHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b1001011x (where x = 0 for write and x = 1 for read)
	I2C2_SCL pin	Input/Output	PF1 pin: clock line is used in open-drain mode.
	I2C2_SDA pin	Input/Output	PF0 pin: data line is used in open-drain mode.
I2C3 bootloader	I2C3	Enabled	The I2C3 configuration is: I2C speed: up to 400 KHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b1001011x (where x = 0 for write and x = 1 for read)
	I2C3_SCL pin	Input/Output	PA8 pin: clock line is used in open-drain mode.
	I2C3_SDA pin	Input/Output	PB4 pin: data line is used in open-drain mode.
I2C4 bootloader	I2C4	Enabled	The I2C4 configuration is: I2C speed: up to 1 MHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b1001011x (where x = 0 for write and x = 1 for read)
	I2C4_SCL pin	Input/Output	PB15 pin: clock line is used in open-drain mode.
	I2C4_SDA pin	Input/Output	PB14 pin: data line is used in open-drain mode.
SPI1 bootloader	SPI1	Enabled	The SPI1 configuration is: – Slave mode – Full Duplex – 8-bit MSB, speed up to 8MHz – Polarity: CPOL Low, CPHA Low, NSS hardware.
	SPI1_MOSI pin	Input	PA7 pin: Slave data Input line, used in push-pull pull-down mode
	SPI1_MISO pin	Output	PA6 pin: Slave data output line, used in push-pull pull-down mode
	SPI1_SCK pin	Input	PA5 pin: Slave clock line, used in push-pull pull-down mode
	SPI1_NSS pin	Input	PA4 pin: slave chip select pin used in push-pull pull-up mode.

Table 67. STM32F413xx/423xx configuration in system memory boot mode (continued)

Bootloader	Feature/Peripheral	State	Comment
SPI3 bootloader	SPI3	Enabled	The SPI3 configuration is: – Slave mode – Full Duplex – 8-bit MSB, speed up to 8MHz – Polarity: CPOL Low, CPHA Low, NSS hardware.
	SPI3_MOSI pin	Input	PC12 pin: Slave data Input line, used in push-pull pull-down mode
	SPI3_MISO pin	Output	PC11 pin: Slave data output line, used in push-pull pull-down mode
	SPI3_SCK pin	Input	PC10 pin: Slave clock line, used in push-pull pull-down mode
	SPI3_NSS pin	Input	PA15 pin: slave chip select pin used in push-pull pull-up mode.
SPI4 bootloader	SPI4	Enabled	The SPI4 configuration is: – Slave mode – Full Duplex – 8-bit MSB, speed up to 8MHz – Polarity: CPOL Low, CPHA Low, NSS hardware.
	SPI4_MOSI pin	Input	PE14 pin: Slave data Input line, used in push-pull pull-down mode
	SPI4_MISO pin	Output	PE13 pin: Slave data output line, used in push-pull pull-down mode
	SP4_SCK pin	Input	PE12 pin: Slave clock line, used in push-pull pull-down mode
	SPI4_NSS pin	Input	PE11 pin: slave chip select pin used in push-pull pull-up mode.
DFU bootloader	USB	Enabled	USB OTG FS configured in forced device mode
	USB_DM pin	Input/Output	PA11 pin: USB DM line.
	USB_DP pin		PA12 pin: USB DP line No external Pull-Up resistor is required.
CAN2 and DFU bootloaders	TIM11	Enabled	This timer is used to determine the value of the HSE. Once HSE frequency is determined, the system clock is configured to 60 MHz using PLL and HSE.

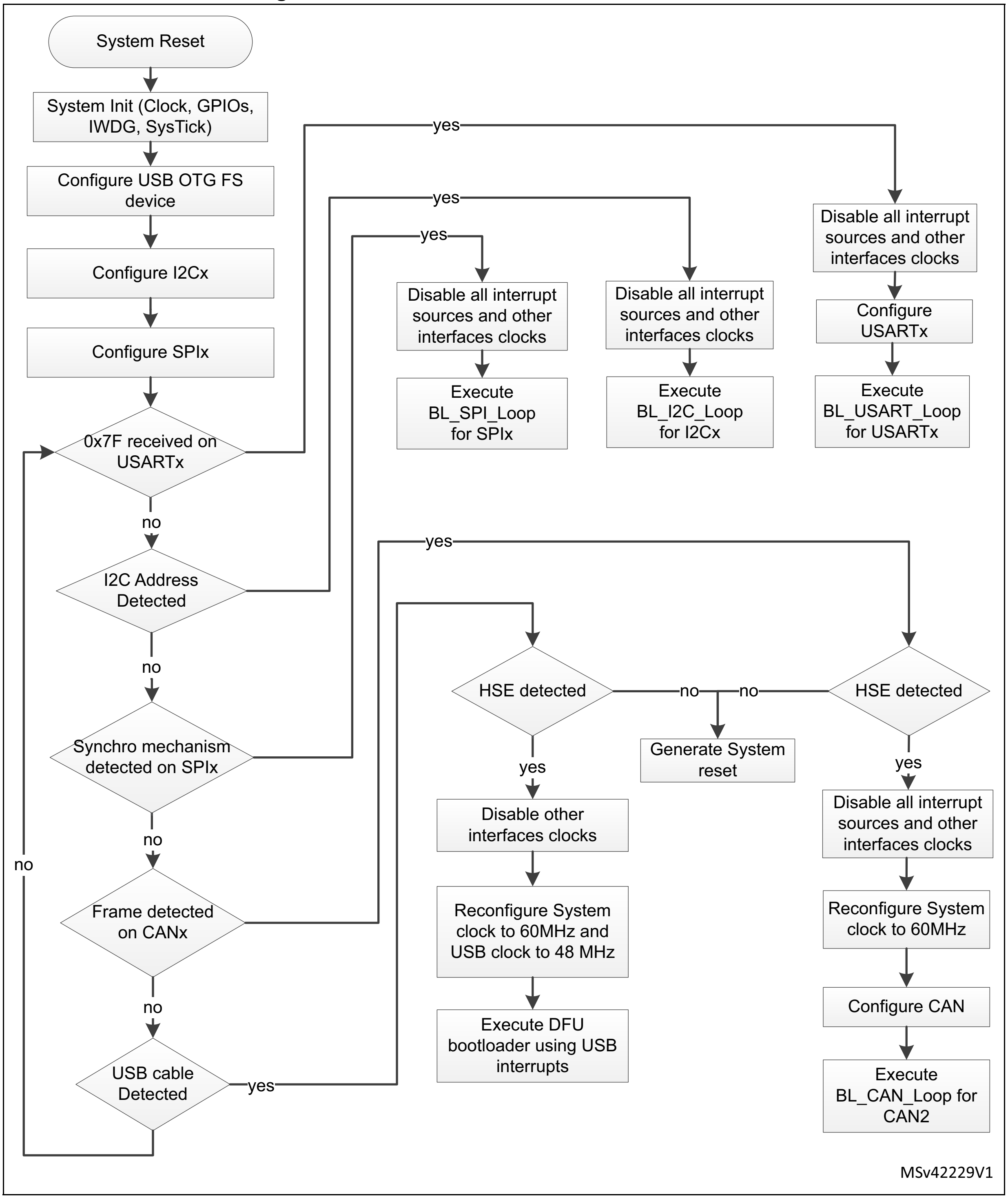
The system clock is derived from the embedded internal high-speed RC for USARTx and I2Cx bootloaders. This internal clock is also used for CAN and DFU (USB FS Device) but only for the selection phase. An external clock multiple of 1 MHz (between 4 and 26 MHz) is required for CAN and DFU bootloader execution after the selection phase.

Note: Due to HSI deviation and since HSI is used to detect HSE value, the user must use low frequency HSE crystal values rather than high frequency values.
Low frequency values are better detected due to larger error margin. For example, it is better to use 8 MHz instead of 25 MHz.

32.2 Bootloader selection

The *Figure 37* shows the bootloader selection mechanism.

Figure 37.Bootloader V9.x selection for STM32F413xx/423xx



32.3 Bootloader version

The following table lists the STM32F413xx/423xx devices bootloader V9.x versions.

Table 68. STM32F413xx/423xx bootloader V9.x versions

Bootloader version number	Description	Known limitations
V9.0	Initial bootloader version	After executing Go command (jump to user code) the bootloader resets AHB1ENR value to 0x0000 0000 and thus CCM RAM, when present, is not active (shall be re-enabled by user code at startup)

33 STM32F42xxx/43xxx devices bootloader

33.1 Bootloader V7.x

33.1.1 Bootloader configuration

The STM32F42xxx/43xxx bootloader is activated by applying pattern5 (described in *Table 2: Bootloader activation patterns*). The following table shows the hardware resources used by this bootloader.

Table 69. STM32F42xxx/43xxx configuration in system memory boot mode

Bootloader	Feature/Peripheral	State	Comment
Common to all bootloaders	RCC	HSI enabled	The system clock frequency is 24 MHz using the PLL. The HSI clock source is used at startup (interface detection phase) and when USART or I2C interfaces are selected (once CAN or DFU bootloader is selected, the clock source will be derived from the external crystal).
		HSE enabled	The system clock frequency is 60 MHz. The HSE clock source is used only when the CAN or the DFU (USB FS Device) interfaces are selected. The external clock must provide a frequency multiple of 1 MHz and ranging from 4 MHz to 26 MHz.
		-	The Clock Security System (CSS) interrupt is enabled for the CAN and DFU bootloaders. Any failure (or removal) of the external clock generates system reset.
	RAM	-	8 Kbyte starting from address 0x20000000 are used by the bootloader firmware
	System memory	-	29 Kbyte starting from address 0x1FFF0000, contain the bootloader firmware
	IWDG	-	The independent watchdog (IWDG) prescaler is configured to its maximum value. It is periodically refreshed to prevent watchdog reset (in case the hardware IWDG option was previously enabled by the user).
	Power	-	Voltage range is set to [1.62 V, 2.1 V]. In this range internal Flash write operations are allowed only in byte format (Half-Word, Word and Double-Word operations are not allowed). The voltage range can be configured in run time using bootloader commands.

Table 69. STM32F42xxx/43xxx configuration in system memory boot mode (continued)

Bootloader	Feature/Peripheral	State	Comment
USART1 bootloader	USART1	Enabled	Once initialized the USART1 configuration is: 8 bits, even parity and 1 Stop bit
	USART1_RX pin	Input	PA10 pin: USART1 in reception mode
	USART1_TX pin	Output	PA9 pin: USART1 in transmission mode
USART3 bootloader (on PB10/PB11)	USART3	Enabled	Once initialized the USART3 configuration is: 8 bits, even parity and 1 Stop bit
	USART3_RX pin	Input	PB11 pin: USART3 in reception mode
	USART3_TX pin	Output	PB10 pin: USART3 in transmission mode
USART3 bootloader (on PC10/PC11)	USART3	Enabled	Once initialized the USART3 configuration is: 8 bits, even parity and 1 Stop bit
	USART3_RX pin	Input	PC11 pin: USART3 in reception mode
	USART3_TX pin	Output	PC10 pin: USART3 in transmission mode
USARTx bootloaders	SysTick timer	Enabled	Used to automatically detect the serial baud rate from the host for USARTx bootloaders.
CAN2 bootloader	CAN2	Enabled	Once initialized the CAN2 configuration is: Baudrate 125 kbps, 11-bit identifier. **Note**: CAN1 is clocked during CAN2 bootloader execution because CAN1 manages the communication between CAN2 and SRAM.
	CAN2_RX pin	Input	PB5 pin: CAN2 in reception mode
	CAN2_TX pin	Output	PB13 pin: CAN2 in transmission mode
I2C1 bootloader	I2C1	Enabled	The I2C1 configuration is: I2C speed: up to 400 KHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b0111000x (where x = 0 for write and x = 1 for read).
	I2C1_SCL pin	Input/Output	PB6 pin: clock line is used in open-drain mode.
	I2C1_SDA pin	Input/Output	PB9 pin: data line is used in open-drain mode.
DFU bootloader	USB	Enabled	USB OTG FS configured in forced device mode
	USB_DM pin	Input/Output	PA11: USB DM line.
	USB_DP pin		PA12: USB DP line No external Pull-up resistor is required
CAN2 and DFU bootloaders	TIM11	Enabled	This timer is used to determine the value of the HSE. Once the HSE frequency is determined, the system clock is configured to 60 MHz using PLL and HSE.

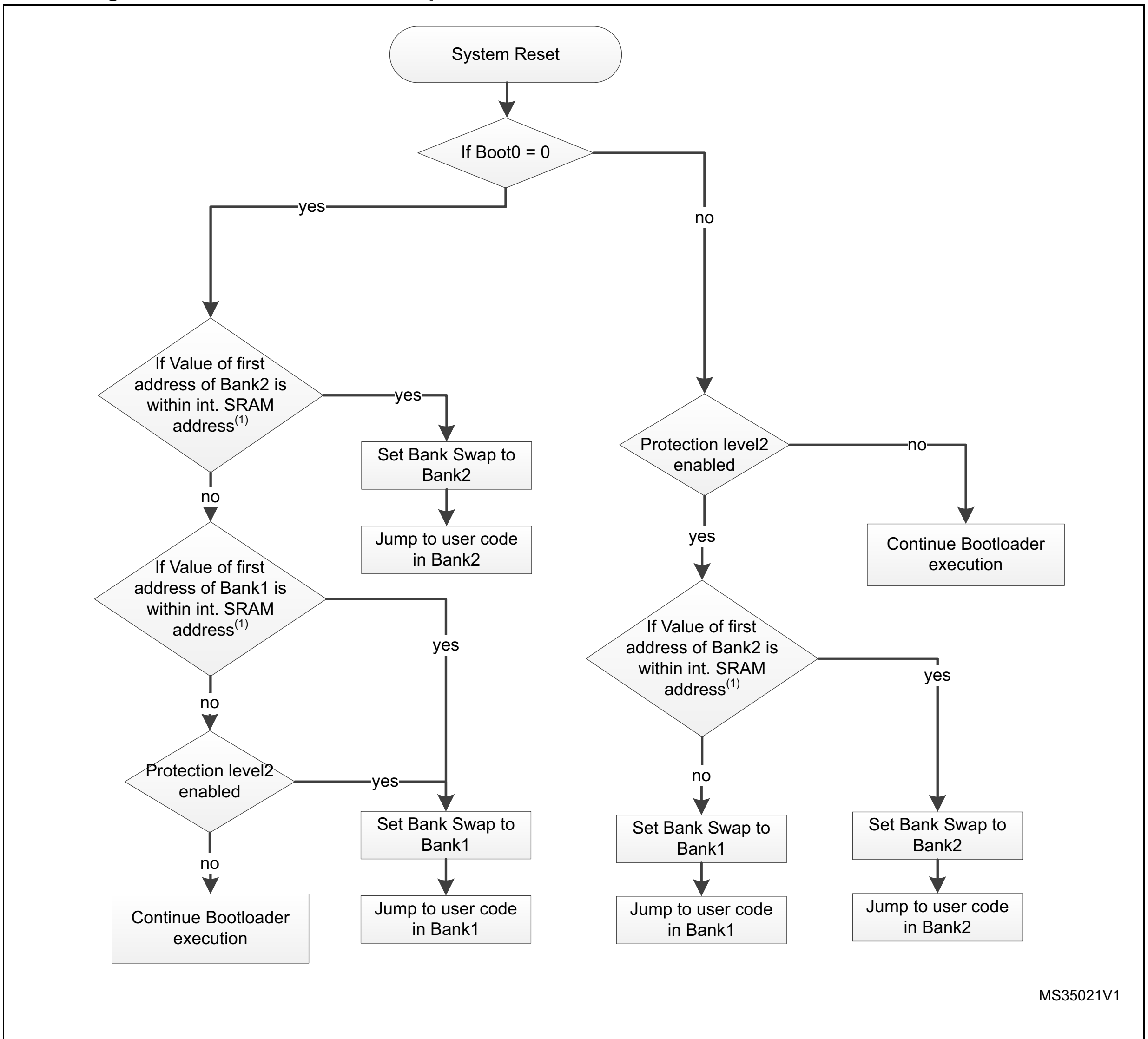
The system clock is derived from the embedded internal high-speed RC for USARTx and I2Cx bootloaders. This internal clock is also used for CAN and DFU (USB FS Device) but only for the selection phase. An external clock multiple of 1 MHz (between 4 and 26 MHz) is required for CAN and DFU bootloader execution after the selection phase.

Note: Due to HSI deviation and since HSI is used to detect HSE value, the user must use low frequency HSE crystal values rather than high frequency values.
Low frequency values are better detected due to larger error margin. For example, it is better to use 8 MHz instead of 25 MHz.

33.1.2 Bootloader selection

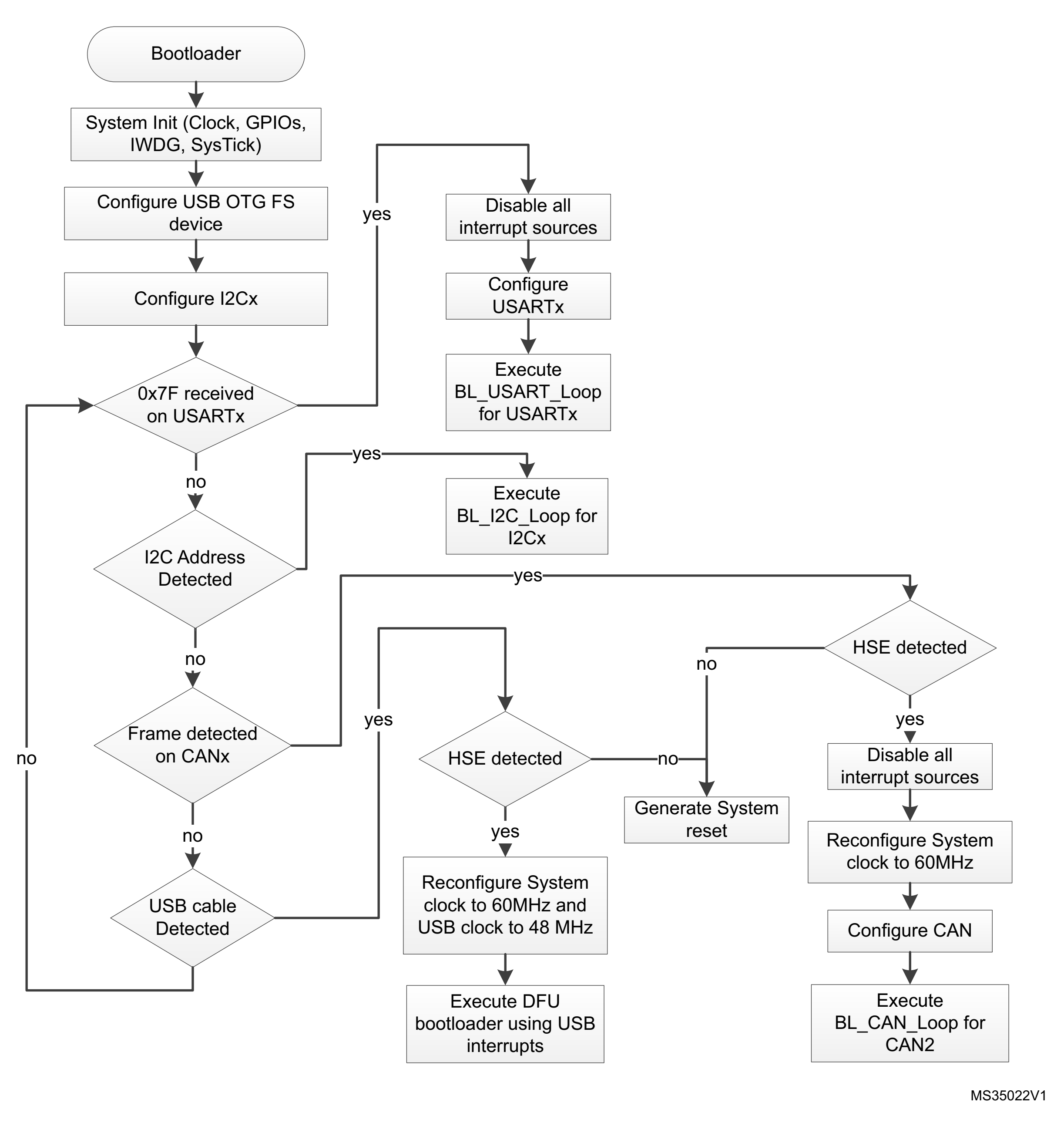
The *Figure 38* and *Figure 39* show the bootloader selection mechanism.

Figure 38. Dual Bank Boot Implementation for STM32F42xxx/43xxx Bootloader V7.x



1. CCM RAM is not considered valid as stack pointer address for the dual bank boot mechanism.

Figure 39. Bootloader V7.x selection for STM32F42xxx/43xxx



33.1.3 Bootloader version

The following table lists the STM32F42xxx/43xxx devices bootloader V7.x versions.

Table 70. STM32F42xxx/43xxx bootloader V7.x versions

Bootloader version number	Description	Known limitations
V7.0	Initial bootloader version	For the CAN interface, the Write Unprotect command is not functional. Instead you can use Write Memory command and write directly to the option bytes in order to disable the write protection. For the USB DFU interface, in Dual Bank mode, the Erase operation is not functional for the second bank. Instead you can return to Single Bank mode, erase desired sector(s) and then reactivate the Dual Bank mode. After executing Go command (jump to user code) the bootloader resets AHB1ENR value to 0x0000 0000 and thus CCM RAM, when present, is not active (shall be re-enabled by user code at startup)

33.2 Bootloader V9.x

33.2.1 Bootloader configuration

The STM32F42xxx/43xxx bootloader is activated by applying pattern5 (described in *Table 2: Bootloader activation patterns*). The following table shows the hardware resources used by this bootloader.

Table 71. STM32F42xxx/43xxx configuration in system memory boot mode

Bootloader	Feature/Peripheral	State	Comment
Common to all bootloaders	RCC	HSI enabled	The system clock frequency is 60 MHz using the PLL. The HSI clock source is used at startup (interface detection phase) and when USART or SPI or I2C interfaces are selected (once CAN or DFU bootloader is selected, the clock source will be derived from the external crystal).
		HSE enabled	The system clock frequency is 60 MHz. The HSE clock source is used only when the CAN or the DFU (USB FS Device) interfaces are selected. The external clock must provide a frequency multiple of 1 MHz and ranging from 4 MHz to 26 MHz.
		-	The Clock Security System (CSS) interrupt is enabled for the CAN and DFU bootloaders. Any failure (or removal) of the external clock generates system reset.
	RAM	-	12 Kbyte starting from address 0x20000000 are used by the bootloader firmware
	System memory	-	29 Kbyte starting from address 0x1FFF0000, contain the bootloader firmware
	IWDG	-	The independent watchdog (IWDG) prescaler is configured to its maximum value. It is periodically refreshed to prevent watchdog reset (in case the hardware IWDG option was previously enabled by the user).
	Power	-	Voltage range is set to [1.62 V, 2.1 V]. In this range internal Flash write operations are allowed only in byte format (Half-Word, Word and Double-Word operations are not allowed). The voltage range can be configured in run time using bootloader commands.
USART1 bootloader	USART1	Enabled	Once initialized the USART1 configuration is: 8-bits, even parity and 1 Stop bit
	USART1_RX pin	Input	PA10 pin: USART1 in reception mode
	USART1_TX pin	Output	PA9 pin: USART1 in transmission mode

Table 71. STM32F42xxx/43xxx configuration in system memory boot mode (continued)

Bootloader	Feature/Peripheral	State	Comment
USART3 bootloader (on PB10/PB11)	USART3	Enabled	Once initialized the USART3 configuration is: 8-bits, even parity and 1 Stop bit
	USART3_RX pin	Input	PB11 pin: USART3 in reception mode
	USART3_TX pin	Output	PB10 pin: USART3 in transmission mode
USART3 bootloader (on PC10/PC11)	USART3	Enabled	Once initialized the USART3 configuration is: 8-bits, even parity and 1 Stop bit
	USART3_RX pin	Input	PC11 pin: USART3 in reception mode
	USART3_TX pin	Output	PC10 pin: USART3 in transmission mode
USARTx bootloaders	SysTick timer	Enabled	Used to automatically detect the serial baud rate from the host for USARTx bootloaders.
CAN2 bootloader	CAN2	Enabled	Once initialized the CAN2 configuration is: Baudrate 125 kbps, 11-bit identifier. **Note:** CAN1 is clocked during CAN2 bootloader execution because CAN1 manages the communication between CAN2 and SRAM.
	CAN2_RX pin	Input	PB5 pin: CAN2 in reception mode
	CAN2_TX pin	Output	PB13 pin: CAN2 in transmission mode
I2C1 bootloader	I2C1	Enabled	The I2C1 configuration is: I2C speed: up to 400 KHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b0111000x (where x = 0 for write and x = 1 for read).
	I2C1_SCL pin	Input/Output	PB6 pin: clock line is used in open-drain mode.
	I2C1_SDA pin	Input/Output	PB9 pin: data line is used in open-drain mode.
I2C2 bootloader	I2C2	Enabled	The I2C2 configuration is: I2C speed: up to 400 KHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b0111000x (where x = 0 for write and x = 1 for read).
	I2C2_SCL pin	Input/Output	PF1 pin: clock line is used in open-drain mode.
	I2C2_SDA pin	Input/Output	PF0 pin: data line is used in open-drain mode.
I2C3 bootloader	I2C3	Enabled	The I2C3 configuration is: I2C speed: up to 400 KHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b0111000x (where x = 0 for write and x = 1 for read).
	I2C3_SCL pin	Input/Output	PA8 pin: clock line is used in open-drain mode.
	I2C3_SDA pin	Input/Output	PC9 pin: data line is used in open-drain mode.

Table 71. STM32F42xxx/43xxx configuration in system memory boot mode (continued)

Bootloader	Feature/Peripheral	State	Comment
SPI1 bootloader	SPI1	Enabled	The SPI1 configuration is: Slave mode, Full Duplex, -bit MSB, Speed up to 8 MHz, Polarity: CPOL Low, CPHA Low, NSS hardware.
	SPI1_MOSI pin	Input	PA7 pin: Slave data Input line, used in push-pull pull-down mode
	SPI1_MISO pin	Output	PA6 pin: Slave data output line, used in push-pull pull-down mode
	SPI1_SCK pin	Input	PA5 pin: Slave clock line, used in push-pull pull-down mode
	SPI1_NSS pin	Input	PA4 pin: slave chip select pin used in push-pull pull-down mode.
SPI2 bootloader	SPI2	Enabled	The SPI2 configuration is: Slave mode, Full Duplex, 8-bit MSB, Speed up to 8 MHz, Polarity: CPOL Low, CPHA Low, NSS hardware.
	SPI2_MOSI pin	Input	PI3 pin: Slave data Input line, used in push-pull pull-down mode
	SPI2_MISO pin	Output	PI2 pin: Slave data output line, used in push-pull pull-down mode
	SPI2_SCK pin	Input	PI1 pin: Slave clock line, used in push-pull pull-down mode
	SPI2_NSS pin	Input	PI0 pin: slave chip select pin used in push-pull pull-down mode.
SPI4 bootloader	SPI4	Enabled	The SPI4 configuration is: Slave mode, Full Duplex, 8-bit MSB, Speed up to 8 MHz, Polarity: CPOL Low, CPHA Low, NSS hardware.
	SPI4_MOSI pin	Input	PE14 pin: Slave data Input line, used in push-pull pull-down mode
	SPI4_MISO pin	Output	PE13 pin: Slave data output line, used in push-pull pull-down mode
	SP4_SCK pin	Input	PE12 pin: Slave clock line, used in push-pull pull-down mode
	SPI4_NSS pin	Input	PE11 pin: slave chip select pin used in push-pull pull-down mode.
DFU bootloader	USB	Enabled	USB OTG FS configured in forced device mode
	USB_DM pin	Input/Output	PA11: USB DM line.
	USB_DP pin		PA12: USB DP line No external Pull-up resistor is required
CAN2 and DFU bootloaders	TIM11	Enabled	This timer is used to determine the value of the HSE. Once the HSE frequency is determined, the system clock is configured to 60 MHz using PLL and HSE.

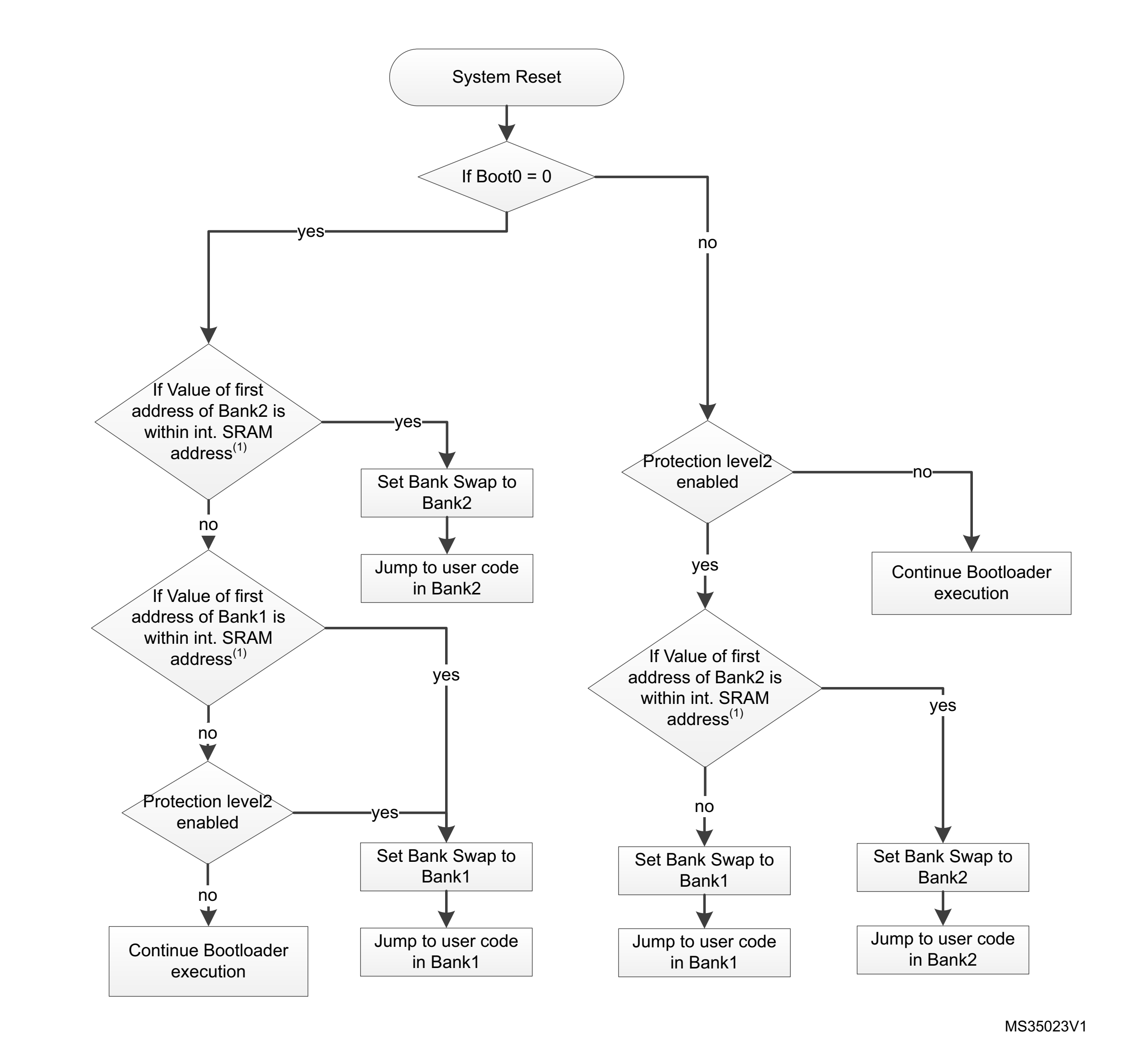
The system clock is derived from the embedded internal high-speed RC for USARTx, I2Cx and SPIx bootloaders. This internal clock is also used for CAN and DFU (USB FS Device) but only for the selection phase. An external clock multiple of 1 MHz (between 4 and 26 MHz) is required for CAN and DFU bootloader execution after the selection phase.

Note: Due to HSI deviation and since HSI is used to detect HSE value, the user must use low frequency HSE crystal values rather than high frequency values.
Low frequency values are better detected due to larger error margin. For example, it is better to use 8 MHz instead of 25 MHz.

33.2.2 Bootloader selection

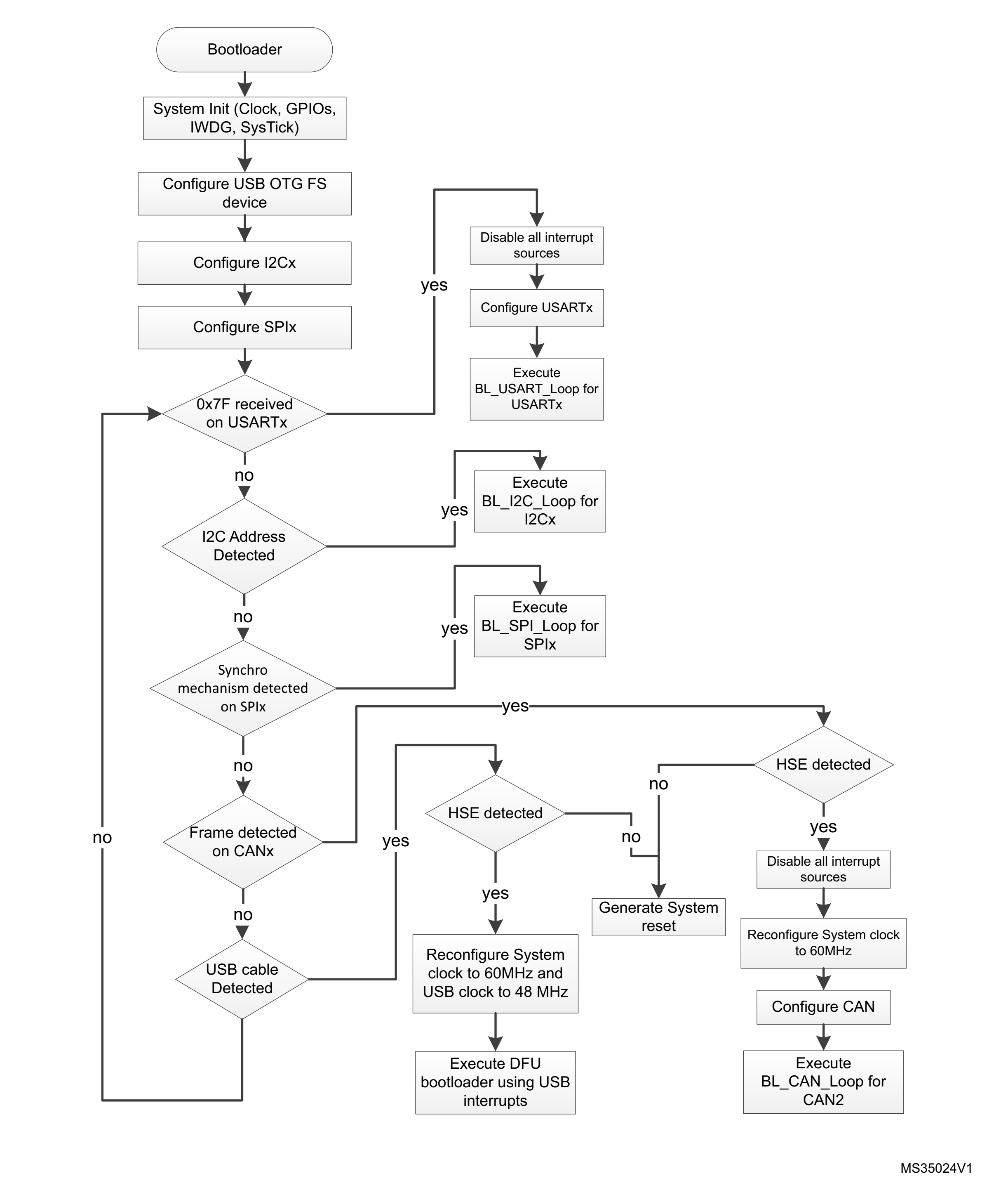
The *Figure 40* and *Figure 41* show the bootloader selection mechanism.

Figure 40. Dual Bank Boot Implementation for STM32F42xxx/43xxx bootloader V9.x



1. CCM RAM is not considered valid as stack pointer address for the dual bank boot mechanism.

Figure 41. Bootloader V9.x selection for STM32F42xxx/43xxx



33.2.3 Bootloader version

The following table lists the STM32F42xxx/43xxx devices bootloader V9.x versions.

Table 72. STM32F42xxx/43xxx bootloader V9.x versions

Bootloader version number	Description	Known limitations
V9.0	This bootloader is an updated version of bootloader v7.0. This new version of bootloader supports I2C2, I2C3, SPI1, SPI2 and SPI4 interfaces. The RAM used by this bootloader is increased from 8Kb to 12Kb. The ID of this bootloader is 0x90 The connection time is increased.	For the USB DFU interface, in Dual Bank mode, the Erase operation is not functional for the second bank. Instead you can return to Single Bank mode, erase desired sector(s) and then reactivate the Dual Bank mode. After executing Go command (jump to user code) the bootloader resets AHB1ENR value to 0x0000 0000 and thus CCM RAM, when present, is not active (shall be re-enabled by user code at startup)
V9.1	This bootloader is an updated version of bootloader v9.0. This new version implements the new I2C No-stretch commands (I2C protocol v1.1) and the capability of disabling PcROP when RDP1 is enabled with ReadOutUnprotect command for all protocols(USB, USART, CAN, I2C and SPI). The ID of this bootloader is 0x91	For the CAN interface, the Write Unprotect command is not functional. Instead you can use Write Memory command and write directly to the option bytes in order to disable the write protection. For the USB DFU interface, in Dual Bank mode, the Erase operation is not functional for the second bank. Instead you can return to Single Bank mode, erase desired sector(s) and then reactivate the Dual Bank mode. After executing Go command (jump to user code) the bootloader resets AHB1ENR value to 0x0000 0000 and thus CCM RAM, when present, is not active (shall be re-enabled by user code at startup)

34 STM32F446xx devices bootloader

34.1 Bootloader configuration

The STM32F446xx bootloader is activated by applying pattern1 (described in *Table 2: Bootloader activation patterns*). The following table shows the hardware resources used by this bootloader.

Table 73.STM32F446xx configuration in system memory boot mode

Bootloader	Feature/Peripheral	State	Comment
Common to all bootloaders	RCC	HSI enabled	The HSI is used at startup as clock source for system clock configured to 60 MHz and for USART, I2C and SPI bootloader operation.
		HSE enabled	The HSE is used only when the CAN or the DFU (USB FS Device) interfaces are selected. In this case the system clock configured to 60 MHz with HSE as clock source. The HSE frequency must be multiple of 1 MHz and ranging from 4 MHz to 26 MHz.
		-	The Clock Security System (CSS) interrupt is enabled for the CAN and DFU bootloaders. Any failure (or removal) of the external clock generates system reset.
	RAM	-	12 Kbyte starting from address 0x20000000 are used by the bootloader firmware
	System memory	-	29 Kbyte starting from address 0x1FFF0000, contain the bootloader firmware
	IWDG	-	The independent watchdog (IWDG) prescaler is configured to its maximum value. It is periodically refreshed to prevent watchdog reset (in case the hardware IWDG option was previously enabled by the user).
	Power	-	The voltage range is [1.71 V, 3.6 V]. In this range: - Flash wait states 3. - System Clock 60 MHz. - Prefetch disabled. - Flash write operation by byte (refer to section bootloader memory management for more information).

Table 73.STM32F446xx configuration in system memory boot mode (continued)

Bootloader	Feature/Peripheral	State	Comment
USART1 bootloader	USART1	Enabled	Once initialized the USART1 configuration is: 8-bits, even parity and 1 Stop bit
	USART1_RX pin	Input	PA10 pin: USART1 in reception mode
	USART1_TX pin	Output	PA9 pin: USART1 in transmission mode
USART3 bootloader (on PB10/PB11)	USART3	Enabled	Once initialized the USART3 configuration is: 8-bits, even parity and 1 Stop bit
	USART3_RX pin	Input	PB11 pin: USART3 in reception mode
	USART3_TX pin	Output	PB10 pin: USART3 in transmission mode
USART3 bootloader (on PC10/PC11)	USART3	Enabled	Once initialized the USART3 configuration is: 8-bits, even parity and 1 Stop bit
	USART3_RX pin	Input	PC11 pin: USART3 in reception mode
	USART3_TX pin	Output	PC10 pin: USART3 in transmission mode
USARTx bootloaders	SysTick timer	Enabled	Used to automatically detect the serial baud rate from the host for USARTx bootloaders.
CAN2 bootloader	CAN2	Enabled	Once initialized the CAN2 configuration is: Baudrate 125 kbps, 11-bit identifier. **Note:** CAN1 is clocked during CAN2 bootloader execution because in CAN1 manages the communication between CAN2 and SRAM.
	CAN2_RX pin	Input	PB5 pin: CAN2 in reception mode
	CAN2_TX pin	Output	PB13 pin: CAN2 in transmission mode
I2C1 bootloader	I2C1	Enabled	The I2C1 configuration is: I2C speed: up to 400 KHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b0111100x (where x = 0 for write and x = 1 for read)
	I2C1_SCL pin	Input/Output	PB6 pin: clock line is used in open-drain mode.
	I2C1_SDA pin	Input/Output	PB9 pin: data line is used in open-drain mode.
I2C2 bootloader	I2C2	Enabled	The I2C2 configuration is: I2C speed: up to 400 KHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b0111100x (where x = 0 for write and x = 1 for read)
	I2C2_SCL pin	Input/Output	PF1 pin: clock line is used in open-drain mode.
	I2C2_SDA pin	Input/Output	PF0 pin: data line is used in open-drain mode.

Table 73.STM32F446xx configuration in system memory boot mode (continued)

Bootloader	Feature/Peripheral	State	Comment
I2C3 bootloader	I2C3	Enabled	The I2C3 configuration is: I2C speed: up to 400 KHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b0111100x (where x = 0 for write and x = 1 for read)
	I2C3_SCL pin	Input/Output	PA8 pin: clock line is used in open-drain mode.
	I2C3_SDA pin	Input/Output	PC9 pin: data line is used in open-drain mode.
SPI1 bootloader	SPI1	Enabled	The SPI1 configuration is: Slave mode, Full Duplex, 8-bit MSB, Speed up to 8 MHz, Polarity: CPOL Low, CPHA Low, NSS hardware.
	SPI1_MOSI pin	Input	PA7 pin: Slave data Input line, used in push-pull pull-down mode
	SPI1_MISO pin	Output	PA6 pin: Slave data output line, used in push-pull pull-down mode
	SPI1_SCK pin	Input	PA5 pin: Slave clock line, used in push-pull pull-down mode
	SPI1_NSS pin	Input	PA4 pin: slave chip select pin used in push-pull pull-up mode.
SPI2 bootloader	SPI2	Enabled	The SPI2 configuration is: Slave mode, Full Duplex, 8-bit MSB, Speed up to 8 MHz, Polarity: CPOL Low, CPHA Low, NSS hardware.
	SPI2_MOSI pin	Input	PB15 pin: Slave data Input line, used in push-pull pull-down mode
	SPI2_MISO pin	Output	PB14 pin: Slave data output line, used in push-pull pull-down mode
	SPI2_SCK pin	Input	PC7 pin: Slave clock line, used in push-pull pull-down mode
	SPI2_NSS pin	Input	PB12 pin: slave chip select pin used in push-pull pull-up mode.

Table 73.STM32F446xx configuration in system memory boot mode (continued)

Bootloader	Feature/Peripheral	State	Comment
SPI4 bootloader	SPI4	Enabled	The SPI4 configuration is: Slave mode, Full Duplex, 8-bit MSB, Speed up to 8 MHz, Polarity: CPOL Low, CPHA Low, NSS hardware.
	SPI4_MOSI pin	Input	PE14 pin: Slave data Input line, used in push-pull pull-down mode
	SPI4_MISO pin	Output	PE13 pin: Slave data output line, used in push-pull pull-down mode
	SPI4_SCK pin	Input	PE12 pin: Slave clock line, used in push-pull pull-down mode
	SPI4_NSS pin	Input	PE11 pin: slave chip select pin used in push-pull pull-up mode.
DFU bootloader	USB	Enabled	USB OTG FS configured in forced device mode
	USB_DM pin	Input/Output	PA11: USB DM line.
	USB_DP pin		PA12: USB DP line No external Pull-up resistor is required
CAN2 and DFU bootloaders	TIM17	Enabled	This timer is used to determine the value of the HSE. Once the HSE frequency is determinated, the system clock is configured to 60 MHz using PLL and HSE.

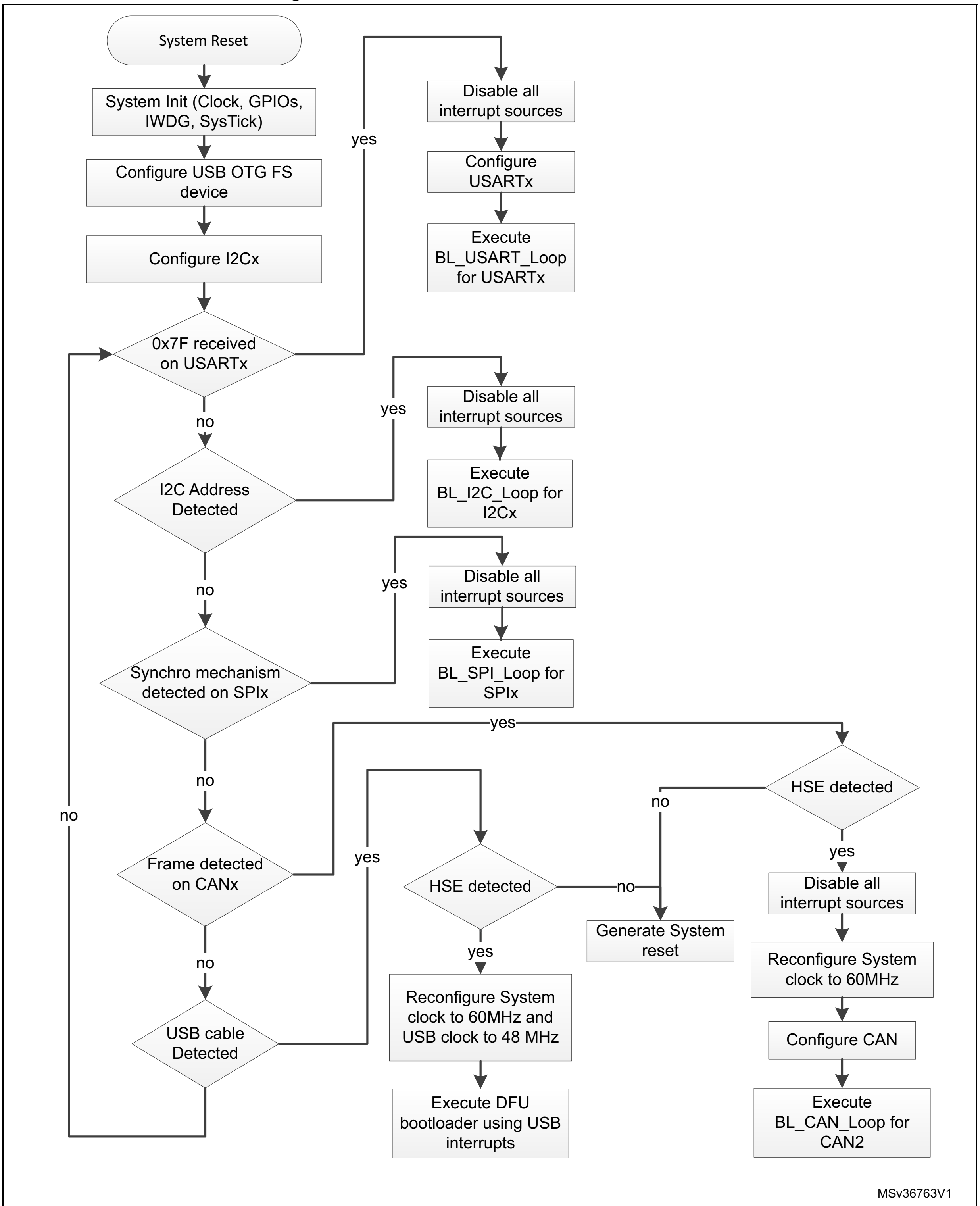
The system clock is derived from the embedded internal high-speed RC for USARTx and I2Cx bootloaders. This internal clock is also used for CAN and DFU (USB FS Device) but only for the selection phase. An external clock multiple of 1 MHz (between 4 and 26 MHz) is required for CAN and DFU bootloader execution after the selection phase.

Note: Due to HSI deviation and since HSI is used to detect HSE value, the user must use low frequency HSE crystal values rather than high frequency values.
Low frequency values are better detected due to larger error margin. For example, it is better to use 8 MHz instead of 25 MHz.

34.2 Bootloader selection

The figure below shows the bootloader selection mechanism.

Figure 42.Bootloader V9.x selection for STM32F446xx



34.3 Bootloader version

The following table lists the STM32F446xx devices bootloader V9.x versions:

Table 74. STM32F446xx bootloader V9.x versions

Bootloader version number	Description	Known limitations
V9.0	Initial bootloader version	After executing Go command (jump to user code) the bootloader resets AHB1ENR value to 0x0000 0000 and thus CCM RAM, when present, is not active (shall be re-enabled by user code at startup)

35 STM32F469xx/479xx devices bootloader

35.1 Bootloader configuration

The STM32F469xx/479xx bootloader is activated by applying pattern5 (described in *Table 2: Bootloader activation patterns*). The following table shows the hardware resources used by this bootloader.

Table 75. STM32F469xx/479xx configuration in system memory boot mode

Bootloader	Feature/Peripheral	State	Comment
Common to all bootloaders	RCC	HSI enabled	The system clock frequency is 60 MHz using the PLL. The HSI clock source is used at startup (interface detection phase) and when USART or SPI or I2C interfaces are selected (once CAN or DFU bootloader is selected, the clock source will be derived from external crystal).
		HSE enabled	The system clock frequency is 60 MHz. The HSE clock source is used only when the CAN or the DFU (USB FS Device) interfaces are selected. The external clock must provide a frequency multiple of 1 MHz and ranging from 4 MHz to 26 MHz.
		-	The Clock Security System (CSS) interrupt is enabled for the CAN and DFU bootloaders. Any failure (or removal) of the external clock generates system reset.
	RAM	-	12 Kbyte starting from address 0x20000000 are used by the bootloader firmware
	System memory	-	29 Kbyte starting from address 0x1FFF0000, contain the bootloader firmware
	IWDG	-	The independent watchdog (IWDG) prescaler is configured to its maximum value. It is periodically refreshed to prevent watchdog reset (in case the hardware IWDG option was previously enabled by the user).
	Power	-	Voltage range is set to [1.62 V, 2.1 V]. In this range internal Flash write operations are allowed only in byte format (Half-Word, Word and Double-Word operations are not allowed). The voltage range can be configured in run time using bootloader commands.

Table 75. STM32F469xx/479xx configuration in system memory boot mode (continued)

Bootloader	Feature/Peripheral	State	Comment
USART1 bootloader	USART1	Enabled	Once initialized the USART1 configuration is: 8-bits, even parity and 1 Stop bit
	USART1_RX pin	Input	PA10 pin: USART1 in reception mode
	USART1_TX pin	Output	PA9 pin: USART1 in transmission mode
USART3 bootloader (on PB10/PB11)	USART3	Enabled	Once initialized the USART3 configuration is: 8-bits, even parity and 1 Stop bit
	USART3_RX pin	Input	PB11 pin: USART3 in reception mode
	USART3_TX pin	Output	PB10 pin: USART3 in transmission mode
USART3 bootloader (on PC10/PC11)	USART3	Enabled	Once initialized the USART3 configuration is: 8-bits, even parity and 1 Stop bit
	USART3_RX pin	Input	PC11 pin: USART3 in reception mode
	USART3_TX pin	Output	PC10 pin: USART3 in transmission mode
USARTx bootloaders	SysTick timer	Enabled	Used to automatically detect the serial baud rate from the host for USARTx bootloaders.
CAN2 bootloader	CAN2	Enabled	Once initialized the CAN2 configuration is: Baudrate 125 kbps, 11-bit identifier. **Note:** CAN1 is clocked during CAN2 bootloader execution because CAN1 manages the communication between CAN2 and SRAM.
	CAN2_RX pin	Input	PB05 pin: CAN2 in reception mode
	CAN2_TX pin	Output	PB13 pin: CAN2 in transmission mode
I2C1 bootloader	I2C1	Enabled	The I2C1 configuration is: I2C speed: up to 400 KHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b1000100x (where x = 0 for write and x = 1 for read).
	I2C1_SCL pin	Input/Output	PB6 pin: clock line is used in open-drain mode.
	I2C1_SDA pin	Input/Output	PB9 pin: data line is used in open-drain mode.
I2C2 bootloader	I2C2	Enabled	The I2C2 configuration is: I2C speed: up to 400 KHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b1000100x (where x = 0 for write and x = 1 for read).
	I2C2_SCL pin	Input/Output	PF0 pin: clock line is used in open-drain mode.
	I2C2_SDA pin	Input/Output	PF1 pin: data line is used in open-drain mode.

Table 75. STM32F469xx/479xx configuration in system memory boot mode (continued)

Bootloader	Feature/Peripheral	State	Comment
I2C3 bootloader	I2C3	Enabled	The I2C3 configuration is: I2C speed: up to 400 KHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b1000100x (where x = 0 for write and x = 1 for read).
	I2C3_SCL pin	Input/Output	PA8 pin: clock line is used in open-drain mode.
	I2C3_SDA pin	Input/Output	PC9 pin: data line is used in open-drain mode.
SPI1 bootloader	SPI1	Enabled	The SPI1 configuration is: Slave mode, Full Duplex, 8-bit MSB, Speed up to 8 MHz, Polarity: CPOL Low, CPHA Low, NSS hardware.
	SPI1_MOSI pin	Input	PA7 pin: Slave data Input line, used in push-pull pull-down mode
	SPI1_MISO pin	Output	PA6 pin: Slave data output line, used in push-pull pull-down mode
	SPI1_SCK pin	Input	PA5 pin: Slave clock line, used in push-pull pull-down mode
	SPI1_NSS pin	Input	PA4 pin: slave chip select pin used in push-pull pull-up mode.
SPI2 bootloader	SPI2	Enabled	The SPI2 configuration is: Slave mode, Full Duplex, 8-bit MSB, Speed up to 8 MHz, Polarity: CPOL Low, CPHA Low, NSS hardware.
	SPI2_MOSI pin	Input	PI3 pin: Slave data Input line, used in push-pull pull-down mode
	SPI2_MISO pin	Output	PI2 pin: Slave data output line, used in push-pull pull-down mode
	SPI2_SCK pin	Input	PI1pin: Slave clock line, used in push-pull pull-down mode
	SPI2_NSS pin	Input	PI0 pin: slave chip select pin used in push-pull pull-up mode.

Table 75. STM32F469xx/479xx configuration in system memory boot mode (continued)

Bootloader	Feature/Peripheral	State	Comment
SPI4 bootloader	SPI4	Enabled	The SPI4 configuration is: Slave mode, Full Duplex, 8-bit MSB, Speed up to 8 MHz, Polarity: CPOL Low, CPHA Low, NSS hardware.
	SPI4_MOSI pin	Input	PE14 pin: Slave data Input line, used in push-pull pull-down mode
	SPI4_MISO pin	Output	PE13 pin: Slave data output line, used in push-pull pull-down mode
	SP4_SCK pin	Input	PE12 pin: Slave clock line, used in push-pull pull-down mode
	SPI4_NSS pin	Input	PE11 pin: slave chip select pin used in push-pull pull-up mode.
DFU bootloader	USB	Enabled	USB OTG FS configured in forced device mode. USB_OTG_FS interrupt vector is enabled and used for USB DFU communications.
	USB_DM pin	Input/Output	PA11 pin: USB DM line.
	USB_DP pin		PA12 pin: USB DP line. No external Pull-Up resistor is required.

The system clock is derived from the embedded internal high-speed RC for USARTx and I2Cx bootloaders. This internal clock is also used for CAN and DFU (USB FS Device) but only for the selection phase. An external clock multiple of 1 MHz (between 4 and 48 MHz) is required for CAN and DFU bootloaders execution after the selection phase.

Note: Due to HSI deviation and since HSI is used to detect HSE value, the user must use low frequency HSE crystal values rather than high frequency values.
Low frequency values are better detected due to larger error margin. For example, it is better to use 8 MHz instead of 25 MHz.

35.2 Bootloader selection

The *Figure 43* and *Figure 44* show the bootloader selection mechanism.

Figure 43. Dual Bank Boot Implementation for STM32F469xx/479xx Bootloader V9.x

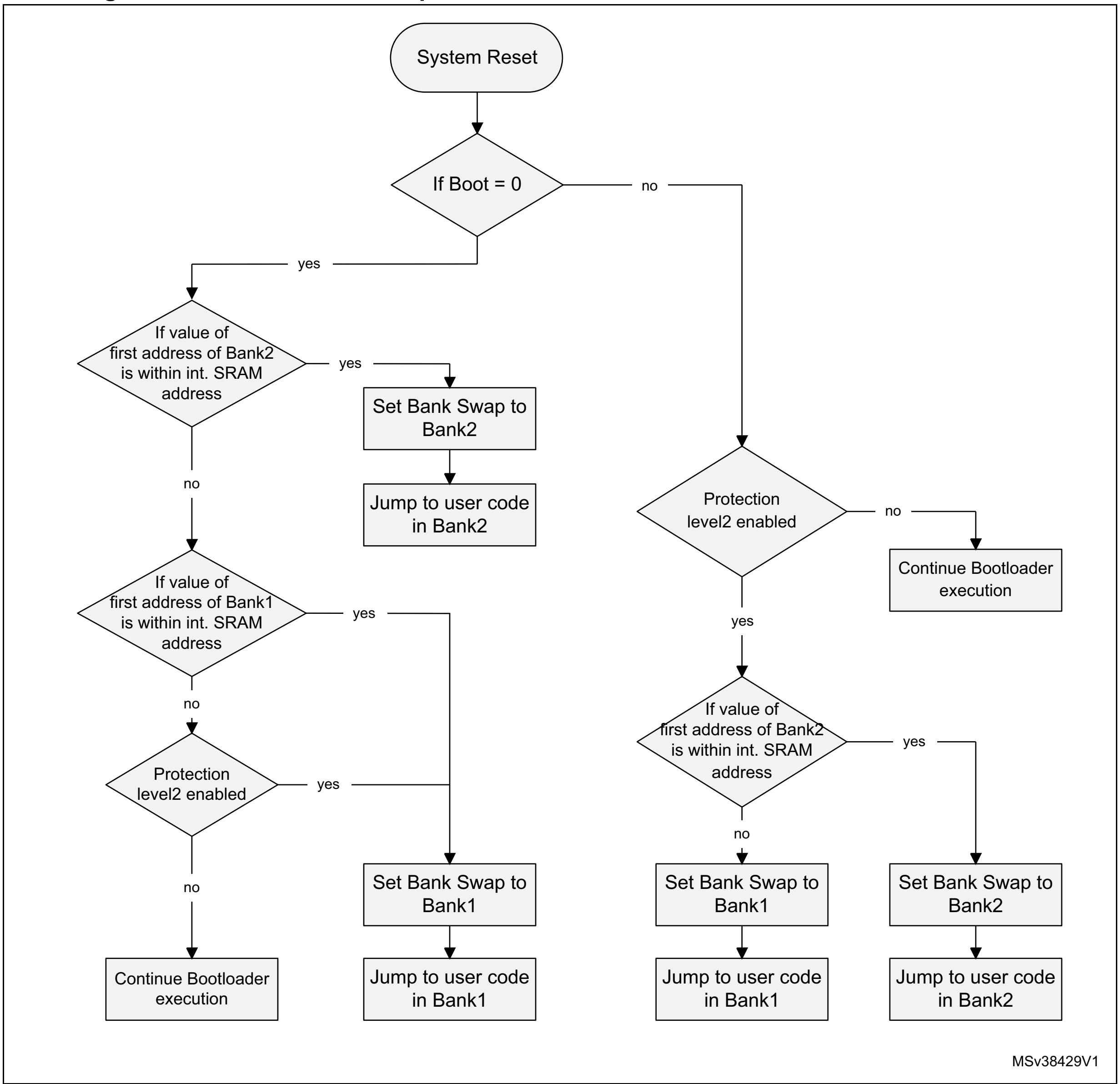
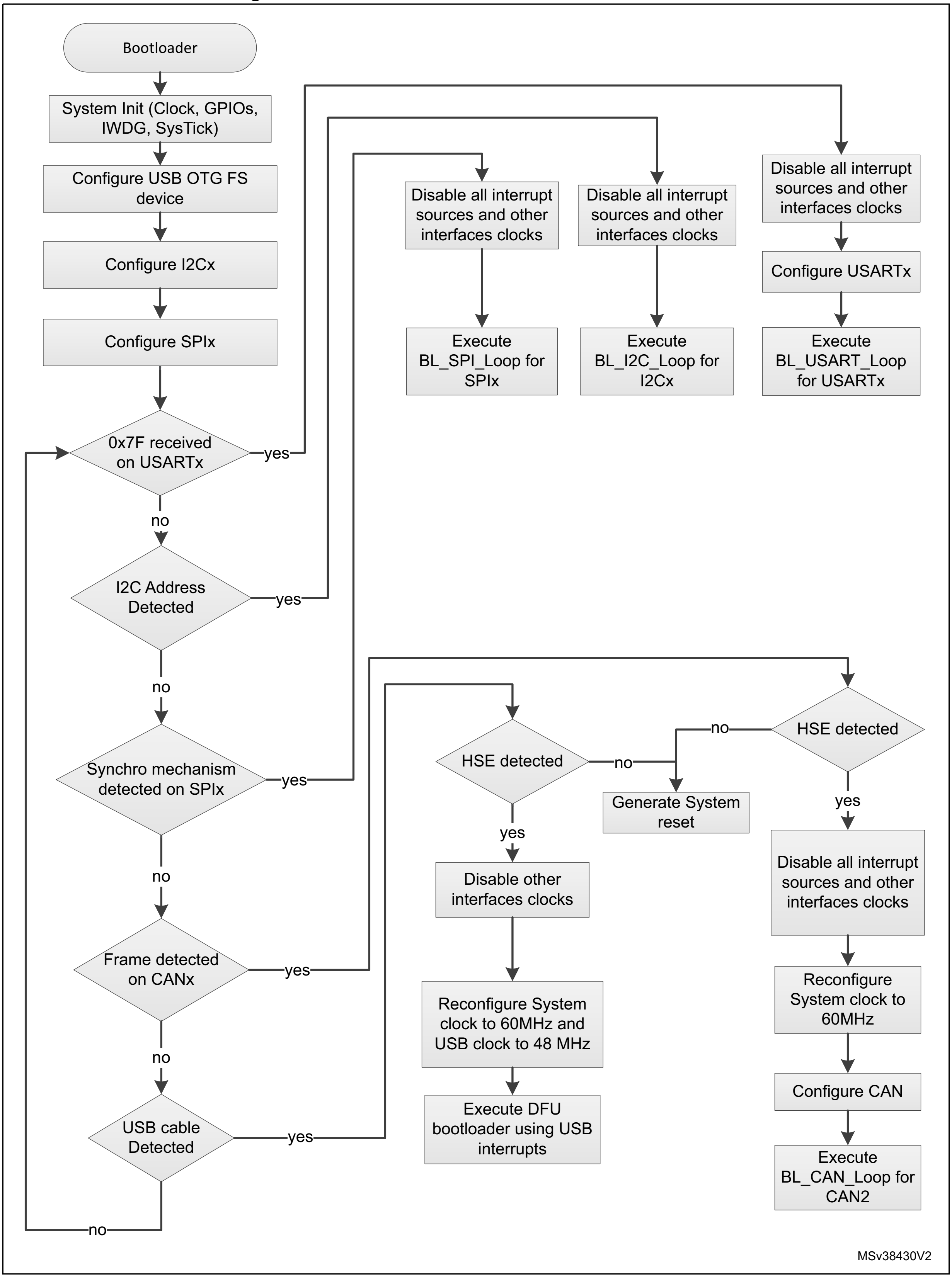


Figure 44.Bootloader V9.x selection for STM32F469xx/479xx



35.3 Bootloader version

The following table lists the STM32F469xx/479xx devices V9.x bootloader versions:

Table 76. STM32F469xx/479xx bootloader V9.x versions

Bootloader version number	Description	Known limitations
V9.0	Initial bootloader version	After executing Go command (jump to user code) the bootloader resets AHB1ENR value to 0x0000 0000 and thus CCM RAM, when present, is not active (shall be re-enabled by user code at startup)

36 STM32F72xxx/73xxx devices bootloader

36.1 Bootloader configuration

The STM32F72xxx/73xxx bootloader is activated by applying pattern8 (described in *Table 2: Bootloader activation patterns*). The *Table 77* shows the hardware resources used by this bootloader.

Table 77. STM32F72xxx/73xxx configuration in system memory boot mode

Bootloader	Feature/Peripheral	State	Comment
Common to all bootloaders	RCC	HSI enabled	The HSI is used at startup as clock source for system clock configured to 60 MHz and for USART and I2C bootloader operation.
		HSE enabled	The HSE is used only when the CAN or the DFU (USB FS Device) interfaces are selected. In this case the system clock configured to 60 MHz with HSE as clock source. The HSE frequency must be multiple of 1 MHz and ranging from 4 MHz to 26 MHz.
		-	The Clock Security System (CSS) interrupt is enabled for the CAN and DFU bootloaders. Any failure (or removal) of the external clock generates system reset.
	RAM	-	16 Kbyte starting from address 0x20000000 are used by the bootloader firmware
	System memory	-	59 Kbyte starting from address 0x1FF00000, contain the bootloader firmware
	IWDG	-	The independent watchdog (IWDG) prescaler is configured to its maximum value. It is periodically refreshed to prevent watchdog reset (in case the hardware IWDG option was previously enabled by the user).
	Power	-	The voltage range is [1.8V, 3.6V] In this range: - Flash wait states 3. - System clock Frequency 60 MHz. - ART Accelerator enabled. - Flash write operation by byte (refer to bootloader memory management section for more information).

Table 77. STM32F72xxx/73xxx configuration in system memory boot mode (continued)

Bootloader	Feature/Peripheral	State	Comment
USART1 bootloader	USART1	Enabled	Once initialized the USART1 configuration is: 8-bits, even parity and 1 Stop bit
	USART1_RX pin	Input	PA10 pin: USART1 in reception mode
	USART1_TX pin	Output	PA9 pin: USART1 in transmission mode
USART3 bootloader (on PB11/PB10)	USART3	Enabled	Once initialized the USART3 configuration is: 8-bits, even parity and 1 Stop bit
	USART3_RX pin	Input	PB11 pin: USART3 in reception mode
	USART3_TX pin	Output	PB10 pin: USART3 in transmission mode
USART3 bootloader (on PC11/PC10)	USART3	Enabled	Once initialized the USART3 configuration is: 8-bits, even parity and 1 Stop bit
	USART3_RX pin	Input	PC11 pin: USART3 in reception mode
	USART3_TX pin	Output	PC10 pin: USART3 in transmission mode
USARTx bootloaders	SysTick timer	Enabled	Used to automatically detect the serial baud rate from the host for USARTx bootloaders.
CAN1 bootloader	CAN1	Enabled	Once initialized the CAN1 configuration is: Baudrate 125 kbps, 11-bit identifier.
	CAN1_RX pin	Input	PD0 pin: CAN1 in reception mode
	CAN1_TX pin	Output	PD1 pin: CAN1 in transmission mode
I2C1 bootloader	I2C1	Enabled	The I2C1 configuration is: I2C speed: up to 400 KHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b1001001x (where x = 0 for write and x = 1 for read)
	I2C1_SCL pin	Input/Output	PB6 pin: clock line is used in open-drain mode.
	I2C1_SDA pin	Input/Output	PB9 pin: data line is used in open-drain mode.

Table 77. STM32F72xxx/73xxx configuration in system memory boot mode (continued)

Bootloader	Feature/Peripheral	State	Comment
I2C2 bootloader	I2C2	Enabled	The I2C2 configuration is: I2C speed: up to 400 KHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b1001101x (where x = 0 for write and x = 1 for read)
	I2C2_SCL pin	Input/Output	PF1 pin: clock line is used in open-drain mode.
	I2C2_SDA pin	Input/Output	PF0 pin: data line is used in open-drain mode.
I2C3 bootloader	I2C3	Enabled	The I2C3 configuration is: I2C speed: up to 400 KHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b1001001x (where x = 0 for write and x = 1 for read)
	I2C3_SCL pin	Input/Output	PA8 pin: clock line is used in open-drain mode.
	I2C3_SDA pin	Input/Output	PC9 pin: data line is used in open-drain mode.
SPI1 bootloader	SPI1	Enabled	The SPI1 configuration is: Slave mode, Full Duplex, 8-bit MSB, Speed up to 8MHz, Polarity: CPOL Low, CPHA Low, NSS hardware.
	SPI1_MOSI pin	Input	PA7 pin: Slave data Input line, used in push-pull pull-down mode
	SPI1_MISO pin	Output	PA6 pin: Slave data output line, used in push-pull pull-down mode
	SPI1_SCK pin	Input	PA5 pin: Slave clock line, used in push-pull pull-down mode
	SPI1_NSS pin	Input	PA4 pin: slave chip select pin used in push-pull pull-up mode.
SPI2 bootloader	SPI2	Enabled	The SPI2 configuration is: Slave mode, Full Duplex, 8-bit MSB, Speed up to 8MHz, Polarity: CPOL Low, CPHA Low, NSS hardware.
	SPI2_MOSI pin	Input	PI3 pin: Slave data Input line, used in push-pull pull-down mode
	SPI2_MISO pin	Output	PI2 pin: Slave data output line, used in push-pull pull-down mode
	SPI2_SCK pin	Input	PI1 pin: Slave clock line, used in push-pull pull-down mode
	SPI2_NSS pin	Input	PI0 pin: slave chip select pin used in push-pull pull-up mode.

Table 77. STM32F72xxx/73xxx configuration in system memory boot mode (continued)

Bootloader	Feature/Peripheral	State	Comment
SPI4 bootloader	SPI4	Enabled	The SPI4 configuration is: Slave mode, Full Duplex, 8-bit MSB, Speed up to 8MHz, Polarity: CPOL Low, CPHA Low, NSS hardware.
	SPI4_MOSI pin	Input	PE14 pin: Slave data Input line, used in push-pull pull-down mode
	SPI4_MISO pin	Output	PE13 pin: Slave data output line, used in push-pull pull-down mode
	SP4_SCK pin	Input	PE12 pin: Slave clock line, used in push-pull pull-down mode
	SPI4_NSS pin	Input	PE11 pin: slave chip select pin used in push-pull pull-up mode.
DFU bootloader	USB	Enabled	USB OTG FS configured in forced device mode
	USB_DM pin	Input/Output	PA11 pin: USB DM line.
	USB_DP pin		PA12 pin: USB DP line No external Pull-Up resistor is required.
CAN1 and DFU bootloaders	TIM11	Enabled	This timer is used to determine the value of the HSE. Once HSE frequency is determined, the system clock is configured to 60 MHz using PLL and HSE.

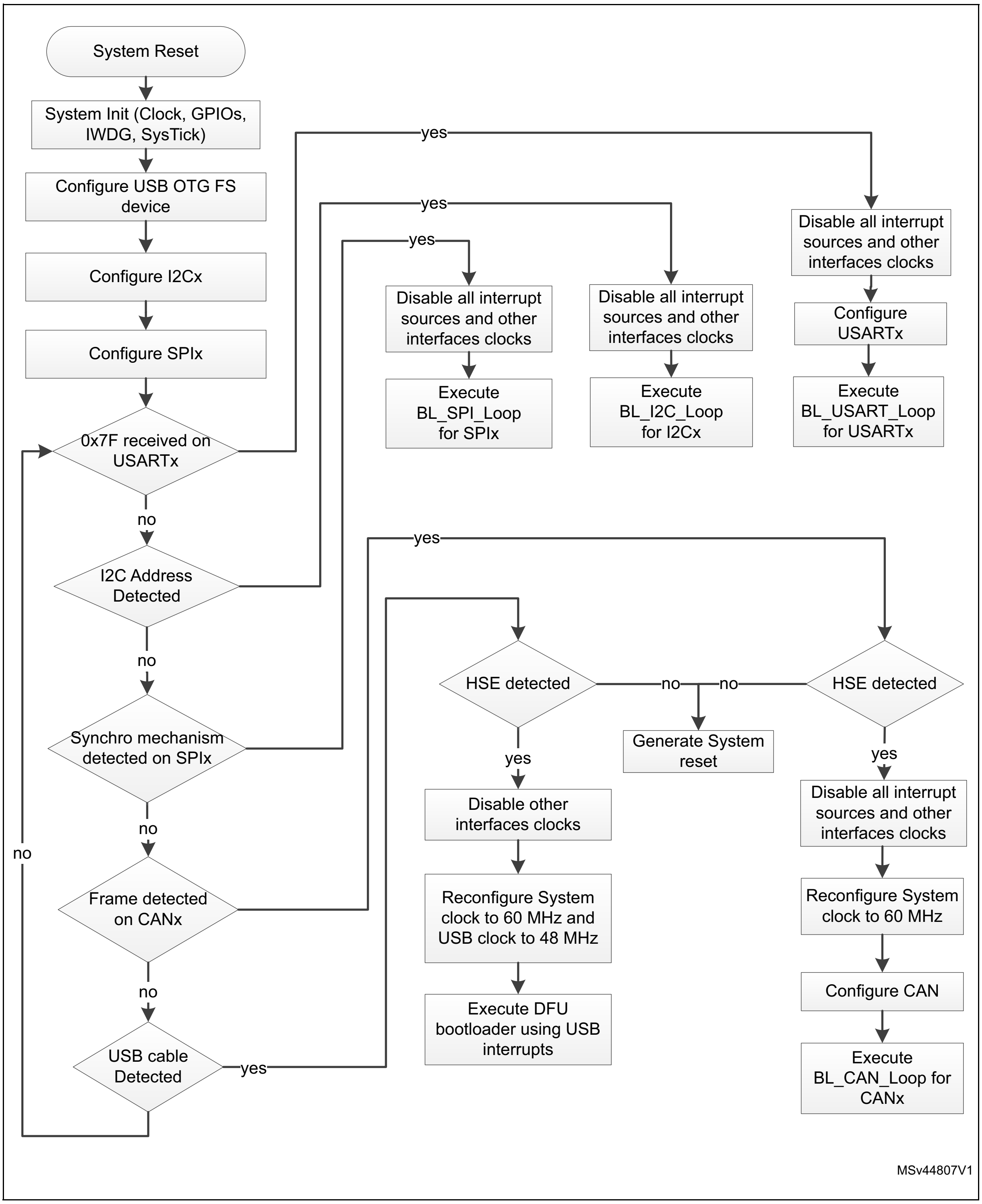
The system clock is derived from the embedded internal high-speed RC for USARTx and I2Cx bootloaders. This internal clock is also used for CAN and DFU (USB FS Device) but only for the selection phase. An external clock multiple of 1 MHz (between 4 and 26 MHz) is required for CAN and DFU bootloader execution after the selection phase.

Note: Due to HSI deviation and since HSI is used to detect HSE value, the user must use low frequency HSE crystal values rather than high frequency values.
Low frequency values are better detected due to larger error margin. For example, it is better to use 8 MHz instead of 25 MHz.

36.2 Bootloader selection

The *Figure 45* below show the bootloader selection mechanism:

Figure 45. Bootloader V9.x selection for STM32F72xxx/73xxx



36.3 Bootloader version

The *Table 78* lists the STM32F72xxx/73xxx devices bootloader V9.x versions.

Table 78. STM32F72xxx/73xxx bootloader V9.x versions

Bootloader version number	Description	Known limitations
V9.0	Initial bootloader version	At high UART baudrates (115200bps) connection may fail due to software jitter leading to wrong baudrate calculation. In that case bootloader may respond with a baudrate up to ± 5% different from host baudrate. Workaround: use baudrates lower than 57600 bps if host tolerance to baudrate error is lower than ± 5%

37 STM32F74xxx/75xxx devices bootloader

Two bootloader versions are available on STM32F74xxx/75xxx:

- V7.x supporting USART1, USART3, CAN2, I2C1, I2C2, I2C3 and DFU (USB FS Device). This version is embedded in STM32F74xxx/75xxx rev. A devices.
- V9.x supporting USART1, USART3, CAN2, I2C1, I2C2, I2C3, SPI1, SPI2, SPI4 and DFU (USB FS Device). This version is embedded in STM32F74xxx/75xxx rev. Z and rev. 1 devices.

Note: When readout protection Level2 is activated, STM32F74xxx/75xxx devices can boot also on system memory and all commands are not accessible except Get, GetID, and GetVersion.

37.1 Bootloader V7.x

37.1.1 Bootloader configuration

The STM32F74xxx/75xxx bootloader is activated by applying pattern8 (described in *Table 2: Bootloader activation patterns*). The following table shows the hardware resources used by this bootloader.

Table 79. STM32F74xxx/75xxx configuration in system memory boot mode

Bootloader	Feature/Peripheral	State	Comment
Common to all bootloaders	RCC	HSI enabled	The HSI is used at startup as clock source for system clock configured to 60 MHz and for USART and I2C bootloader operation.
		HSE enabled	The HSE is used only when the CAN or the DFU (USB FS Device) interfaces are selected. In this case the system clock configured to 60 MHz with HSE as clock source. The HSE frequency must be multiple of 1 MHz and ranging from 4 MHz to 26 MHz.
		-	The Clock Security System (CSS) interrupt is enabled for the CAN and DFU bootloaders. Any failure (or removal) of the external clock generates system reset.
	RAM	-	16 Kbyte starting from address 0x20000000 are used by the bootloader firmware
	System memory	-	60 Kbyte starting from address 0x1FF00000, contain the bootloader firmware
	IWDG	-	The independent watchdog (IWDG) prescaler is configured to its maximum value. It is periodically refreshed to prevent watchdog reset (in case the hardware IWDG option was previously enabled by the user).
	Power	-	The voltage range is [1.8V, 3.6V]. In this range: - Flash wait states 3. - System clock Frequency 60 MHz. - ART Accelerator enabled. - Flash write operation by byte (refer to bootloader memory management section for more information).
USART1 bootloader	USART1	Enabled	Once initialized the USART1 configuration is: 8-bits, even parity and 1 Stop bit
	USART1_RX pin	Input	PA10 pin: USART1 in reception mode
	USART1_TX pin	Output	PA9 pin: USART1 in transmission mode
USART3 bootloader (on PB10/PB11)	USART3	Enabled	Once initialized the USART3 configuration is: 8-bits, even parity and 1 Stop bit
	USART3_RX pin	Input	PB11 pin: USART3 in reception mode
	USART3_TX pin	Output	PB10 pin: USART3 in transmission mode

Table 79. STM32F74xxx/75xxx configuration in system memory boot mode (continued)

Bootloader	Feature/Peripheral	State	Comment
USART3 bootloader (on PC10/PC11)	USART3	Enabled	Once initialized the USART3 configuration is: 8-bits, even parity and 1 Stop bit
	USART3_RX pin	Input	PC11 pin: USART3 in reception mode
	USART3_TX pin	Output	PC10 pin: USART3 in transmission mode
USARTx bootloaders	SysTick timer	Enabled	Used to automatically detect the serial baud rate from the host for USARTx bootloaders.
CAN2 bootloader	CAN2	Enabled	Once initialized the CAN2 configuration is: Baudrate 125 kbps, 11-bit identifier. **Note:** CAN1 is clocked during CAN2 bootloader execution because CAN1 manages the communication between CAN2 and SRAM.
	CAN2_RX pin	Input	PB5 pin: CAN2 in reception mode
	CAN2_TX pin	Output	PB13 pin: CAN2 in transmission mode
I2C1 bootloader	I2C1	Enabled	The I2C1 configuration is: I2C speed: up to 400 KHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b1000101x (where x = 0 for write and x = 1 for read)
	I2C1_SCL pin	Input/Output	PB6 pin: clock line is used in open-drain mode.
	I2C1_SDA pin	Input/Output	PB9 pin: data line is used in open-drain mode.
I2C2 bootloader	I2C2	Enabled	The I2C2 configuration is: I2C speed: up to 400 KHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b1000101x (where x = 0 for write and x = 1 for read)
	I2C2_SCL pin	Input/Output	PF1 pin: clock line is used in open-drain mode.
	I2C2_SDA pin	Input/Output	PF0 pin: data line is used in open-drain mode.
I2C3 bootloader	I2C3	Enabled	The I2C3 configuration is: I2C speed: up to 400 KHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b1000101x (where x = 0 for write and x = 1 for read)
	I2C3_SCL pin	Input/Output	PA8 pin: clock line is used in open-drain mode.
	I2C3_SDA pin	Input/Output	PC9 pin: data line is used in open-drain mode.
DFU bootloader	USB	Enabled	USB OTG FS configured in forced device mode.
	USB_DM pin	Input/Output	PA11 pin: USB DM line.
	USB_DP pin		PA12 pin: USB DP line No external Pull-Up resistor is required.
CAN2 and DFU bootloaders	TIM11	Enabled	This timer is used to determine the value of the HSE. Once HSE frequency is determined, the system clock is configured to 60 MHz using PLL and HSE.

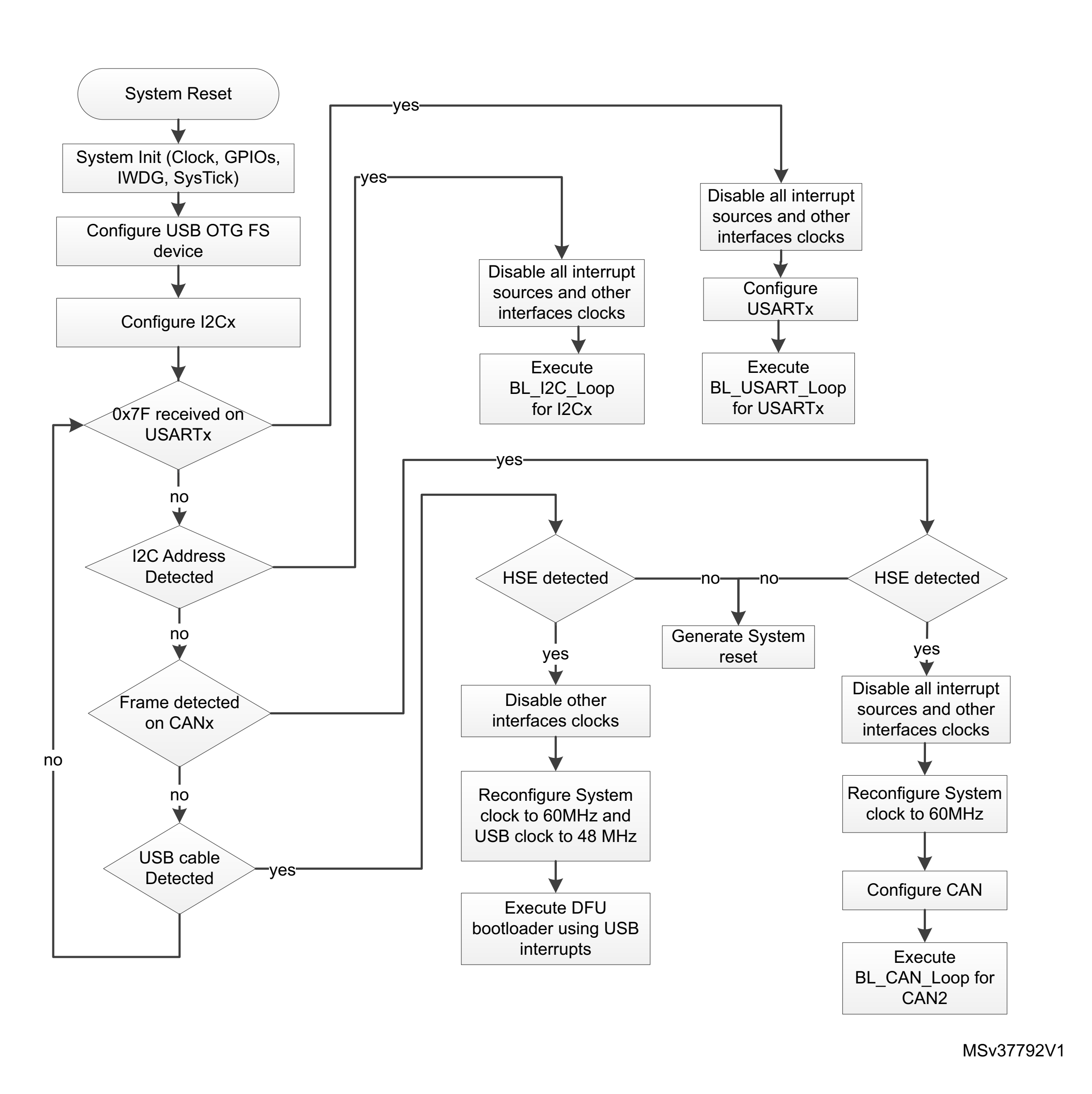
The system clock is derived from the embedded internal high-speed RC for USARTx and I2Cx bootloaders. This internal clock is also used for CAN and DFU (USB FS Device) but only for the selection phase. An external clock multiple of 1 MHz (between 4 and 26 MHz) is required for CAN and DFU bootloader execution after the selection phase.

Note: Due to HSI deviation and since HSI is used to detect HSE value, the user must use low frequency HSE crystal values rather than high frequency values.
Low frequency values are better detected due to larger error margin. For example, it is better to use 8 MHz instead of 25 MHz.

37.1.2 Bootloader selection

The figure below shows the bootloader selection mechanism.

Figure 46.Bootloader V7.x selection for STM32F74xxx/75xxx



37.1.3 Bootloader version

The following table lists the STM32F74xxx/75xxx devices bootloader V7.x versions:

Table 80. STM32F74xxx/75xxx bootloader V7.x versions

Bootloader version number	Description	Known limitations
V7.0	Initial bootloader version	At high UART baudrates (115200bps) connection may fail due to software jitter leading to wrong baudrate calculation. In that case bootloader may respond with a baudrate up to ± 5% different from host baudrate. Workaround: use baudrates lower than 57600 bps if host tolerance to baudrate error is lower than ± 5%

37.2 Bootloader V9.x

37.2.1 Bootloader configuration

The STM32F74xxx/75xxx bootloader is activated by applying pattern8 (described in *Table 2: Bootloader activation patterns*). The following table shows the hardware resources used by this bootloader.

Table 81. STM32F74xxx/75xxx configuration in system memory boot mode

Bootloader	Feature/Peripheral	State	Comment
Common to all bootloaders	RCC	HSI enabled	The HSI is used at startup as clock source for system clock configured to 60 MHz and for USART, I2C and SPI bootloader operation.
		HSE enabled	The HSE is used only when the CAN or the DFU (USB FS Device) interfaces are selected. In this case the system clock configured to 60 MHz with HSE as clock source. The HSE frequency must be multiple of 1 MHz and ranging from 4 MHz to 26 MHz.
		-	The Clock Security System (CSS) interrupt is enabled for the CAN and DFU bootloaders. Any failure (or removal) of the external clock generates system reset.
	RAM	-	16 Kbyte starting from address 0x20000000 are used by the bootloader firmware
	System memory	-	60 Kbyte starting from address 0x1FF00000, contain the bootloader firmware
	IWDG	-	The independent watchdog (IWDG) prescaler is configured to its maximum value. It is periodically refreshed to prevent watchdog reset (in case the hardware IWDG option was previously enabled by the user).
	Power	-	The voltage range is [1.8V, 3.6V] In this range: - Flash wait states 3. - System clock Frequency 60 MHz. - ART Accelerator enabled. - Flash write operation by byte (refer to bootloader memory management section for more information).

Table 81. STM32F74xxx/75xxx configuration in system memory boot mode (continued)

Bootloader	Feature/Peripheral	State	Comment
USART1 bootloader	USART1	Enabled	Once initialized the USART1 configuration is: 8-bits, even parity and 1 Stop bit
	USART1_RX pin	Input	PA10 pin: USART1 in reception mode
	USART1_TX pin	Output	PA9 pin: USART1 in transmission mode
USART3 bootloader (on PB10/PB11)	USART3	Enabled	Once initialized the USART3 configuration is: 8-bits, even parity and 1 Stop bit
	USART3_RX pin	Input	PB11 pin: USART3 in reception mode
	USART3_TX pin	Output	PB10 pin: USART3 in transmission mode
USART3 bootloader (on PC10/PC11)	USART3	Enabled	Once initialized the USART3 configuration is: 8-bits, even parity and 1 Stop bit
	USART3_RX pin	Input	PC11 pin: USART3 in reception mode
	USART3_TX pin	Output	PC10 pin: USART3 in transmission mode
USARTx bootloaders	SysTick timer	Enabled	Used to automatically detect the serial baud rate from the host for USARTx bootloaders.
CAN2 bootloader	CAN2	Enabled	Once initialized the CAN2 configuration is: Baudrate 125 kbps, 11-bit identifier. **Note:** CAN1 is clocked during CAN2 bootloader execution because CAN1 manages the communication between CAN2 and SRAM.
	CAN2_RX pin	Input	PB5 pin: CAN2 in reception mode
	CAN2_TX pin	Output	PB13 pin: CAN2 in transmission mode
I2C1 bootloader	I2C1	Enabled	The I2C1 configuration is: I2C speed: up to 400 KHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b1000101x (where x = 0 for write and x = 1 for read)
	I2C1_SCL pin	Input/output	PB6 pin: clock line is used in open-drain mode.
	I2C1_SDA pin	Input/output	PB9 pin: data line is used in open-drain mode.
I2C2 bootloader	I2C2	Enabled	The I2C2 configuration is: I2C speed: up to 400 KHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b1000101x (where x = 0 for write and x = 1 for read)
	I2C2_SCL pin	Input/output	PF1 pin: clock line is used in open-drain mode.
	I2C2_SDA pin	Input/output	PF0 pin: data line is used in open-drain mode.

Table 81. STM32F74xxx/75xxx configuration in system memory boot mode (continued)

Bootloader	Feature/Peripheral	State	Comment
I2C3 bootloader	I2C3	Enabled	The I2C3 configuration is: I2C speed: up to 400 KHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b1000101x (where x = 0 for write and x = 1 for read)
	I2C3_SCL pin	Input/output	PA8 pin: clock line is used in open-drain mode.
	I2C3_SDA pin	Input/output	PC9 pin: data line is used in open-drain mode.
SPI1 bootloader	SPI1	Enabled	The SPI1 configuration is: Slave mode, Full Duplex, 8-bit MSB, Speed up to 8 MHz, Polarity: CPOL Low, CPHA Low, NSS hardware.
	SPI1_MOSI pin	Input	PA7 pin: Slave data Input line, used in push-pull pull-down mode
	SPI1_MISO pin	Output	PA6 pin: Slave data output line, used in push-pull pull-down mode
	SPI1_SCK pin	Input	PA5 pin: Slave clock line, used in push-pull pull-down mode
	SPI1_NSS pin	Input	PA4 pin: slave chip select pin used in push-pull pull-up mode.
SPI2 bootloader	SPI2	Enabled	The SPI2 configuration is: Slave mode, Full Duplex, 8-bit MSB, Speed up to 8 MHz, Polarity: CPOL Low, CPHA Low, NSS hardware.
	SPI2_MOSI pin	Input	PI3 pin: Slave data Input line, used in push-pull pull-down mode
	SPI2_MISO pin	Output	PI2 pin: Slave data output line, used in push-pull pull-down mode
	SPI2_SCK pin	Input	PI1 pin: Slave clock line, used in push-pull pull-down mode
	SPI2_NSS pin	Input	PI0 pin: slave chip select pin used in push-pull pull-up mode.

Table 81. STM32F74xxx/75xxx configuration in system memory boot mode (continued)

Bootloader	Feature/Peripheral	State	Comment
SPI4 bootloader	SPI4	Enabled	The SPI4 configuration is: Slave mode, Full Duplex, 8-bit MSB, Speed up to 8 MHz, Polarity: CPOL Low, CPHA Low, NSS hardware.
	SPI4_MOSI pin	Input	PE14 pin: Slave data Input line, used in push-pull pull-down mode
	SPI4_MISO pin	Output	PE13 pin: Slave data output line, used in push-pull pull-down mode
	SP4_SCK pin	Input	PE12 pin: Slave clock line, used in push-pull pull-down mode
	SPI4_NSS pin	Input	PE11 pin: slave chip select pin used in push-pull pull-up mode.
DFU bootloader	USB	Enabled	USB OTG FS configured in forced device mode.
	USB_DM pin	Input/Output	PA11 pin: USB DM line.
	USB_DP pin		PA12 pin: USB DP line No external Pull-Up resistor is required.
CAN2 and DFU bootloaders	TIM11	Enabled	This timer is used to determine the value of the HSE. Once HSE frequency is determined, the system clock is configured to 60 MHz using PLL and HSE.

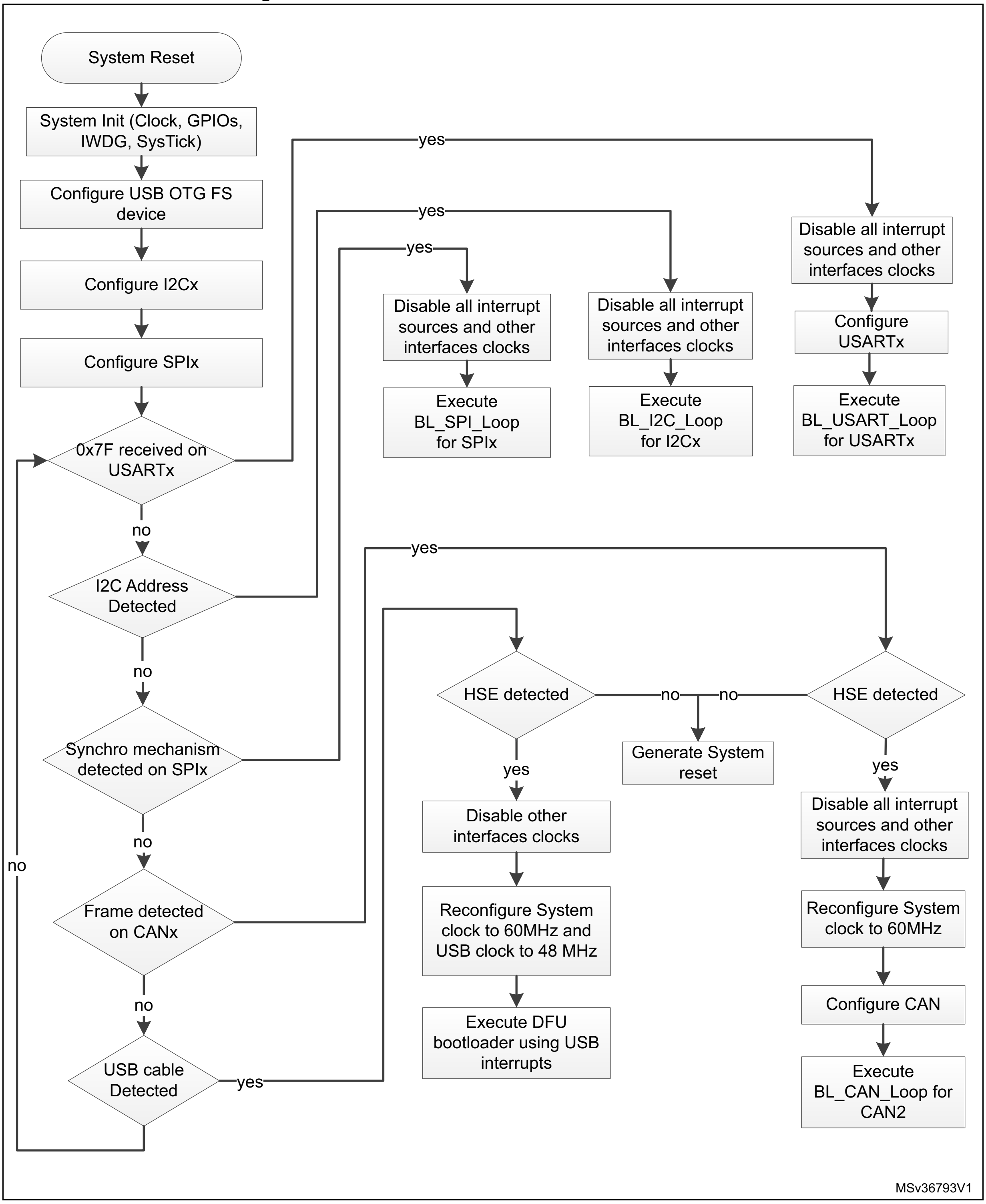
The system clock is derived from the embedded internal high-speed RC for USARTx, I2Cx and SPIx bootloaders. This internal clock is also used for CAN and DFU (USB FS Device) but only for the selection phase. An external clock multiple of 1 MHz (between 4 and 26 MHz) is required for CAN and DFU bootloader execution after the selection phase.

Note: Due to HSI deviation and since HSI is used to detect HSE value, the user must use low frequency HSE crystal values rather than high frequency values.
Low frequency values are better detected due to larger error margin. For example, it is better to use 8 MHz instead of 25 MHz.

37.2.2 Bootloader selection

The *Figure 47* shows the bootloader selection mechanism.

Figure 47.Bootloader V9.x selection for STM32F74xxx/75xxx



37.2.3 Bootloader version

The following table lists the STM32F74xxx/75xxx bootloader V9.x versions:

Table 82. STM32F74xxx/75xxx bootloader V9.x versions

Bootloader version number	Description	Known limitations
V9.0	Initial bootloader version	At high UART baudrates (115200bps) connection may fail due to software jitter leading to wrong baudrate calculation. In that case bootloader may respond with a baudrate up to ± 5% different from host baudrate. Workaround: use baudrates lower than 57600 bps if host tolerance to baudrate error is lower than ± 5%

38 STM32F76xxx/77xxx devices bootloader

38.1 Bootloader configuration

The STM32F76xxx/77xxx bootloader is activated by applying pattern9 (described in *Table 2: Bootloader activation patterns*). The following table shows the hardware resources used by this bootloader.

Table 83. STM32F76xxx/77xxx configuration in system memory boot mode

Bootloader	Feature/Peripheral	State	Comment
Common to all bootloaders	RCC	HSI enabled	The HSI is used at startup as clock source for system clock configured to 60 MHz and for USART and I2C bootloader operation.
		HSE enabled	The HSE is used only when the CAN or the DFU (USB FS Device) interfaces are selected. In this case the system clock configured to 60 MHz with HSE as clock source. The HSE frequency must be multiple of 1 MHz and ranging from 4 MHz to 26 MHz.
		-	The Clock Security System (CSS) interrupt is enabled for the CAN and DFU bootloaders. Any failure (or removal) of the external clock generates system reset.
	RAM	-	16 Kbyte starting from address 0x20000000 are used by the bootloader firmware
	System memory	-	59 Kbyte starting from address 0x1FF00000, contain the bootloader firmware
	IWDG	-	The independent watchdog (IWDG) prescaler is configured to its maximum value. It is periodically refreshed to prevent watchdog reset (in case the hardware IWDG option was previously enabled by the user).
	Power	-	The voltage range is [1.8V, 3.6V] In this range: - Flash wait states 3. - System clock Frequency 60 MHz. - ART Accelerator enabled. - Flash write operation by byte (refer to bootloader memory management section for more information).

Table 83. STM32F76xxx/77xxx configuration in system memory boot mode (continued)

Bootloader	Feature/Peripheral	State	Comment
USART1 bootloader	USART1	Enabled	Once initialized the USART1 configuration is: 8-bits, even parity and 1 Stop bit
	USART1_RX pin	Input	PA10 pin: USART1 in reception mode
	USART1_TX pin	Output	PA9 pin: USART1 in transmission mode
USART3 bootloader (on PB11/PB10)	USART3	Enabled	Once initialized the USART3 configuration is: 8-bits, even parity and 1 Stop bit
	USART3_RX pin	Input	PB11 pin: USART3 in reception mode
	USART3_TX pin	Output	PB10 pin: USART3 in transmission mode
USART3 bootloader (on PC11/PC10)	USART3	Enabled	Once initialized the USART3 configuration is: 8-bits, even parity and 1 Stop bit
	USART3_RX pin	Input	PC11 pin: USART3 in reception mode
	USART3_TX pin	Output	PC10 pin: USART3 in transmission mode
USARTx bootloaders	SysTick timer	Enabled	Used to automatically detect the serial baud rate from the host for USARTx bootloaders.
CAN2 bootloader	CAN2	Enabled	Once initialized the CAN2 configuration is: Baudrate 125 kbps, 11-bit identifier. **Note:** CAN1 is clocked during CAN2 bootloader execution because CAN1 manages the communication between CAN2 and SRAM.
	CAN2_RX pin	Input	PB5 pin: CAN2 in reception mode
	CAN2_TX pin	Output	PB13 pin: CAN2 in transmission mode
I2C1 bootloader	I2C1	Enabled	The I2C1 configuration is: I2C speed: up to 400 KHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b1001001x (where x = 0 for write and x = 1 for read)
	I2C1_SCL pin	Input/Output	PB6 pin: clock line is used in open-drain mode.
	I2C1_SDA pin	Input/Output	PB9 pin: data line is used in open-drain mode.
I2C2 bootloader	I2C2	Enabled	The I2C2 configuration is: I2C speed: up to 400 KHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b1001001x (where x = 0 for write and x = 1 for read)
	I2C2_SCL pin	Input/Output	PF1 pin: clock line is used in open-drain mode.
	I2C2_SDA pin	Input/Output	PF0 pin: data line is used in open-drain mode.

Table 83. STM32F76xxx/77xxx configuration in system memory boot mode (continued)

Bootloader	Feature/Peripheral	State	Comment
I2C3 bootloader	I2C3	Enabled	The I2C3 configuration is: I2C speed: up to 400 KHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b1001001x (where x = 0 for write and x = 1 for read)
	I2C3_SCL pin	Input/Output	PA8 pin: clock line is used in open-drain mode.
	I2C3_SDA pin	Input/Output	PC9 pin: data line is used in open-drain mode.
SPI1 bootloader	SPI1	Enabled	The SPI1 configuration is: Slave mode, Full Duplex, 8-bit MSB, Speed up to 8MHz, Polarity: CPOL Low, CPHA Low, NSS hardware.
	SPI1_MOSI pin	Input	PA7 pin: Slave data Input line, used in push-pull pull-down mode
	SPI1_MISO pin	Output	PA6 pin: Slave data output line, used in push-pull pull-down mode
	SPI1_SCK pin	Input	PA5 pin: Slave clock line, used in push-pull pull-down mode
	SPI1_NSS pin	Input	PA4 pin: slave chip select pin used in push-pull pull-up mode.
SPI2 bootloader	SPI2	Enabled	The SPI2 configuration is: Slave mode, Full Duplex, 8-bit MSB, Speed up to 8MHz, Polarity: CPOL Low, CPHA Low, NSS hardware.
	SPI2_MOSI pin	Input	PI3 pin: Slave data Input line, used in push-pull pull-down mode
	SPI2_MISO pin	Output	PI2 pin: Slave data output line, used in push-pull pull-down mode
	SPI2_SCK pin	Input	PI1 pin: Slave clock line, used in push-pull pull-down mode
	SPI2_NSS pin	Input	PI0 pin: slave chip select pin used in push-pull pull-up mode.

Table 83. STM32F76xxx/77xxx configuration in system memory boot mode (continued)

Bootloader	Feature/Peripheral	State	Comment
SPI4 bootloader	SPI4	Enabled	The SPI4 configuration is: Slave mode, Full Duplex, 8-bit MSB, Speed up to 8MHz, Polarity: CPOL Low, CPHA Low, NSS hardware.
	SPI4_MOSI pin	Input	PE14 pin: Slave data Input line, used in push-pull pull-down mode
	SPI4_MISO pin	Output	PE13 pin: Slave data output line, used in push-pull pull-down mode
	SP4_SCK pin	Input	PE12 pin: Slave clock line, used in push-pull pull-down mode
	SPI4_NSS pin	Input	PE11 pin: slave chip select pin used in push-pull pull-up mode.
DFU bootloader	USB	Enabled	USB OTG FS configured in forced device mode
	USB_DM pin	Input/Output	PA11 pin: USB DM line.
	USB_DP pin		PA12 pin: USB DP line No external Pull-Up resistor is required.
CAN2 and DFU bootloaders	TIM11	Enabled	This timer is used to determine the value of the HSE. Once HSE frequency is determined, the system clock is configured to 60 MHz using PLL and HSE.

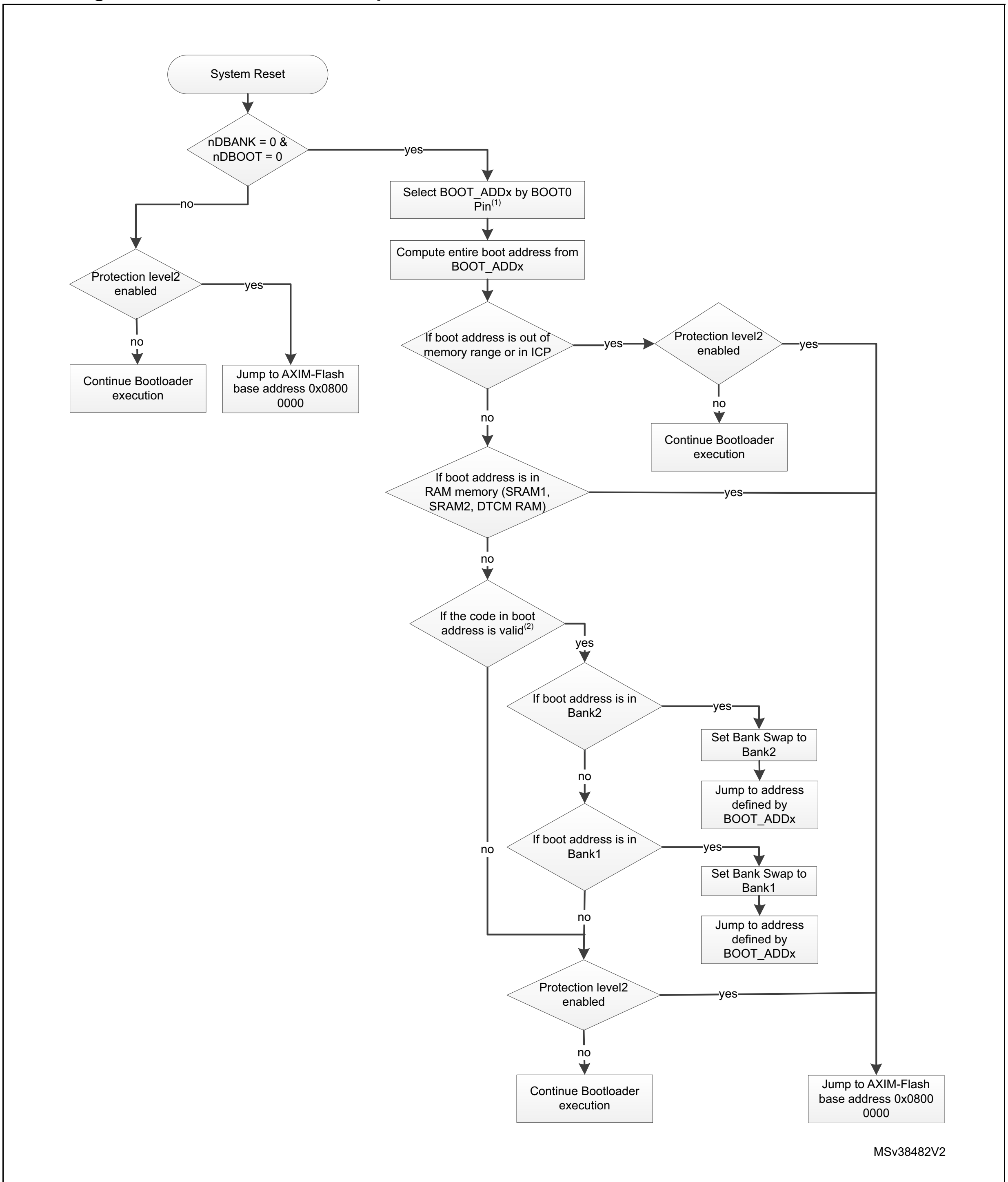
The system clock is derived from the embedded internal high-speed RC for USARTx and I2Cx bootloaders. This internal clock is also used for CAN and DFU (USB FS Device) but only for the selection phase. An external clock multiple of 1 MHz (between 4 and 26 MHz) is required for CAN and DFU bootloader execution after the selection phase.

Note: Due to HSI deviation and since HSI is used to detect HSE value, the user must use low frequency HSE crystal values rather than high frequency values.
Low frequency values are better detected due to larger error margin. For example, it is better to use 8 MHz instead of 25 MHz.

38.2 Bootloader selection

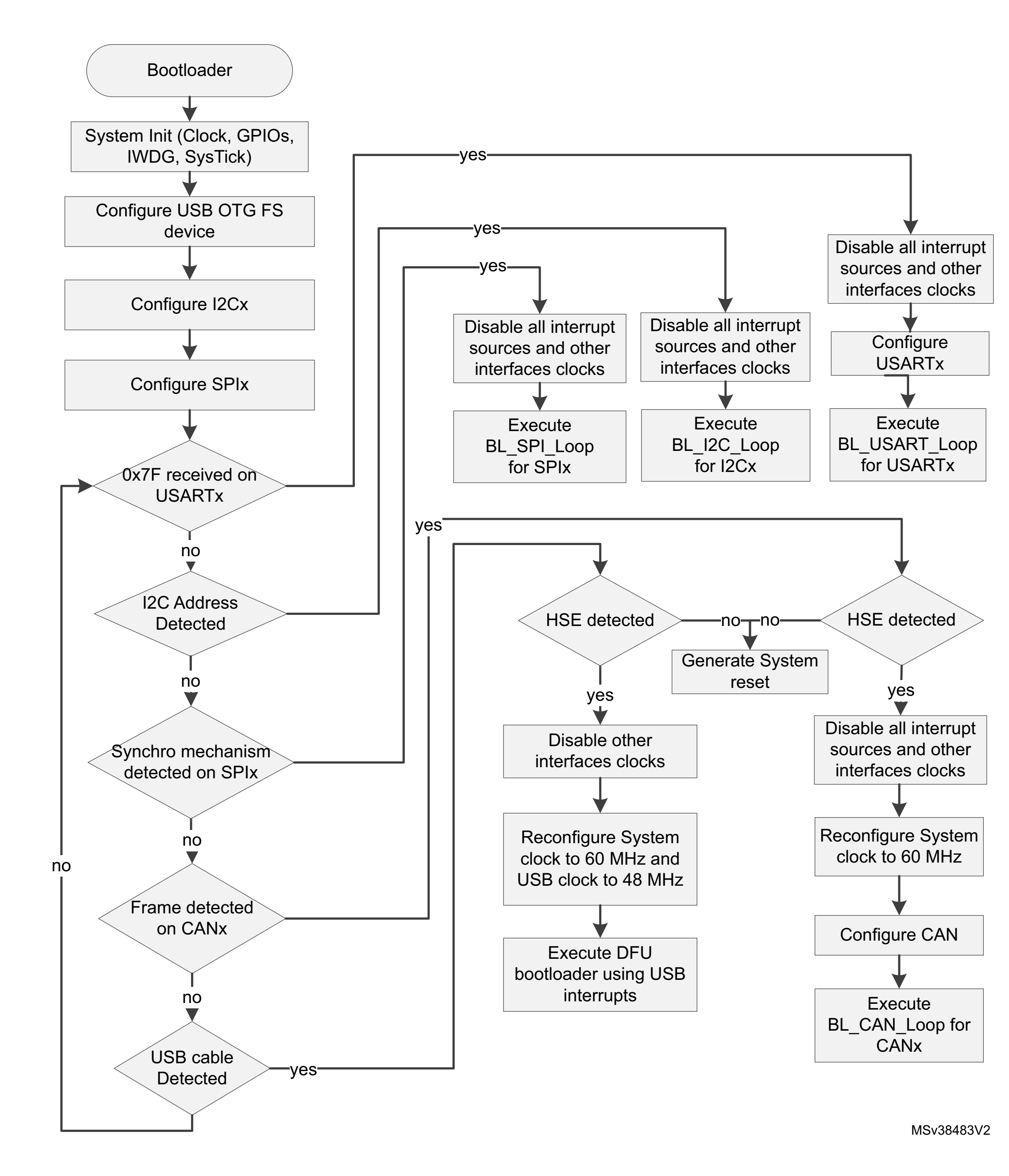
The *Figure 48* and *Figure 49* show the bootloader selection mechanism.

Figure 48. Dual Bank Boot Implementation for STM32F76xxx/77xxx Bootloader V9.x



1. Only BOOT_ADD0 value is considered whatever the BOOT0 pin state, as described in Known limitation under *Table 84*.
2. ITCM RAM is not considered valid as stack pointer address for the dual bank boot mechanism.

Figure 49. Bootloader V9.x selection for STM32F76xxx/77xxx



38.3 Bootloader version

The following table lists the STM32F76xxx/77xxx devices bootloader V9.x versions.

Table 84. STM32F76xxx/77xxx bootloader V9.x versions

Bootloader version number	Description	Known limitations
V9.3	Initial bootloader version	When the Flash memory is configured to the dual bank boot mode (nDBANK=nDBOOT=0), whatever the BOOT0 Pin state only BOOT_ADD0 value is considered (when BOOT0 Pin=1, BOOT_ADD0 value is considered not the BOOT_ADD1). Workaround: in order to manage dual bank boot with BOOT_ADD0 only, please refer to the AN4826: "STM32F7 Series Flash memory dual bank mode” At high UART baudrates (115200bps) connection may fail due to software jitter leading to wrong baudrate calculation. In that case bootloader may respond with a baudrate up to ± 5% different from host baudrate. Workaround: use baudrates lower than 57600 bps if host tolerance to baudrate error is lower than ± 5%

39 STM32G03xxx/ STM32G04xxx devices bootloader

39.1 Bootloader configuration

The STM32G03xxx/G04xxx bootloader is activated by applying pattern11 (described in *Table 2: Bootloader activation patterns*). The following table shows the hardware resources used by this bootloader.

Table 85. STM32G03xxx/G04xxx configuration in system memory boot mode

Bootloader	Feature/Peripheral	State	Comment
Common to all bootloaders	RCC	HSI enabled	The system clock frequency is 24 MHz (using PLL clocked by HSI).
	RAM	-	4 Kbytes starting from address 0x20000000 are used by the bootloader firmware
	System memory	-	8 Kbytes starting from address 0x1FFF0000
	IWDG	-	The independent watchdog (IWDG) prescaler is configured to its maximum value. It is periodically refreshed to prevent watchdog reset (in case the hardware IWDG option was previously enabled by the user).
Securable memory area	-	-	The Address to jump to for the secrable memory area: @0x1FFF1D00
USART1 bootloader	USART1	Enabled	Once initialized the USART1 configuration is: 8-bits, even parity and 1 Stop bit
	USART1_RX pin	Input	PA10 pin: USART1 in reception mode
	USART1_TX pin	Output	PA9 pin: USART1 in transmission mode
USART2 bootloader	USART2	Enabled	Once initialized the USART2 configuration is: 8-bits, even parity and 1 Stop bit
	USART2_RX pin	Input	PA3 pin: USART2 in reception mode
	USART2_TX pin	Output	PA2 pin: USART2 in transmission mode
USARTx bootloader	SysTick timer	Enabled	Used to automatically detect the serial baud rate from the host for USARTx bootloaders.
I2C1 bootloader	I2C1	Enabled	The I2C1 configuration is: I2C speed: up to 1 MHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b1010001x (where x = 0 for write and x = 1 for read)
	I2C1_SCL pin	Input/Output	PB6 pin: clock line is used in open-drain mode.
	I2C1_SDA pin	Input/Output	PB7 pin: data line is used in open-drain mode.

Table 85. STM32G03xxx/G04xxx configuration in system memory boot mode (continued)

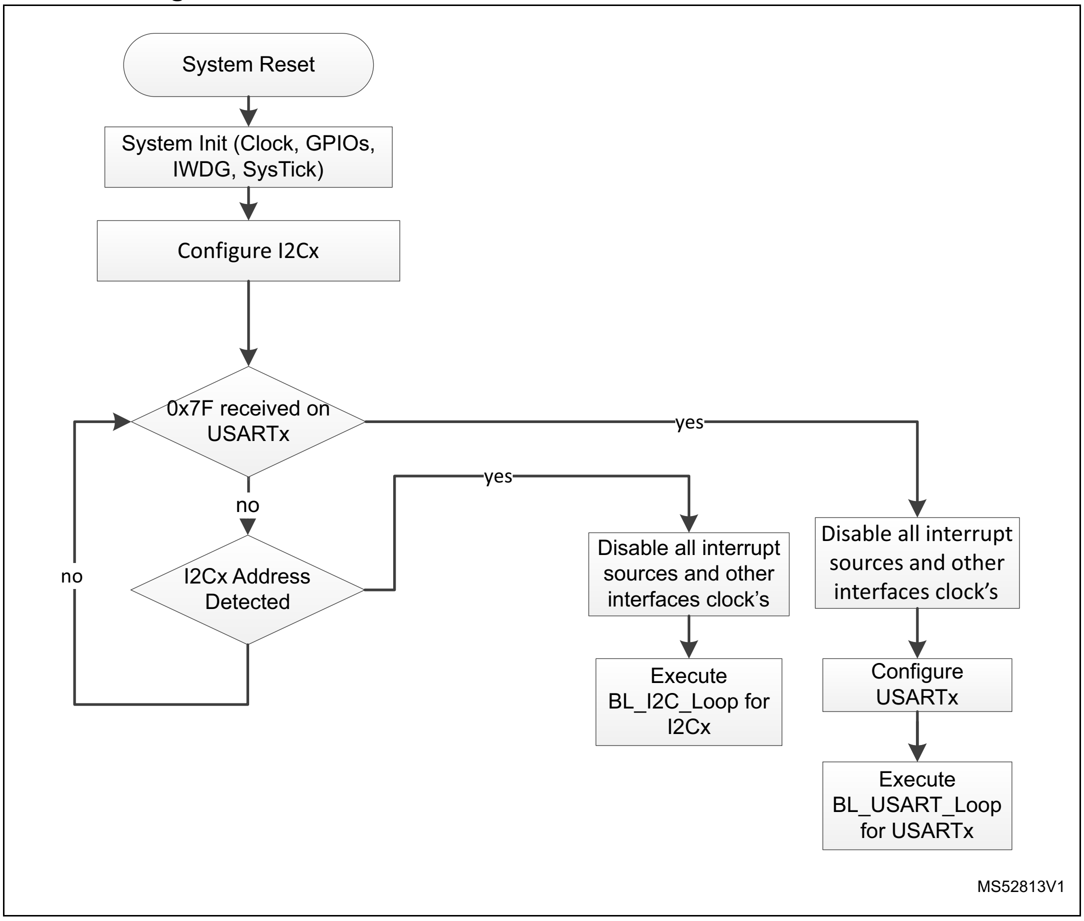
Bootloader	Feature/Peripheral	State	Comment
I2C2 bootloader	I2C2	Enabled	The I2C2 configuration is: I2C speed: up to 1 MHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b1010001x (where x = 0 for write and x = 1 for read)
	I2C2_SCL pin	Input/Output	PB10 pin: clock line is used in open-drain mode.
	I2C2_SDA pin	Input/Output	PB11 pin: data line is used in open-drain mode.

Note: On SO8 packages, USART1 PA9/PA10 IOs are remapped on PA11/PA12

39.2 Bootloader selection

Figure 50 shows the bootloader selection mechanism.

Figure 50. Bootloader V5.x selection for STM32G03xxx/G04xxx



39.3 Bootloader version

Table 86 lists the STM32G03xxx/G4xxx devices bootloader versions.

Table 86. STM32G03xx/04xxx bootloader versions

Bootloader version number	Description	Known limitations
V5.1	Initial bootloader version	– Supporting only 48 and 32 pins packages – Issue is seen in both packages, if PA3 stay to low level, system will stay stuck in the USART2 detection sequence and no other interface will be detected.
V5.2	Add support to small packages 8/20 and 28 pins	Issue is seen in all packages (except SO8, no PA3 pin) if PA3 stay to low level, system will stay stuck in the USART2 detection sequence and no other interface will be detected.
V5.3	Fix V5.2 limitations	None

40 STM32G07xxx/08xxx device bootloader

40.1 Bootloader configuration

The STM32G07xxx/G08xxx bootloader is activated by applying pattern11 (described in *Table 2: Bootloader activation patterns*). The following table shows the hardware resources used by this bootloader.

Table 87. STM32G07xxx/8xxx configuration in system memory boot mode

Bootloader	Feature/Peripheral	State	Comment
Common to all bootloaders	RCC	HSI enabled	The system clock frequency is 24 MHz (using PLL clocked by HSI).
	RAM	-	12 Kbytes starting from address 0x20000000 are used by the bootloader firmware
	System memory	-	28 Kbytes starting from address 0x1FFF0000, contain the bootloader firmware
	IWDG	-	The independent watchdog (IWDG) prescaler is configured to its maximum value. It is periodically refreshed to prevent watchdog reset (in case the hardware IWDG option was previously enabled by the user).
Securable memory area	-	-	The Address to jump to for the secrable memory area: @0x1FFF6800
USART1 bootloader	USART1	Enabled	Once initialized the USART1 configuration is: 8-bits, even parity and 1 Stop bit
	USART1_RX pin	Input	PA10 pin: USART1 in reception mode
	USART1_TX pin	Output	PA9 pin: USART1 in transmission mode
USART2 bootloader	USART2	Enabled	Once initialized the USART2 configuration is: 8-bits, even parity and 1 Stop bit
	USART2_RX pin	Input	PA3 pin: USART2 in reception mode
	USART2_TX pin	Output	PA2 pin: USART2 in transmission mode
USART3 bootloader	USART3	Enabled	Once initialized the USART3 configuration is: 8-bits, even parity and 1 Stop bit
	USART3_RX pin	Input	PC11 pin: USART3 in reception mode
	USART3_TX pin	Output	PC10 pin: USART3 in transmission mode
I2C1 bootloader	I2C1	Enabled	The I2C1 configuration is: I2C speed: up to 1 MHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b1010001x (where x = 0 for write and x = 1 for read)
	I2C1_SCL pin	Input/Output	PB6 pin: clock line is used in open-drain mode.
	I2C1_SDA pin	Input/Output	PB7 pin: data line is used in open-drain mode.

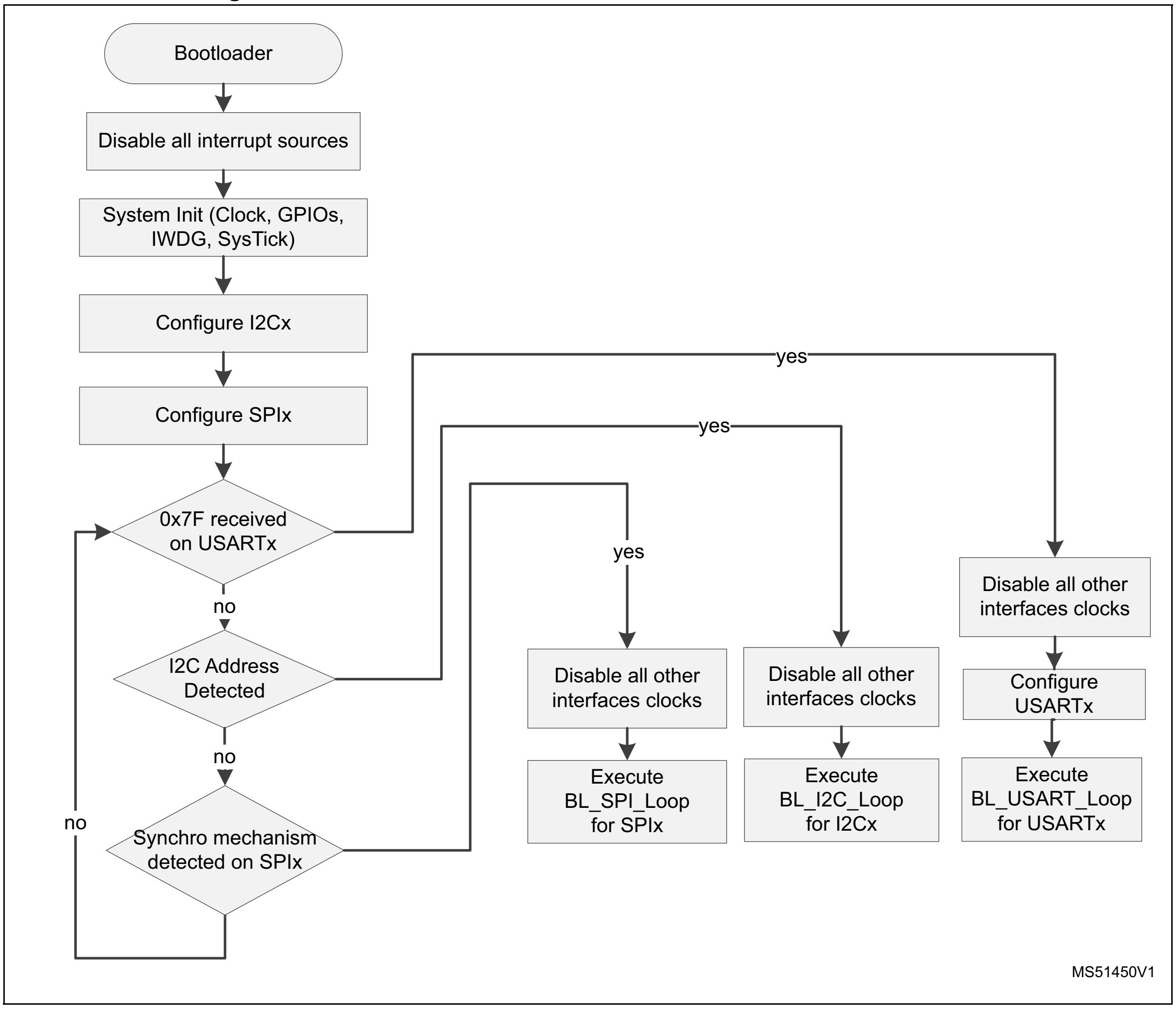
Table 87. STM32G07xxx/8xxx configuration in system memory boot mode (continued)

Bootloader	Feature/Peripheral	State	Comment
I2C2 bootloader	I2C2	Enabled	The I2C2 configuration is: I2C speed: up to 1 MHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b1010001x (where x = 0 for write and x = 1 for read)
	I2C2_SCL pin	Input/Output	PB10 pin: clock line is used in open-drain mode.
	I2C2_SDA pin	Input/Output	PB11 pin: data line is used in open-drain mode.
SPI1 bootloader	SPI1	Enabled	The SPI1 configuration is: – Slave mode – Full Duplex – 8-bit MSB – Speed up to 8 MHz – Polarity: CPOL Low, CPHA Low, NSS hardware.
	SPI1_MOSI pin	Input	PA7 pin: Slave data Input line, used in push-pull, pull-down mode.
	SPI1_MISO pin	Output	PA6 pin: Slave data output line, used in push-pull, pull-down mode.
	SPI1_SCK pin	Input	PA5 pin: Slave clock line, used in push-pull, pull-down mode.
	SPI1_NSS pin	Input	PA4 pin: slave chip select pin used in push-pull, pull-up mode. **Note**: This IO can be tied to Gnd if the SPI Master does not use it.
SPI2 bootloader	SPI2	Enabled	The SPI2 configuration is: – Slave mode – Full Duplex – 8-bit MSB – Speed up to 8 MHz – Polarity: CPOL Low, CPHA Low, NSS hardware.
	SPI2_MOSI pin	Input	PB15 pin: Slave data Input line, used in push-pull, pull-down mode.
	SPI2_MISO pin	Output	PB14 pin: Slave data output line, used in push-pull, pull-down mode.
	SPI2_SCK pin	Input	PB13 pin: Slave clock line, used in push-pull, pull-down mode.
	SPI2_NSS pin	Input	PB12 pin: slave chip select pin used in push-pull, pull-up. **Note**: This IO can be tied to GND if the SPI master does not use it.

40.2 Bootloader selection

Figure 51 shows the bootloader selection mechanism.

Figure 51. Bootloader V11.0 selection for STM32G07xxx/G08xxx



40.3 Bootloader version

Table 88 lists the STM32G07xxx/8xxx devices bootloader versions.

Table 88. STM32G07xx/08xxx bootloader versions

Bootloader version number	Description	Known limitations
V11.0	Initial bootloader version	Not supporting packages smaller then LQFP64
V11.1	Supporting all packages	None
V11.2	Add securable memory area feature	None

41 STM32G431xx/441xx devices bootloader

41.1 Bootloader configuration

The STM32G431xx/441xx bootloader is activated by applying pattern15 (described in *Table 2: Bootloader activation patterns*). The following table shows the hardware resources used by this bootloader.

Table 89. STM32G431xx/441xx configuration in system memory boot mode

Bootloader	Feature/Peripheral	State	Comment
Common to all bootloaders	RCC	HSI enabled	The system clock frequency is 72 MHz (using the PLL clocked by HSI)
		-	The clock recovery system (CRS) is enabled for the DFU bootloader to allow USB to be clocked by HSI48 48 MHz
	RAM	-	16 Kbyte starting from address 0x20000000 are used by the bootloader firmware
	System memory	-	28 Kbyte starting from address 0x1FFF0000, contain the bootloader firmware
	IWDG	-	The independent watchdog (IWDG) prescaler is configured to its maximum value. It is periodically refreshed to prevent watchdog reset (in case the hardware IWDG option was previously enabled by the user).
Securable memory area	-	-	The address to jump to the exit securable memory area @0x1FFF6800
USART1 bootloader	USART1	Enabled	Once initialized the USART1 configuration is: 8-bits, even parity and 1 Stop bit
	USART1_RX pin	Input	PA10 pin: USART1 in reception mode
	USART1_TX pin	Output	PA9 pin: USART1 in transmission mode
USART2 bootloader	USART2	Enabled	Once initialized the USART2 configuration is: 8-bits, even parity and 1 Stop bit
	USART2_RX pin	Input	PA3 pin: USART2 in reception mode
	USART2_TX pin	Output	PA2 pin: USART2 in transmission mode
USART3 bootloader	USART3	Enabled	Once initialized the USART3 configuration is: 8-bits, even parity and 1 Stop bit
	USART3_RX pin	Input	PC11 pin: USART3 in reception mode
	USART3_TX pin	Output	PC10 pin: USART3 in transmission mode

Table 89. STM32G431xx/441xx configuration in system memory boot mode (continued)

Bootloader	Feature/Peripheral	State	Comment
I2C2 bootloader	I2C2	Enabled	The I2C2 configuration is: I2C speed: up to 1 MHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b1010100x (where x = 0 for write and x = 1 for read)
	I2C2_SCL pin	Input/Output	PC4 pin: clock line is used in open-drain mode.
	I2C2_SDA pin	Input/Output	PA8 pin: data line is used in open-drain mode.
I2C3 bootloader	I2C3	Enabled	The I2C3 configuration is: I2C speed: up to 1 MHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b1010100x (where x = 0 for write and x = 1 for read)
	I2C3_SCL pin	Input/Output	PC8 pin: clock line is used in open-drain mode.
	I2C3_SDA pin	Input/Output	PC9 pin: data line is used in open-drain mode.
SPI1 bootloader	SPI1	Enabled	The SPI1 configuration is: – Slave mode – Full Duplex – 8-bit MSB – Speed up to 8 MHz – Polarity: CPOL Low, CPHA Low, NSS hardware.
	SPI1_MOSI pin	Input	PA7 pin: Slave data Input line, used in push-pull, no pull-up no pull-down mode.
	SPI1_MISO pin	Output	PA6 pin: Slave data output line, used in push-pull, no pull-up no pull-down mode.
	SPI1_SCK pin	Input	PA5 pin: Slave clock line, used in push-pull no pull-up, no pull-up no pull-down mode.
	SPI1_NSS pin	Input	PA4 pin: slave chip select pin used in push-pull, no pull-up no pull-down mode.

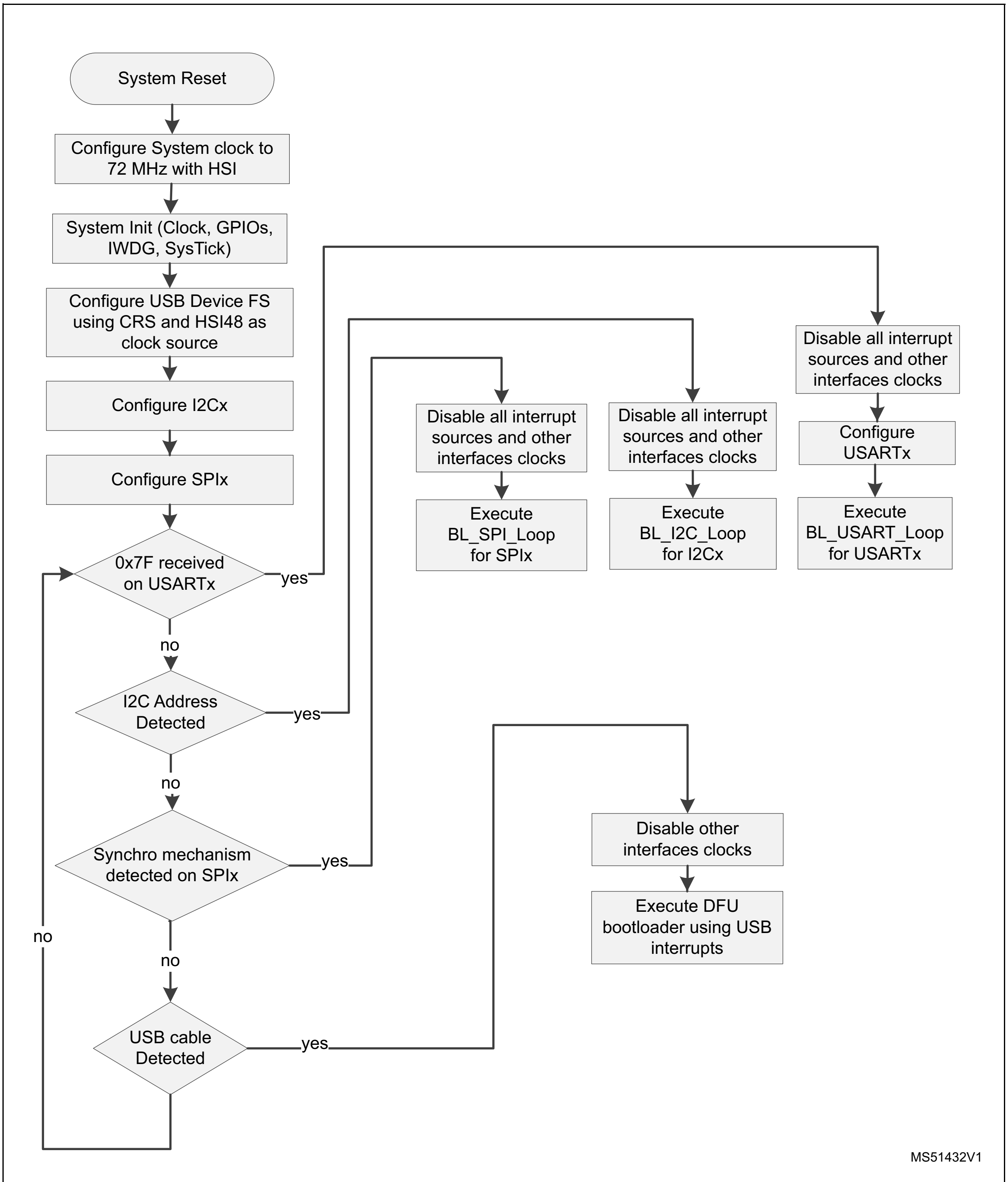
Table 89. STM32G431xx/441xx configuration in system memory boot mode (continued)

Bootloader	Feature/Peripheral	State	Comment
SPI2 bootloader	SPI2	Enabled	The SPI2 configuration is: – Slave mode – Full Duplex – 8-bit MSB – Speed up to 8 MHz – Polarity: CPOL Low, CPHA Low, NSS hardware.
	SPI2_MOSI pin	Input	PB15 pin: Slave data Input line, used in push-pull, no pull-up no pull-down mode.
	SPI2_MISO pin	Output	PB14 pin: Slave data output line, used in push-pull, no pull-up no pull-down mode.
	SPI2_SCK pin	Input	PB13 pin: Slave clock line, used in push-pull, no pull-up no pull-down mode.
	SPI2_NSS pin	Input	PB12 pin: slave chip select pin used in push-pull, no pull-up no pull-down mode. Note: This IO can be tied to GND if the SPI Master does not use it.
DFU bootloader	USB	Enabled	USB FS configured in forced device mode. USB FS interrupt vector is enabled and used for USB DFU communications.
	USB_DM pin	Input/Output	PA11: USB DM line.
	USB_DP pin		PA12: USB DP line No external Pull-up resistor is required

41.2 Bootloader selection

The figure below shows the bootloader selection mechanism.

Figure 52. Bootloader selection for STM32G431xx/441xx



41.3 Bootloader version

Table 90. STM32G431xx/441xx bootloader version

Bootloader version number	Description	Known limitations
V13.3	Initial bootloader version	None

42 STM32G47xxx/48xxx devices bootloader

42.1 Bootloader Configuration

The STM32G47xxx/48xxx bootloader is activated by applying pattern14 (described in *Table 2: Bootloader activation patterns*). The following table shows the hardware resources used by this bootloader

Table 91. STM32G47xxx/48xxx configuration in system memory boot mode

Bootloader	Feature/Peripheral	State	Comment
Common to all bootloaders	RCC	HSI enabled	The system clock frequency is 72 MHz (using the PLL clocked by HSI)
		-	The clock recovery system (CRS) is enabled for the DFU bootloader to allow USB to be clocked by HSI48 48 MHz
	RAM	-	16 Kbyte starting from address 0x20000000 are used by the bootloader firmware
	System memory	-	28 Kbyte starting from address 0x1FFF0000, contain the bootloader firmware
	IWDG	-	The independent watchdog (IWDG) prescaler is configured to its maximum value. It is periodically refreshed to prevent watchdog reset (in case the hardware IWDG option was previously enabled by the user).
Securable memory area	-	-	The address to jump to the exit securable memory area @0x1FFF6800
USART1 bootloader	USART1	Enabled	Once initialized the USART1 configuration is: 8-bits, even parity and 1 Stop bit
	USART1_RX pin	Input	PA10 pin: USART1 in reception mode
	USART1_TX pin	Output	PA9 pin: USART1 in transmission mode
USART2 bootloader	USART2	Enabled	Once initialized the USART2 configuration is: 8-bits, even parity and 1 Stop bit
	USART2_RX pin	Input	PA3 pin: USART2 in reception mode
	USART2_TX pin	Output	PA2 pin: USART2 in transmission mode
USART3 bootloader	USART3	Enabled	Once initialized the USART3 configuration is: 8-bits, even parity and 1 Stop bit
	USART3_RX pin	Input	PC11 pin: USART3 in reception mode
	USART3_TX pin	Output	PC10 pin: USART3 in transmission mode

Table 91. STM32G47xxx/48xxx configuration in system memory boot mode (continued)

Bootloader	Feature/Peripheral	State	Comment
I2C2 bootloader	I2C2	Enabled	The I2C2 configuration is: I2C speed: up to 1 MHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b1010100x (where x = 0 for write and x = 1 for read)
	I2C2_SCL pin	Input/Output	PC4 pin: clock line is used in open-drain mode.
	I2C2_SDA pin	Input/Output	PA8 pin: data line is used in open-drain mode.
I2C3 bootloader	I2C3	Enabled	The I2C3 configuration is: I2C speed: up to 1 MHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b1010100x (where x = 0 for write and x = 1 for read)
	I2C3_SCL pin	Input/Output	PC8 pin: clock line is used in open-drain mode.
	I2C3_SDA pin	Input/Output	PC9 pin: data line is used in open-drain mode.
I2C4 bootloader	I2C4	Enabled	The I2C4 configuration is: I2C speed: up to 1 MHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b1010100x (where x = 0 for write and x = 1 for read)
	I2C4_SCL pin	Input/Output	PC6 pin: clock line is used in open-drain mode.
	I2C4_SDA pin	Input/Output	PC7 pin: data line is used in open-drain mode.
SPI1 bootloader	SPI1	Enabled	The SPI1 configuration is: – Slave mode – Full Duplex – 8-bit MSB – Speed up to 8 MHz – Polarity: CPOL Low, CPHA Low, NSS hardware.
	SPI1_MOSI pin	Input	PA7 pin: Slave data Input line, used in push-pull, no pull-up no pull-down mode.
	SPI1_MISO pin	Output	PA6 pin: Slave data output line, used in push-pull, no pull-up no pull-down mode.
	SPI1_SCK pin	Input	PA5 pin: Slave clock line, used in push-pull no pull-up, no pull-up no pull-down mode.
	SPI1_NSS pin	Input	PA4 pin: slave chip select pin used in push-pull, no pull-up no pull-down mode.

Table 91. STM32G47xxx/48xxx configuration in system memory boot mode (continued)

<table>
<tr><th>Bootloader</th><th>Feature/Peripheral</th><th>State</th><th>Comment</th></tr>
<tr><td rowspan="5">SPI2 bootloader</td><td>SPI2</td><td>Enabled</td><td>The SPI2 configuration is:
– Slave mode
– Full Duplex
– 8-bit MSB
– Speed up to 8 MHz
– Polarity: CPOL Low, CPHA Low, NSS hardware.</td></tr>
<tr><td>SPI2_MOSI pin</td><td>Input</td><td>PB15 pin: Slave data Input line, used in push-pull, no pull-up no pull-down mode.</td></tr>
<tr><td>SPI2_MISO pin</td><td>Output</td><td>PB14 pin: Slave data output line, used in push-pull, no pull-up no pull-down mode.</td></tr>
<tr><td>SPI2_SCK pin</td><td>Input</td><td>PB13 pin: Slave clock line, used in push-pull, no pull-up no pull-down mode.</td></tr>
<tr><td>SPI2_NSS pin</td><td>Input</td><td>PB12 pin: slave chip select pin used in push-pull, no pull-up no pull-down mode.
Note: This IO can be tied to GND if the SPI Master does not use it.</td></tr>
<tr><td rowspan="3">DFU bootloader</td><td>USB</td><td>Enabled</td><td>USB FS configured in forced device mode.
USB FS interrupt vector is enabled and used for USB DFU communications.
Note: VDDUSB IO must be connected to 3.3 V for USB to be operational.</td></tr>
<tr><td>USB_DM pin</td><td rowspan="2">Input/Output</td><td>PA11: USB DM line.</td></tr>
<tr><td>USB_DP pin</td><td>PA12: USB DP line
No external Pull-up resistor is required</td></tr>
</table>

42.2 Bootloader selection

The figures below show the bootloader selection mechanism.

Figure 53. Bootloader selection for STM32G47xxx/48xxx

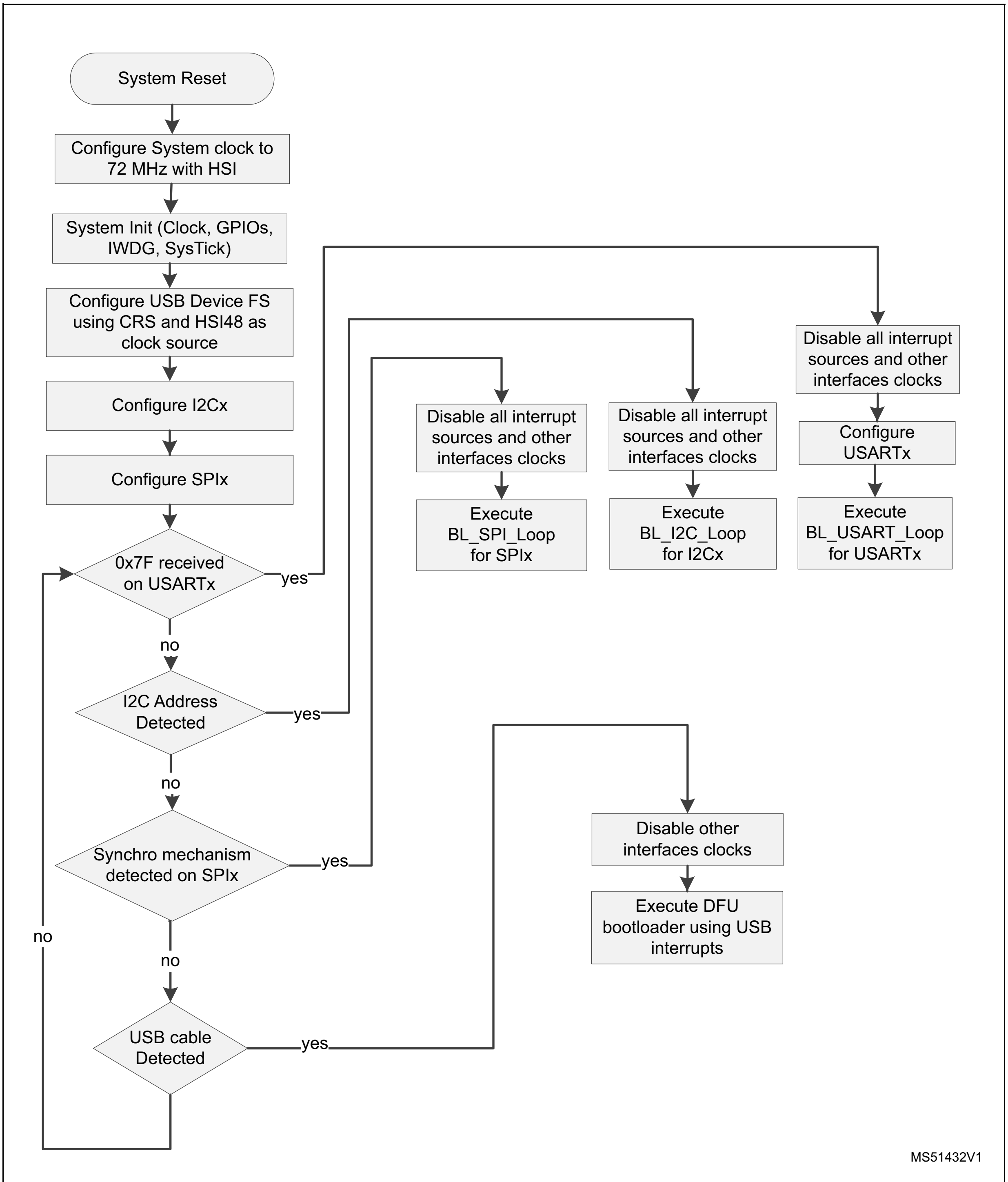
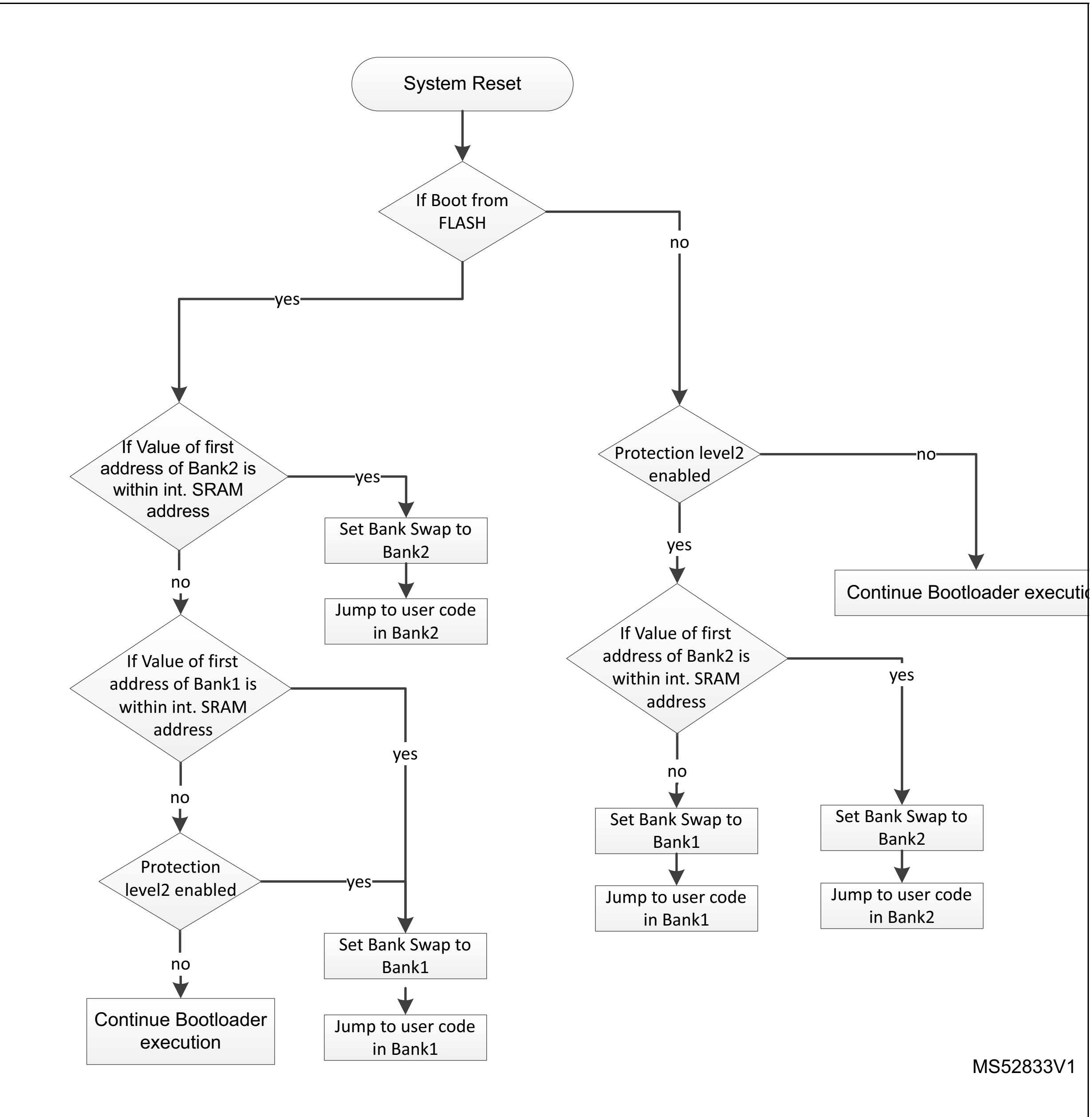


Figure 54. Dual bank boot implementation for STM32G47xxx/48xxx bootloader V13.x



42.3 Bootloader version

Table 92. STM32G47xxx/48xxx bootloader version

Bootloader version number	Description	Known limitations
V13.3 (0xD3)	Initial bootloader version	Boot from bank2 is not working
V13.4 (0xD4)	Fix V13.3 limitations	None

43 STM32H74xxx/75xxx devices bootloader

43.1 Bootloader configuration

The STM32H74xxx/75xxx bootloader is activated by applying pattern10 (described in *Table 2: Bootloader activation patterns*). The following table shows the hardware resources used by this bootloader.

Table 93. STM32H74xxx/75xxx configuration in system memory boot mode

Bootloader	Feature/Peripheral	State	Comment
Common to all bootloaders	RCC	HSI enabled	The system clock frequency is 64 MHz using the HSI. The HSI clock source is used at startup (interface detection phase) and when USART or SPI or I2C interface is selected.
		-	The clock recovery system (CRS) is enabled for the DFU bootloader to allow USB to be clocked by HSI48 48 MHz
		-	Clock used for the FDCAN is fixed to 20 MHz and is derived from PLLQ
	RAM	-	16 Kbyte starting from address 0x20000000, and 208 Kbyte starting from address 0x24000000 are used by the bootloader firmware
	System memory	-	122 Kbyte starting from address 0x1FFF0000, contain the bootloader firmware
	IWDG	-	The independent watchdog (IWDG) prescaler is configured to its maximum value. It is periodically refreshed to prevent watchdog reset (in case the hardware IWDG option was previously enabled by the user).
	Power	-	Voltage range is set to Voltage Range 3.
USART1 bootloader (on PA9/PA10)	USART1	Enabled	Once initialized the USART1 configuration is: 8-bits, even parity and 1 Stop bit
	USART1_RX pin	Input	PA10 pin: USART1 in reception mode
	USART1_TX pin	Output	PA9 pin: USART1 in transmission mode
USART1 bootloader (on PB14/PB15)	USART1	Enabled	Once initialized the USART1 configuration is: 8-bits, even parity and 1 Stop bit
	USART1_RX pin	Input	PB15 pin: USART1 in reception mode
	USART1_TX pin	Output	PB14 pin: USART1 in transmission mode
USART2 bootloader	USART2	Enabled	Once initialized the USART2 configuration is: 8-bits, even parity and 1 Stop bit
	USART2_RX pin	Input	PA3 pin: USART2 in reception mode
	USART2_TX pin	Output	PA2 pin: USART2 in transmission mode

Table 93. STM32H74xxx/75xxx configuration in system memory boot mode (continued)

Bootloader	Feature/Peripheral	State	Comment
USART3 bootloader	USART3	Enabled	Once initialized the USART3 configuration is: 8-bits, even parity and 1 Stop bit
	USART3_RX pin	Input	PB11 pin: USART3 in reception mode
	USART3_TX pin	Output	PB10 pin: USART3 in transmission mode
I2C1 bootloader	I2C1	Enabled	The I2C1 configuration is: I2C speed: up to 400 KHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b1001110x (where x = 0 for write and x = 1 for read)
	I2C1_SCL pin	Input/Output	PB6 pin: clock line is used in open-drain mode.
	I2C1_SDA pin	Input/Output	PB9 pin: data line is used in open-drain mode.
I2C2 bootloader	I2C2	Enabled	The I2C2 configuration is: I2C speed: up to 400 KHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b1001110x (where x = 0 for write and x = 1 for read)
	I2C2_SCL pin	Input/Output	PF1 pin: clock line is used in open-drain mode.
	I2C2_SDA pin	Input/Output	PF0 pin: data line is used in open-drain mode.
I2C3 bootloader	I2C3	Enabled	The I2C3 configuration is: I2C speed: up to 400 KHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b1001110x (where x = 0 for write and x = 1 for read)
	I2C3_SCL pin	Input/Output	PA8 pin: clock line is used in open-drain mode.
	I2C3_SDA pin	Input/Output	PC9 pin: data line is used in open-drain mode.
SPI1 bootloader	SPI1	Enabled	The SPI1 configuration is: – Slave mode – Full Duplex – 8-bit MSB – Speed up to 8 MHz – Polarity: CPOL Low, CPHA Low, NSS hardware.
	SPI1_MOSI pin	Input	PA7 pin: Slave data Input line, used in push-pull, no pull-up no pull-down mode.
	SPI1_MISO pin	Output	PA6 pin: Slave data output line, used in push-pull, no pull-up no pull-down mode.
	SPI1_SCK pin	Input	PA5 pin: Slave clock line, used in push-pull no pull-up, no pull-up no pull-down mode.
	SPI1_NSS pin	Input	PA4 pin: slave chip select pin used in push-pull, no pull-up no pull-down mode.

Table 93. STM32H74xxx/75xxx configuration in system memory boot mode (continued)

Bootloader	Feature/Peripheral	State	Comment
SPI2 bootloader	SPI2	Enabled	The SPI2 configuration is: – Slave mode – Full Duplex – 8-bit MSB – Speed up to 8 MHz – Polarity: CPOL Low, CPHA Low, NSS hardware.
	SPI2_MOSI pin	Input	PI3 pin: Slave data Input line, used in push-pull, no pull-up no pull-down mode.
	SPI2_MISO pin	Output	PI2 pin: Slave data output line, used in push-pull, no pull-up no pull-down mode.
	SPI2_SCK pin	Input	PI1 pin: Slave clock line, used in push-pull, no pull-up no pull-down mode.
	SPI2_NSS pin	Input	PI0 pin: slave chip select pin used in push-pull, no pull-up no pull-down mode.
SPI3 bootloader	SPI3	Enabled	The SPI3 configuration is: – Slave mode – Full Duplex – 8-bit MSB – Speed up to 8 MHz – Polarity: CPOL Low, CPHA Low, NSS hardware.
	SPI3_MOSI pin	Input	PC12 pin: Slave data Input line, used in push-pull, no pull-up no-pull down mode
	SPI3_MISO pin	Output	PC11 pin: Slave data output line, used in push-pull, no pull-up no-pull down mode.
	SPI3_SCK pin	Input	PC10 pin: Slave clock line, used in push-pull, no pull-up no-pull down mode.
	SPI3_NSS pin	Input	PA15 pin: slave chip select pin used in push-pull, no pull-up no pull-down mode.
SPI4 bootloader	SPI4	Enabled	The SPI4 configuration is: – Slave mode – Full Duplex – 8-bit MSB – Speed up to 8 MHz – Polarity: CPOL Low, CPHA Low, NSS hardware.
	SPI4_MOSI pin	Input	PE14 pin: Slave data Input line, used in push-pull, no pull-up no pull-down mode.
	SPI4_MISO pin	Output	PE13 pin: Slave data output line, used in push-pull, no pull-up no pull-down mode.
	SPI4_SCK pin	Input	PE12 pin: Slave clock line, used in push-pull, no pull-up no pull-down mode.
	SPI4_NSS pin	Input	PE11 pin: slave chip select pin used in push-pull, no pull-up no pull-down mode.

Table 93. STM32H74xxx/75xxx configuration in system memory boot mode (continued)

Bootloader	Feature/Peripheral	State	Comment
DFU bootloader	USB	Enabled	USB FS configured in forced device mode. USB FS interrupt vector is enabled and used for USB DFU communications.
	USB_DM pin	Input/Output	PA11: USB DM line.
	USB_DP pin		PA12: USB DP line No external Pull-up resistor is required
FDCAN bootloader	FDCAN1	Enabled	Once initialized the FDCAN1 configuration is: bit-rate 0.5 Mbps FrameFormat = FDCAN_FRAME_FD_BRS Mode = FDCAN_MODE_NORMAL AutoRetransmission = ENABLE TransmitPause = DISABLE ProtocolException = ENABLE
	FDCAN1_Rx pin	Input	PH14 pin: FDCAN1 in reception mode
	FDCAN1_Tx pin	Output	PH13 pin: FDCAN1 in transmission mode

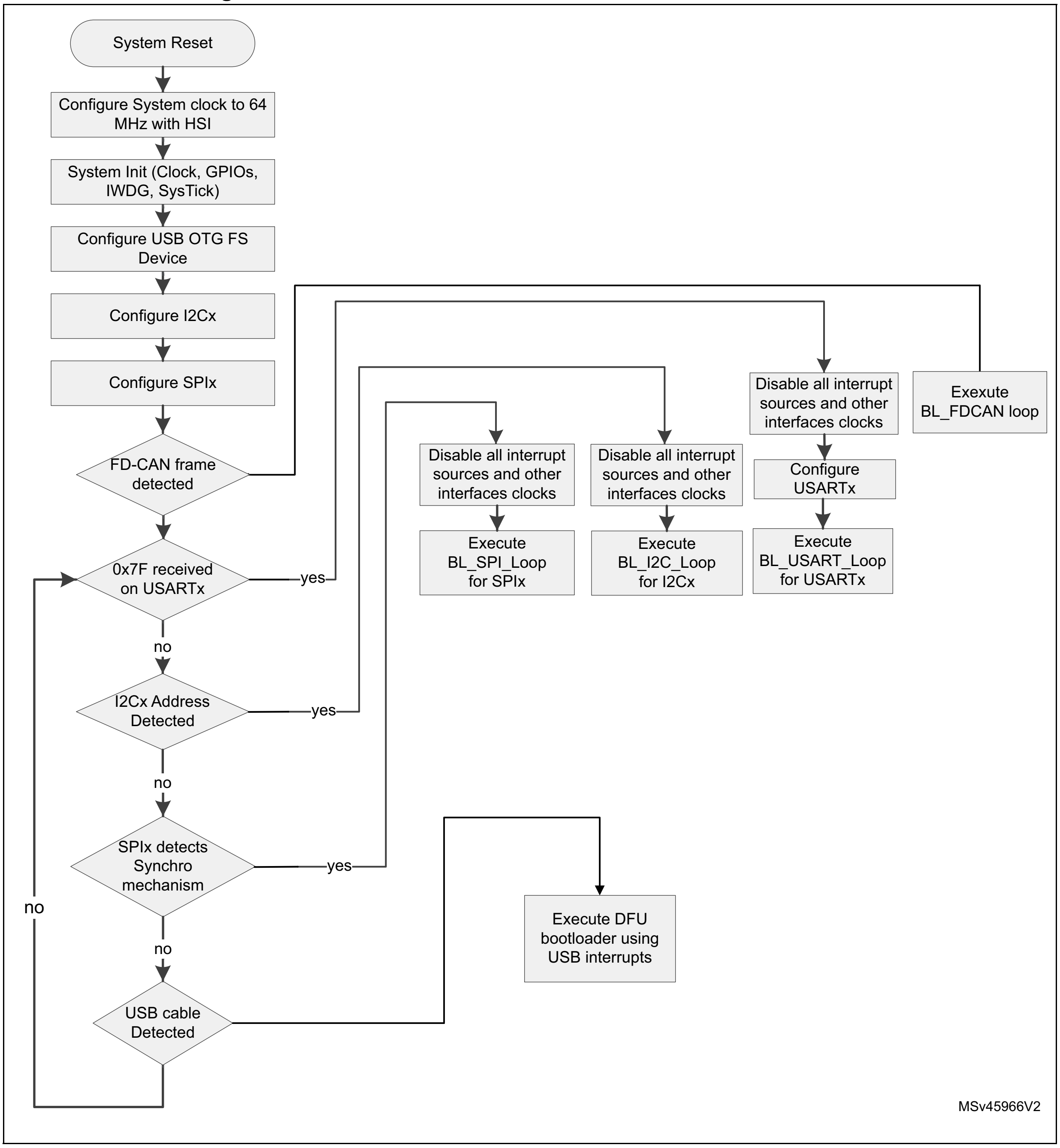
Note: To be able to connect to the bootloader USART1 using PB14/PB15 pins, you need to send two synchronization bytes.

DFU mode doesn't support USBREGEN mode. If STM32 is powered by 1.8 V source, it is not possible to use the BL DFU unless 3.3 V is provided

43.2 Bootloader selection

The *Figure 55* shows the bootloader selection mechanism.

Figure 55. Bootloader V9.x selection for STM32H74xxx/75xxx



43.3 Bootloader version

Table 94 lists the STM32H74xxx/75xxx devices bootloader versions.

Table 94. STM32H74xxx/75xxx bootloader version

Bootloader version number	Description	Known limitations
V13.2 (0xD2)	Initial bootloader version	– "Go" Command is not working – USART2 connection is not working – SPI1 connection is not working – Mass erase is not working well on I2C (Only Bank2 is erased in this command)
V13.3 (0xD3)	– Switch USB clock input from HSE to HSI48 with CRS – Fix known limitations on the V13.2	– Bank erase is not working on USART/SPI and I2C – DFU bootloader mass-erase not working
V9.0 (0x90)	– Add support of FDCAN interface – Fix V13.3 limitations – V9.0 is the latest version in production and replaces V13.2 and V13.3	– First ACK not received on "Go" Command when using USART or SPI – Limitation on the FDCAN write memory, write of data with length > 63 bytes is failing – If PB15 is set to GND, we'll not be able to connect to BL interfaces. Only the USB is able to connect as it's using interrupt for detection. PB15 must not be pulled down if USART1 on PB14/PB15 is not used – Jump issue on some application. Application stack pointer must inferior to (RAM end @ - 16 bytes) to guarantee it is working

44 STM32H7A3xx/B3xx devices bootloader

44.1 Bootloader configuration

The STM32H7A3xx/7B3xx bootloader is activated by applying pattern10 (described in *Table 2: Bootloader activation patterns*). The following table shows the hardware resources used by this bootloader.

Table 95. STM32H7A3xx/7B3xx configuration in system memory boot mode

Bootloader	Feature/Peripheral	State	Comment
Common to all bootloaders	RCC	HSI enabled	The system clock frequency is 64 MHz using the HSI.
		-	The clock recovery system (CRS) is enabled for the DFU bootloader to allow USB to be clocked by HSI48 48 MHz
		-	Clock used for the FDCAN is fixed to 20 MHz and is derived from PLLQ
	RAM	-	16 Kbyte starting from address 0x24000000 are used by the bootloader firmware
	System memory	-	40 Kbytes starting from address 0x1FFFA000, contain the bootloader firmware
	IWDG	-	The independent watchdog (IWDG) prescaler is configured to its maximum value. It is periodically refreshed to prevent watchdog reset (in case the hardware IWDG option was previously enabled by the user).
USART1 bootloader	USART1	Enabled	Once initialized the USART1 configuration is: 8-bits, even parity and 1 Stop bit
	USART1_RX pin	Input	PA10 pin: USART1 in reception mode
	USART1_TX pin	Output	PA9 pin: USART1 in transmission mode
USART2 bootloader	USART2	Enabled	Once initialized the USART2 configuration is: 8-bits, even parity and 1 Stop bit
	USART2_RX pin	Input	PA3 pin: USART2 in reception mode
	USART2_TX pin	Output	PA2 pin: USART2 in transmission mode
USART3 bootloader on (PB10/PB11)	USART3	Enabled	Once initialized the USART3 configuration is: 8-bits, even parity and 1 Stop bit
	USART3_RX pin	Input	PB11 pin: USART3 in reception mode
	USART3_TX pin	Output	PB10 pin: USART3 in transmission mode
USART3 bootloader on (PD8/PD9)	USART3	Enabled	Once initialized the USART3 configuration is: 8-bits, even parity and 1 Stop bit
	USART3_RX pin	Input	PD9 pin: USART3 in reception mode
	USART3_TX pin	Output	PD8 pin: USART3 in transmission mode

Table 95. STM32H7A3xx/7B3xx configuration in system memory boot mode (continued)

Bootloader	Feature/Peripheral	State	Comment
I2C1 bootloader	I2C1	Enabled	The I2C1 configuration is: I2C speed: up to 400 KHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b10101111x (where x = 0 for write and x = 1 for read)
	I2C1_SCL pin	Input/Output	PB6 pin: clock line is used in open-drain mode.
	I2C1_SDA pin	Input/Output	PB9 pin: data line is used in open-drain mode.
I2C2 bootloader	I2C2	Enabled	The I2C2 configuration is: I2C speed: up to 400 KHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b10101111x (where x = 0 for write and x = 1 for read)
	I2C2_SCL pin	Input/Output	PF1 pin: clock line is used in open-drain mode.
	I2C2_SDA pin	Input/Output	PF0 pin: data line is used in open-drain mode.
I2C3 bootloader	I2C3	Enabled	The I2C3 configuration is: I2C speed: up to 400 KHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b10101111x (where x = 0 for write and x = 1 for read)
	I2C3_SCL pin	Input/Output	PA8 pin: clock line is used in open-drain mode.
	I2C3_SDA pin	Input/Output	PC9 pin: data line is used in open-drain mode.
SPI1 bootloader	SPI1	Enabled	The SPI1 configuration is: – Slave mode – Full Duplex – 8-bit MSB – Speed up to 8 MHz – Polarity: CPOL Low, CPHA Low, NSS hardware.
	SPI1_MOSI pin	Input	PA7 pin: Slave data Input line, used in push-pull, no pull-up no pull-down mode.
	SPI1_MISO pin	Output	PA6 pin: Slave data output line, used in push-pull, no pull-up no pull-down mode.
	SPI1_SCK pin	Input	PA5 pin: Slave clock line, used in push-pull no pull-up, no pull-up no pull-down mode.
	SPI1_NSS pin	Input	PA4 pin: slave chip select pin used in push-pull, no pull-up no pull-down mode.

Table 95. STM32H7A3xx/7B3xx configuration in system memory boot mode (continued)

Bootloader	Feature/Peripheral	State	Comment
SPI2 bootloader	SPI2	Enabled	The SPI2 configuration is: – Slave mode – Full Duplex – 8-bit MSB – Speed up to 8 MHz – Polarity: CPOL Low, CPHA Low, NSS hardware.
	SPI2_MOSI pin	Input	PB15 pin: Slave data Input line, used in push-pull, no pull-up no pull-down mode.
	SPI2_MISO pin	Output	PB14 pin: Slave data output line, used in push-pull, no pull-up no pull-down mode.
	SPI2_SCK pin	Input	PB13 pin: Slave clock line, used in push-pull, no pull-up no pull-down mode.
	SPI2_NSS pin	Input	PB12 pin: slave chip select pin used in push-pull, no pull-up no pull-down mode.
SPI3 bootloader	SPI3	Enabled	The SPI3 configuration is: – Slave mode – Full Duplex – 8-bit MSB – Speed up to 8 MHz – Polarity: CPOL Low, CPHA Low, NSS hardware.
	SPI3_MOSI pin	Input	PC12 pin: Slave data Input line, used in push-pull, no pull-up no-pull down mode
	SPI3_MISO pin	Output	PC11 pin: Slave data output line, used in push-pull, no pull-up no-pull down mode.
	SPI3_SCK pin	Input	PC10 pin: Slave clock line, used in push-pull, no pull-up no-pull down mode.
	SPI3_NSS pin	Input	PA15 pin: slave chip select pin used in push-pull, no pull-up no pull-down mode.
DFU bootloader	USB	Enabled	USB FS configured in forced device mode. USB FS interrupt vector is enabled and used for USB DFU communications.
	USB_DM pin	Input/Output	PA11: USB DM line.
	USB_DP pin		PA12: USB DP line No external Pull-up resistor is required

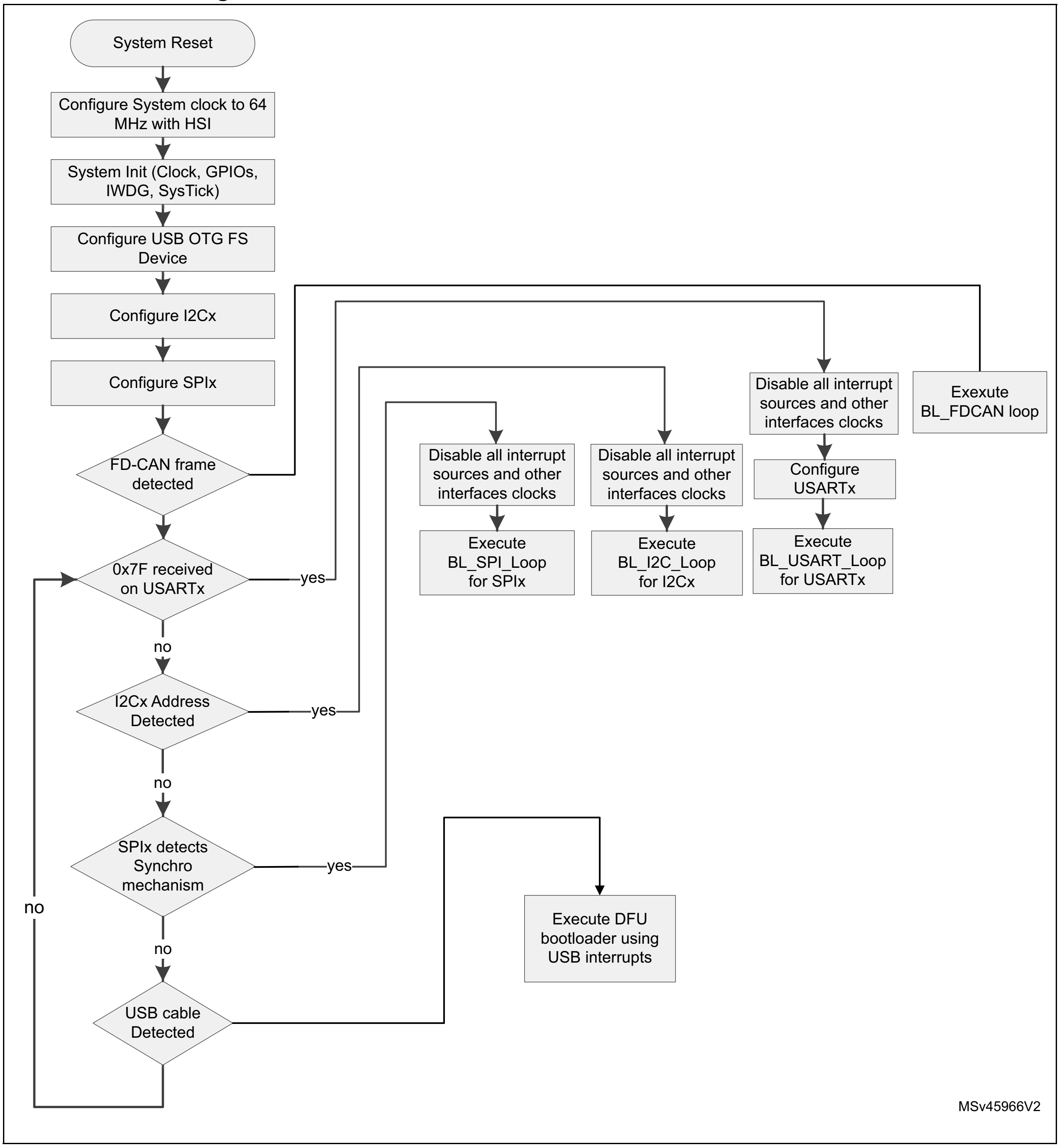
Table 95. STM32H7A3xx/7B3xx configuration in system memory boot mode (continued)

Bootloader	Feature/Peripheral	State	Comment
FDCAN bootloader on (PH13/PH14)	FDCAN1	Enabled	Once initialized the FDCAN1 configuration is: bit-rate 0.5 Mbps FrameFormat = FDCAN_FRAME_FD_BRS Mode = FDCAN_MODE_NORMAL AutoRetransmission = ENABLE TransmitPause = DISABLE ProtocolException = ENABLE
	FDCAN1_Rx pin	Input	PH14 pin: FDCAN1 in reception mode
	FDCAN1_Tx pin	Output	PH13 pin: FDCAN1 in transmission mode
FDCAN bootloader on (PD1/PD0)	FDCAN1	Enabled	Once initialized the FDCAN1 configuration is: bit-rate 0.5 Mbps FrameFormat = FDCAN_FRAME_FD_BRS Mode = FDCAN_MODE_NORMAL AutoRetransmission = ENABLE TransmitPause = DISABLE ProtocolException = ENABLE
	FDCAN1_Rx pin	Input	PD0 pin: FDCAN1 in reception mode
	FDCAN1_Tx pin	Output	PD1 pin: FDCAN1 in transmission mode

44.2 Bootloader selection

The *Figure 55* shows the bootloader selection mechanism.

Figure 56. Bootloader V9.x selection for STM32H7A3xx/7B3xx



44.3 Bootloader version

Table 94 lists the STM32H7A3xx/7B3xx devices bootloader versions.

Table 96. STM32H7A3xx/7B3xx bootloader version

Bootloader version number	Description	Known limitations
V9.0	Initial bootloader version on cut 1.1 samples	– String returned describing the Flash memory size when using USB is wrong. Expected value is (256 x 8 KB) but returned (256 x 2 KB) – OTP memory is not supported by the bootloader

45 STM32L01xxx/02xxx devices bootloader

45.1 Bootloader configuration

The STM32L01xxx/02xxx bootloader is activated by applying pattern6 (described in *Table 2: Bootloader activation patterns*). The following *Table 97* shows the hardware resources used by this bootloader.

Table 97. STM32L01xxx/02xxx configuration in system memory boot mode

Bootloader	Feature/Peripheral	State	Comment
Common to all bootloaders	RCC	HSI enabled	The system clock frequency is 32 MHz with HSI 16 MHz as clock source.
	RAM	-	2 Kbyte starting from address 0x20000000 are used by the bootloader firmware
	System memory	-	4 Kbyte starting from address 0x1FF00000, contain the bootloader firmware
	IWDG	-	The independent watchdog (IWDG) prescaler is configured to its maximum value. It is periodically refreshed to prevent watchdog reset (in case the hardware IWDG option was previously enabled by the user).
USART1 bootloader (on PA9/PA10)	USART1	Enabled	Once initialized the USART1 configuration is: 8-bits, even parity and 1 Stop bit
	USART1_RX pin	Input	PA10 pin: USART1 in reception mode
	USART1_TX pin	Output	PA9 pin: USART1 in transmission mode
USART2 bootloader (on PA2/PA3)	USART2	Enabled	Once initialized the USART2 configuration is: 8-bits, even parity and 1 Stop bit
	USART2_RX pin	Input	PA3 pin: USART2 in reception mode
	USART2_TX pin	Output	PA2 pin: USART2 in transmission mode
USART2 bootloader	SysTick timer	Enabled	Used to automatically detect the serial baud rate from the host for USARTx bootloaders.
SPI1 bootloader (for all device packages except TSSOP14)	SPI1	Enabled	The SPI1 configuration is: Slave mode, Full Duplex, 8-bit MSB, Speed up to 8 MHz, Polarity: CPOL Low, CPHA Low, NSS hardware.
	SPI1_MOSI pin	Input	PA7 pin: Slave data Input line, used in push-pull pull-down mode
	SPI1_MISO pin	Output	PA6 pin: Slave data output line, used in push-pull pull-down mode
	SPI1_SCK pin	Input	PA5 pin: Slave clock line, used in push-pull pull-down mode
	SPI1_NSS pin	Input	PA4 pin: slave chip select pin used in push-pull pull-up mode. **Note:** This IO can be tied to GND if the SPI Master does not use it.

Table 97. STM32L01xxx/02xxx configuration in system memory boot mode (continued)

Bootloader	Feature/Peripheral	State	Comment
SPI1 bootloader (only for devices on TSSOP14 package)	SPI1	Enabled	The SPI1 configuration is: Slave mode, Full Duplex, 8-bit MSB, Speed up to 8 MHz, Polarity: CPOL Low, CPHA Low, NSS hardware.
	SPI1_MOSI pin	Input	PA7 pin: Slave data Input line, used in push-pull pull-down mode
	SPI1_MISO pin	Output	PA14 pin: Slave data output line, used in push-pull pull-down mode. **Note**: This IO is also used as SWCLK for debug interface, as consequence debugger can not connect to the device in "on-the-fly" mode when the bootloader is running.
	SPI1_SCK pin	Input	PA13 pin: Slave clock line, used in push-pull pull-down mode
	SPI1_NSS pin	Input	PA4 pin: slave chip select pin used in push-pull pull-up mode. **Note:** NSS pin synchronization is required on bootloader with SPI1 interface for devices on TSSOP14 package.

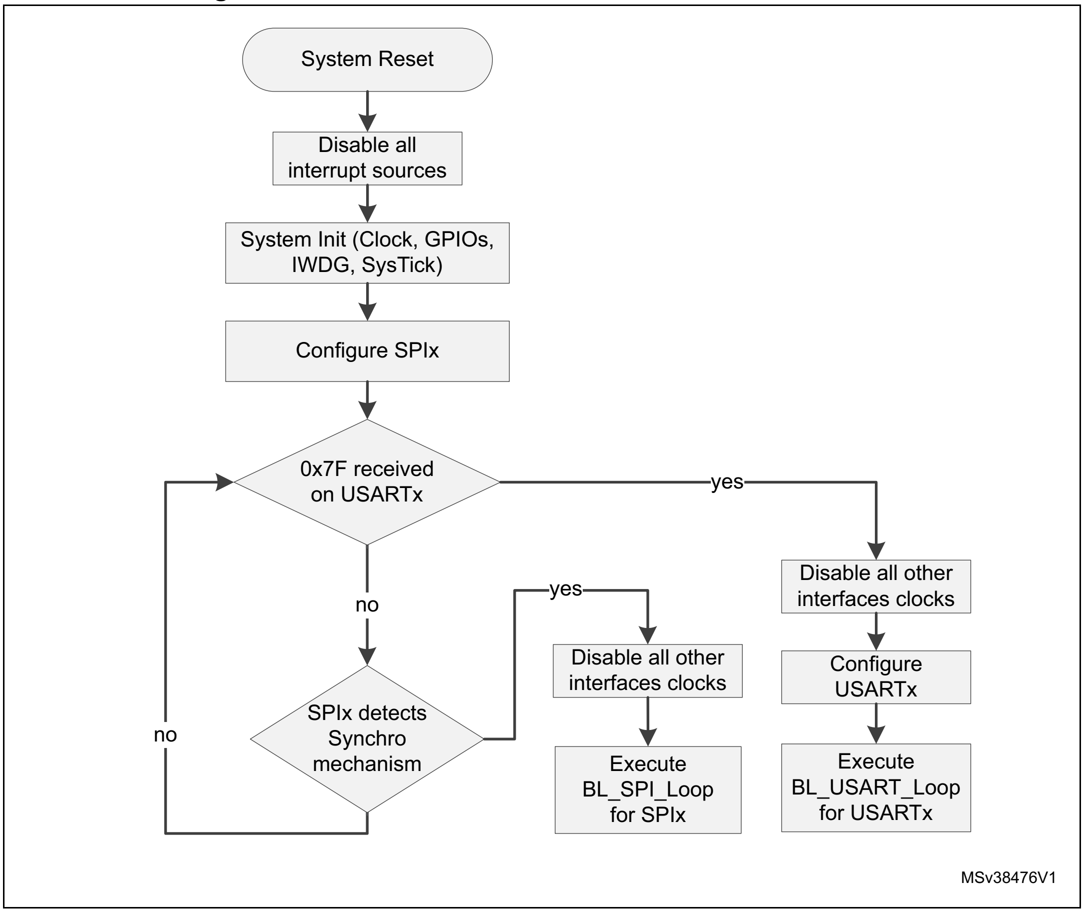
The system clock is derived from the embedded internal high-speed RC for all bootloader interfaces. No external quartz is required for bootloader operations.

Note: Due to empty check mechanism present on this product, it is not possible to jump from user code to system bootloader. Such jump results in a jump back to user flash space. But if the first 4 bytes of user lash memory (at 0x0800 0000) are empty at the moment of the jump (ie. erase first sector before jump or execute code from SRAM while Flash is empty), then system bootloader will be executed when jumped to.

45.2 Bootloader selection

The *Table 57* shows the bootloader selection mechanism.

Figure 57. Bootloader selection for STM32L01xxx/02xxx



45.3 Bootloader version

The following table lists the STM32L01xxx/02xxx devices bootloader versions.

Table 98. STM32L01xxx/02xxx bootloader versions

Bootloader version number	Description	Known limitations
V12.2	Initial bootloader version	Bootloader not functional with SPI1 interface for devices on TSSOP14 package.
V12.3	This bootloader is an updated version of bootloader V12.2. This new version add support of SPI interface for devices on TSSOP14 package.	For the SPI1 interface for devices in TSSOP14, a falling edge on NSS pin is required before staring communication, to properly synchronize the SPI interface. If the NSS pin is grounded (all time from device reset) the SPI communication is not synchronized and bootloader does not work properly with the SPI interface.

46 STM32L031xx/041xx devices bootloader

46.1 Bootloader configuration

The STM32L031xx/041xx bootloader is activated by applying pattern2 (described in *Table 2: Bootloader activation patterns*). The following table shows the hardware resources used by this bootloader.

Table 99. STM32L031xx/041xx configuration in system memory boot mode

Bootloader	Feature/Peripheral	State	Comment
Common to all bootloaders	RCC	HSI enabled	The system clock frequency is 32 MHz with HSI 16 MHz as clock source.
	RAM	-	4 Kbyte starting from address 0x20000000 are used by the bootloader firmware
	System memory	-	4 Kbyte starting from address 0x1FF00000, contain the bootloader firmware
	IWDG	-	The independent watchdog (IWDG) prescaler is configured to its maximum value. It is periodically refreshed to prevent watchdog reset (in case the hardware IWDG option was previously enabled by the user).
USART2 bootloader (on PA9/PA10)	USART2	Enabled	Once initialized the USART2 configuration is: 8-bits, even parity and 1 Stop bit
	USART2_RX pin	Input	PA10 pin: USART2 in reception mode
	USART2_TX pin	Output	PA9 pin: USART2 in transmission mode
USART2 bootloader (on PA2/PA3)	USART2	Enabled	Once initialized the USART2 configuration is: 8-bits, even parity and 1 Stop bit
	USART2_RX pin	Input	PA3 pin: USART2 in reception mode
	USART2_TX pin	Output	PA2 pin: USART2 in transmission mode
USART2 bootloader	SysTick timer	Enabled	Used to automatically detect the serial baud rate from the host for USARTx bootloaders.

Table 99. STM32L031xx/041xx configuration in system memory boot mode (continued)

Bootloader	Feature/Peripheral	State	Comment
SPI1 bootloader	SPI1	Enabled	The SPI1 configuration is: Slave mode, Full Duplex, 8-bit MSB, Speed up to 8 MHz, Polarity: CPOL Low, CPHA Low, NSS hardware.
	SPI1_MOSI pin	Input	PA7 pin: Slave data Input line, used in push-pull pull-down mode
	SPI1_MISO pin	Output	PA6 pin: Slave data output line, used in push-pull pull-down mode
	SPI1_SCK pin	Input	PA5 pin: Slave clock line, used in push-pull pull-down mode
	SPI1_NSS pin	Input	PA4 pin: slave chip select pin used in push-pull pull-up mode. **Note:** This IO can be tied to GND if the SPI Master does not use it.

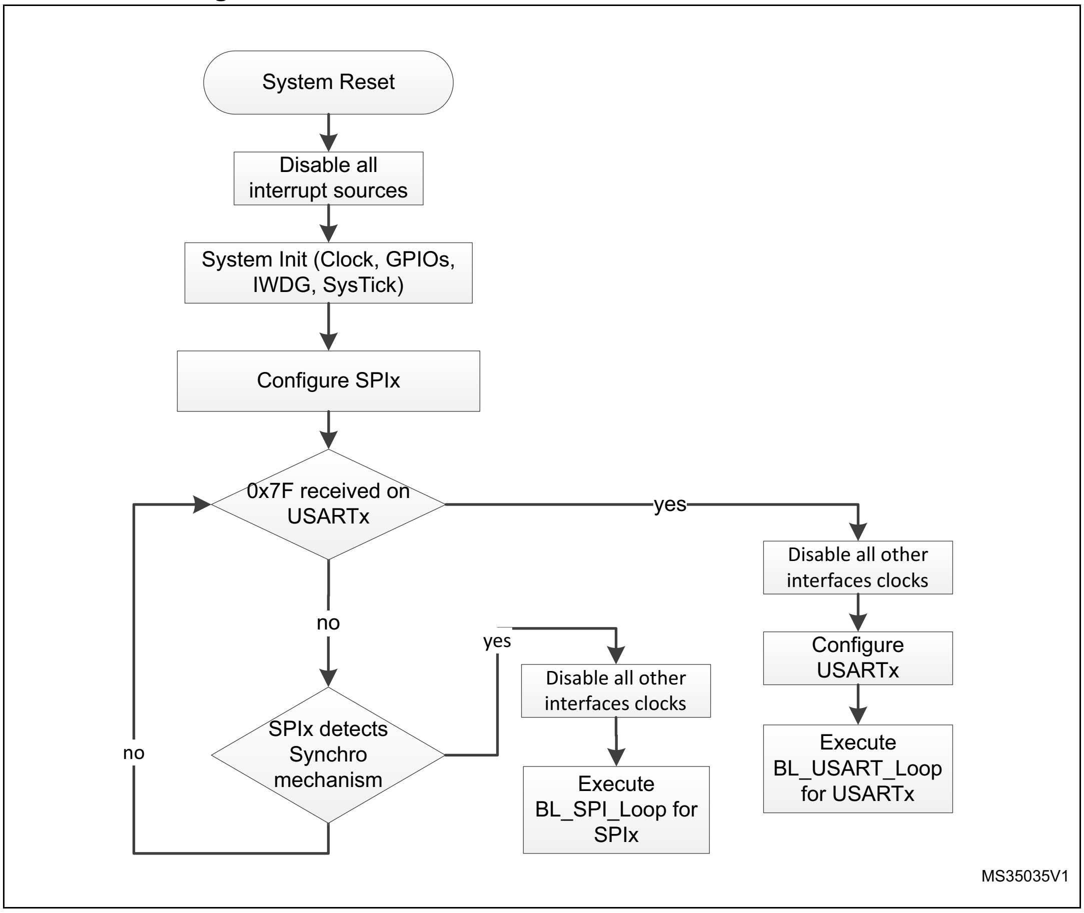
The system clock is derived from the embedded internal high-speed RC for all bootloader interfaces. No external quartz is required for bootloader operations.

The bootloader Read/Write commands don’t support SRAM memory space for this product.

46.2 Bootloader selection

The *Figure 58* shows the bootloader selection mechanism.

Figure 58. Bootloader selection for STM32L031xx/041xx



46.3 Bootloader version

The *Table 100* lists the STM32L031xx/041xx devices bootloader versions:

Table 100. STM32L031xx/041xx bootloader versions

Bootloader version number	Description	Known limitations
V12.0	Initial bootloader version	None

47 STM32L05xxx/06xxx devices bootloader

47.1 Bootloader configuration

The STM32L05xxx/06xxx bootloader is activated by applying pattern1 (described in *Table 2: Bootloader activation patterns*). The following table shows the hardware resources used by this bootloader.

Table 101. STM32L05xxx/06xxx configuration in system memory boot mode

Bootloader	Feature/Peripheral	State	Comment
Common to all bootloaders	RCC	HSI enabled	The system clock frequency is 32 MHz with HSI 16 MHz as clock source.
	Power	-	Voltage range is set to Voltage Range 1.
	RAM	-	4 Kbyte starting from address 0x20000000 are used by the bootloader firmware
	System memory	-	4 Kbyte starting from address 0x1FF00000, contain the bootloader firmware
	IWDG	-	The independent watchdog (IWDG) prescaler is configured to its maximum value. It is periodically refreshed to prevent watchdog reset (in case the hardware IWDG option was previously enabled by the user).
USART1 bootloader	USART1	Enabled	Once initialized the USART1 configuration is: 8-bits, even parity and 1 Stop bit
	USART1_RX pin	Input	PA10 pin: USART1 in reception mode
	USART1_TX pin	Output	PA9 pin: USART1 in transmission mode
USART2 bootloader	USART2	Enabled	Once initialized the USART2 configuration is: 8-bits, even parity and 1 Stop bit
	USART2_RX pin	Input	PA3 pin: USART2 in reception mode
	USART2_TX pin	Output	PA2 pin: USART2 in transmission mode
USARTx bootloaders	SysTick timer	Enabled	Used to automatically detect the serial baud rate from the host for USARTx bootloaders.

Table 101. STM32L05xxx/06xxx configuration in system memory boot mode (continued)

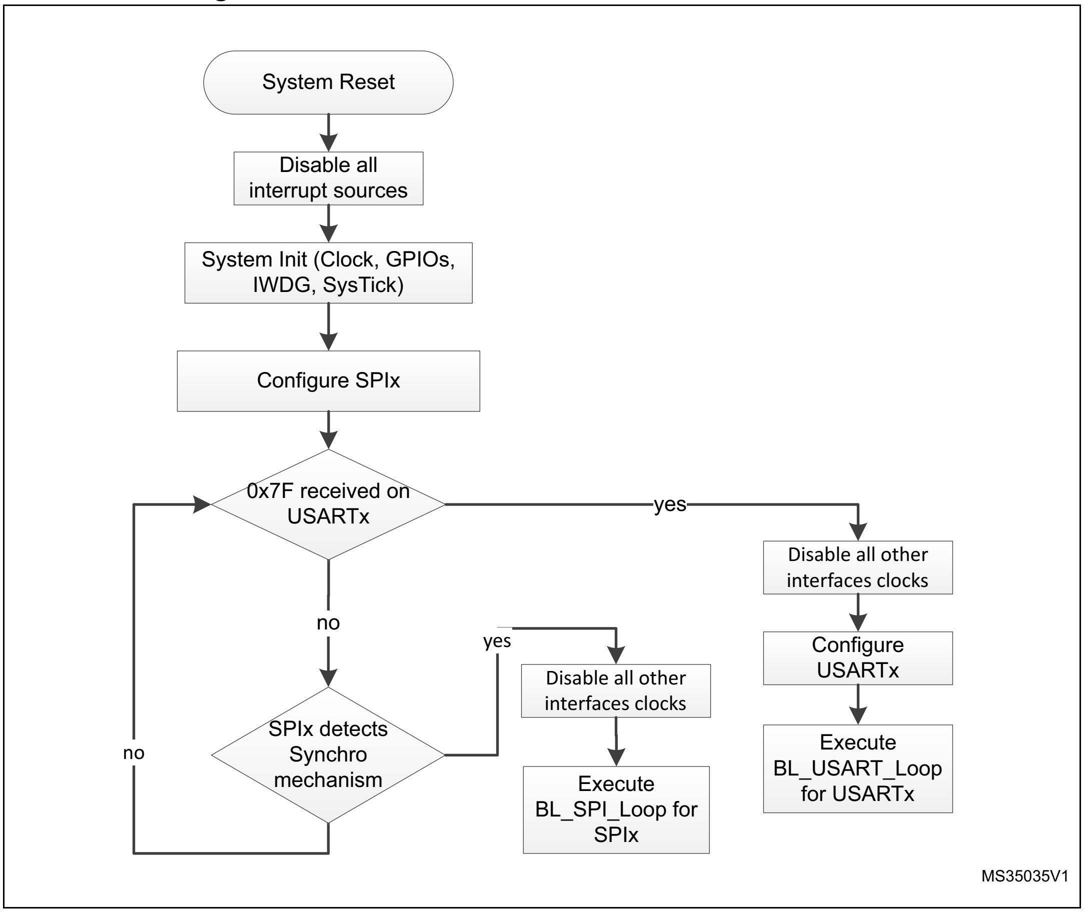
Bootloader	Feature/Peripheral	State	Comment
SPI1 bootloader	SPI1	Enabled	The SPI1 configuration is: Slave mode, Full Duplex, 8-bit MSB, Speed up to 8 MHz, Polarity: CPOL Low, CPHA Low, NSS hardware.
	SPI1_MOSI pin	Input	PA7 pin: Slave data Input line, used in push-pull pull-down mode
	SPI1_MISO pin	Output	PA6 pin: Slave data output line, used in push-pull pull-down mode
	SPI1_SCK pin	Input	PA5 pin: Slave clock line, used in push-pull pull-down mode
	SPI1_NSS pin	Input	PA4 pin: slave chip select pin used in push-pull pull-down mode.
SPI2 bootloader	SPI2	Enabled	The SPI2 configuration is: Slave mode, Full Duplex, 8-bit MSB, Speed up to 8 MHz, Polarity: CPOL Low, CPHA Low, NSS hardware.
	SPI2_MOSI pin	Input	PB15 pin: Slave data Input line, used in push-pull pull-down mode
	SPI2_MISO pin	Output	PB14 pin: Slave data output line, used in push-pull pull-down mode
	SPI2_SCK pin	Input	PB13 pin: Slave clock line, used in push-pull pull-down mode
	SPI2_NSS pin	Input	PB12 pin: slave chip select pin used in push-pull pull-down mode.

The system clock is derived from the embedded internal high-speed RC for all bootloader interfaces. No external quartz is required for bootloader operations.

47.2 Bootloader selection

The figure below shows the bootloader selection mechanism.

Figure 59. Bootloader selection for STM32L05xxx/06xxx



47.3 Bootloader version

The following table lists the STM32L05xxx/06xxx devices bootloader versions:

Table 102. STM32L05xxx/06xxx bootloader versions

Bootloader version number	Description	Known limitations
V12.0	Initial bootloader version	None

48 STM32L07xxx/08xxx devices bootloader

Two bootloader versions are available on STM32L07xxx/08xxx devices:

- V4.x supporting USART1, USART2 and DFU (USB FS Device).
  This version is embedded in STM32L072xx/73xx and STM32L082xx/83xx devices.
- V11.x supporting USART1, USART2, I2C1, I2C2, SPI1 and SPI2.
  This version is embedded in other STM32L071xx/081xx devices.

48.1 Bootloader V4.x

48.1.1 Bootloader configuration

The STM32L07xxx/08xxx bootloader is activated by applying pattern2 or pattern7 when dual bank boot feature is available (described in *Table 2: Bootloader activation patterns*). The *Table 103* shows the hardware resources used by this bootloader.

Table 103. STM32L07xxx/08xxx configuration in system memory boot mode

Bootloader	Feature/Peripheral	State	Comment
Common to all bootloaders	RCC	HSI enabled	The system clock frequency is 32 MHz with HSI 16 MHz as clock source.
	RAM	-	4 Kbyte starting from address 0x20000000 are used by the bootloader firmware.
	System memory	-	8 Kbyte starting from address 0x1FF00000, contain the bootloader firmware.
	IWDG	-	The independent watchdog (IWDG) prescaler is configured to its maximum value. It is periodically refreshed to prevent watchdog reset (in case the hardware IWDG option was previously enabled by the user).
USART1 bootloader	USART1	Enabled	Once initialized the USART1 configuration is: 8-bits, even parity and 1 Stop bit
	USART1_RX pin	Input	PA10 pin: USART2 in reception mode
	USART1_TX pin	Output	PA9 pin: USART2 in transmission mode
USART2 bootloader	USART2	Enabled	Once initialized the USART2 configuration is: 8-bits, even parity and 1 Stop bit
	USART2_RX pin	Input	PA3 pin: USART2 in reception mode
	USART2_TX pin	Output	PA2 pin: USART2 in transmission mode
USARTx bootloaders	SysTick timer	Enabled	Used to automatically detect the serial baud rate from the host for USARTx bootloaders.

Table 103. STM32L07xxx/08xxx configuration in system memory boot mode (continued)

Bootloader	Feature/Peripheral	State	Comment
DFU bootloader	USB	Enabled	USB FS configured in forced device mode. USB FS interrupt vector is enabled and used for USB DFU communications.
	USB_DM pin	Input/Output	PA11 pin: USB FS DM line
	USB_DP pin		PA12 pin: USB FS DP line. No external Pull-up resistor is required.

The system clock is derived from the embedded internal high-speed RC for all bootloader interfaces. No external quartz is required for bootloader operations.

48.1.2 Bootloader selection

The *Figure 60* and *Figure 61* show the bootloader selection mechanism.

Figure 60. Dual Bank Boot Implementation for STM32L07xxx/08xxx bootloader V4.x

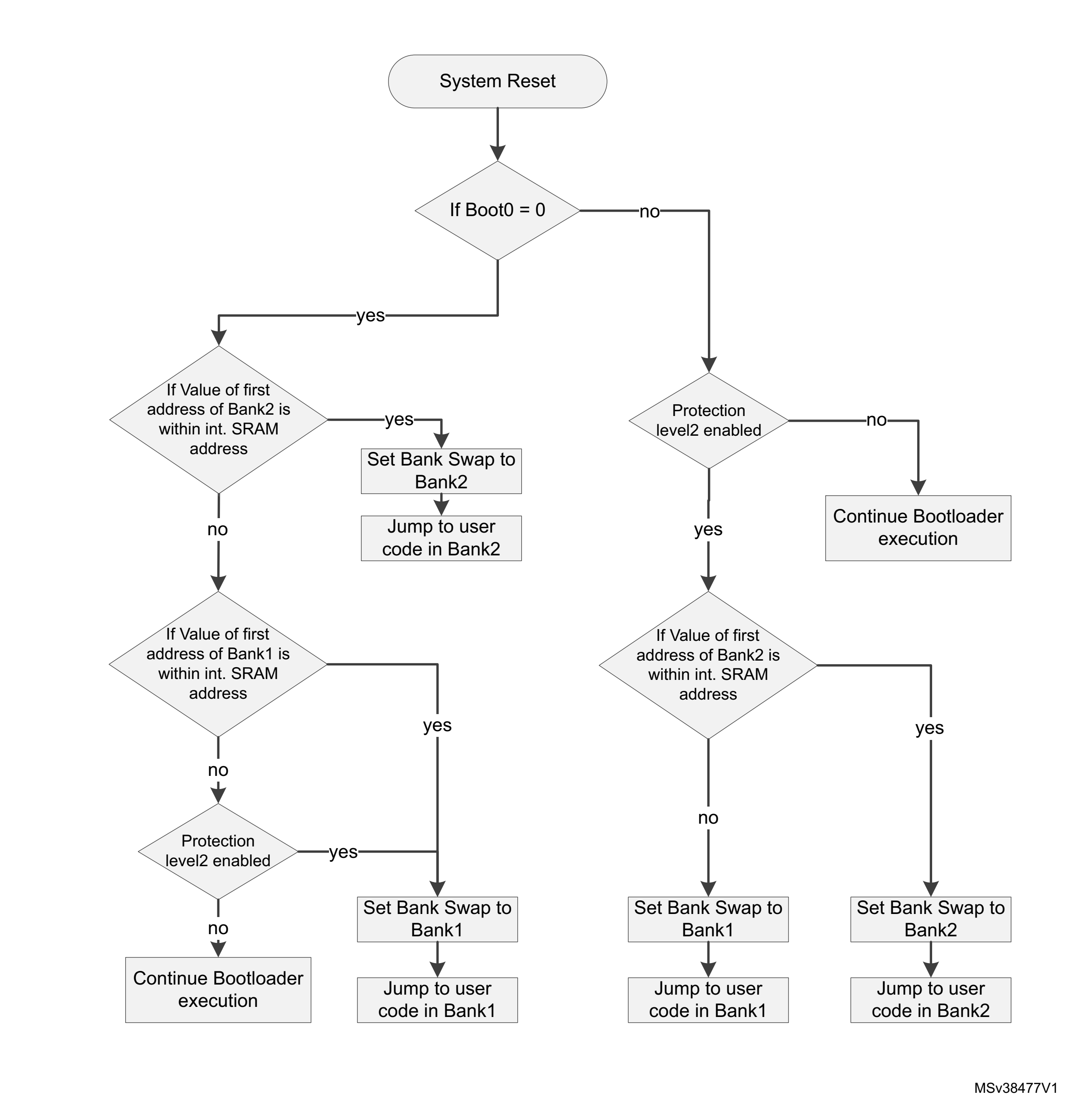
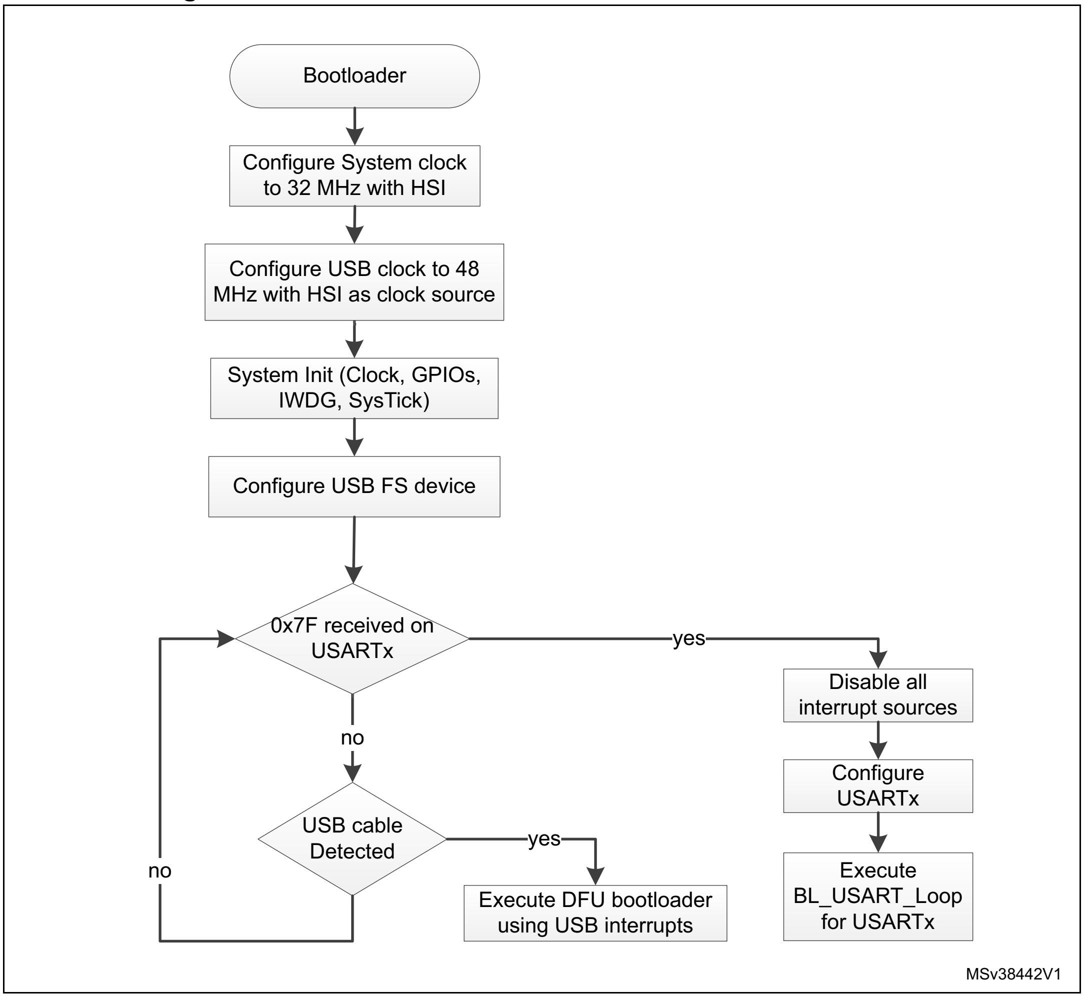


Figure 61. Bootloader V4.x selection for STM32L07xxx/08xxx



48.1.3 Bootloader version

The *Table 104* lists the STM32L07xxx/08xxx devices bootloader versions:

Table 104. STM32L07xxx/08xxx bootloader versions

Bootloader version number	Description	Known limitations
V4.0	Initial bootloader version	None
V4.1	This bootloader is an updated version of bootloader V4.0. This new version implements the Dual Bank Boot feature.	None

48.2 Bootloader V11.x

48.2.1 Bootloader configuration

The STM32L07xxx/08xxx bootloader is activated by applying pattern2 or pattern7 when dual bank boot feature is available (described in *Table 2: Bootloader activation patterns*). The *Table 105* shows the hardware resources used by this bootloader.

Table 105. STM32L07xxx/08xxx configuration in system memory boot mode

Bootloader	Feature/Peripheral	State	Comment
Common to all bootloaders	RCC	HSI enabled	The system clock frequency is 32 MHz with HSI 16 MHz as clock source.
	RAM	-	5 Kbyte starting from address 0x20000000 are used by the bootloader firmware
	System memory	-	8 Kbyte starting from address 0x1FF00000, contain the bootloader firmware
	IWDG	-	The independent watchdog (IWDG) prescaler is configured to its maximum value. It is periodically refreshed to prevent watchdog reset (in case the hardware IWDG option was previously enabled by the user).
USART1 bootloader	USART1	Enabled	Once initialized the USART1 configuration is: 8-bits, even parity and 1 Stop bit
	USART1_RX pin	Input	PA10 pin: USART2 in reception mode
	USART1_TX pin	Output	PA9 pin: USART2 in transmission mode
USART2 bootloader	USART2	Enabled	Once initialized the USART2 configuration is: 8-bits, even parity and 1 Stop bit
	USART2_RX pin	Input	PA3 pin: USART2 in reception mode
	USART2_TX pin	Output	PA2 pin: USART2 in transmission mode
USARTx bootloaders	SysTick timer	Enabled	Used to automatically detect the serial baud rate from the host for USARTx bootloaders.
I2C1 bootloader	I2C1	Enabled	The I2C1 configuration is: I2C speed: up to 400 KHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b1000010x (where x = 0 for write and x = 1 for read)
	I2C1_SCL pin	Input/Output	PB6 pin: I2C1 clock line is used in open-drain mode.
	I2C1_SDA pin	Input/Output	PB7 pin: I2C1 data line is used in open-drain mode.

Table 105. STM32L07xxx/08xxx configuration in system memory boot mode (continued)

Bootloader	Feature/Peripheral	State	Comment
I2C2 bootloader	I2C2	Enabled	The I2C2 configuration is: I2C speed: up to 400 KHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b1000010x (where x = 0 for write and x = 1 for read)
	I2C2_SCL pin	Input/Output	PB10 pin: I2C2 clock line is used in open-drain mode.
	I2C2_SDA pin	Input/Output	PB11 pin: I2C2 data line is used in open-drain mode.
SPI1 bootloader	SPI1	Enabled	The SPI1 configuration is: Slave mode, Full Duplex, 8-bit MSB, Speed up to 8 MHz, Polarity: CPOL Low, CPHA Low, NSS hardware.
	SPI1_MOSI pin	Input	PA7 pin: Slave data Input line, used in push-pull pull-down mode
	SPI1_MISO pin	Output	PA6 pin: Slave data output line, used in push-pull pull-down mode
	SPI1_SCK pin	Input	PA5 pin: Slave clock line, used in push-pull pull-down mode
	SPI1_NSS pin	Input	PA4 pin: slave chip select pin used in push-pull pull-up mode. **Note**: This IO can be tied to Gnd if the SPI Master does not use it.
SPI2 bootloader	SPI2	Enabled	The SPI2 configuration is: Slave mode, Full Duplex, 8-bit MSB, Speed up to 8 MHz, Polarity: CPOL Low, CPHA Low, NSS hardware.
	SPI2_MOSI pin	Input	PB15 pin: Slave data Input line, used in push-pull pull-down mode
	SPI2_MISO pin	Output	PB14 pin: Slave data output line, used in push-pull pull-down mode
	SPI2_SCK pin	Input	PB13 pin: Slave clock line, used in push-pull pull-down mode
	SPI2_NSS pin	Input	PB12 pin: slave chip select pin used in push-pull pull-up mode. **Note**: This IO can be tied to GND if the SPI Master does not use it.

The system clock is derived from the embedded internal high-speed RC for all bootloader interfaces. No external quartz is required for bootloader operations.

48.2.2 Bootloader selection

The *Figure 62* and *Figure 63* show the bootloader selection mechanism.

Figure 62. Dual Bank Boot Implementation for STM32L07xxx/08xxx bootloader V11.x

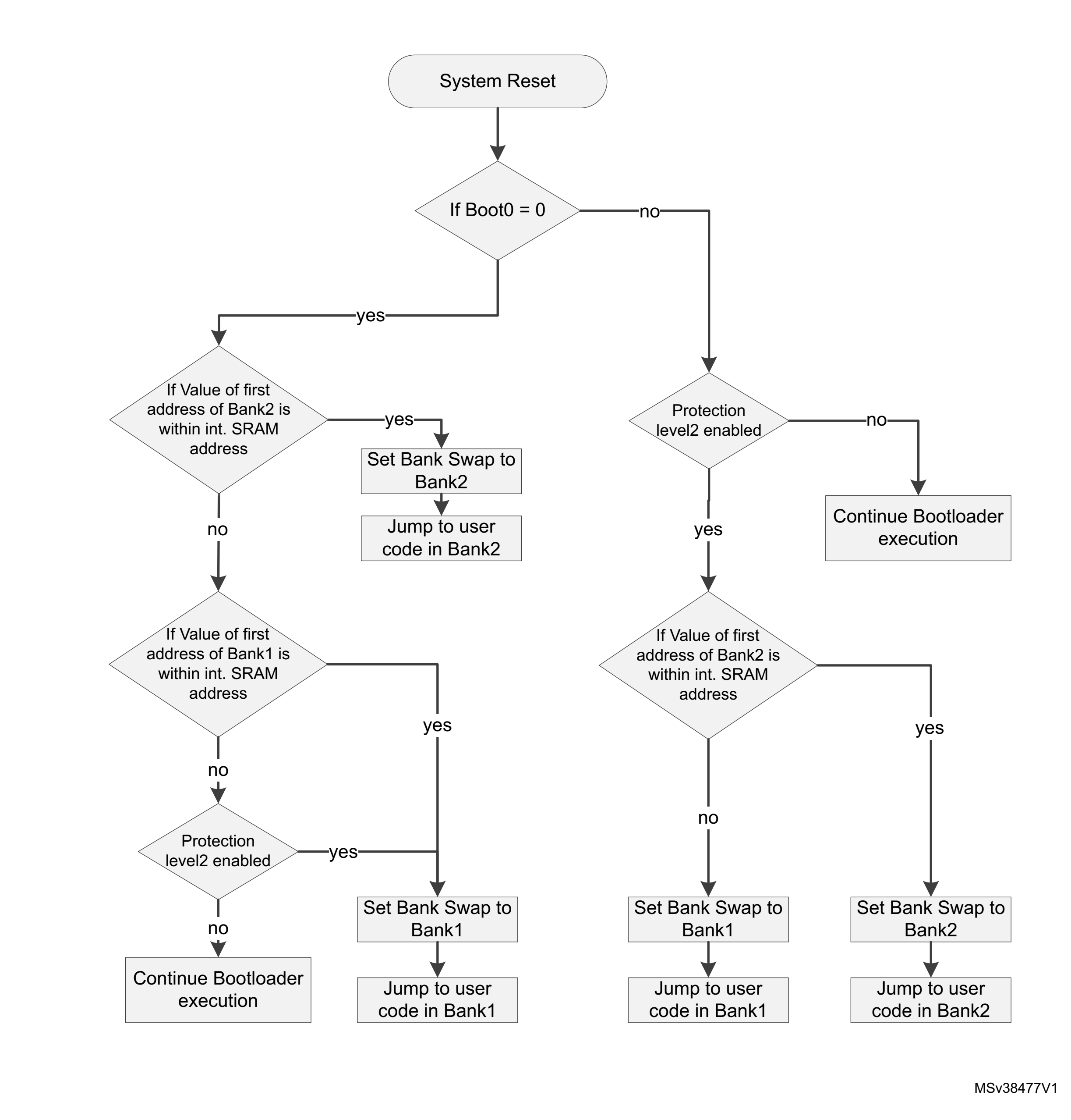
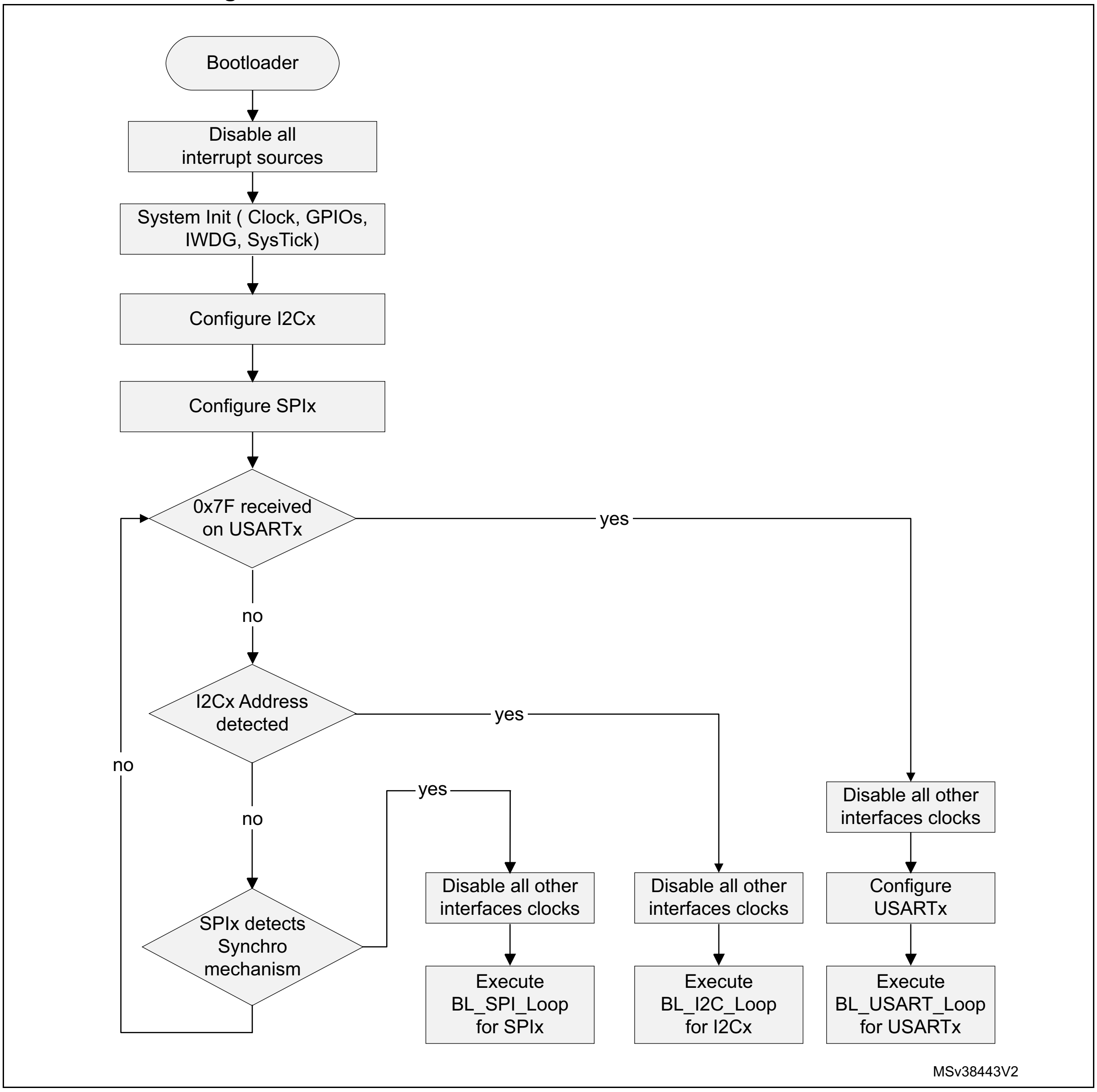


Figure 63. Bootloader V11.x selection for STM32L07xxx/08xxx



48.2.3 Bootloader version

The following table lists the STM32L07xxx/08xxx devices bootloader versions:

Table 106. STM32L07xxx/08xxx bootloader V11.x versions

Bootloader version number	Description	Known limitations
V11.1	Initial bootloader version	None
V11.2	This bootloader is an updated version of bootloader V11.1. This new version implements the Dual Bank Boot feature.	None

49 STM32L1xxx6(8/B)A devices bootloader

49.1 Bootloader configuration

The STM32L1xxx6(8/B)A bootloader is activated by applying pattern1 (described in *Table 2: Bootloader activation patterns*). The following table shows the hardware resources used by this bootloader.

Table 107. STM32L1xxx6(8/B)A configuration in system memory boot mode

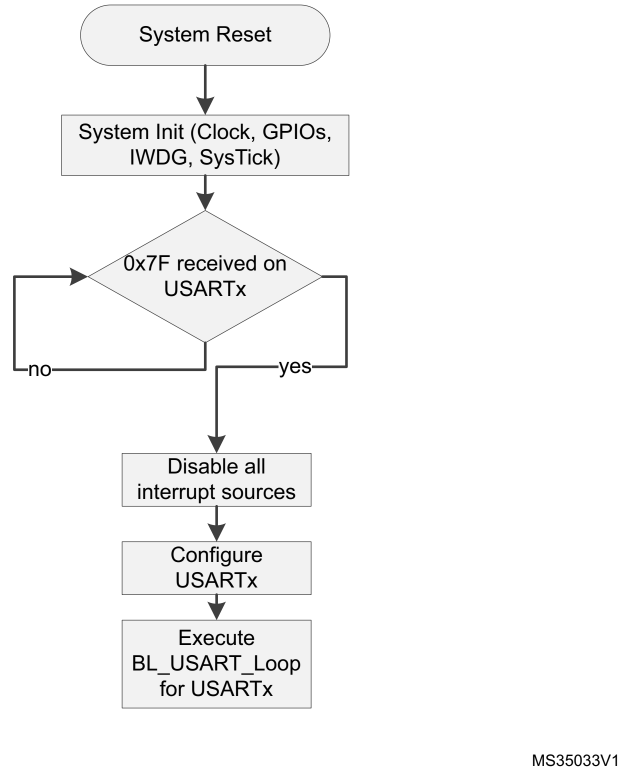
Bootloader	Feature/Peripheral	State	Comment
Common to all bootloaders	RCC	HSI enabled	The system clock frequency is 16 MHz.
	RAM	-	2 Kbyte starting from address 0x20000000 are used by the bootloader firmware.
	System memory	-	4 Kbyte starting from address 0x1FF00000 contain the bootloader firmware.
	IWDG	-	The independent watchdog (IWDG) prescaler is configured to its maximum value and is periodically refreshed to prevent watchdog reset (in case the hardware IWDG option was previously enabled by the user).
	Power	-	Voltage range is set to Voltage Range 1.
USART1 bootloader	USART1	Enabled	Once initialized, the USART1 configuration is: 8 bits, even parity and 1 Stop bit.
	USART1_RX pin	Input	PA10 pin: USART1 in reception mode
	USART1_TX pin	Output	PA9 pin: USART1 in transmission mode
USART2 bootloader	USART2	Enabled	Once initialized, the USART2 configuration is: 8 bits, even parity and 1 Stop bit.
	USART2_RX pin	Input	PD6 pin: USART2 in reception mode
	USART2_TX pin	Output	PD5 pin: USART2 in transmission mode
USARTx bootloaders	SysTick timer	Enabled	Used to automatically detect the serial baud rate from the host.

The system clock is derived from the embedded internal high-speed RC, no external quartz is required for the bootloader execution.

49.2 Bootloader selection

The figure below shows the bootloader selection mechanism.

Figure 64. Bootloader selection for STM32L1xxx6(8/B)A devices



49.3 Bootloader version

The following table lists the STM32L1xxx6(8/B)A devices bootloader versions:

Table 108. STM32L1xxx6(8/B)A bootloader versions

Bootloader version number	Description	Known limitations
V2.0	Initial bootloader version	When a Read Memory command or Write Memory command is issued with an unsupported memory address and a correct address checksum (ie. address 0x6000 0000), the command is aborted by the bootloader device, but the NACK (0x1F) is not sent to the host. As a result, the next 2 bytes (which are the number of bytes to be read/written and its checksum) are considered as a new command and its checksum.(1)

1. If the “number of data - 1” (N-1) to be read/written is not equal to a valid command code, then the limitation is not perceived from the host since the command is NACKed anyway (as an unsupported new command).

50 STM32L1xxx6(8/B) devices bootloader

50.1 Bootloader configuration

The STM32L1xxx6(8/B) bootloader is activated by applying pattern1 (described in *Table 2: Bootloader activation patterns*). The following table shows the hardware resources used by this bootloader.

Table 109. STM32L1xxx6(8/B) configuration in system memory boot mode

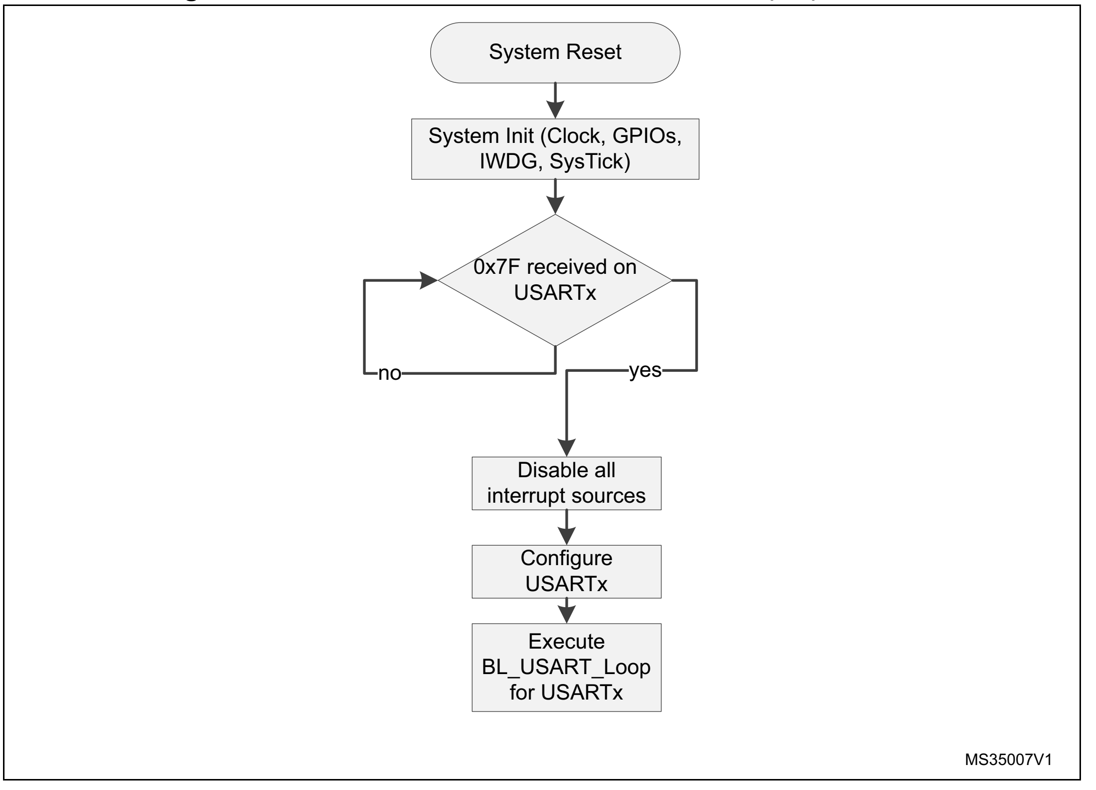
Bootloader	Feature/Peripheral	State	Comment
Common to all bootloaders	RCC	HSI enabled	The system clock frequency is 16 MHz.
	RAM	-	2 Kbyte starting from address 0x20000000 are used by the bootloader firmware.
	System memory	-	4 Kbyte starting from address 0x1FF00000 contain the bootloader firmware.
	IWDG	-	The independent watchdog (IWDG) prescaler is configured to its maximum value and is periodically refreshed to prevent watchdog reset (in case the hardware IWDG option was previously enabled by the user).
	Power	-	Voltage range is set to Voltage Range 1.
USART1 bootloader	USART1	Enabled	Once initialized, the USART1 configuration is: 8 bits, even parity and 1 Stop bit.
	USART1_RX pin	Input	PA10 pin: USART1 in reception mode
	USART1_TX pin	Output	PA9 pin: USART1 in transmission mode
USART2 bootloader	USART2	Enabled	Once initialized, the USART2 configuration is: 8 bits, even parity and 1 Stop bit.
	USART2_RX pin	Input	PD6 pin: USART2 in reception mode
	USART2_TX pin	Output	PD5 pin: USART2 in transmission mode
USARTx bootloaders	SysTick timer	Enabled	Used to automatically detect the serial baud rate from the host.

The system clock is derived from the embedded internal high-speed RC, no external quartz is required for the bootloader execution.

50.2 Bootloader selection

The figure below shows the bootloader selection mechanism.

Figure 65. Bootloader selection for STM32L1xxx6(8/B) devices



50.3 Bootloader version

The following table lists the STM32L1xxx6(8/B) devices bootloader versions:

Table 110. STM32L1xxx6(8/B) bootloader versions

Bootloader version number	Description	Known limitations
V2.0	Initial bootloader version	When a Read Memory command or Write Memory command is issued with an unsupported memory address and a correct address checksum (ie. address 0x6000 0000), the command is aborted by the bootloader device, but the NACK (0x1F) is not sent to the host. As a result, the next 2 bytes (which are the number of bytes to be read/written and its checksum) are considered as a new command and its checksum.(1)

1. If the “number of data - 1” (N-1) to be read/written is not equal to a valid command code, then the limitation is not perceived from the host since the command is NACKed anyway (as an unsupported new command).

51 STM32L1xxxC devices bootloader

51.1 Bootloader configuration

The STM32L1xxxC bootloader is activated by applying pattern1 (described in *Table 2: Bootloader activation patterns*). The following table shows the hardware resources used by this bootloader.

Table 111. STM32L1xxxC configuration in system memory boot mode

Bootloader	Feature/Peripheral	State	Comment
Common to all bootloaders	RCC	HSI enabled	The system clock frequency is 16 MHz using the HSI. This is used only for USARTx bootloaders and during USB detection for DFU bootloader (once the DFU bootloader is selected, the clock source is derived from the external crystal).
		HSE enabled	The external clock is mandatory only for the DFU bootloader and must be in the following range: [24, 16, 12, 8, 6, 4, 3, 2] MHz. The PLL is used to generate the USB 48 MHz clock and the 32 MHz clock for the system clock.
		-	The Clock Security System (CSS) interrupt is enabled for the DFU bootloader. Any failure (or removal) of the external clock generates a system reset.
	RAM	-	4 Kbyte starting from address 0x20000000 are used by the bootloader firmware.
	System memory	-	8 Kbyte starting from address 0x1FF00000 contains the bootloader firmware.
	IWDG	-	The independent watchdog (IWDG) prescaler is configured to its maximum value and is periodically refreshed to prevent watchdog resets (in case the hardware IWDG option was previously enabled by the user).
	Power	-	Voltage range is set to Voltage Range 1.
USART1 bootloader	USART1	Enabled	Once initialized, the USART1 configuration is 8 bits, even parity and 1 stop bit.
	USART1_RX pin	Input	PA10 pin: USART1 in reception mode
	USART1_TX pin	Output	PA9 pin: USART1 in transmission mode
USART2 bootloader	USART2	Enabled	Once initialized, the USART2 configuration is 8 bits, even parity and 1 stop bit. The USART2 uses its remapped pins.
	USART2_RX pin	Input	PD6 pin: USART2 in reception mode
	USART2_TX pin	Output	PD5 pin: USART2 in transmission mode

Table 111. STM32L1xxxC configuration in system memory boot mode (continued)

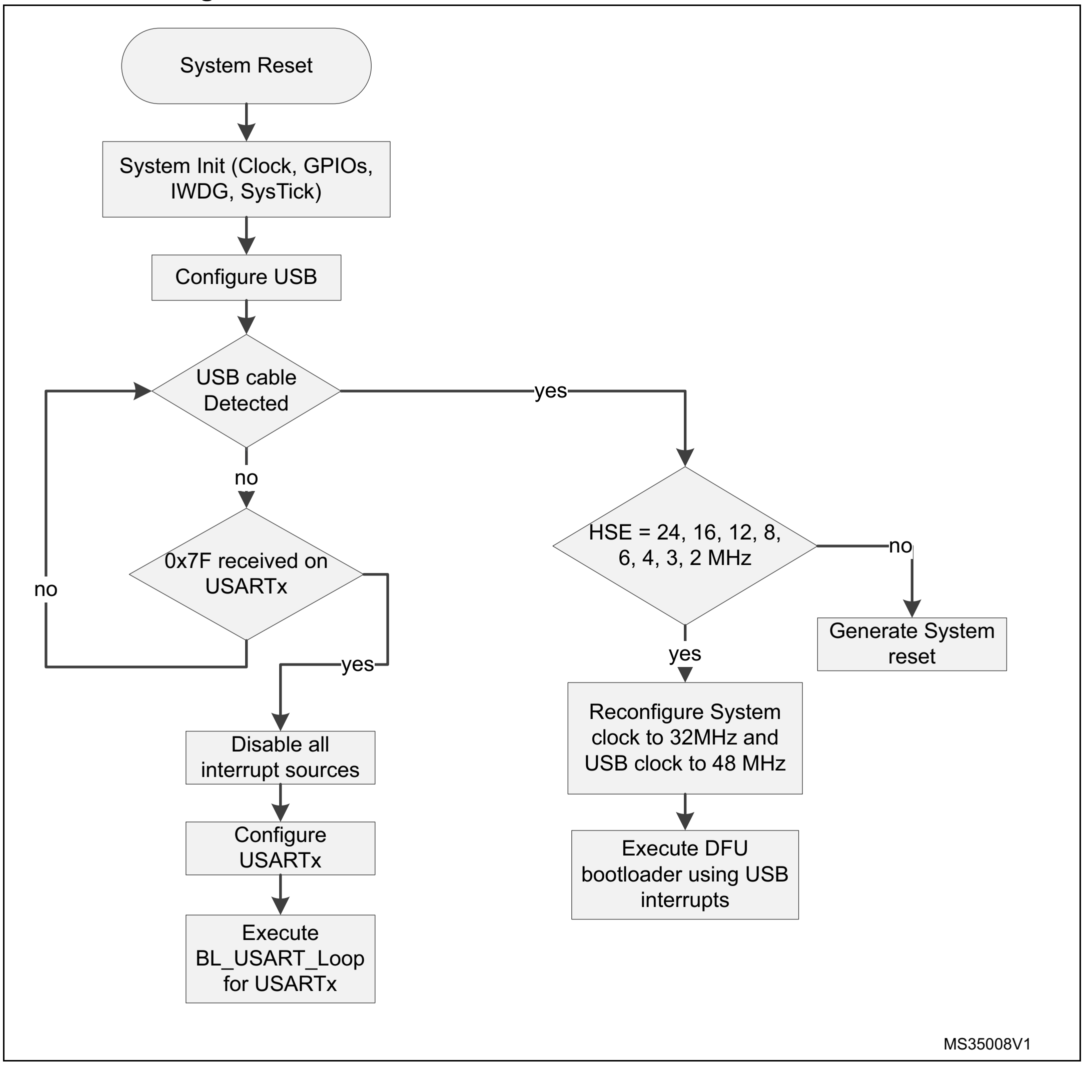
Bootloader	Feature/Peripheral	State	Comment
USARTx bootloaders	SysTick timer	Enabled	Used to automatically detect the serial baud rate from the host for the USARTx bootloader.
DFU bootloader	USB	Enabled	USB used in FS mode
	USB_DM pin	Input/Output	PA11: USB DM line.
	USB_DP pin		PA12: USB DP line An external pull-up resistor 1.5 KOhm must be connected to USB_DP pin.

The system clock is derived from the embedded internal high-speed RC for the USARTx bootloader. This internal clock is also used the for DFU bootloader but only for the selection phase. An external clock in the range of [24, 16, 12, 8, 6, 4, 3, 2] MHz is required for the execution of the DFU bootloader after the selection phase.

51.2 Bootloader selection

The figure below shows the bootloader selection mechanism.

Figure 66. Bootloader selection for STM32L1xxxC devices



51.3 Bootloader version

The following table lists the STM32L1xxxC devices bootloader versions:

Table 112. STM32L1xxxC bootloader versions

Bootloader version number	Description	Known limitations
V4.0	Initial bootloader version	For the USART interface, two consecutive NACKs instead of 1 NACK are sent when a Read Memory or Write Memory command is sent and the RDP level is active.

52 STM32L1xxxD devices bootloader

52.1 Bootloader configuration

The STM32L1xxxD bootloader is activated by applying pattern4 (described in *Table 2: Bootloader activation patterns*). The following table shows the hardware resources used by this bootloader.

Table 113. STM32L1xxxD configuration in system memory boot mode

Bootloader	Feature/Peripheral	State	Comment
Common to all bootloaders	RCC	HSI enabled	The system clock frequency is 16 MHz using the HSI. This is used only for USARTx bootloaders and during USB detection for DFU bootloader (once the DFU bootloader is selected, the clock source will be derived from the external crystal).
		HSE enabled	The external clock is mandatory only for DFU bootloader and it must be in the following range: [24, 16, 12, 8, 6, 4, 3, 2] MHz. The PLL is used to generate the USB 48 MHz clock and the 32 MHz clock for the system clock.
		-	The Clock Security System (CSS) interrupt is enabled for the DFU bootloader. Any failure (or removal) of the external clock generates system reset.
	RAM	-	4 Kbyte starting from address 0x20000000 are used by the bootloader firmware.
	System memory	-	8 Kbyte starting from address 0x1FF00000 contains the bootloader firmware.
	IWDG	-	The independent watchdog (IWDG) prescaler is configured to its maximum value and is periodically refreshed to prevent watchdog reset (in case the hardware IWDG option was previously enabled by the user).
	Power	-	Voltage range is set to Voltage Range 1.
USART1 bootloader	USART1	Enabled	Once initialized, the USART1 configuration is: 8 bits, even parity and 1 Stop bit.
	USART1_RX pin	Input	PA10 pin: USART1 in reception mode
	USART1_TX pin	Output	PA9 pin: USART1 in transmission mode

Table 113. STM32L1xxxD configuration in system memory boot mode (continued)

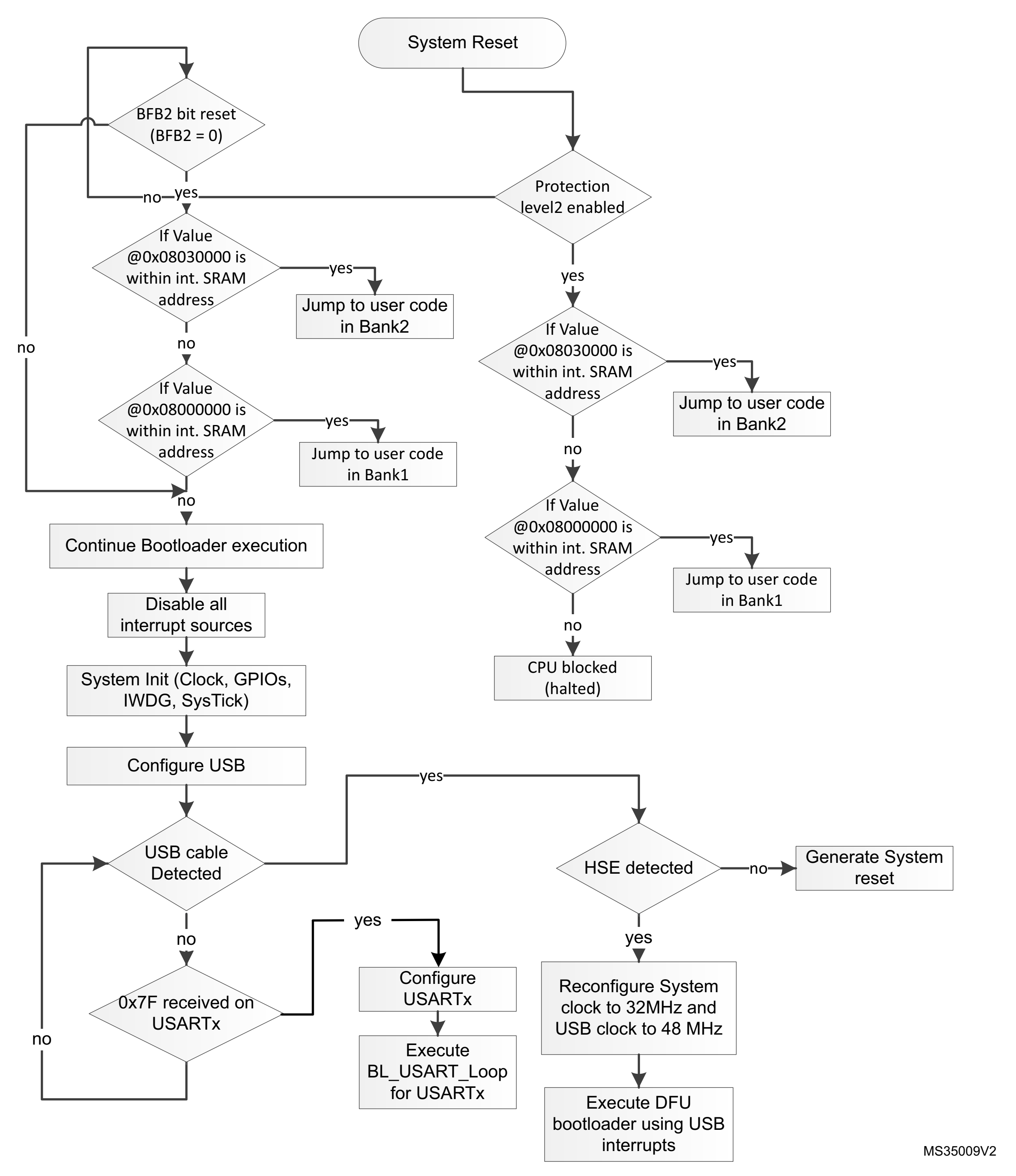
<table>
<tr><th>Bootloader</th><th>Feature/Peripheral</th><th>State</th><th>Comment</th></tr>
<tr><td rowspan="3">USART2 bootloader</td><td>USART2</td><td>Enabled</td><td>Once initialized, the USART2 configuration is: 8 bits, even parity and 1 Stop bit. The USART2 uses its remapped pins.</td></tr>
<tr><td>USART2_RX pin</td><td>Input</td><td>PD6 pin: USART2 in reception mode</td></tr>
<tr><td>USART2_TX pin</td><td>Output</td><td>PD5 pin: USART2 in transmission mode</td></tr>
<tr><td>USARTx bootloaders</td><td>SysTick timer</td><td>Enabled</td><td>Used to automatically detect the serial baud rate from the host for USARTx bootloader.</td></tr>
<tr><td rowspan="3">DFU bootloader</td><td>USB</td><td>Enabled</td><td>USB used in FS mode</td></tr>
<tr><td>USB_DM pin</td><td rowspan="2">Input/Output</td><td>PA11: USB DM line.</td></tr>
<tr><td>USB_DP pin</td><td>PA12: USB DP line
An external pull-up resistor 1.5 KOhm must be connected to USB_DP pin.</td></tr>
</table>

The system clock is derived from the embedded internal high-speed RC for USARTx bootloader. This internal clock is used also for DFU bootloader but only for the selection phase. An external clock in the range of [24, 16, 12, 8, 6, 4, 3, 2] MHz is required for DFU bootloader execution after the selection phase.

52.2 Bootloader selection

The figure below shows the bootloader selection mechanism.

Figure 67. Bootloader selection for STM32L1xxxD devices



52.3 Bootloader version

The following table lists the STM32L1xxxD devices bootloader versions:

Table 114. STM32L1xxxD bootloader versions

Bootloader version number	Description	Known limitations
V4.1	Initial bootloader version	– In the bootloader code the PA13 (JTMS/SWDIO) I/O output speed is configured to 400 KHz, as consequence some debugger can not connect to the device in Serial Wire mode when the bootloader is running. – When the DFU bootloader is selected, the RTC is reset and thus all RTC information (calendar, alarm, ...) will be lost including backup registers. **Note**: When the USART bootloader is selected there is no change on the RTC configuration (including backup registers).
V4.2	Fix V4.1 limitations (available on Rev.Z devices only.)	– Stack overflow by 8 bytes when jumping to Bank1/Bank2 if BFB2=0 or when Read Protection level is set to 2. Workaround: the user code should force in the startup file the top of stack address before to jump to the main program. This can be done in the “Reset_Handler” routine. – When the Stack of the user code is placed outside the SRAM (ie. @ 0x2000C000) the bootloader cannot jump to that user code which is considered invalid. This might happen when using compilers which place the stack at a non-physical address at the top of the SRAM (ie. @ 0x2000C000). Workaround: place manually the stack at a physical address.
V4.5	Fix V4.2 limitations. DFU interface robustness enhancements (available on Rev.Y devices only).	– For the USART interface, two consecutive NACKs (instead of 1 NACK) are sent when a Read Memory or Write Memory command is sent and the RDP level is active.

53 STM32L1xxxE devices bootloader

53.1 Bootloader configuration

The STM32L1xxxE bootloader is activated by applying pattern4 (described in *Table 2: Bootloader activation patterns*). The following table shows the hardware resources used by this bootloader.

Table 115. STM32L1xxxE configuration in system memory boot mode

Bootloader	Feature/Peripheral	State	Comment
Common to all bootloaders	RCC	HSI enabled	The system clock frequency is 16 MHz using the HSI. This is used only for USARTx bootloaders and during USB detection for DFU bootloader (once the DFU bootloader is selected, the clock source will be derived from the external crystal).
		HSE enabled	The external clock is mandatory only for DFU bootloader and it must be in the following range: [24, 16, 12, 8, 6, 4, 3, 2] MHz. The PLL is used to generate the USB 48 MHz clock and the 32 MHz clock for the system clock.
		-	The Clock Security System (CSS) interrupt is enabled for the DFU bootloader. Any failure (or removal) of the external clock generates system reset.
	RAM	-	4 Kbyte starting from address 0x20000000 are used by the bootloader firmware.
	System memory	-	8 Kbyte starting from address 0x1FF00000 contains the bootloader firmware.
	IWDG	-	The independent watchdog (IWDG) prescaler is configured to its maximum value and is periodically refreshed to prevent watchdog reset (in case the hardware IWDG option was previously enabled by the user).
	Power	-	Voltage range is set to Voltage Range 1.
USART1 bootloader	USART1	Enabled	Once initialized, the USART1 configuration is: 8 bits, even parity and 1 Stop bit.
	USART1_RX pin	Input	PA10 pin: USART1 in reception mode
	USART1_TX pin	Output	PA9 pin: USART1 in transmission mode

Table 115. STM32L1xxxE configuration in system memory boot mode (continued)

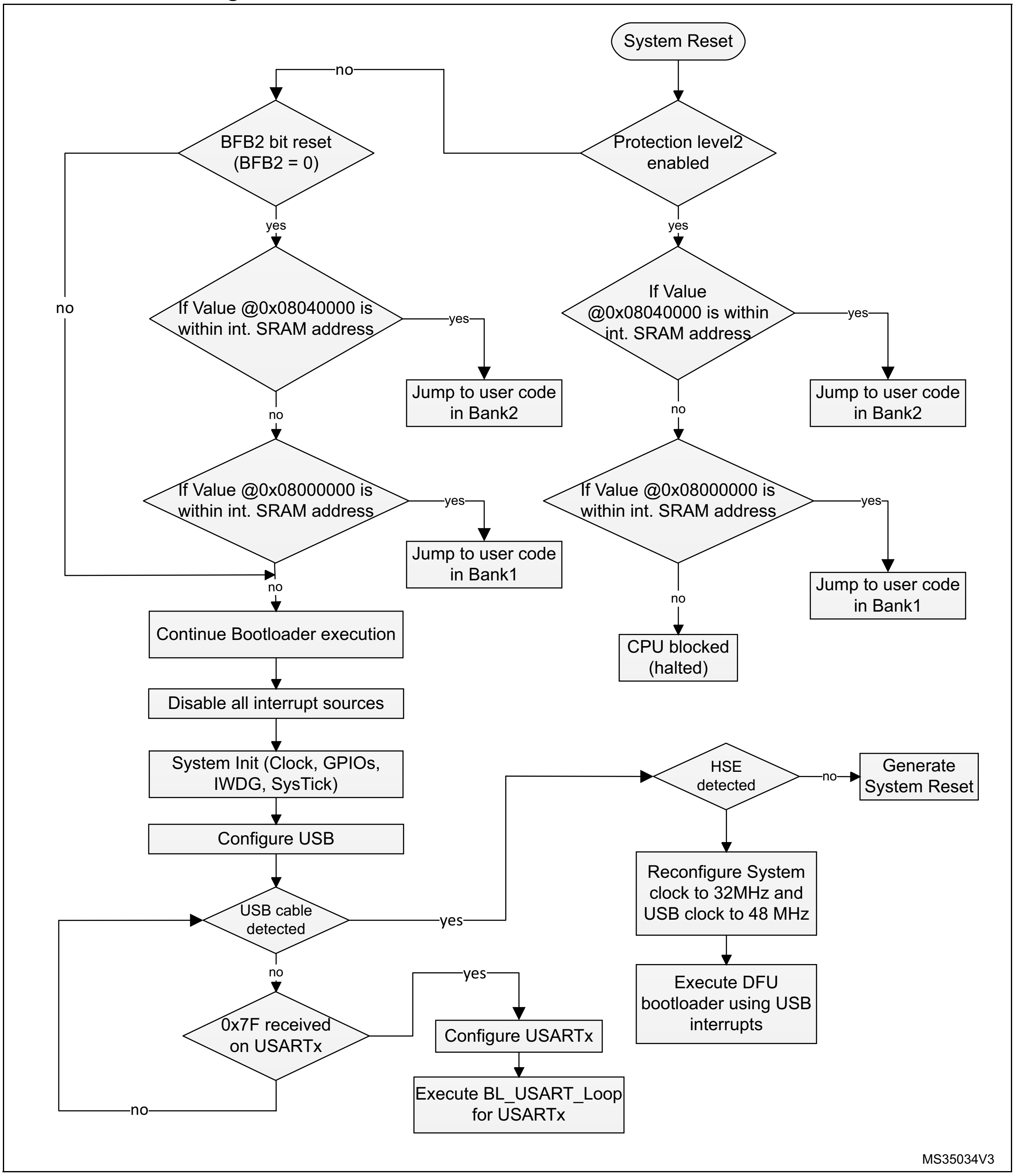
Bootloader	Feature/Peripheral	State	Comment
USART2 bootloader	USART2	Enabled	Once initialized, the USART2 configuration is: 8 bits, even parity and 1 Stop bit. The USART2 uses its remapped pins.
	USART2_RX pin	Input	PD6 pin: USART2 in reception mode
	USART2_TX pin	Output	PD5 pin: USART2 in transmission mode
USARTx bootloaders	SysTick timer	Enabled	Used to automatically detect the serial baud rate from the host for USARTx bootloader.
DFU bootloader	USB	Enabled	USB used in FS mode
	USB_DM pin	Input/Output	PA11: USB DM line.
	USB_DP pin		PA12: USB DP line An external pull-up resistor 1.5 KOhm must be connected to USB_DP pin.

The system clock is derived from the embedded internal high-speed RC for USARTx bootloader. This internal clock is used also for DFU bootloader but only for the selection phase. An external clock in the range of [24, 16, 12, 8, 6, 4, 3, 2] MHz is required for DFU bootloader execution after the selection phase.

53.2 Bootloader selection

The figure below shows the bootloader selection mechanism.

Figure 68. Bootloader selection for STM32L1xxxE devices



53.3 Bootloader version

The following table lists the STM32L1xxxE devices bootloader versions:

Table 116. STM32L1xxxE bootloader versions

Bootloader version number	Description	Known limitations
V4.0	Initial bootloader version	For the USART interface, two consecutive NACKs (instead of 1 NACK) are sent when a Read Memory or Write Memory command is sent and the RDP level is active.

54 STM32L412xx/422xx devices bootloader

54.1 Bootloader configuration

The STM32L412xx/422xx bootloader is activated by applying pattern6 (described in *Table 2: Bootloader activation patterns*). The following table shows the hardware resources used by this bootloader.

Table 117. STM32L412xx/422xx configuration in system memory boot mode

Bootloader	Feature/Peripheral	State	Comment
Common to all bootloaders	RCC	HSI enabled	The HSI is used at startup as clock source for system clock configured to 72 MHz and for USART, I2C, SPI and USB bootloader operation.
		-	The clock recovery system (CRS) is enabled for the DFU bootloader to allow USB to be clocked by HSI48 48 MHz.
	RAM	-	12 Kbyte starting from address 0x20000000 are used by the bootloader firmware
	System memory	-	28 Kbyte starting from address 0x1FFF0000, contain the bootloader firmware
	IWDG	-	The independent watchdog (IWDG) prescaler is configured to its maximum value. It is periodically refreshed to prevent watchdog reset (in case the hardware IWDG option was previously enabled by the user).
	Power	-	The DFU can’t be used to communicate with bootloader if the voltage scaling range 2 is selected. Bootloader firmware doesn’t configure voltage scaling range value in PWR_CR1 register.
USART1 bootloader	USART1	Enabled	Once initialized the USART1 configuration is: 8-bits, even parity and 1 Stop bit
	USART1_RX pin	Input	PA10 pin: USART1 in reception mode
	USART1_TX pin	Output	PA9 pin: USART1 in transmission mode
USART2 bootloader	USART2	Enabled	Once initialized the USART2 configuration is: 8-bits, even parity and 1 Stop bit
	USART2_RX pin	Input	PA3 pin: USART2 in reception mode
	USART2_TX pin	Output	PA2 pin: USART2 in transmission mode
USART3 bootloader	USART3	Enabled	Once initialized the USART3 configuration is: 8-bits, even parity and 1 Stop bit
	USART3_RX pin	Input	PC11 pin: USART3 in reception mode
	USART3_TX pin	Output	PC10 pin: USART3 in transmission mode
USARTx bootloaders	SysTick timer	Enabled	Used to automatically detect the serial baud rate from the host for USARTx bootloaders.

Table 117. STM32L412xx/422xx configuration in system memory boot mode (continued)

Bootloader	Feature/Peripheral	State	Comment
I2C1 bootloader	I2C1	Enabled	The I2C1 configuration is: I2C speed: up to 1 MHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b1010010x (where x = 0 for write and x = 1 for read)
	I2C1_SCL pin	Input/Output	PB6 pin: clock line is used in open-drain mode.
	I2C1_SDA pin	Input/Output	PB7 pin: data line is used in open-drain mode.
I2C2 bootloader	I2C2	Enabled	The I2C2 configuration is: I2C speed: up to 1 MHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b1010010x (where x = 0 for write and x = 1 for read)
	I2C2_SCL pin	Input/Output	PB10 pin: clock line is used in open-drain mode.
	I2C2_SDA pin	Input/Output	PB11 pin: data line is used in open-drain mode.
I2C3 bootloader	I2C3	Enabled	The I2C3 configuration is: I2C speed: up to 1 MHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b1010010x (where x = 0 for write and x = 1 for read)
	I2C3_SCL pin	Input/Output	PC0 pin: clock line is used in open-drain mode.
	I2C3_SDA pin	Input/Output	PC1 pin: data line is used in open-drain mode.
SPI1 bootloader	SPI1	Enabled	The SPI1 configuration is: – Slave mode – Full Duplex – 8-bit MSB – Speed up to 8 MHz – Polarity: CPOL Low, CPHA Low, NSS hardware.
	SPI1_MOSI pin	Input	PA7 pin: Slave data Input line, used in push-pull pull-down mode
	SPI1_MISO pin	Output	PA6 pin: Slave data output line, used in push-pull pull-down mode
	SPI1_SCK pin	Input	PA5 pin: Slave clock line, used in push-pull pull-down mode
	SPI1_NSS pin	Input	PA4 pin: slave chip select pin used in push-pull pull-up mode. **Note:** This IO can be tied to Gnd if the SPI Master does not use it.

Table 117. STM32L412xx/422xx configuration in system memory boot mode (continued)

Bootloader	Feature/Peripheral	State	Comment
SPI2 bootloader	SPI2	Enabled	The SPI2 configuration is: – Slave mode – Full Duplex – 8-bit MSB – Speed up to 8 MHz Polarity: CPOL Low, CPHA Low, NSS hardware
	SPI2_MOSI pin	Input	PB15 pin: Slave data Input line, used in push-pull pull-down mode
	SPI2_MISO pin	Output	PB14 pin: Slave data output line, used in push-pull pull-down mode
	SPI2_SCK pin	Input	PB13 pin: Slave clock line, used in push-pull pull-down mode
	SPI2_NSS pin	Input	PB12 pin: slave chip select pin used in push-pull pull-up mode. **Note:** This IO can be tied to Gnd if the SPI Master does not use it.
DFU bootloader	USB	Enabled	USB FS configured in forced device mode. USB FS interrupt vector is enabled and used for USB DFU communications. **Note:** VDDUSB IO must be connected to 3.3V for USB to be operational.
	USB_DM pin	Input/Output	PA11: USB DM line.
	USB_DP pin		PA12: USB DP line No external Pull-up resistor is required

54.2 Bootloader selection

The figures below show the bootloader selection mechanism.

Figure 69. Dual bank boot Implementation for STM32L412xx/422xx bootloader V9.x

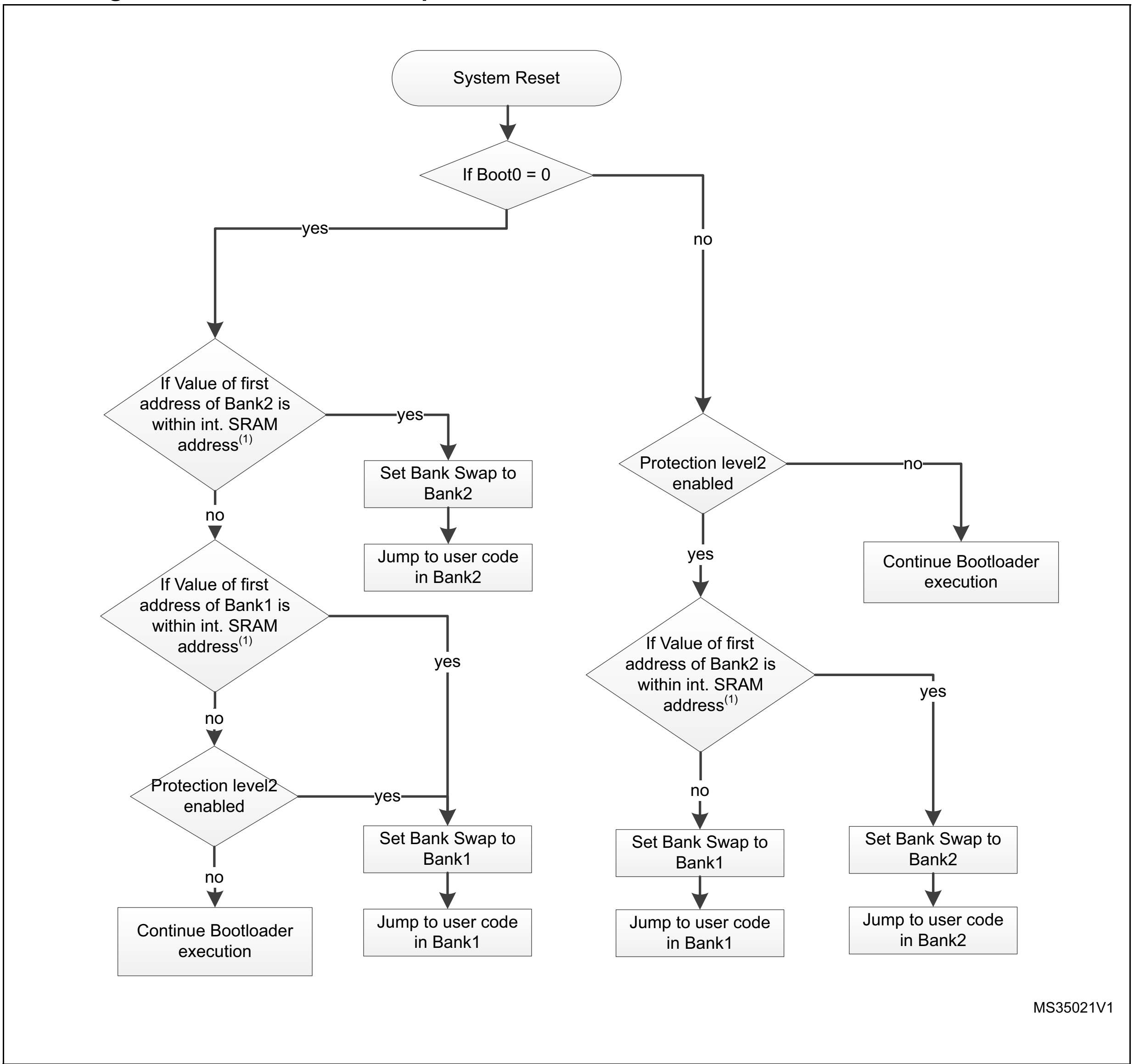
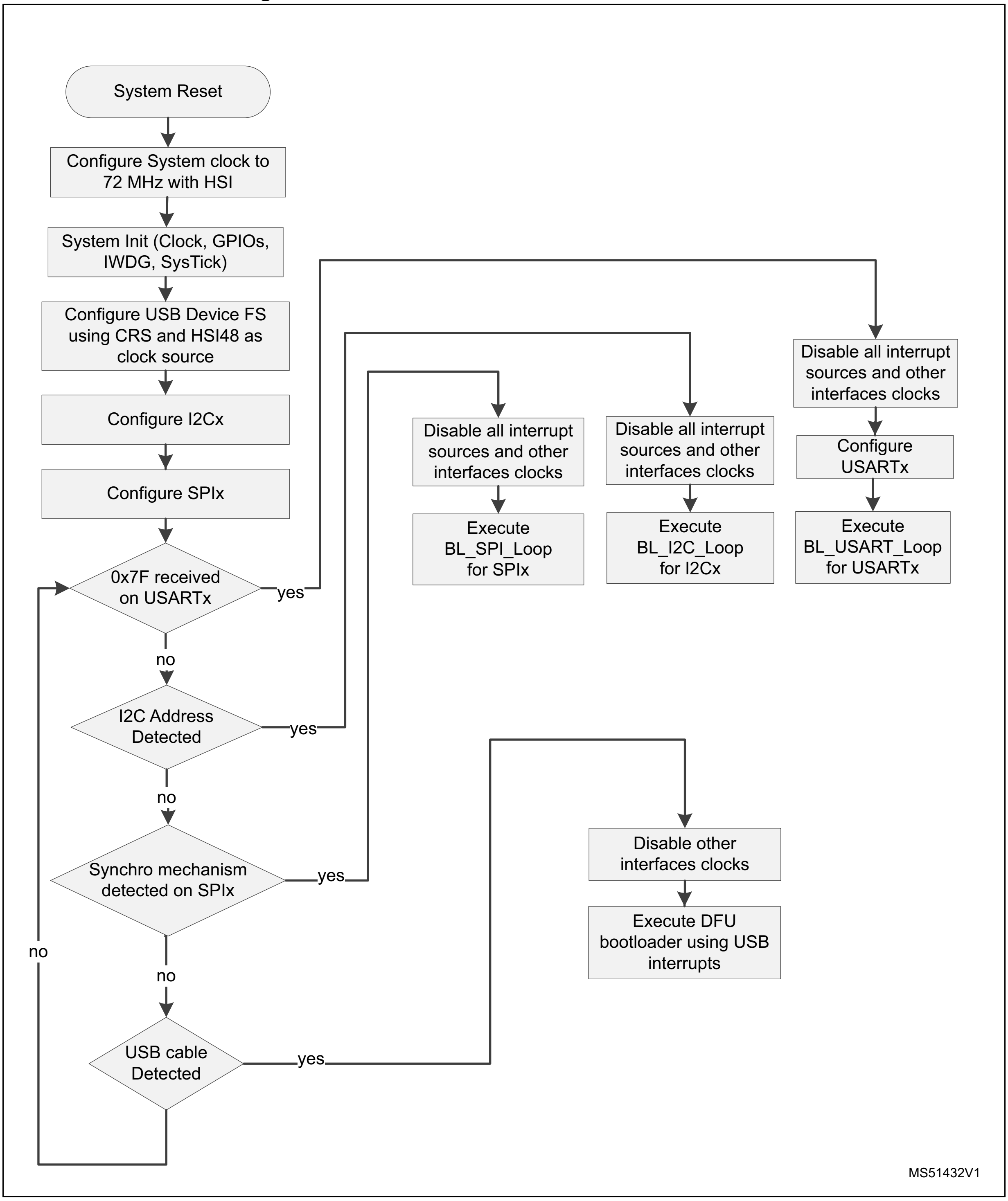


Figure 70.Bootloader V13.x selection for STM32L412xx/422xx



54.3 Bootloader version

The *Table 118* lists the STM32L412xx/422xx devices bootloader version.

Table 118. STM32L412xx/422xx bootloader versions

Bootloader version number	Description	Known limitations
V13.1	Initial bootloader version	– On connection phase, USART responds with two ACK bytes (0x79) instead of only one. – PcROP option bytes cannot be written as Bootloader uses Byte access while PcROP must be accessed using Half-Word access. **Workaround**: load a code snippest in SRAM using Bootloader interface then jump to it, and that code would write PcROP value.

55 STM32L43xxx/44xxx devices bootloader

55.1 Bootloader configuration

The bootloader V9.1 version is updated to fix known limitations relative to USB-DFU interface, and is implemented on devices with version information ID equal to 0x10 (refer to *Table 120* for more details).

The STM32L43xxx/44xxx bootloader is activated by applying pattern6 (described in *Table 2: Bootloader activation patterns*). The following table shows the hardware resources used by this bootloader.

Table 119. STM32L43xxx/44xxx configuration in system memory boot mode

Bootloader	Feature/Peripheral	State	Comment
Common to all bootloaders	RCC	HSI enabled	The HSI is used at startup as clock source for system clock configured to 60 MHz and for USART, I2C, SPI and USB bootloader operation.
		-	The clock recovery system (CRS) is enabled for the DFU bootloader to allow USB to be clocked by HSI48 48 MHz.
		HSE enabled	The HSE is used only when the CAN interface is selected. The HSE must have one of the following values [24,20,18,16,12,9,8,6,4] MHz.
		-	The Clock Security System (CSS) interrupt is enabled when HSE is enabled. Any failure (or removal) of the external clock generates system reset
	RAM	-	12 Kbyte starting from address 0x20000000 are used by the bootloader firmware
	System memory	-	28 Kbyte starting from address 0x1FFF0000, contain the bootloader firmware
	IWDG	-	The independent watchdog (IWDG) prescaler is configured to its maximum value. It is periodically refreshed to prevent watchdog reset (in case the hardware IWDG option was previously enabled by the user).
	Power	-	The DFU can't be used to communicate with bootloader if the voltage scaling range 2 is selected. Bootloader firmware doesn't configure voltage scaling range value in PWR_CR1 register.
USART1 bootloader	USART1	Enabled	Once initialized the USART1 configuration is: 8-bits, even parity and 1 Stop bit
	USART1_RX pin	Input	PA10 pin: USART1 in reception mode
	USART1_TX pin	Output	PA9 pin: USART1 in transmission mode

Table 119. STM32L43xxx/44xxx configuration in system memory boot mode (continued)

Bootloader	Feature/Peripheral	State	Comment
USART2 bootloader	USART2	Enabled	Once initialized the USART2 configuration is: 8-bits, even parity and 1 Stop bit
	USART2_RX pin	Input	PA3 pin: USART2 in reception mode
	USART2_TX pin	Output	PA2 pin: USART2 in transmission mode
USART3 bootloader	USART3	Enabled	Once initialized the USART3 configuration is: 8-bits, even parity and 1 Stop bit
	USART3_RX pin	Input	PC11 pin: USART3 in reception mode
	USART3_TX pin	Output	PC10 pin: USART3 in transmission mode
USARTx bootloaders	SysTick timer	Enabled	Used to automatically detect the serial baud rate from the host for USARTx bootloaders.
I2C1 bootloader	I2C1	Enabled	The I2C1 configuration is: I2C speed: up to 1 MHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b1001000x (where x = 0 for write and x = 1 for read)
	I2C1_SCL pin	Input/Output	PB6 pin: clock line is used in open-drain mode.
	I2C1_SDA pin	Input/Output	PB7 pin: data line is used in open-drain mode.
I2C2 bootloader	I2C2	Enabled	The I2C2 configuration is: I2C speed: up to 1 MHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b1001000x (where x = 0 for write and x = 1 for read)
	I2C2_SCL pin	Input/Output	PB10 pin: clock line is used in open-drain mode.
	I2C2_SDA pin	Input/Output	PB11 pin: data line is used in open-drain mode.
I2C3 bootloader	I2C3	Enabled	The I2C3 configuration is: I2C speed: up to 1 MHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b1001000x (where x = 0 for write and x = 1 for read)
	I2C3_SCL pin	Input/Output	PC0 pin: clock line is used in open-drain mode.
	I2C3_SDA pin	Input/Output	PC1 pin: data line is used in open-drain mode.

Table 119. STM32L43xxx/44xxx configuration in system memory boot mode (continued)

Bootloader	Feature/Peripheral	State	Comment
SPI1 bootloader	SPI1	Enabled	The SPI1 configuration is: – Slave mode – Full Duplex – 8-bit MSB – Speed up to 8 MHz – Polarity: CPOL Low, CPHA Low, NSS hardware.
	SPI1_MOSI pin	Input	PA7 pin: Slave data Input line, used in push-pull pull-down mode
	SPI1_MISO pin	Output	PA6 pin: Slave data output line, used in push-pull pull-down mode
	SPI1_SCK pin	Input	PA5 pin: Slave clock line, used in push-pull pull-down mode
	SPI1_NSS pin	Input	PA4 pin: slave chip select pin used in push-pull pull-down mode. **Note**: This IO can be tied to Gnd if the SPI Master does not use it.
SPI2 bootloader	SPI2	Enabled	The SPI2 configuration is: – Slave mode – Full Duplex – 8-bit MSB – Speed up to 8 MHz Polarity: CPOL Low, CPHA Low, NSS hardware
	SPI2_MOSI pin	Input	PB15 pin: Slave data Input line, used in push-pull pull-down mode
	SPI2_MISO pin	Output	PB14 pin: Slave data output line, used in push-pull pull-down mode
	SPI2_SCK pin	Input	PB13 pin: Slave clock line, used in push-pull pull-down mode
	SPI2_NSS pin	Input	PB12 pin: slave chip select pin used in push-pull pull-down mode. **Note:** This IO can be tied to Gnd if the SPI Master does not use it.
CAN1 bootloader	CAN1	Enabled	Once initialized the CAN1 configuration is: Baudrate 125 kbps, 11 -bit identifier.
	CAN1_RX pin	Input	PB8 pin: CAN1 in reception mode
	CAN1_TX pin	Output	PB9 pin: CAN1 in transmission mode
	TIM16	Enabled	This timer is used to determine the value of the HSE. Once the HSE frequency is determined, the system clock is configured to 60 MHz using PLL and HSE.

Table 119. STM32L43xxx/44xxx configuration in system memory boot mode (continued)

Bootloader	Feature/Peripheral	State	Comment
DFU bootloader	USB	Enabled	USB FS configured in forced device mode. USB FS interrupt vector is enabled and used for USB DFU communications. **Note:** VDDUSB IO must be connected to 3.3V for USB to be operational.
	USB_DM pin	Input/Output	PA11: USB DM line.
	USB_DP pin		PA12: USB DP line No external Pull-up resistor is required

55.2 Bootloader selection

The figures below show the bootloader selection mechanism.

Figure 71. Dual bank boot Implementation for STM32L3x2xx/44xxx bootloader V9.x

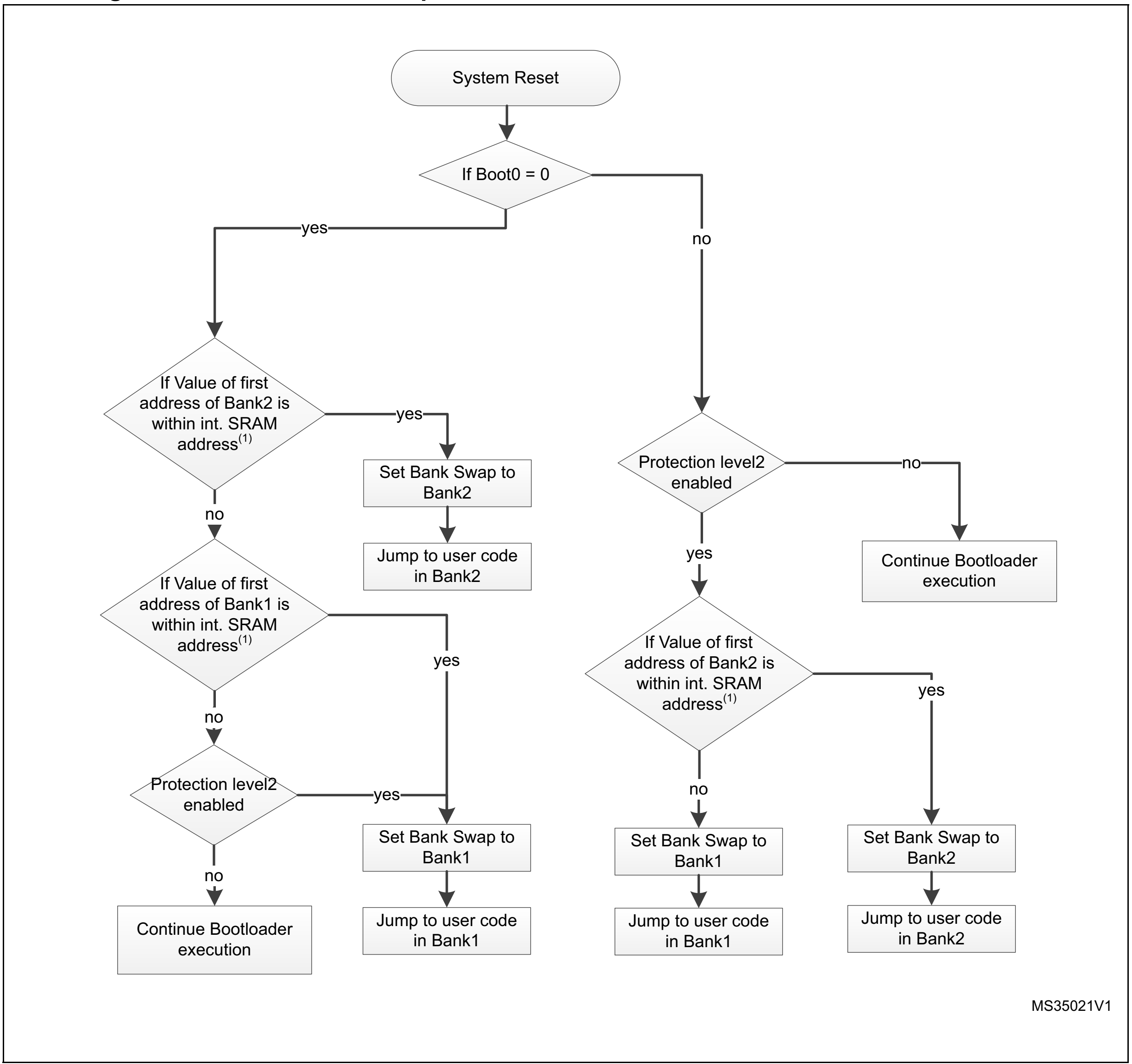
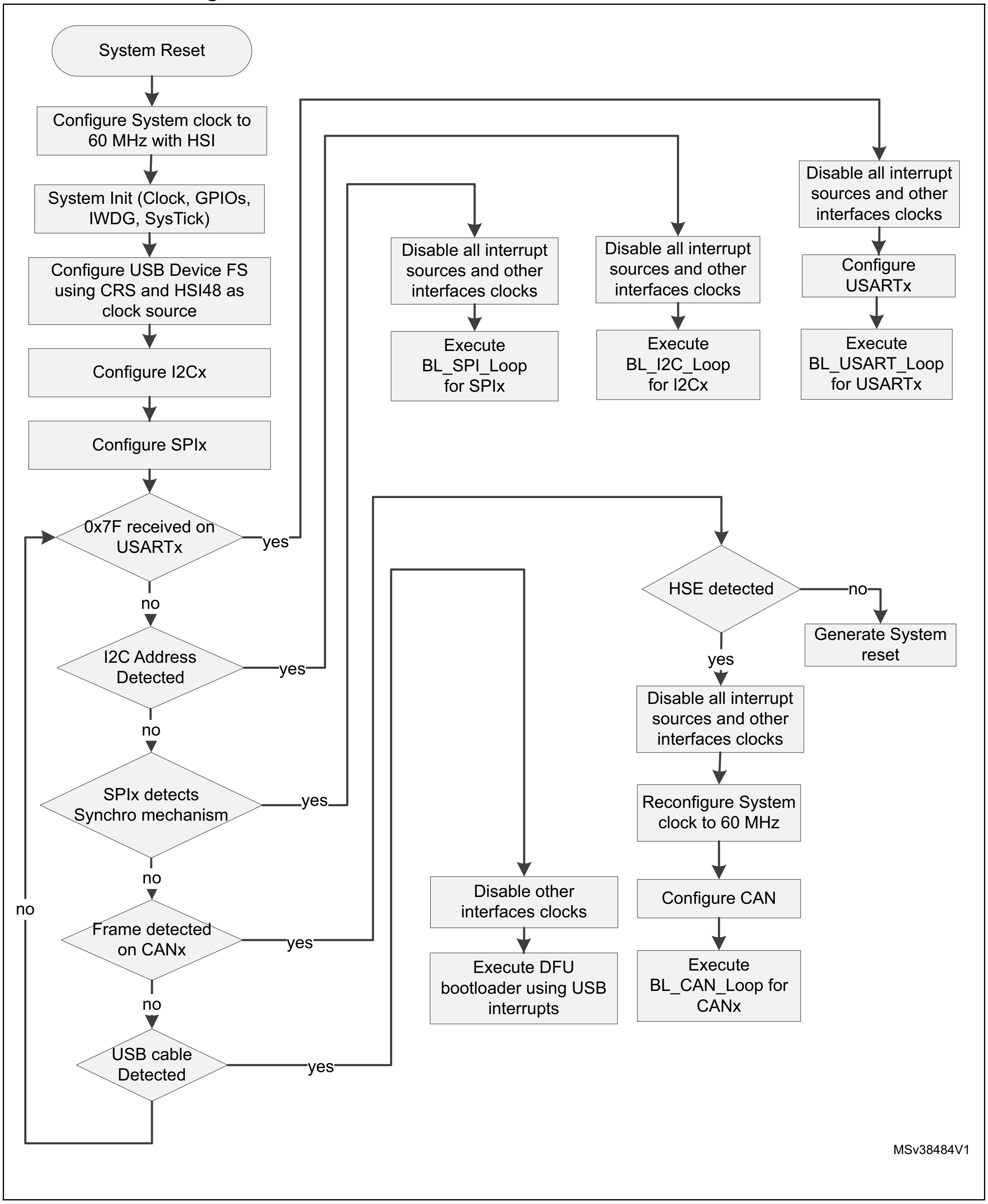


Figure 72. Bootloader V9.x selection for STM32L43xxx/44xxx



55.3 Bootloader version

The *Table 120* lists the STM32L43xxx/44xxx devices bootloader versions.

Table 120. STM32L43xxx/44xxx bootloader versions

Bootloader version number	Description	Known limitations
V9.1	Initial bootloader version	Check the Version Information ID of your STM32L43xxx/44xxx device, which can be read at 0x1FFF6FF2 address. **Version Information ID equal to 0xFF**: – For memory write operations using DFU interface: If the buffer size is larger than 256 bytes and not multiple of 8 bytes, the write memory operation result is corrupted. Workaround: if the file size is larger than 256 bytes, add byte padding to align it on 8-bytes multiple size. – For the USB-DFU interface, the CRS (clock recovery system) is not correctly configured and this may lead to random USB communication errors (depending on temperature and voltage). In most case communication error will manifest by a "Stall" response to setup packets. – On the “Go” command, system bootloader de-init clears the RTCAPBEN bit in the RCC_APB1ENR register Workaround: manually call __HAL_RCC_RTC_CLK_ENABLE() in the software which sets the RTCAPBEN bit. **Version Information ID equal to 0x10**: None – PcROP option bytes cannot be written as Bootloader uses Byte access while PcROP must be accessed using Half-Word access. **Workaround**: load a code snippiest in SRAM using Bootloader interface then jump to it, and that code would write PcROP value.

56 STM32L45xxx/46xxx devices bootloader

56.1 Bootloader configuration

The STM32L45xxx/46xxx bootloader is activated by applying pattern6 (described in *Table 2: Bootloader activation patterns*). The following table shows the hardware resources used by this bootloader.

Table 121. STM32L45xxx/46xxx configuration in system memory boot mode

Bootloader	Feature/Peripheral	State	Comment
Common to all bootloaders	RCC	HSI enabled	The HSI is used at startup as clock source for system clock configured to 72 MHz and for USART, I2C, SPI and USB bootloader operation.
		-	The clock recovery system (CRS) is enabled for the DFU bootloader to allow USB to be clocked by HSI48 48 MHz.
		HSE enabled	The system clock frequency is 60 MHz. The HSE is used only when the CAN interface is selected . The HSE must have one of the following values [24,20,18,16,12,9,8,6,4] MHz.
		-	The Clock Security System (CSS) interrupt is enabled when HSE is enabled. Any failure (or removal) of the external clock generates system reset
	RAM	-	12 Kbyte starting from address 0x20000000 are used by the bootloader firmware
	System memory	-	28 Kbyte starting from address 0x1FFF0000, contain the bootloader firmware
	IWDG	-	The independent watchdog (IWDG) prescaler is configured to its maximum value. It is periodically refreshed to prevent watchdog reset (in case the hardware IWDG option was previously enabled by the user).
	Power	-	The DFU can't be used to communicate with bootloader if the voltage scaling range 2 is selected. Bootloader firmware doesn't configure voltage scaling range value in PWR_CR1 register.
USART1 bootloader	USART1	Enabled	Once initialized the USART1 configuration is: 8-bits, even parity and 1 Stop bit
	USART1_RX pin	Input	PA10 pin: USART1 in reception mode
	USART1_TX pin	Output	PA9 pin: USART1 in transmission mode

Table 121. STM32L45xxx/46xxx configuration in system memory boot mode (continued)

Bootloader	Feature/Peripheral	State	Comment
USART2 bootloader	USART2	Enabled	Once initialized the USART2 configuration is: 8-bits, even parity and 1 Stop bit
	USART2_RX pin	Input	PA3 pin: USART2 in reception mode
	USART2_TX pin	Output	PA2 pin: USART2 in transmission mode
USART3 bootloader	USART3	Enabled	Once initialized the USART3 configuration is: 8-bits, even parity and 1 Stop bit
	USART3_RX pin	Input	PC11 pin: USART3 in reception mode
	USART3_TX pin	Output	PC10 pin: USART3 in transmission mode
USARTx bootloaders	SysTick timer	Enabled	Used to automatically detect the serial baud rate from the host for USARTx bootloaders.
I2C1 bootloader	I2C1	Enabled	The I2C1 configuration is: I2C speed: up to 1 MHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b1001010x (where x = 0 for write and x = 1 for read)
	I2C1_SCL pin	Input/Output	PB6 pin: clock line is used in open-drain mode.
	I2C1_SDA pin	Input/Output	PB7 pin: data line is used in open-drain mode.
I2C2 bootloader	I2C2	Enabled	The I2C2 configuration is: I2C speed: up to 1 MHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b1001010x (where x = 0 for write and x = 1 for read)
	I2C2_SCL pin	Input/Output	PB10 pin: clock line is used in open-drain mode.
	I2C2_SDA pin	Input/Output	PB11 pin: data line is used in open-drain mode.
I2C3 bootloader	I2C3	Enabled	The I2C3 configuration is: I2C speed: up to 1 MHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b1001010x (where x = 0 for write and x = 1 for read)
	I2C3_SCL pin	Input/Output	PC0 pin: clock line is used in open-drain mode.
	I2C3_SDA pin	Input/Output	PC1 pin: data line is used in open-drain mode.

Table 121. STM32L45xxx/46xxx configuration in system memory boot mode (continued)

Bootloader	Feature/Peripheral	State	Comment
SPI1 bootloader	SPI1	Enabled	The SPI1 configuration is: – Slave mode – Full Duplex – 8-bit MSB – Speed up to 8 MHz – Polarity: CPOL Low, CPHA Low, NSS hardware.
	SPI1_MOSI pin	Input	PA7 pin: Slave data Input line, used in push-pull pull-down mode
	SPI1_MISO pin	Output	PA6 pin: Slave data output line, used in push-pull pull-down mode
	SPI1_SCK pin	Input	PA5 pin: Slave clock line, used in push-pull pull-down mode
	SPI1_NSS pin	Input	PA4 pin: slave chip select pin used in push-pull pull-down mode. **Note**: This IO can be tied to Gnd if the SPI Master does not use it.
SPI2 bootloader	SPI2	Enabled	The SPI2 configuration is: – Slave mode – Full Duplex – 8-bit MSB – Speed up to 8 MHz – Polarity: CPOL Low, CPHA Low, NSS hardware.
	SPI2_MOSI pin	Input	PB15 pin: Slave data Input line, used in push-pull pull-down mode
	SPI2_MISO pin	Output	PB14 pin: Slave data output line, used in push-pull pull-down mode
	SPI2_SCK pin	Input	PB13 pin: Slave clock line, used in push-pull pull-down mode
	SPI2_NSS pin	Input	PB12 pin: slave chip select pin used in push-pull pull-down mode. **Note**: This IO can be tied to Gnd if the SPI Master does not use it.
CAN1 bootloader	CAN1	Enabled	Once initialized the CAN1 configuration is: Baudrate 125 kbps, 11 -bit identifier.
	CAN1_RX pin	Input	PB8 pin: CAN1 in reception mode
	CAN1_TX pin	Output	PB9 pin: CAN1 in transmission mode
	TIM16	Enabled	This timer is used to determine the value of the HSE. Once the HSE frequency is determined, the system clock is configured to 60 MHz using PLL and HSE.

Table 121. STM32L45xxx/46xxx configuration in system memory boot mode (continued)

Bootloader	Feature/Peripheral	State	Comment
DFU bootloader	USB	Enabled	USB FS configured in forced device mode. USB FS interrupt vector is enabled and used for USB DFU communications. **Note:** VDDUSB IO must be connected to 3.3V for USB to be operational.
	USB_DM pin	Input/Output	PA11: USB DM line.
	USB_DP pin		PA12: USB DP line No external Pull-up resistor is required

56.2 Bootloader selection

The figures below show the bootloader selection mechanism.

Figure 73. Dual bank boot Implementation for STM32L45xxx/46xxx bootloader V9.x

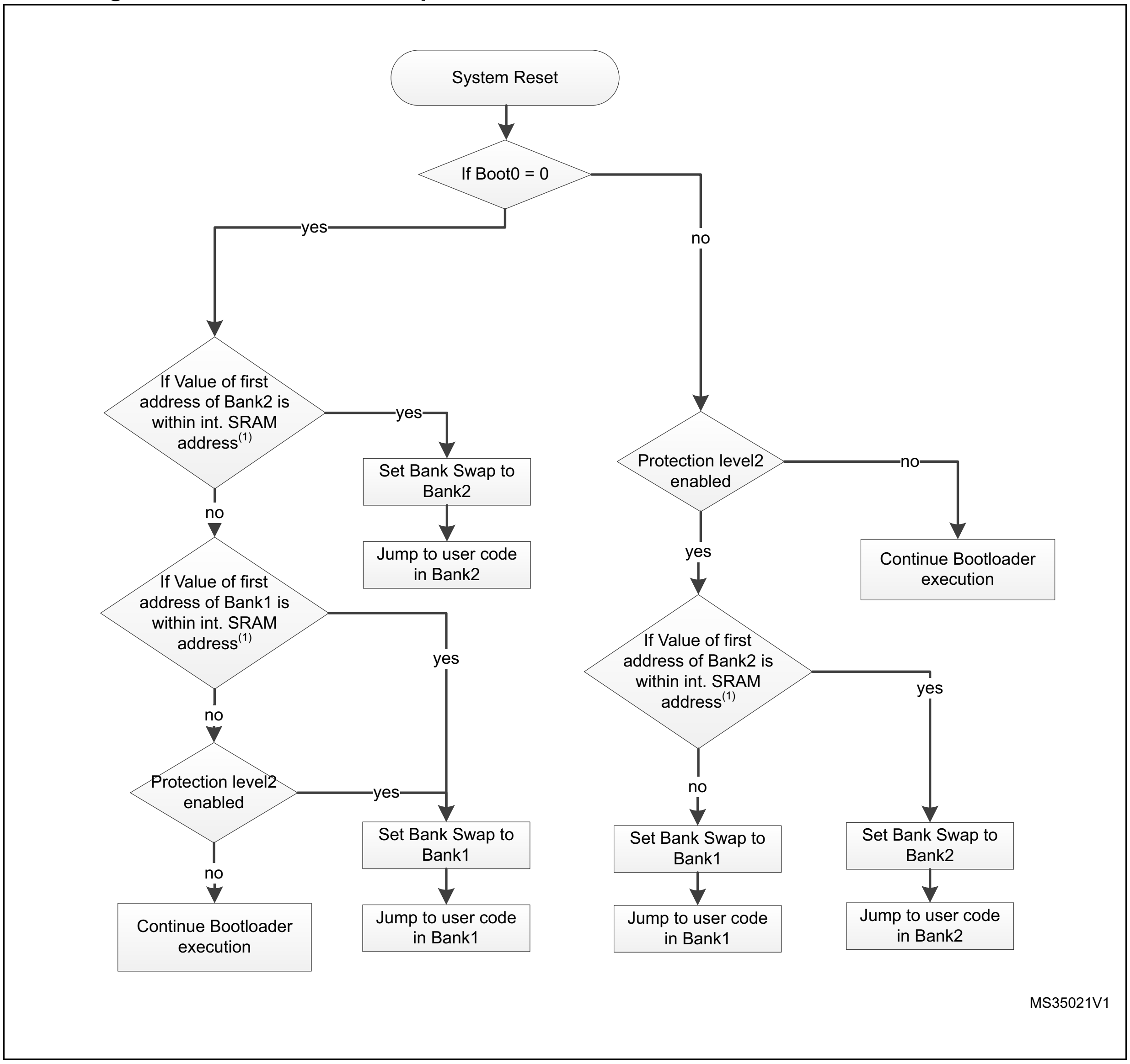
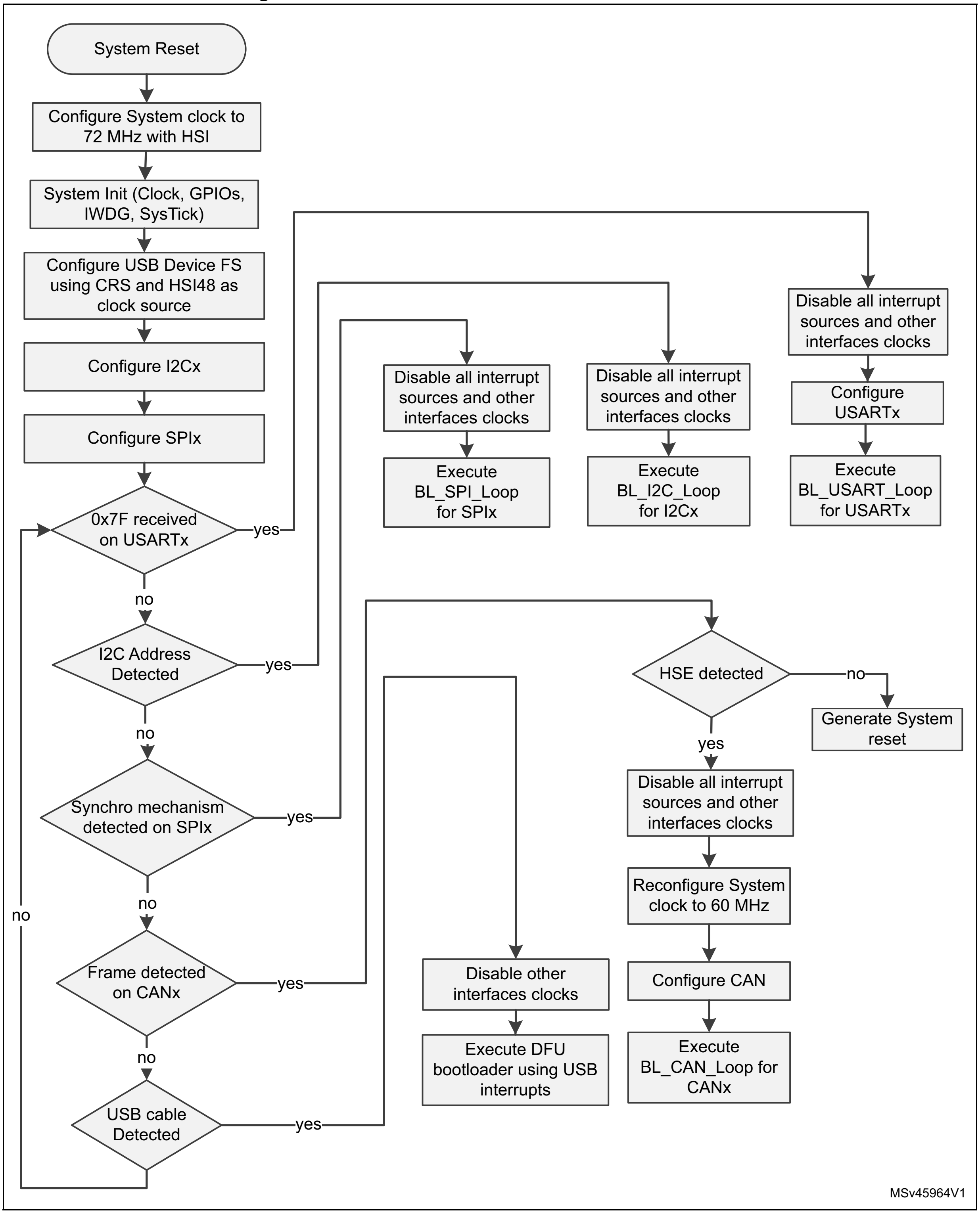


Figure 74.Bootloader V9.x selection for STM32L45xxx/46xxx



56.3 Bootloader version

Table 122 lists the STM32L45xxx/46xxx devices bootloader versions.

Table 122. STM32L45xxx/46xxx bootloader versions

Bootloader version number	Description	Known limitations
V9.2	Initial bootloader version	– PcROP option bytes cannot be written as Bootloader uses Byte access while PcROP must be accessed using Half-Word access. **Workaround**: load a code snippiest in SRAM using Bootloader interface then jump to it, and that code would write PcROP value.

57 STM32L47xxx/48xxx devices bootloader

Two bootloader versions are available on STM32L47xxx/48xxx:

- V10.x supporting USART, I2C and DFU (USB FS Device).
  This version is embedded in STM32L47xxx/48xxx rev. 2 and rev. 3 devices.
- V9.x supporting USART, I2C, SPI, CAN and DFU (USB FS Device).
  This version is embedded in STM32L47xxx/48xxx rev. 4 devices.

57.1 Bootloader V10.x

57.1.1 Bootloader configuration

The STM32L47xxx/48xxx bootloader is activated by applying pattern7 (described in *Table 2: Bootloader activation patterns*). The following table shows the hardware resources used by this bootloader.

Table 123. STM32L47xxx/48xxx configuration in system memory boot mode

Bootloader	Feature/Peripheral	State	Comment
Common to all bootloaders	RCC	HSI enabled	The HSI is used at startup as clock source for system clock configured to 24 MHz and for USART and I2C bootloader operation.
		HSE enabled	The HSE is used only when the USB interface is selected and the LSE is not present. The HSE must have one of the following values [24,20,18,16,12,9,8,6,4] MHz.
		LSE enabled	The LSE is used to trim the MSI which is configured to 48 MHz as USB clock source. The LSE must be equal to 32,768 KHz. If the LSE is not detected, the HSE will be used instead if USB is connected.
		MSI enabled	The MSI is configured to 48 MHz and will be used as USB clock source. The MSI is used only if LSE is detected, otherwise, HSE will be used if USB is connected.
		-	The Clock Security System (CSS) interrupt is enabled when LSE or HSE is enabled. Any failure (or removal) of the external clock generates system reset.
	RAM	-	12 Kbyte starting from address 0x20000000 are used by the bootloader firmware
	System memory	-	28 Kbyte starting from address 0x1FFF0000, contain the bootloader firmware
	IWDG	-	The independent watchdog (IWDG) prescaler is configured to its maximum value. It is periodically refreshed to prevent watchdog reset (in case the hardware IWDG option was previously enabled by the user).
	Power	-	The DFU can't be used to communicate with bootloader if the voltage scaling range 2 is selected. Bootloader firmware doesn't configure voltage scaling range value in PWR_CR1 register.

Table 123. STM32L47xxx/48xxx configuration in system memory boot mode (continued)

Bootloader	Feature/Peripheral	State	Comment
USART1 bootloader	USART1	Enabled	Once initialized the USART1 configuration is: 8-bits, even parity and 1 Stop bit
	USART1_RX pin	Input	PA10 pin: USART1 in reception mode
	USART1_TX pin	Output	PA9 pin: USART1 in transmission mode
USART2 bootloader	USART2	Enabled	Once initialized the USART2 configuration is: 8-bits, even parity and 1 Stop bit
	USART2_RX pin	Input	PA3 pin: USART2 in reception mode
	USART2_TX pin	Output	PA2 pin: USART2 in transmission mode
USART3 bootloader	USART3	Enabled	Once initialized the USART3 configuration is: 8-bits, even parity and 1 Stop bit
	USART3_RX pin	Input	PC11 pin: USART3 in reception mode
	USART3_TX pin	Output	PC10 pin: USART3 in transmission mode
USARTx bootloaders	SysTick timer	Enabled	Used to automatically detect the serial baud rate from the host for USARTx bootloaders.
I2C1 bootloader	I2C1	Enabled	The I2C1 configuration is: I2C speed: up to 400 KHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b1000011x (where x = 0 for write and x = 1 for read)
	I2C1_SCL pin	Input/Output	PB6 pin: clock line is used in open-drain mode.
	I2C1_SDA pin	Input/Output	PB7 pin: data line is used in open-drain mode.
I2C2 bootloader	I2C2	Enabled	The I2C2 configuration is: I2C speed: up to 400 KHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b1000011x (where x = 0 for write and x = 1 for read)
	I2C2_SCL pin	Input/Output	PB10 pin: clock line is used in open-drain mode.
	I2C2_SDA pin	Input/Output	PB11 pin: data line is used in open-drain mode.
I2C3 bootloader	I2C3	Enabled	The I2C3 configuration is: I2C speed: up to 400 KHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address is 0b1000011x (where x = 0 for write and x = 1 for read)
	I2C3_SCL pin	Input/Output	PC0 pin: clock line is used in open-drain mode.
	I2C3_SDA pin	Input/Output	PC1 pin: data line is used in open-drain mode.
DFU bootloader	USB	Enabled	USB OTG FS configured in forced device mode
	USB_DM pin	Input/Output	PA11: USB DM line.
	USB_DP pin		PA12: USB DP line No external Pull-up resistor is required
	TIM17	Enabled	This timer is used to determine the value of the HSE. Once the HSE frequency is determined, the system clock is configured to 24 MHz using PLL and HSE.

For USARTx and I2Cx bootloaders no external clock is required.

USB bootloader (DFU) requires either an LSE (low-speed external clock) or a HSE (high-speed external clock) :

- In case, the LSE is present regardless the HSE presence, the MSI will be configured and trimmed by the LSE to provide an accurate clock equal to 48 MHz which is the clock source of the USB. The system clock is kept clocked to 24 MHz by the HSI.
- In case, the HSE is present, the system clock and USB clock will be configured respectively to 24 MHz and 48 MHz with HSE as clock source.

57.1.2 Bootloader selection

The *Figure 75* and *Figure 76* show the bootloader selection mechanism.

Figure 75. Dual Bank Boot Implementation for STM32L47xxx/48xxx bootloader V10.x

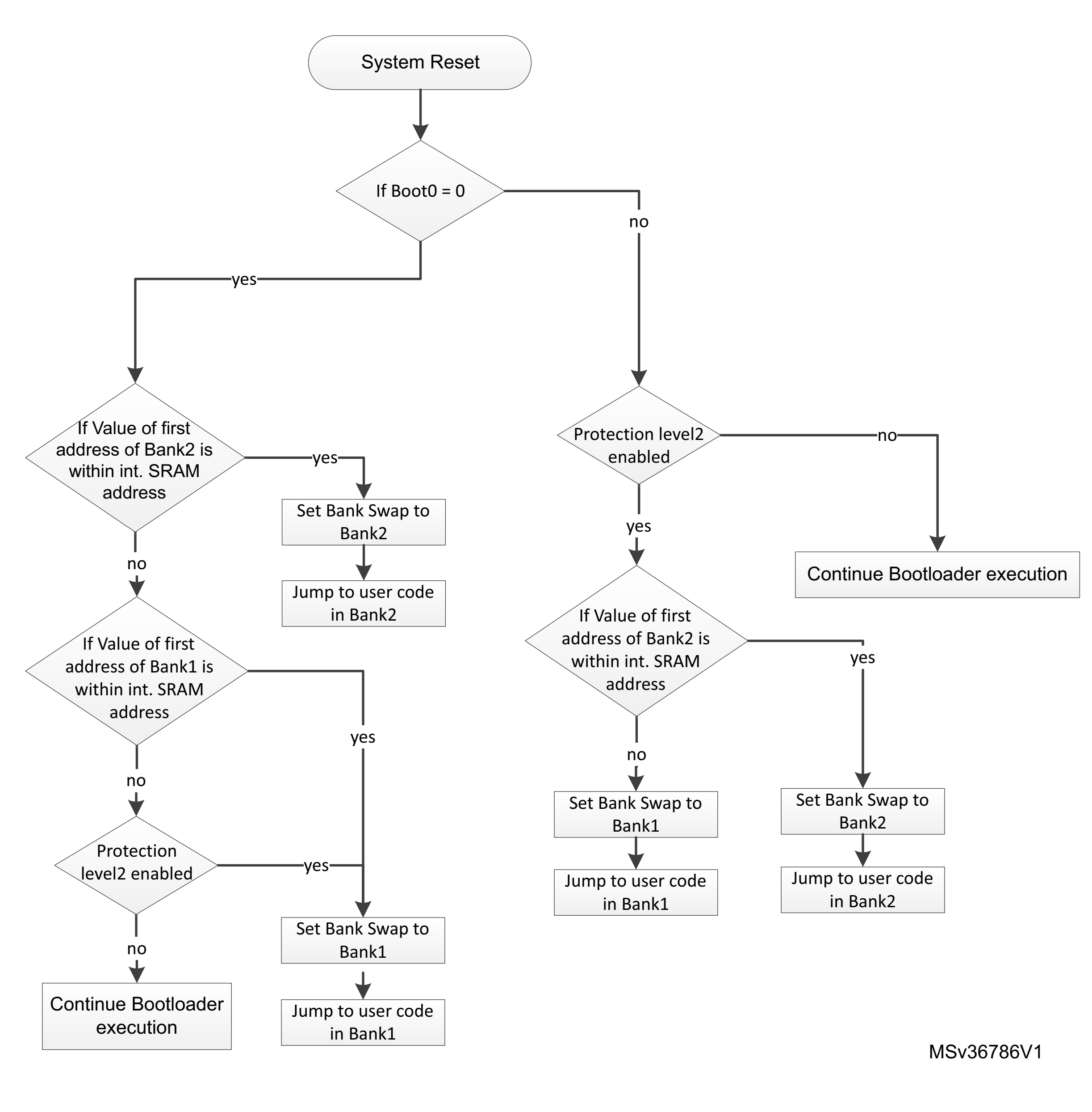
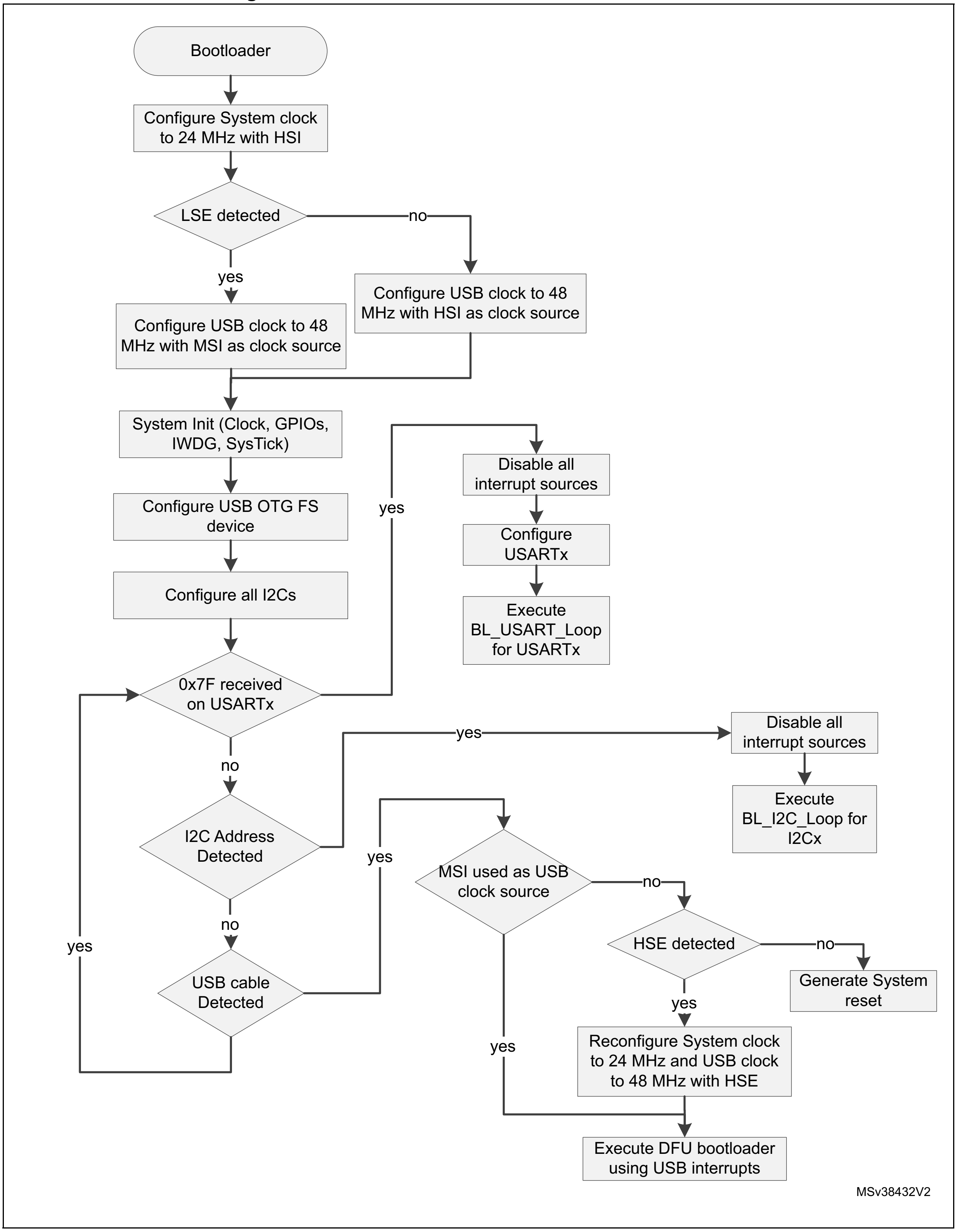


Figure 76.Bootloader V10.x selection for STM32L47xxx/48xxx



57.1.3 Bootloader version

The following table lists the STM32L47xxx/48xxx devices bootloader V10.x versions:

Table 124. STM32L47xxx/48xxx bootloader V10.x versions

Bootloader version number	Description	Known limitations
V10.1	Initial bootloader version	For memory write operations using DFU interface: If the buffer size is larger than 256 bytes and not multiple of 8 bytes, the write memory operation result is corrupted. Workaround: if the file size is larger than 256 bytes, add byte padding to align it on 8-bytes multiple size. Write in SRAM is corrupted.
V10.2	Fix write in SRAM issue	For memory write operations using DFU interface: If the buffer size is larger than 256 bytes and not multiple of 8 bytes, the write memory operation result is corrupted. Workaround: if the file size is larger than 256 bytes, add byte padding to align it on 8-bytes multiple size.
V10.3	Add support of MSI as USB clock source (MSI is trimmed by LSE). Update dual bank boot feature to support the case when user stack is mapped in SRAM2.	– For memory write operations using DFU interface: If the buffer size is larger than 256 bytes and not multiple of 8 bytes, the write memory operation result is corrupted. Workaround: if the file size is larger than 256 bytes, add byte padding to align it on 8-bytes multiple size. – PcROP option bytes cannot be written as Bootloader uses Byte access while PcROP must be accessed using Half-Word access. **Workaround**: load a code snippiest in SRAM using Bootloader interface then jump to it, and that code would write PcROP value.

57.2 Bootloader V9.x

57.2.1 Bootloader configuration

The STM32L47xxx/48xxx bootloader is activated by applying pattern7 (described in *Table 2: Bootloader activation patterns*). The following table shows the hardware resources used by this bootloader.

Table 125. STM32L47xxx/48xxx configuration in system memory boot mode

Bootloader	Feature/Peripheral	State	Comment
Common to all bootloaders	RCC	HSI enabled	The HSI is used at startup as clock source for system clock configured to 72 MHz and for USART and I2C bootloader operation.
		HSE enabled	The HSE is used only when the USB interface is selected and the LSE is not present. The HSE must have one of the following values [24,20,18,16,12,8,6,4] MHz. System is clocked at 72 MHz if USB is used or 60 MHz if CAN is used.
		LSE enabled	The LSE is used to trim the MSI which is configured to 48 MHz as USB clock source. The LSE must be equal to 32,768 KHz. If the LSE is not detected, the HSE will be used instead if USB is connected.
		MSI enabled	The MSI is configured to 48 MHz and will be used as USB clock source. The MSI is used only if LSE is detected, otherwise, HSE will be used if USB is connected.
		CSS	The Clock Security System (CSS) interrupt is enabled when LSE or HSE is enabled. Any failure (or removal) of the external clock generates system reset.
	RAM	-	13 Kbyte starting from address 0x20000000 are used by the bootloader firmware
	System memory	-	28 Kbyte starting from address 0x1FFF0000, contain the bootloader firmware
	IWDG	-	The independent watchdog (IWDG) prescaler is configured to its maximum value. It is periodically refreshed to prevent watchdog reset (in case the hardware IWDG option was previously enabled by the user).
	Power	-	The DFU can’t be used to communicate with bootloader if the voltage scaling range 2 is selected. Bootloader firmware doesn’t configure voltage scaling range value in PWR_CR1 register.
USART1 bootloader	USART1	Enabled	Once initialized the USART1 configuration is: 8-bits, even parity and 1 Stop bit
	USART1_RX pin	Input	PA10 pin: USART2 in reception mode
	USART1_TX pin	Output	PA9 pin: USART2 in transmission mode

Table 125. STM32L47xxx/48xxx configuration in system memory boot mode (continued)

Bootloader	Feature/Peripheral	State	Comment
USART2 bootloader	USART2	Enabled	Once initialized the USART2 configuration is: 8-bits, even parity and 1 Stop bit
	USART2_RX pin	Input	PA3 pin: USART2 in reception mode
	USART2_TX pin	Output	PA2 pin: USART2 in transmission mode
USART3 bootloader	USART3	Enabled	Once initialized the USART3 configuration is: 8-bits, even parity and 1 Stop bit
	USART3_RX pin	Input	PC11 pin: USART3 in reception mode
	USART3_TX pin	Output	PC10 pin: USART3 in transmission mode
USARTx bootloaders	SysTick timer	Enabled	Used to automatically detect the serial baud rate from the host for USARTx bootloaders.
I2C1 bootloader	I2C1	Enabled	The I2C1 configuration is: I2C speed: up to 400 KHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b1000011x (where x = 0 for write and x = 1 for read)
	I2C1_SCL pin	Input/Output	PB6 pin: clock line is used in open-drain mode.
	I2C1_SDA pin	Input/Output	PB7 pin: data line is used in open-drain mode.
I2C2 bootloader	I2C2	Enabled	The I2C2 configuration is: I2C speed: up to 400 KHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b1000011x (where x = 0 for write and x = 1 for read)
	I2C2_SCL pin	Input/Output	PB10 pin: clock line is used in open-drain mode.
	I2C2_SDA pin	Input/Output	PB11 pin: data line is used in open-drain mode.
I2C3 bootloader	I2C3	Enabled	The I2C3 configuration is: I2C speed: up to 400 KHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b1000011x (where x = 0 for write and x = 1 for read)
	I2C3_SCL pin	Input/Output	PC0 pin: clock line is used in open-drain mode.
	I2C3_SDA pin	Input/Output	PC1 pin: data line is used in open-drain mode.
SPI1 bootloader	SPI1	Enabled	The SPI1 configuration is: Slave mode, Full Duplex, 8-bit MSB, Speed up to 8 MHz, Polarity: CPOL Low, CPHA Low, NSS hardware.
	SPI1_MOSI pin	Input	PA7 pin: Slave data Input line, used in push-pull pull-down mode
	SPI1_MISO pin	Output	PA6 pin: Slave data output line, used in push-pull pull-down mode
	SPI1_SCK pin	Input	PA5 pin: Slave clock line, used in push-pull pull-down mode
	SPI1_NSS pin	Input	PA4 pin: slave chip select pin used in push-pull pull-down mode.

Table 125. STM32L47xxx/48xxx configuration in system memory boot mode (continued)

Bootloader	Feature/Peripheral	State	Comment
SPI2 bootloader	SPI2	Enabled	The SPI2 configuration is: Slave mode, Full Duplex, 8-bit MSB, Speed up to 8 MHz, Polarity: CPOL Low, CPHA Low, NSS hardware
	SPI2_MOSI pin	Input	PB15 pin: Slave data Input line, used in push-pull pull-down mode
	SPI2_MISO pin	Output	PB14 pin: Slave data output line, used in push-pull pull-down mode
	SPI2_SCK pin	Input	PB13 pin: Slave clock line, used in push-pull pull-down mode
	SPI2_NSS pin	Input	PB12 pin: slave chip select pin used in push-pull pull-down mode.
CAN1 bootloader	CAN1	Enabled	Once initialized the CAN1 configuration is: Baudrate 125 kbps, 11-bit identifier.
	CAN1_RX pin	Input	PB8 pin: CAN1 in reception mode
	CAN1_TX pin	Output	PB9 pin: CAN1 in transmission mode
DFU bootloader	USB	Enabled	USB FS configured in forced device mode. USB FS interrupt vector is enabled and used for USB DFU communications. **Note**: VDDUSB IO must be connected to 3.3V for USB to be operational.
	USB_DM pin	Input/Output	PA11 pin: USB FS DM line
	USB_DP pin		PA12 pin: USB FS DP line. No external Pull-up resistor is required.

In case, the HSE is present, the system clock and USB clock will be configured respectively to 72 MHz and 48 MHz with PLL (clocked by HSE) as a clock source.

57.2.2 Bootloader selection

The *Figure 77* and *Figure 78* show the bootloader selection mechanism.

Figure 77. Dual Bank Boot Implementation for STM32L47xxx/48xxx bootloader V9.x

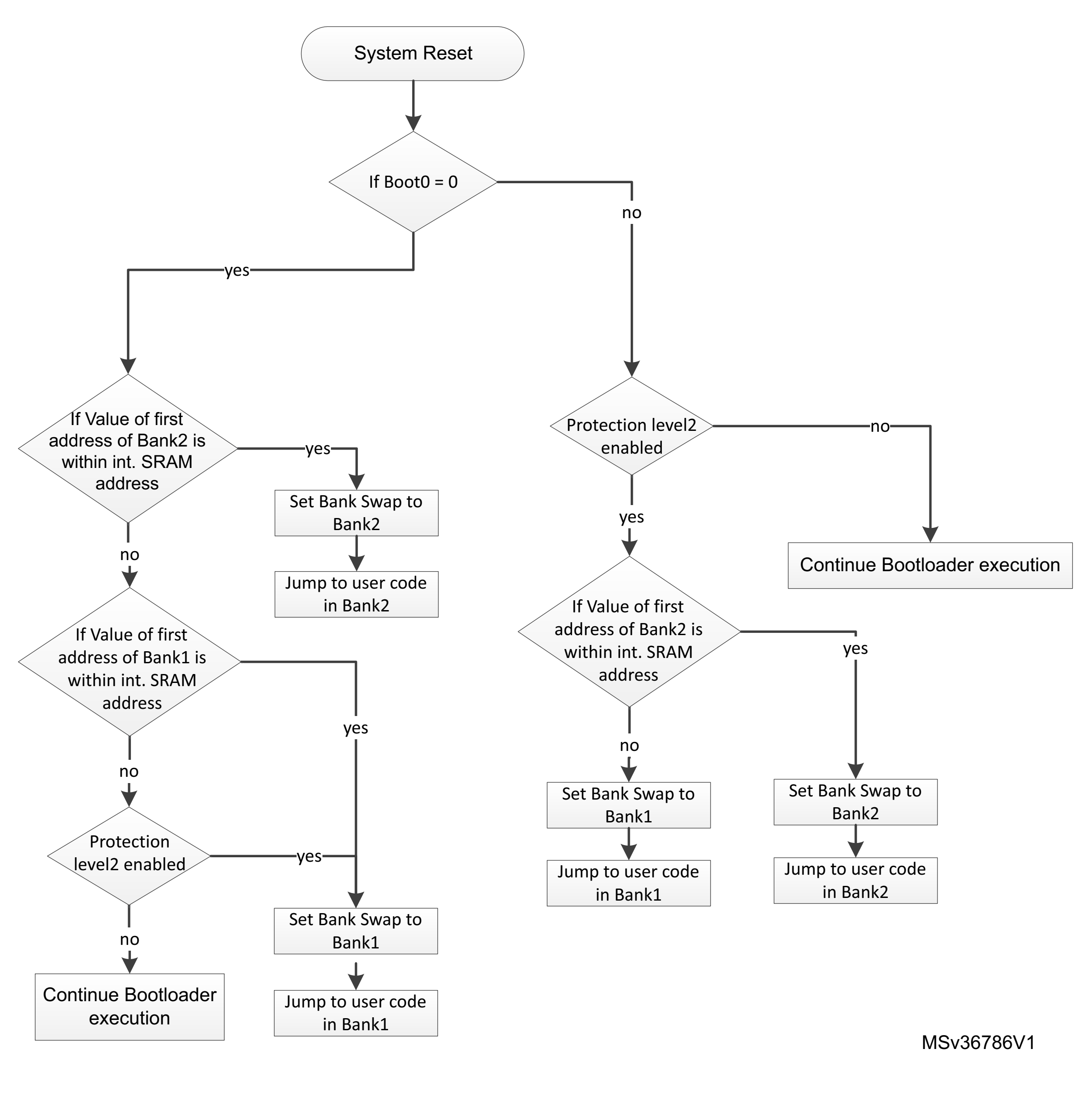
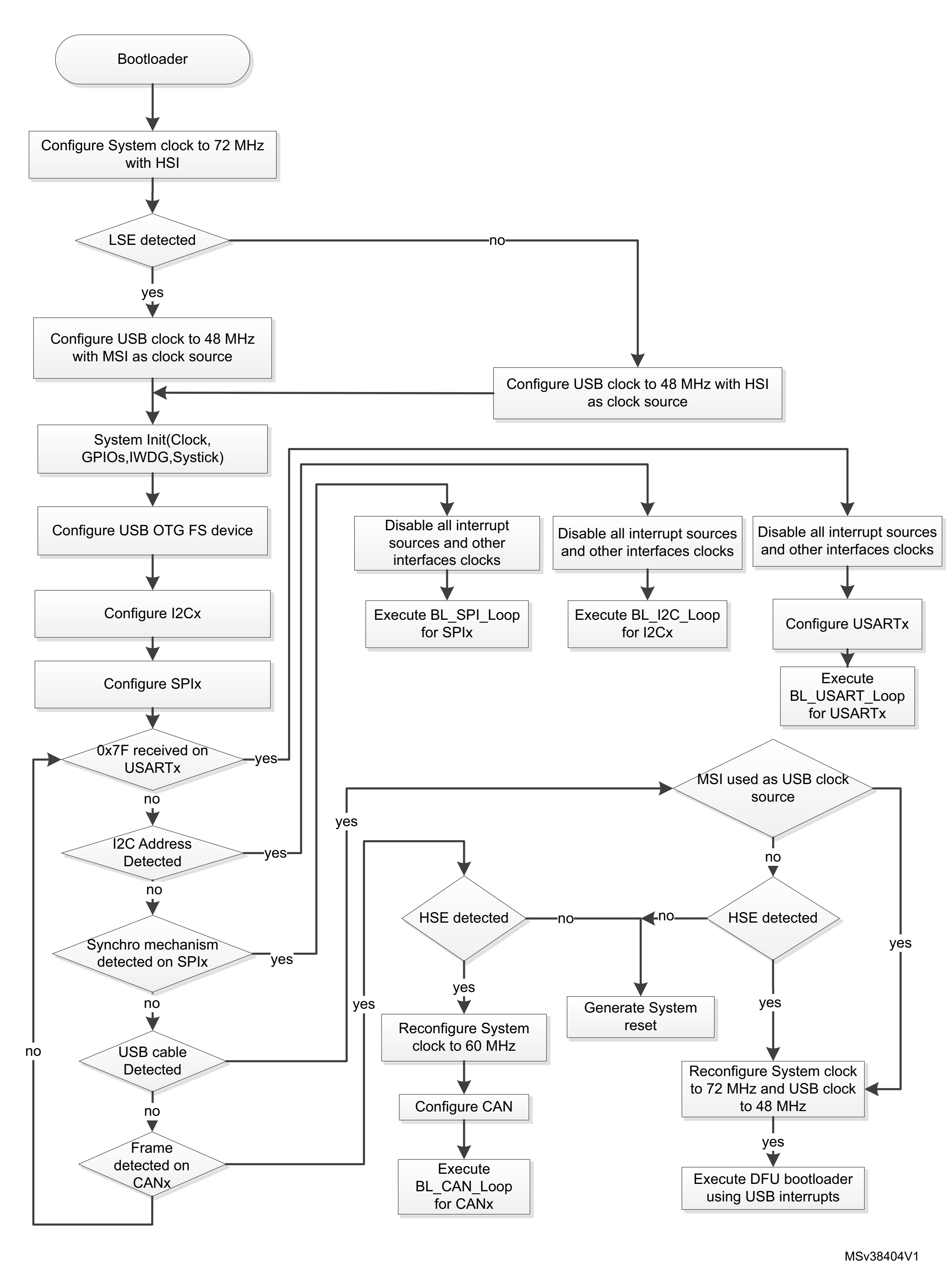


Figure 78.Bootloader V9.x selection for STM32L47xxx/48xxx



57.2.3 Bootloader version

The following table lists the STM32L47xxx/48xxx devices bootloader V9.x versions:

Table 126. STM32L47xxx/48xxx bootloader V9.x versions

Bootloader version number	Description	Known limitations
V9.0	Initial bootloader version	For memory write operations using DFU interface: If the buffer size is larger than 256 bytes and not multiple of 8 bytes, the write memory operation result is corrupted. Workaround: if the file size is larger than 256 bytes, add byte padding to align it on 8-bytes multiple size. Write in SRAM is corrupted
V9.1	Deprecated version (not used)	None
V9.2	Fix write in SRAM issue	– For memory write operations using DFU interface: If the buffer size is larger than 256 bytes and not multiple of 8 bytes, the write memory operation result is corrupted. Workaround: if the file size is larger than 256 bytes, add byte padding to align it on 8-bytes multiple size. – PcROP option bytes cannot be written as Bootloader uses Byte access while PcROP must be accessed using Half-Word access. **Workaround**: load a code snippiest in SRAM using Bootloader interface then jump to it, and that code would write PcROP value.

58 STM32L496xx/4A6xx devices bootloader

58.1 Bootloader configuration

The STM32L496xx/4A6xx bootloader is activated by applying pattern6 (described in *Table 2: Bootloader activation patterns*). The *Table 127* shows the hardware resources used by this bootloader.

Table 127. STM32L496xx/4A6xx configuration in system memory boot mode

Bootloader	Feature/Peripheral	State	Comment
Common to all bootloaders	RCC	HSI enabled	The HSI is used at startup as clock source for system clock configured to 72 MHz and for USART, I2C and SPI bootloader operation.
		-	The clock recovery system (CRS) is enabled for the DFU bootloader to allow USB to be clocked by HSI 48 MHz.
		HSE enabled	The HSE is used only when the CAN interface is selected . The HSE must have one of the following value [24,20,18,16,12,9,8,6,4] MHz.
		-	The Clock Security System (CSS) interrupt is enabled when HSE is enabled. Any failure (or removal) of the external clock generates system reset
	RAM	-	12 Kbyte starting from address 0x20000000 are used by the bootloader firmware
	System memory	-	28 Kbyte starting from address 0x1FFF0000, contain the bootloader firmware
	IWDG	-	The independent watchdog (IWDG) prescaler is configured to its maximum value. It is periodically refreshed to prevent watchdog reset (in case the hardware IWDG option was previously enabled by the user).
	Power	-	The DFU can't be used to communicate with bootloader if the voltage scaling range 2 is selected. Bootloader firmware doesn't configure voltage scaling range value in PWR_CR1 register.
USART1 bootloader	USART1	Enabled	Once initialized the USART1 configuration is: 8-bits, even parity and 1 Stop bit
	USART1_RX pin	Input	PA10 pin: USART1 in reception mode
	USART1_TX pin	Output	PA9 pin: USART1 in transmission mode

Table 127. STM32L496xx/4A6xx configuration in system memory boot mode (continued)

Bootloader	Feature/Peripheral	State	Comment
USART2 bootloader	USART2	Enabled	Once initialized the USART2 configuration is: 8-bits, even parity and 1 Stop bit
	USART2_RX pin	Input	PA3 pin: USART2 in reception mode
	USART2_TX pin	Output	PA2 pin: USART2 in transmission mode
USART3 bootloader	USART3	Enabled	Once initialized the USART3 configuration is: 8-bits, even parity and 1 Stop bit
	USART3_RX pin	Input	PC11 pin: USART3 in reception mode
	USART3_TX pin	Output	PC10 pin: USART3 in transmission mode
USARTx bootloaders	SysTick timer	Enabled	Used to automatically detect the serial baud rate from the host for USARTx bootloaders.
I2C1 bootloader	I2C1	Enabled	The I2C1 configuration is: I2C speed: up to 1 MHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b1001100x (where x = 0 for write and x = 1 for read)
	I2C1_SCL pin	Input/Output	PB6 pin: clock line is used in open-drain mode.
	I2C1_SDA pin	Input/Output	PB7 pin: data line is used in open-drain mode.
I2C2 bootloader	I2C2	Enabled	The I2C2 configuration is: I2C speed: up to 1 MHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b1001100x (where x = 0 for write and x = 1 for read)
	I2C2_SCL pin	Input/Output	PB10 pin: clock line is used in open-drain mode.
	I2C2_SDA pin	Input/Output	PB11 pin: data line is used in open-drain mode.
I2C3 bootloader	I2C3	Enabled	The I2C3 configuration is: I2C speed: up to 1 MHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b1001100x (where x = 0 for write and x = 1 for read)
	I2C3_SCL pin	Input/Output	PC0 pin: clock line is used in open-drain mode.
	I2C3_SDA pin	Input/Output	PC1 pin: data line is used in open-drain mode.

Table 127. STM32L496xx/4A6xx configuration in system memory boot mode (continued)

Bootloader	Feature/Peripheral	State	Comment
SPI1 bootloader	SPI1	Enabled	The SPI1 configuration is: – Slave mode – Full Duplex – 8-bit MSB – Speed up to 8 MHz – Polarity: CPOL Low, CPHA Low, NSS hardware.
	SPI1_MOSI pin	Input	PA7 pin: Slave data Input line, used in push-pull pull-down mode
	SPI1_MISO pin	Output	PA6 pin: Slave data output line, used in push-pull pull-down mode
	SPI1_SCK pin	Input	PA5 pin: Slave clock line, used in push-pull pull-down mode
	SPI1_NSS pin	Input	PA4 pin: slave chip select pin used in push-pull pull-down mode. **Note**: This IO can be tied to Gnd if the SPI Master does not use it.
SPI2 bootloader	SPI2	Enabled	The SPI2 configuration is: – Slave mode – Full Duplex – 8-bit MSB – Speed up to 8 MHz – Polarity: CPOL Low, CPHA Low, NSS hardware.
	SPI2_MOSI pin	Input	PB15 pin: Slave data Input line, used in push-pull pull-down mode
	SPI2_MISO pin	Output	PB14 pin: Slave data output line, used in push-pull pull-down mode
	SPI2_SCK pin	Input	PB13 pin: Slave clock line, used in push-pull pull-down mode
	SPI2_NSS pin	Input	PB12 pin: slave chip select pin used in push-pull pull-down mode. **Note:** This IO can be tied to GND if the SPI Master does not use it.
CAN1 bootloader	CAN1	Enabled	Once initialized the CAN1 configuration is: Baudrate 125 kbps, 11 -bit identifier.
	CAN1_RX pin	Input	PB8 pin: CAN1 in reception mode
	CAN1_TX pin	Output	PB9 pin: CAN1 in transmission mode
	TIM16	Enabled	This timer is used to determine the value of the HSE. Once the HSE frequency is determined, the system clock is configured to 60 MHz using PLL and HSE.

Table 127. STM32L496xx/4A6xx configuration in system memory boot mode (continued)

Bootloader	Feature/Peripheral	State	Comment
DFU bootloader	USB	Enabled	USB OTG FS configured in forced device mode. USB OTG FS interrupt vector is enabled and used for USB DFU communications. **Note:** VDDUSB IO must be connected to 3.3V for USB to be operational.
	USB_DM pin	Input/Output	PA11: USB DM line.
	USB_DP pin		PA12: USB DP line No external Pull-up resistor is required

58.2 Bootloader selection

The figures below show the bootloader selection mechanism.

Figure 79. Dual bank boot Implementation for STM32L496xx/4A6xx bootloader V9.x

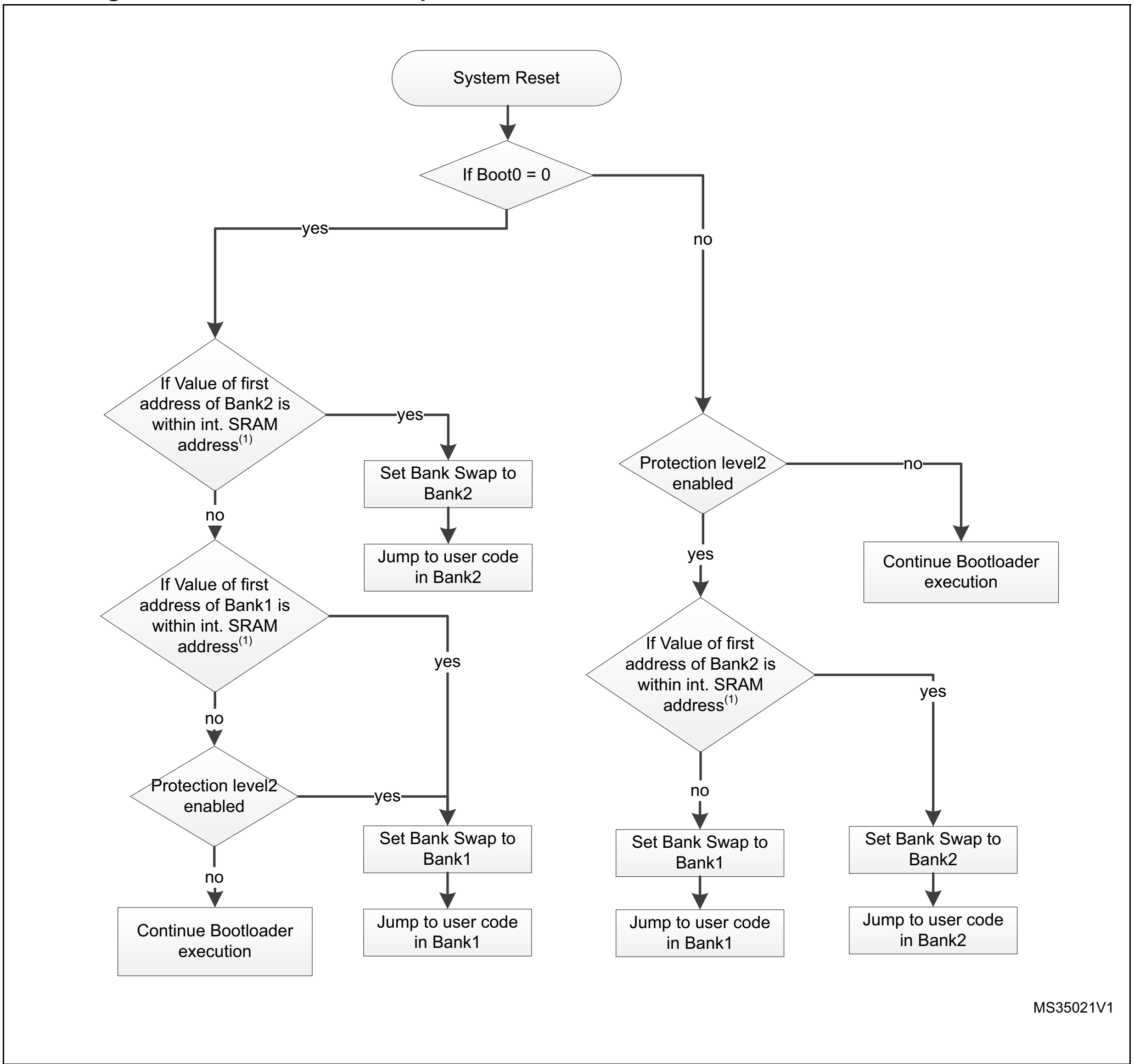
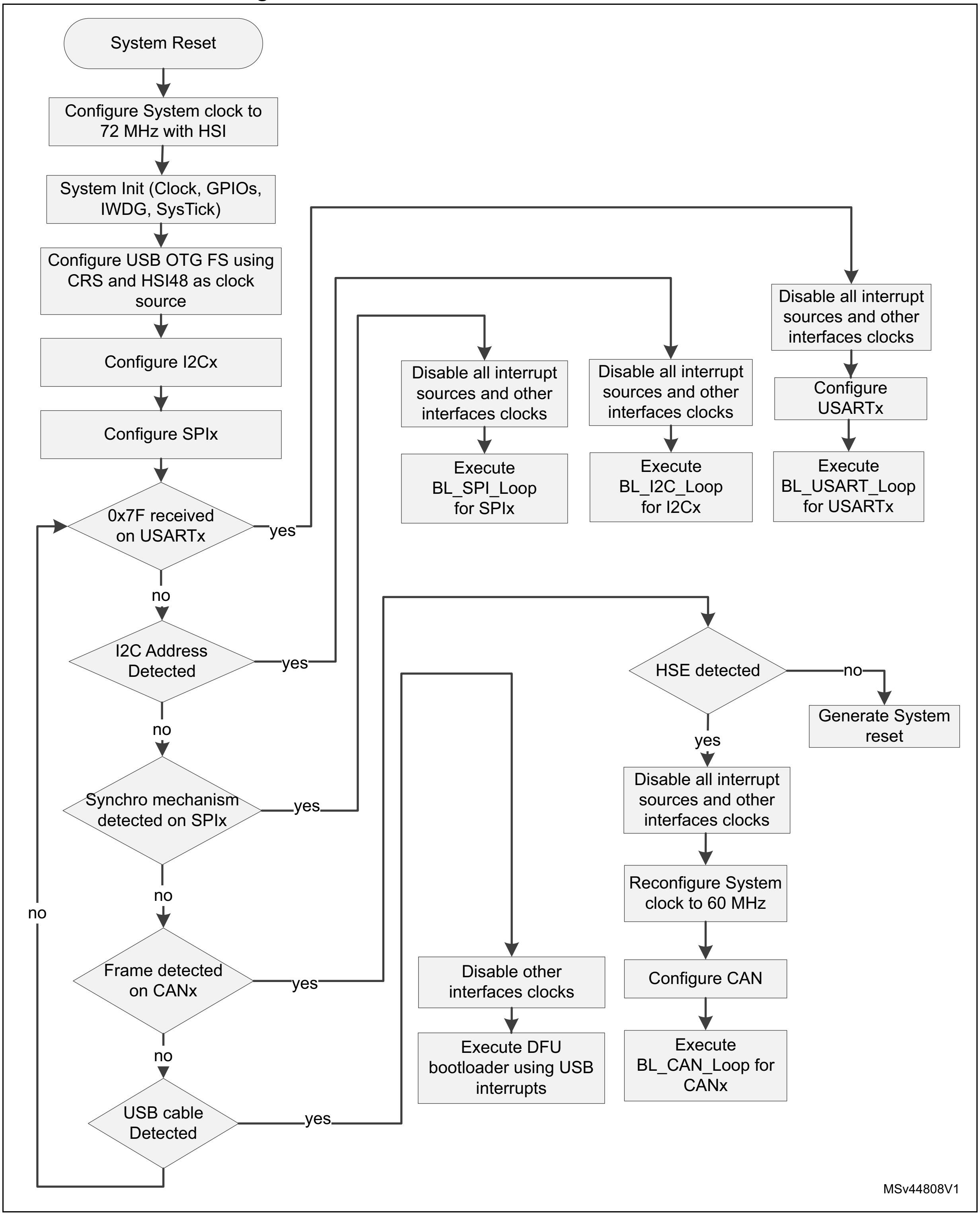


Figure 80.Bootloader V9.x selection for STM32L496xx/4A6xx



58.3 Bootloader version

The *Table 128* lists the STM32L496xx/4A6xx devices bootloader versions.

Table 128. STM32L496xx/4A6xx bootloader version

Bootloader version number	Description	Known limitations
V9.3	Initial bootloader version	– The Bank Erase command is aborted by the bootloader device, and the NACK (0x1F) is sent to the host. Workaround: Perform Bank erase operation through page erase using the Erase command (0x44). – SPI write operation fail **Limitation**: a. During Bootloader SPI write Flash memory operation, some random 64-bits (2 double-words) may be left blank at 0xFF. **Root cause**: a. Bootloader uses 64-bits cast write operation which is interrupted by SPI DMA and it leads to double access on same Flash memory address and the 64-bits are not written **Workarounds**: a. WA1: add a delay between sending write command and its ACK request. Its duration should be the duration of the 256-Bytes Flash memory write time. b. WA2: read back after write and in case of error start write again. c. WA3: Patch in RAM to write in Flash memory that implements write memory without 64-bits cast. WA1 and WA3 are more efficient than WA2 in terms of total programming time **How critical is the limitation**: a. The limitation leads to a modification in customer SPI host software by adding 3-4 ms delay to each write operation. b. The delay is not waste because it’s anyway the Flash memory write period of time that host has to wait anyway (so instead of waiting by sending ACK requests, host will wait by delay). c. Limitation has been seen only on SPI and cannot impact USART/I2C/CAN. – PcROP option bytes cannot be written as Bootloader uses Byte access while PcROP must be accessed using Half-Word access. **Workaround**: load a code snippiest in SRAM using Bootloader interface then jump to it, and that code would write PcROP value.

59 STM32L4P5xx/4Q5xx devices bootloader

59.1 Bootloader configuration

The STM32L4P5xx/4Q5xx bootloader is activated by applying pattern7 (described in *Table 2: Bootloader activation patterns*). The *Table 131* shows the hardware resources used by this bootloader.

Table 129. STM32L4P5xx/4Q5xx configuration in system memory boot mode

Bootloader	Feature/Peripheral	State	Comment
Common to all bootloaders	RCC	HSI enabled	The HSI is used at startup as clock source for system clock configured to 60 MHz and for USART, I2C, SPI and USB bootloader operation.
		-	The clock recovery system (CRS) is enabled for the DFU bootloader to allow USB to be clocked by HSI 48 MHz.
		HSE enabled	The HSE is used only when the CAN interface is selected . The HSE must have one of the following value [24,20,18,16,12,9,8,6,4] MHz.
		-	The Clock Security System (CSS) interrupt is enabled when HSE is enabled. Any failure (or removal) of the external clock generates system reset
	RAM	-	16 Kbytes starting from address 0x20000000 are used by the bootloader firmware
	System memory	-	28 Kbytes starting from address 0x1FFF0000, contain the bootloader firmware
	IWDG	-	The independent watchdog (IWDG) prescaler is configured to its maximum value. It is periodically refreshed to prevent watchdog reset (in case the hardware IWDG option was previously enabled by the user).
	Power	-	The DFU can’t be used to communicate with bootloader if the voltage scaling range 2 is selected. Bootloader firmware doesn’t configure voltage scaling range value in PWR_CR1 register.
USART1 bootloader	USART1	Enabled	Once initialized the USART1 configuration is: 8-bits, even parity and 1 Stop bit
	USART1_RX pin	Input	PA10 pin: USART1 in reception mode
	USART1_TX pin	Output	PA9 pin: USART1 in transmission mode

Table 129. STM32L4P5xx/4Q5xx configuration in system memory boot mode (continued)

Bootloader	Feature/Peripheral	State	Comment
USART2 bootloader	USART2	Enabled	Once initialized the USART2 configuration is: 8-bits, even parity and 1 Stop bit
	USART2_RX pin	Input	PA3 pin: USART2 in reception mode
	USART2_TX pin	Output	PA2 pin: USART2 in transmission mode
USART3 bootloader	USART3	Enabled	Once initialized the USART3 configuration is: 8-bits, even parity and 1 Stop bit
	USART3_RX pin	Input	PC11 pin: USART3 in reception mode
	USART3_TX pin	Output	PC10 pin: USART3 in transmission mode
I2C1 bootloader	I2C1	Enabled	The I2C1 configuration is: I2C speed: up to 1 MHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b1011011x (where x = 0 for write and x = 1 for read)
	I2C1_SCL pin	Input/Output	PB6 pin: clock line is used in open-drain mode.
	I2C1_SDA pin	Input/Output	PB7 pin: data line is used in open-drain mode.
I2C2 bootloader	I2C2	Enabled	The I2C2 configuration is: I2C speed: up to 1 MHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b1011011x (where x = 0 for write and x = 1 for read)
	I2C2_SCL pin	Input/Output	PB10 pin: clock line is used in open-drain mode.
	I2C2_SDA pin	Input/Output	PB11 pin: data line is used in open-drain mode.
I2C3 bootloader	I2C3	Enabled	The I2C3 configuration is: I2C speed: up to 1 MHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b1011011x (where x = 0 for write and x = 1 for read)
	I2C3_SCL pin	Input/Output	PC0 pin: clock line is used in open-drain mode.
	I2C3_SDA pin	Input/Output	PC1 pin: data line is used in open-drain mode.

Table 129. STM32L4P5xx/4Q5xx configuration in system memory boot mode (continued)

Bootloader	Feature/Peripheral	State	Comment
SPI1 bootloader	SPI1	Enabled	The SPI1 configuration is: – Slave mode – Full Duplex – 8-bit MSB – Speed up to 8 MHz – Polarity: CPOL Low, CPHA Low, NSS hardware.
	SPI1_MOSI pin	Input	PA7 pin: Slave data Input line, used in push-pull pull-down mode
	SPI1_MISO pin	Output	PA6 pin: Slave data output line, used in push-pull pull-down mode
	SPI1_SCK pin	Input	PA5 pin: Slave clock line, used in push-pull pull-down mode
	SPI1_NSS pin	Input	PA4 pin: slave chip select pin used in push-pull pull-up mode. Note: This IO can be tied to Gnd if the SPI Master does not use it.
SPI2 bootloader	SPI2	Enabled	The SPI2 configuration is: – Slave mode – Full Duplex – 8-bit MSB – Speed up to 8 MHz – Polarity: CPOL Low, CPHA Low, NSS hardware.
	SPI2_MOSI pin	Input	PB15 pin: Slave data Input line, used in push-pull pull-down mode
	SPI2_MISO pin	Output	PB14 pin: Slave data output line, used in push-pull pull-down mode
	SPI2_SCK pin	Input	PB13 pin: Slave clock line, used in push-pull pull-down mode
	SPI2_NSS pin	Input	PB12 pin: slave chip select pin used in push-pull pull-up mode. **Note:** This IO can be tied to Gnd if the SPI Master does not use it.
CAN1 bootloader	CAN1	Enabled	Once initialized the CAN1 configuration is: Baudrate 125 kbps, 11 -bit identifier.
	CAN1_RX pin	Input	PB8 pin: CAN1 in reception mode
	CAN1_TX pin	Output	PB9 pin: CAN1 in transmission mode

Table 129. STM32L4P5xx/4Q5xx configuration in system memory boot mode (continued)

Bootloader	Feature/Peripheral	State	Comment
DFU bootloader	USB	Enabled	USB FS configured in forced device mode. USB FS interrupt vector is enabled and used for USB DFU communications. **Note:** VDDUSB IO must be connected to 3.3V for USB to be operational.
	USB_DM pin	Input/Output	PA11: USB DM line.
	USB_DP pin		PA12: USB DP line No external Pull-up resistor is required

59.2 Bootloader selection

The *Figure 83* and *Figure 84* show the bootloader selection mechanisms.

Figure 81. Dual bank boot implementation for STM32L4P5xx/4Q5xx bootloader V9.x

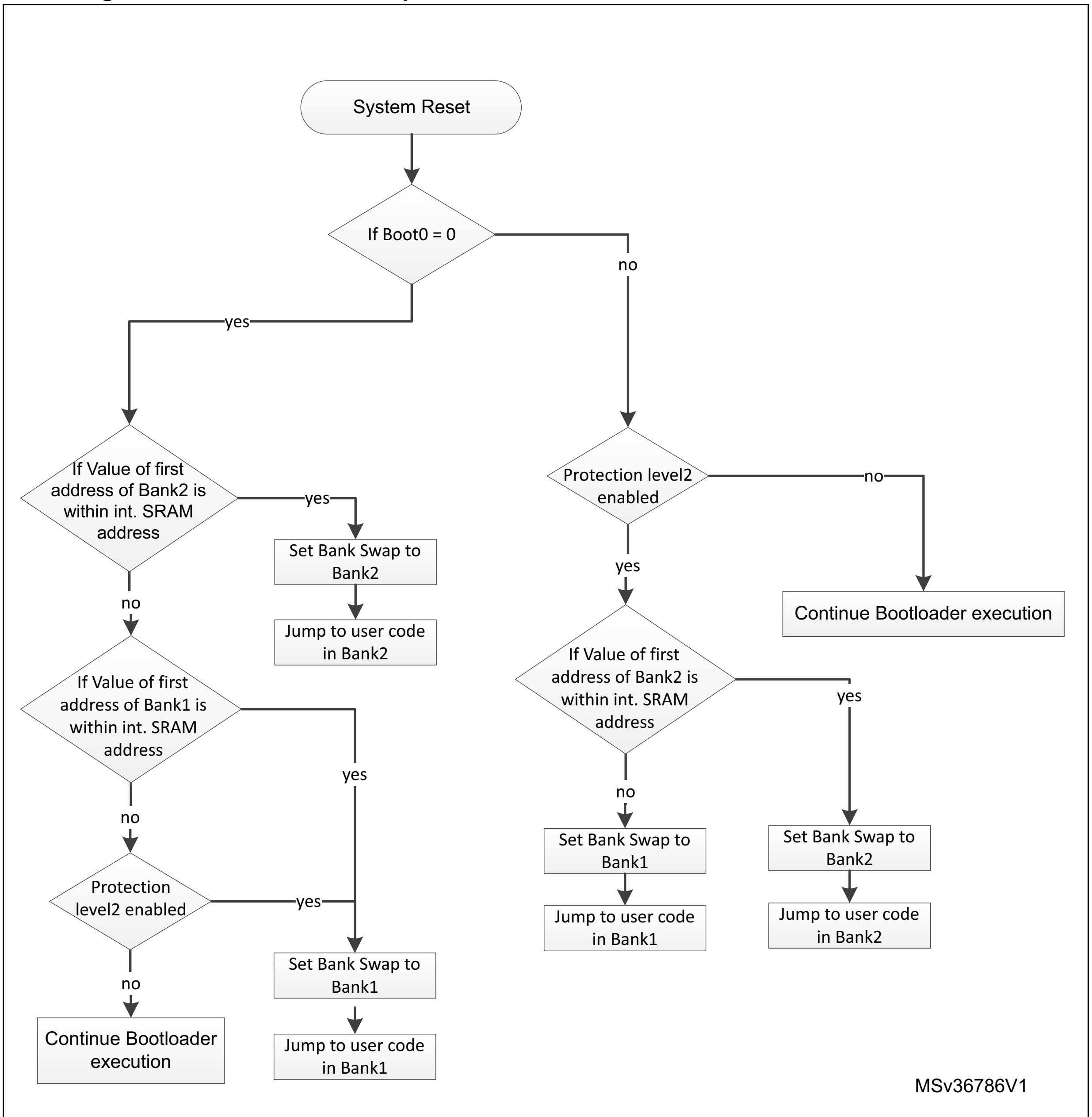
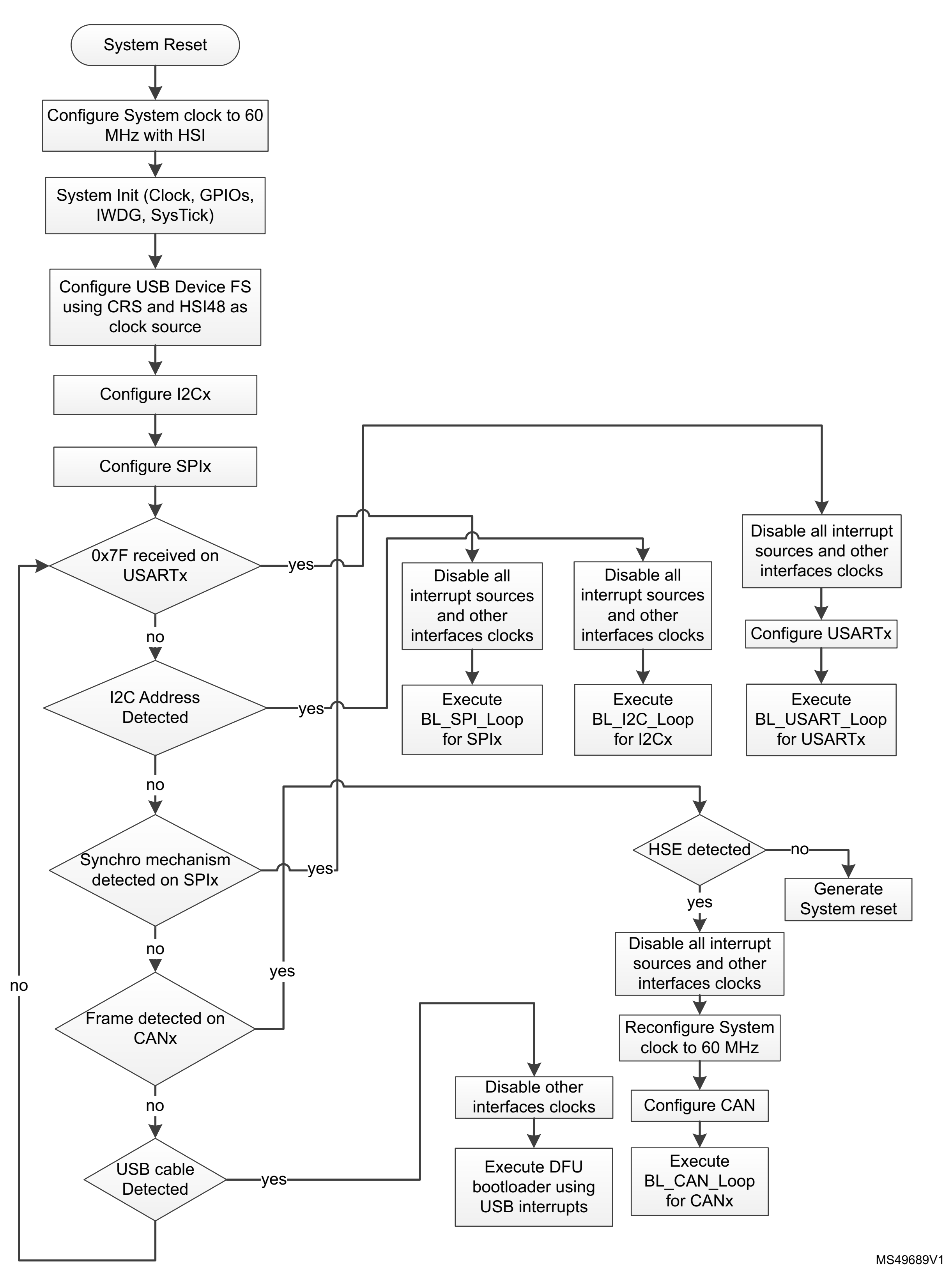


Figure 82.Bootloader V9.x selection for STM32L4P5xx/4Q5xx



59.3 Bootloader version

The *Table 130* lists the STM32L4P5xx/4Q5xx devices bootloader versions.

Table 130. STM32L4P5xx/4Q5xx bootloader versions

Bootloader version number	Description	Known limitations
V9.0	Initial bootloader version ON CUT 1.0 samples	– PcROP option bytes cannot be written as bootloader uses byte access while PcROP must be accessed using half-word access. **Workaround**: load a code snippet in SRAM using bootloader interface then jump to it, and that code writes PcROP value.

60 STM32L4Rxxx/4Sxxx devices bootloader

60.1 Bootloader configuration

The STM32L4Rxx/4Sxx bootloader is activated by applying pattern6 (described in *Table 2: Bootloader activation patterns*). The *Table 131* shows the hardware resources used by this bootloader.

Table 131. STM32L4Rxxx/4Sxxx configuration in system memory boot mode

Bootloader	Feature/Peripheral	State	Comment
Common to all bootloaders	RCC	HSI enabled	The HSI is used at startup as clock source for system clock configured to 60 MHz and for USART, I2C, SPI and USB bootloader operation.
		-	The clock recovery system (CRS) is enabled for the DFU bootloader to allow USB to be clocked by HSI 48 MHz.
		HSE enabled	The HSE is used only when the CAN interface is selected . The HSE must have one of the following value [24,20,18,16,12,9,8,6,4] MHz.
		-	The Clock Security System (CSS) interrupt is enabled when HSE is enabled. Any failure (or removal) of the external clock generates system reset
	RAM	-	12 Kbytes starting from address 0x20000000 are used by the bootloader firmware
	System memory	-	28672 bytes starting from address 0x1FFF0000, contain the bootloader firmware
	IWDG	-	The independent watchdog (IWDG) prescaler is configured to its maximum value. It is periodically refreshed to prevent watchdog reset (in case the hardware IWDG option was previously enabled by the user).
	Power	-	The DFU can't be used to communicate with bootloader if the voltage scaling range 2 is selected. Bootloader firmware doesn't configure voltage scaling range value in PWR_CR1 register.

Table 131. STM32L4Rxxx/4Sxxx configuration in system memory boot mode (continued)

Bootloader	Feature/Peripheral	State	Comment
USART1 bootloader	USART1	Enabled	Once initialized the USART1 configuration is: 8-bits, even parity and 1 Stop bit
	USART1_RX pin	Input	PA10 pin: USART1 in reception mode
	USART1_TX pin	Output	PA9 pin: USART1 in transmission mode
USART2 bootloader	USART2	Enabled	Once initialized the USART2 configuration is: 8-bits, even parity and 1 Stop bit
	USART2_RX pin	Input	PA3 pin: USART2 in reception mode
	USART2_TX pin	Output	PA2 pin: USART2 in transmission mode
USART3 bootloader	USART3	Enabled	Once initialized the USART3 configuration is: 8-bits, even parity and 1 Stop bit
	USART3_RX pin	Input	PC11 pin: USART3 in reception mode
	USART3_TX pin	Output	PC10 pin: USART3 in transmission mode
USARTx bootloaders	SysTick timer	Enabled	Used to automatically detect the serial baud rate from the host for USARTx bootloaders.
I2C1 bootloader	I2C1	Enabled	The I2C1 configuration is: I2C speed: up to 1 MHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b1010000x (where x = 0 for write and x = 1 for read)
	I2C1_SCL pin	Input/Output	PB6 pin: clock line is used in open-drain mode.
	I2C1_SDA pin	Input/Output	PB7 pin: data line is used in open-drain mode.
I2C2 bootloader	I2C2	Enabled	The I2C2 configuration is: I2C speed: up to 1 MHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b1010000x (where x = 0 for write and x = 1 for read)
	I2C2_SCL pin	Input/Output	PB10 pin: clock line is used in open-drain mode.
	I2C2_SDA pin	Input/Output	PB11 pin: data line is used in open-drain mode.

Table 131. STM32L4Rxxx/4Sxxx configuration in system memory boot mode (continued)

Bootloader	Feature/Peripheral	State	Comment
I2C3 bootloader	I2C3	Enabled	The I2C3 configuration is: I2C speed: up to 1 MHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b1010000x (where x = 0 for write and x = 1 for read)
	I2C3_SCL pin	Input/Output	PC0 pin: clock line is used in open-drain mode.
	I2C3_SDA pin	Input/Output	PC1 pin: data line is used in open-drain mode.
SPI1 bootloader	SPI1	Enabled	The SPI1 configuration is: – Slave mode – Full Duplex – 8-bit MSB – Speed up to 8 MHz – Polarity: CPOL Low, CPHA Low, NSS hardware.
	SPI1_MOSI pin	Input	PA7 pin: Slave data Input line, used in push-pull pull-down mode
	SPI1_MISO pin	Output	PA6 pin: Slave data output line, used in push-pull pull-down mode
	SPI1_SCK pin	Input	PA5 pin: Slave clock line, used in push-pull pull-down mode
	SPI1_NSS pin	Input	PA4 pin: slave chip select pin used in push-pull pull-up mode. Note: This IO can be tied to Gnd if the SPI Master does not use it.
SPI2 bootloader	SPI2	Enabled	The SPI2 configuration is: – Slave mode – Full Duplex – 8-bit MSB – Speed up to 8 MHz – Polarity: CPOL Low, CPHA Low, NSS hardware.
	SPI2_MOSI pin	Input	PB15 pin: Slave data Input line, used in push-pull pull-down mode
	SPI2_MISO pin	Output	PB14 pin: Slave data output line, used in push-pull pull-down mode
	SPI2_SCK pin	Input	PB13 pin: Slave clock line, used in push-pull pull-down mode
	SPI2_NSS pin	Input	PB12 pin: slave chip select pin used in push-pull pull-up mode. **Note:** This IO can be tied to Gnd if the SPI Master does not use it.

Table 131. STM32L4Rxxx/4Sxxx configuration in system memory boot mode (continued)

Bootloader	Feature/Peripheral	State	Comment
CAN1 bootloader	CAN1	Enabled	Once initialized the CAN1 configuration is: Baudrate 125 kbps, 11 -bit identifier.
	CAN1_RX pin	Input	PB8 pin: CAN1 in reception mode
	CAN1_TX pin	Output	PB9 pin: CAN1 in transmission mode
	TIM16	Enabled	This timer is used to determine the value of the HSE. Once the HSE frequency is determined, the system clock is configured to 60 MHz using PLL and HSE.
DFU bootloader	USB	Enabled	USB FS configured in forced device mode. USB FS interrupt vector is enabled and used for USB DFU communications. **Note:** VDDUSB IO must be connected to 3.3V for USB to be operational.
	USB_DM pin	Input/Output	PA11: USB DM line.
	USB_DP pin		PA12: USB DP line No external Pull-up resistor is required

60.2 Bootloader selection

The *Figure 83* and *Figure 84* show the bootloader selection mechanisms.

Figure 83. Dual bank boot implementation for STM32L4Rxxx/STM32L4Sxxx bootloader V9.x

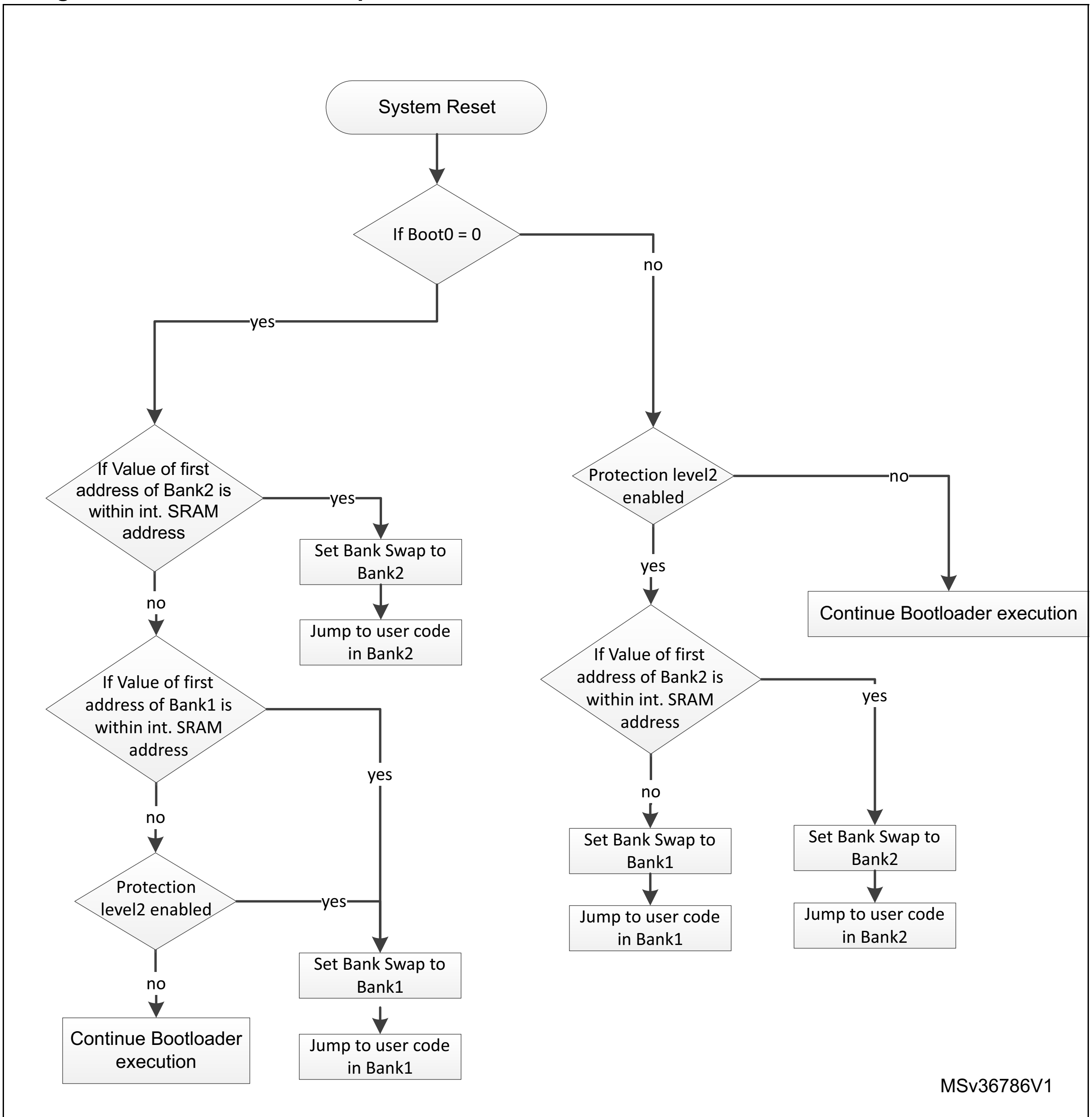
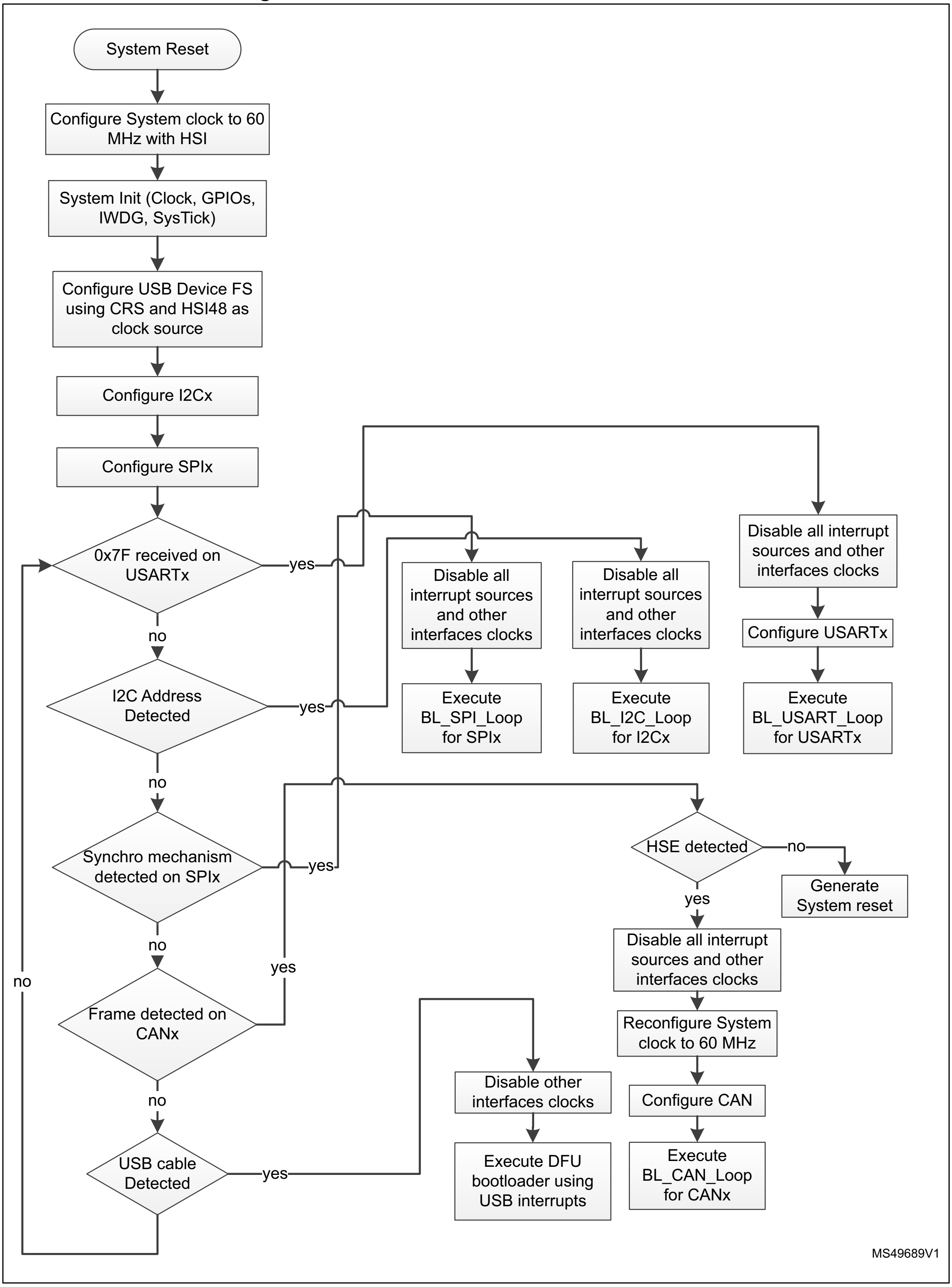


Figure 84.Bootloader V9.x selection for STM32L4Rxx/4Sxx



60.3 Bootloader version

The *Table 132* lists the STM32L4Rxx/4Sxx devices bootloader versions.

Table 132. STM32L4Rxx/4Sxx bootloader versions

Bootloader version number	Description	Known limitations
V9.0	Initial bootloader version ON CUT 1.0 samples	– None

61 STM32L552xx/STM32L562xx devices bootloader

61.1 Bootloader configuration

The STM32L552xx/562xx bootloader is activated by applying pattern12 (described in *Table 2: Bootloader activation patterns*). The following table shows the hardware resources used by this bootloader.

Table 133. STM32L552xx/562xx configuration in system memory boot mode

<table>
<tr><th>Bootloader</th><th>Feature/Peripheral</th><th>State</th><th>Comment</th></tr>
<tr><td rowspan="6">Common to all bootloaders</td><td rowspan="3">RCC</td><td>HSI enabled</td><td>The system clock frequency is 60 MHz (using PLL clocked by HSI).</td></tr>
<tr><td>-</td><td>The clock recovery system (CRS) is enabled for the DFU bootloader to allow USB to be clocked by HSI 48 MHz.</td></tr>
<tr><td>-</td><td>20 MHZ derived from the PLLQ is used for FDCAN</td></tr>
<tr><td>RAM</td><td>-</td><td>16 Kbytes starting from address 0x20000000 are used by the bootloader firmware</td></tr>
<tr><td>System memory</td><td>-</td><td>32 Kbytes starting from address 0x0BF90000.</td></tr>
<tr><td>IWDG</td><td>-</td><td>The independent watchdog (IWDG) prescaler is configured to its maximum value. It is periodically refreshed to prevent watchdog reset (in case the hardware IWDG option was previously enabled by the user).</td></tr>
<tr><td rowspan="3">USART1 bootloader</td><td>USART1</td><td>Enabled</td><td>Once initialized the USART1 configuration is: 8-bits, even parity and 1 Stop bit</td></tr>
<tr><td>USART1_RX pin</td><td>Input</td><td>PA10 pin: USART1 in reception mode</td></tr>
<tr><td>USART1_TX pin</td><td>Output</td><td>PA9 pin: USART1 in transmission mode</td></tr>
<tr><td rowspan="3">USART2 bootloader</td><td>USART2</td><td>Enabled</td><td>Once initialized the USART2 configuration is: 8-bits, even parity and 1 Stop bit</td></tr>
<tr><td>USART2_RX pin</td><td>Input</td><td>PA3 pin: USART2 in reception mode</td></tr>
<tr><td>USART2_TX pin</td><td>Output</td><td>PA2 pin: USART2 in transmission mode</td></tr>
<tr><td rowspan="3">USART3 bootloader</td><td>USART3</td><td>Enabled</td><td>Once initialized the USART3 configuration is: 8-bits, even parity and 1 Stop bit</td></tr>
<tr><td>USART3_RX pin</td><td>Input</td><td>PC11 pin: USART3 in reception mode</td></tr>
<tr><td>USART3_TX pin</td><td>Output</td><td>PC10 pin: USART3 in transmission mode</td></tr>
</table>

Table 133. STM32L552xx/562xx configuration in system memory boot mode (continued)

Bootloader	Feature/Peripheral	State	Comment
I2C1 bootloader	I2C1	Enabled	The I2C1 configuration is: I2C speed: up to 1 MHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b1010000x (where x = 0 for write and x = 1 for read)
	I2C1_SCL pin	Input/Output	PB6 pin: clock line is used in open-drain mode.
	I2C1_SDA pin	Input/Output	PB7 pin: data line is used in open-drain mode.
I2C2 bootloader	I2C2	Enabled	The I2C2 configuration is: I2C speed: up to 1 MHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b1010000x (where x = 0 for write and x = 1 for read)
	I2C2_SCL pin	Input/Output	PB10 pin: clock line is used in open-drain mode.
	I2C2_SDA pin	Input/Output	PB11 pin: data line is used in open-drain mode.
I2C3 bootloader	I2C3	Enabled	The I2C3 configuration is: I2C speed: up to 1 MHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b1010000x (where x = 0 for write and x = 1 for read)
	I2C3_SCL pin	Input/Output	PC0 pin: clock line is used in open-drain mode.
	I2C3_SDA pin	Input/Output	PC1 pin: data line is used in open-drain mode.
SPI1 bootloader	SPI1	Enabled	The SPI1 configuration is: – Slave mode – Full Duplex – 8-bit MSB – Speed up to 8 MHz – Polarity: CPOL Low, CPHA Low, NSS hardware.
	SPI1_MOSI pin	Input	PA7 pin: Slave data Input line, used in push-pull pull-down mode
	SPI1_MISO pin	Output	PA6 pin: Slave data output line, used in push-pull pull-down mode
	SPI1_SCK pin	Input	PA5 pin: Slave clock line, used in push-pull pull-down mode
	SPI1_NSS pin	Input	PA4 pin: slave chip select pin used in push-pull pull-up mode. Note: This IO can be tied to Gnd if the SPI Master does not use it.

Table 133. STM32L552xx/562xx configuration in system memory boot mode (continued)

Bootloader	Feature/Peripheral	State	Comment
SPI2 bootloader	SPI2	Enabled	The SPI2 configuration is: – Slave mode – Full Duplex – 8-bit MSB – Speed up to 8 MHz – Polarity: CPOL Low, CPHA Low, NSS hardware.
	SPI2_MOSI pin	Input	PB15 pin: Slave data Input line, used in push-pull pull-down mode
	SPI2_MISO pin	Output	PB14 pin: Slave data output line, used in push-pull pull-down mode
	SPI2_SCK pin	Input	PB13 pin: Slave clock line, used in push-pull pull-down mode
	SPI2_NSS pin	Input	PB12 pin: slave chip select pin used in push-pull pull-up mode. **Note:** This IO can be tied to Gnd if the SPI Master does not use it.
SPI3 bootloader	SPI3	Enabled	The SPI configuration is: – Slave mode – Full Duplex – 8-bit MSB – Speed up to 8 MHz – Polarity: CPOL Low, CPHA Low, NSS hardware.
	SPI3_MOSI pin	Input	PB5 pin: Slave data Input line, used in push-pull pull-down mode
	SPI3_MISO pin	Output	PG10 pin: Slave data output line, used in push-pull pull-down mode
	SPI3_SCK pin	Input	PG9 pin: Slave clock line, used in push-pull pull-down mode
	SPI3_NSS pin	Input	PG12 pin: slave chip select pin used in push-pull pull-up mode. **Note:** This IO can be tied to Gnd if the SPI Master does not use it.
FDCAN bootloader	FDCAN1	Enabled	Once initialized the FDCAN1 configuration is: Bitrate 0.5 Mbps FrameFormat = FDCAN_FRAME_FD_BRS Mode = FDCAN_MODE_NORMAL AutoRetransmission = ENABLE TransmitPause = DISABLE ProtocolException = ENABLE
	FDCAN1_Rx pin	Input/	PB9 pin: FDCAN1 in reception mode
	FDCAN1_Tx pin	Output	PB8 pin: FDCAN1 in transmission mode

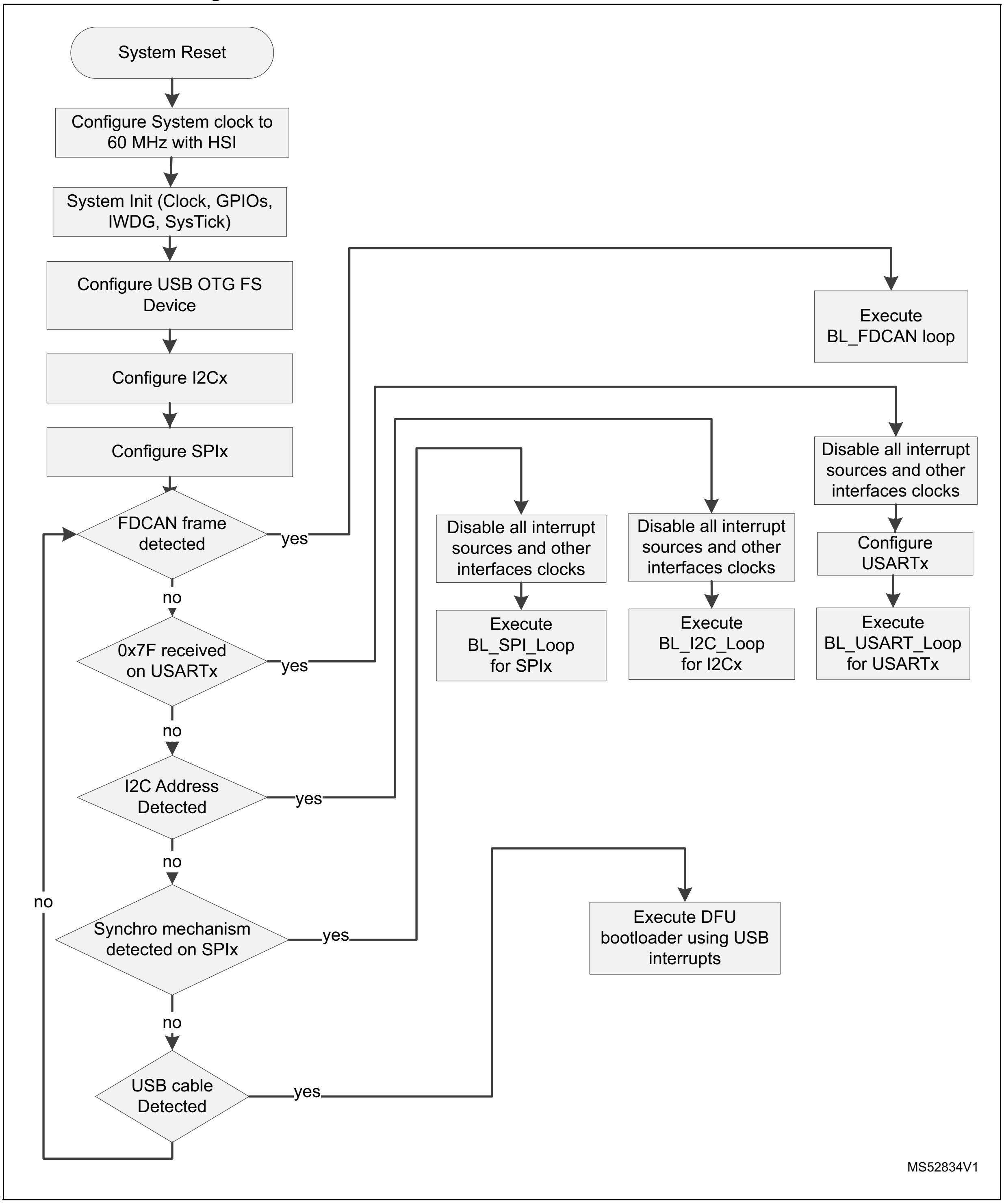
Table 133. STM32L552xx/562xx configuration in system memory boot mode (continued)

Bootloader	Feature/Peripheral	State	Comment
DFU bootloader	USB	Enabled	USB FS configured in forced device mode. USB FS interrupt vector is enabled and used for USB DFU communications. **Note:** VDDUSB IO must be connected to 3.3V for USB to be operational.
	USB_DM pin	Input/Output	PA11: USB DM line.
	USB_DP pin		PA12: USB DP line No external Pull-up resistor is required

61.2 Bootloader selection

The figure below shows the bootloader selection mechanism.

Figure 85. Bootloader V9.x selection for STM32L552xx/562xx



61.3 Bootloader version

The Table 134 lists the STM32L552xx/562xx devices bootloader versions.

Table 134. STM32L552xx/562xx bootloader versions

Bootloader version number	Description	Known limitations
V13.0	Initial bootloader version on cut1.0 samples	– USART3 not working – SPI3 not working – OB launch not working on USB-DFU – No read/write SRAM2 in all protocols – Read Secure Option bytes only implemented on USART/I2C – Regression from TZen=1 to TZen=0 is done automatically on RDP regression
V9.0	Release supported only in cut2.0 – Fix all issues on previous release – Add FDCAN support – New command added for TZen disable – Support of sales type 256KB	– Not able to set TZen to ‘1’ option byte using all interfaces of the BL No WA available – Cannot set RDP level 0.5 nor option bytes in RDP level 0.5 using BL interfaces No WA available – Multiple reset seen when enabling HW IWDG option byte in TZen = ’1’ No WA available – Not able to set secure option bytes setting when TZen = ‘1’ and RDP level is 0 No WA available – “Go” Command on USB is not working
V9.1	– Fix all known limitations of previous release – Add enable BOOT_LOCK BL command – Add support of RDP L1 to 0.5 regression	Option byte programming is not working properly when using FDCAN interface This makes the change of the Option byte not effective until a power off power on.
V9.2	– Fix all known limitations of previous release – Version for Sslicon revision Z	None

Note: When jumping to the BL the cache must be disabled.

62 STM32WB50xx/55xx devices bootloader

62.1 Bootloader configuration

The STM32WBxxx bootloader is activated by applying pattern6 (described in *Table 2: Bootloader activation patterns*). The following table shows the hardware resources used by this bootloader.

Table 135. STM32WB50xx/55xx configuration in system memory boot mode

Bootloader	Feature/Peripheral	State	Comment
Common to all bootloaders	RCC	MSI enabled	The system clock frequency is 64 MHz (using PLL clocked by MSI).
		-	The clock recovery system (CRS) is enabled for the DFU bootloader to allow USB to be clocked by HSI 48 MHz.
	RAM	-	20 Kbytes starting from address 0x20000000 are used by the bootloader firmware
	System memory	-	28 Kbytes starting from address 0x1FFF0000, contain the bootloader firmware
	IWDG	-	The independent watchdog (IWDG) prescaler is configured to its maximum value. It is periodically refreshed to prevent watchdog reset (in case the hardware IWDG option was previously enabled by the user).
USART1 bootloader	USART1	Enabled	Once initialized the USART1 configuration is: 8-bits, even parity and 1 Stop bit
	USART1_RX pin	Input	PA10 pin: USART1 in reception mode
	USART1_TX pin	Output	PA9 pin: USART1 in transmission mode
I2C1 bootloader	I2C1	Enabled	The I2C1 configuration is: I2C speed: up to 1 MHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b1001111x (where x = 0 for write and x = 1 for read)
	I2C1_SCL pin	Input/Output	PB6 pin: clock line is used in open-drain mode.
	I2C1_SDA pin	Input/Output	PB7 pin: data line is used in open-drain mode.

Table 135. STM32WB50xx/55xx configuration in system memory boot mode (continued)

Bootloader	Feature/Peripheral	State	Comment
I2C3 bootloader	I2C3	Enabled	The I2C3 configuration is: I2C speed: up to 1 MHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b1001111x (where x = 0 for write and x = 1 for read)
	I2C3_SCL pin	Input/Output	PC0 pin: clock line is used in open-drain mode.
	I2C3_SDA pin	Input/Output	PC1 pin: data line is used in open-drain mode.
SPI1 bootloader	SPI1	Enabled	The SPI1 configuration is: – Slave mode – Full Duplex – 8-bit MSB – Speed up to 8 MHz – Polarity: CPOL Low, CPHA Low, NSS hardware.
	SPI1_MOSI pin	Input	PA7 pin: Slave data Input line, used in push-pull pull-down mode
	SPI1_MISO pin	Output	PA6 pin: Slave data output line, used in push-pull pull-down mode
	SPI1_SCK pin	Input	PA5 pin: Slave clock line, used in push-pull pull-down mode
	SPI1_NSS pin	Input	PA4 pin: slave chip select pin used in push-pull pull-up mode. Note: This IO can be tied to Gnd if the SPI Master does not use it.
SPI2 bootloader	SPI2	Enabled	The SPI2 configuration is: – Slave mode – Full Duplex – 8-bit MSB – Speed up to 8 MHz – Polarity: CPOL Low, CPHA Low, NSS hardware.
	SPI2_MOSI pin	Input	PB15 pin: Slave data Input line, used in push-pull pull-down mode
	SPI2_MISO pin	Output	PB14 pin: Slave data output line, used in push-pull pull-down mode
	SPI2_SCK pin	Input	PB13 pin: Slave clock line, used in push-pull pull-down mode
	SPI2_NSS pin	Input	PB12 pin: slave chip select pin used in push-pull pull-up mode. **Note:** This IO can be tied to Gnd if the SPI Master does not use it.

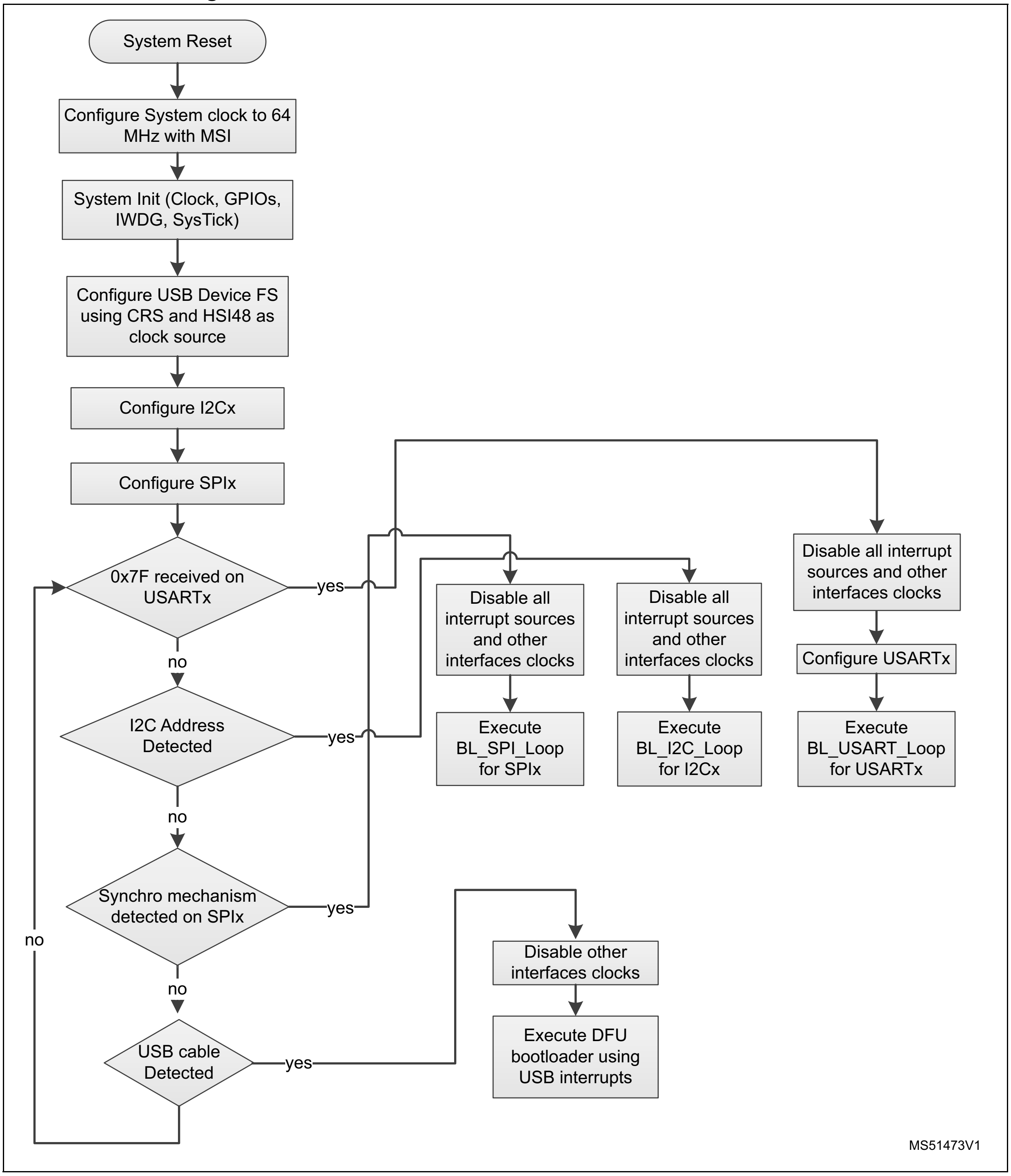
Table 135. STM32WB50xx/55xx configuration in system memory boot mode (continued)

Bootloader	Feature/Peripheral	State	Comment
DFU bootloader	USB	Enabled	USB FS configured in forced device mode. USB FS interrupt vector is enabled and used for USB DFU communications. **Note:** VDDUSB IO must be connected to 3.3V for USB to be operational.
	USB_DM pin	Input/Output	PA11: USB DM line.
	USB_DP pin		PA12: USB DP line No external Pull-up resistor is required

62.2 Bootloader selection

The figure below shows the bootloader selection mechanism.

Figure 86. Bootloader V13.0 selection for STM32WB50xx/55xx



62.3 Bootloader version

Table 136. STM32WB50xx/55xx bootloader versions

Bootloader version number	Description	Known limitations
V13.5	Initial bootloader version	– Readout Unprotect Command is not working properly as at the end of the command an NVIC_SystemReset is done instead of a FLASH option bytes reload. This makes the change of the RDP level not effective until a power off power on.

Note: Instability when performing multiple resets during operations ongoing causing Overrun or FrameError errors on USART Bootloader and not recoverable unless Hardware Reset is performed. Fixed by workaround in FUS V1.0.1 and V1.0.2.

63 STM32WLE5xx devices bootloader

63.1 Bootloader configuration

The STM32WLE5xx bootloader is activated by applying pattern13 (described in *Table 2: Bootloader activation patterns*). The following table shows the hardware resources used by this bootloader.

Table 137. STM32WLE5xx configuration in system memory boot mode

Bootloader	Feature/Peripheral	State	Comment
Common to all bootloaders	RCC	HSI enabled	The system clock frequency is 48 MHz (using PLL clocked by HSI).
	RAM	-	8 Kbytes starting from address 0x20000000 are used by the bootloader firmware
	System memory	-	16 Kbytes starting from address 0x1FFF0000, contain the bootloader firmware
	IWDG	-	The independent watchdog (IWDG) prescaler is configured to its maximum value. It is periodically refreshed to prevent watchdog reset (in case the hardware IWDG option was previously enabled by the user).
USART1 bootloader	USART1	Enabled	Once initialized the USART1 configuration is: 8-bits, even parity and 1 Stop bit
	USART1_RX pin	Input	PA10 pin: USART1 in reception mode
	USART1_TX pin	Output	PA9 pin: USART1 in transmission mode
USART2 bootloader	USART2	Enabled	Once initialized the USART1 configuration is: 8-bits, even parity and 1 Stop bit
	USART2_RX pin	Input	PA3 pin: USART1 in reception mode
	USART2_TX pin	Output	PA2 pin: USART1 in transmission mode

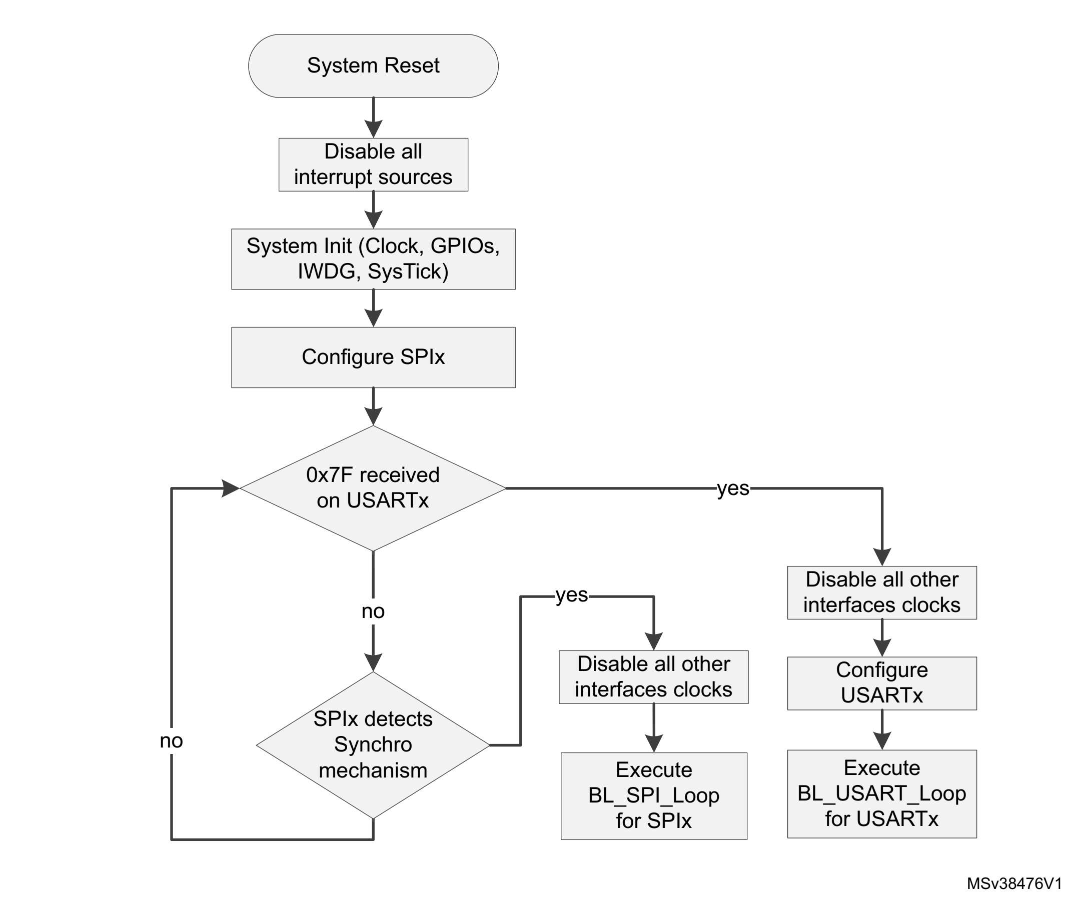
Table 137. STM32WLE5xx configuration in system memory boot mode (continued)

Bootloader	Feature/Peripheral	State	Comment
SPI1 bootloader	SPI1	Enabled	The SPI1 configuration is: – Slave mode – Full Duplex – 8-bit MSB – Speed up to 8 MHz – Polarity: CPOL Low, CPHA Low, NSS hardware.
	SPI1_MOSI pin	Input	PA7 pin: Slave data Input line, used in push-pull pull-down mode
	SPI1_MISO pin	Output	PA6 pin: Slave data output line, used in push-pull pull-down mode
	SPI1_SCK pin	Input	PA5 pin: Slave clock line, used in push-pull pull-down mode
	SPI1_NSS pin	Input	PA4 pin: slave chip select pin used in push-pull pull-up mode. Note: This IO can be tied to Gnd if the SPI Master does not use it.
SPI2 bootloader	SPI2	Enabled	The SPI2 configuration is: – Slave mode – Full Duplex – 8-bit MSB – Speed up to 8 MHz – Polarity: CPOL Low, CPHA Low, NSS hardware.
	SPI2_MOSI pin	Input	PB15 pin: Slave data Input line, used in push-pull pull-down mode
	SPI2_MISO pin	Output	PB14 pin: Slave data output line, used in push-pull pull-down mode
	SPI2_SCK pin	Input	PB13 pin: Slave clock line, used in push-pull pull-down mode
	SPI2_NSS pin	Input	PB12 pin: slave chip select pin used in push-pull pull-up mode. **Note:** This IO can be tied to Gnd if the SPI Master does not use it.

63.2 Bootloader selection

The figure below shows the bootloader selection mechanism.

Figure 87. Bootloader V12.x selection for STM32WLE5xx



63.3 Bootloader version

Table 138. STM32WLE5xx bootloader versions

Bootloader version number	Description	Known limitations
V12.2	Initial bootloader version on cut 1.1 samples	– None

64 Device-dependent bootloader parameters

The bootloader protocol's command set and sequences for each serial peripheral are the same for all STM32 devices. However, some parameters depend on device and bootloader version:

- PID (Product ID)
- Valid RAM memory addresses (RAM area used during bootloader execution is not accessible) accepted by the bootloader when the Read Memory, Go and Write Memory commands are requested.
- System Memory area.

The table below shows the values of these parameters for each STM32 device bootloader in production.

Table 139. Bootloader device-dependent parameters

STM32 series	Device	PID	BL ID	RAM memory	System memory
F0	STM32F05xxx and STM32F030x8 devices	0x440	0x21	0x20000800 - 0x20001FFF	0x1FFFEC00 - 0x1FFFF7FF
	STM32F03xx4/6	0x444	0x10	0x20000800 - 0x20000FFF	
	STM32F030xC	0x442	0x52	0x20001800 - 0x20007FFF	0x1FFFD800 - 0x1FFFF7FF
	STM32F04xxx	0x445	0xA1	NA	0x1FFFC400 - 0x1FFFF7FF
	STM32F070x6	0x445	0xA2	NA	0x1FFFC400 - 0x1FFFF7FF
	STM32F070xB	0x448	0xA2	NA	0x1FFFC800 - 0x1FFFF7FF
	STM32F071xx/072xx	0x448	0xA1	0x20001800 - 0x20003FFF	0x1FFFC800 - 0x1FFFF7FF
	STM32F09xxx	0x442	0x50	NA	0x1FFFD800 - 0x1FFFF7FF

Table 139. Bootloader device-dependent parameters (continued)

STM32 series	Device		PID	BL ID	RAM memory	System memory
F1	STM32F10xxx	Low-density	0x412	NA	0x20000200 - 0x200027FF	0x1FFFF000 - 0x1FFFF7FF
		Medium-density	0x410	NA	0x20000200 - 0x20004FFF	
		High-density	0x414	NA	0x20000200 - 0x2000FFFF	
		Medium-density value line	0x420	0x10	0x20000200 - 0x20001FFF	
		High-density value line	0x428	0x10	0x20000200 - 0x20007FFF	
	STM32F105xx/107xx		0x418	NA	0x20001000 - 0x2000FFFF	0x1FFFB000 - 0x1FFFF7FF
	STM32F10xxx XL-density		0x430	0x21	0x20000800 - 0x20017FFF	0x1FFFE000 - 0x1FFFF7FF
F2	STM32F2xxxx		0x411	0x20	0x20002000 - 0x2001FFFF	0x1FFF0000 - 0x1FFF77FF
				0x33		
F3	STM32F373xx		0x432	0x41	0x20001400 - 0x20007FFF	0x1FFFD800 - 0x1FFFF7FF
	STM32F378xx			0x50	0x20001000 - 0x20007FFF	
	STM32F302xB(C)/303xB(C)		0x422	0x41	0x20001400 - 0x20009FFF	
	STM32F358xx			0x50		
	STM32F301xx/302x4(6/8)		0x439	0x40	0x20001800 - 0x20003FFF	
	STM32F318xx			0x50		
	STM32F303x4(6/8)/ 334xx/328xx		0x438	0x50	0x20001800 - 0x20002FFF	
	STM32F302xD(E)/303xD(E)		0x446	0x40	0x20001800 - 0x2000FFFF	
	STM32F398xx		0x446	0x50	0x20001800 - 0x2000FFFF	

Table 139. Bootloader device-dependent parameters (continued)

STM32 series	Device	PID	BL ID	RAM memory	System memory
F4	STM32F40xxx/41xxx	0x413	0x31	0x20002000 - 0x2001FFFF	0x1FFF0000 - 0x1FFF77FF
			0x90	0x20003000 - 0x2001FFFF	
	STM32F42xxx/43xxx	0x419	0x70	0x20003000 - 0x2002FFFF	
			0x91		
	STM32F401xB(C)	0x423	0xD1	0x20003000 - 0x2000FFFF	
	STM32F401xD(E)	0x433	0xD1	0x20003000 - 0x20017FFF	
	STM32F410xx	0x458	0xB1	0x20003000 - 0x20007FFF	
	STM32F411xx	0x431	0xD0	0x20003000 - 0x2001FFFF	
	STM32F412xx	0x441	0x90	0x20003000 - 0x2003FFFF	
	STM32F446xx	0x421	0x90	0x20003000 - 0x2001FFFF	
	STM32F469xx/479xx	0x434	0x90	0x20003000 - 0x2005FFFF	
	STM32F413xx/423xx	0x463	0x90	0x20003000 - 0x2004FFFF	
F7	STM32F72xxx/73xxx	0x452	0x90	0x20004000 - 0x2003FFFF	0x1FF00000 - 0x1FF0EDBF
	STM32F74xxx/75xxx	0x449	0x70	0x20004000 - 0x2004FFFF	0x1FF00000 - 0x1FF0EDBF
			0x90	0x20004000 - 0x2004FFFF	0x1FF00000 - 0x1FF0EDBF
	STM32F76xxx/77xxx	0x451	0x93	0x20004000 - 0x2007FFFF	0x1FF00000 - 0x1FF0EDBF
G0	STM32G03xxx/04xxx	0x466	0x52	0x20000000 - 0x20000FFF	0x1FFF0000 - 0x1FFF1FFF
	STM32G07xxx/08xxx	0x460	0xB2	0x20000000 - 0x200026FF	0x1FFF0000 - 0x1FFF6FFF
G4	STM32G431xx/441xx	0x468	0xD3	0x20000000 – 0x20004000	0x1FFF0000 - 0x1FFF7000
	STM32G47xxx/48xxx	0x469	0xD4	0x20000000 – 0x20004000	0x1FFF0000 - 0x1FFF7000

Table 139. Bootloader device-dependent parameters (continued)

STM32 series	Device	PID	BL ID	RAM memory	System memory
H7	STM32H74xxx/75xxx	0x450	0x90	0x20004100 - 0x2001FFFF 0x24034000 - 0x2407FFFF	0x1FF00000 - 0x1FF1E7FF
	STM32H7A3xx/B3xx	0x480	0x90	0x20004100 - 0x2001FFFF 0x24034000 - 0x2407FFFF	0x1FF00000 - 0x1FF13FFF
L0	STM32L01xxx/02xxx	0x457	0xC3	NA	0x1FF00000 - 0x1FF00FFF
	STM32L031xx/041xx	0x425	0xC0	0x20001000 - 0x20001FFF	0x1FF00000 - 0x1FF00FFF
	STM32L05xxx/06xxx	0x417	0xC0	0x20001000 - 0x20001FFF	0x1FF00000 - 0x1FF00FFF
	STM32L07xxx/08xxx	0x447	0x41	0x20001000 - 0x20004FFF	0x1FF00000 - 0x1FF01FFF
			0xB2	0x20001400 - 0x20004FFF	
L1	STM32L1xxx6(8/B)	0x416	0x20	0x20000800 - 0x20003FFF	0x1FF00000 - 0x1FF01FFF
	STM32L1xxx6(8/B)A	0x429	0x20	0x20001000 - 0x20007FFF	
	STM32L1xxxC	0x427	0x40		
	STM32L1xxxD	0x436	0x45	0x20001000 - 0x2000BFFF	
	STM32L1xxxE	0x437	0x40	0x20001000 - 0x20013FFF	
L4	STM32L412xx/422xx	0x464	0xD1	0x20000000 - 0x200020FF	0x1FFF0000 - 0x1FFF6FFF
	STM32L43xxx/44xxx	0x435	0x91	0x20003100 - 0x2000BFFF	0x1FFF0000 - 0x1FFF6FFF
	STM32L45xxx/46xxx	0x462	0x92	0x20003100 - 0x2001FFFF	0x1FFF0000 - 0x1FFF6FFF
	STM32L47xxx/48xxx	0x415	0xA3	0x20003000 - 0x20017FFF	0x1FFF0000 - 0x1FFF6FFF
			0x92	0x20003100 - 0x20017FFF	
	STM32L496xx/4A6xx	0x461	0x93	0x20003100 - 0x2003FFFF	0x1FFF0000 - 0x1FFF6FFF
	STM32L4Rxx/4Sxx	0x470	0x95	0x20003200 - 0x2009FFFF	0x1FFF0000 - 0x1FFF6FFF
	STM32L4P5xx /Q5xx	0x471	0x90	0x20004000 - 0x2004FFFF	0x1FFF0000 - 0x1FFF6FFF

Table 139. Bootloader device-dependent parameters (continued)

STM32 series	Device	PID	BL ID	RAM memory	System memory
L5	STM32L552xx/562xx	0x472	0x92	0x20000000 - 0x20004000	0x0BF90000 - 0x0BF97FFF
WB	STM32WB50xx/WB55xx	0x495	0xD5	0x20000000 – 0x20005000	0x1FFF0000 - 0x1FFF7000
WL	STM32WLE5xx	0x497	0xC2	0x20000000 – 0x20001FFF	0x1FFF0000 - 0x1FFF3FFF

65 Bootloader timing

This section presents the typical timings of the bootloader firmware that should be used to ensure correct synchronization between host and STM32 device.

Two types of timings will be described herein:

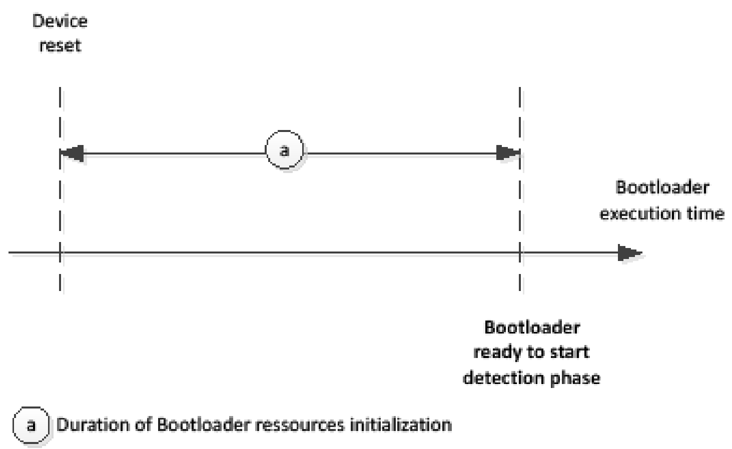
- STM32 device bootloader resources initialization duration.
- Communication interface selection duration.

After these timings the bootloader is ready to receive and execute host commands.

65.1 Bootloader Startup timing

After bootloader reset, the host should wait until the STM32 bootloader is ready to start detection phase with a specific interface communication. This time corresponds to bootloader startup timing, during which resources used by bootloader are initialized.

Figure 88. Bootloader Startup timing description



The table below contains the minimum startup timing for each STM32 product:

Table 140. Bootloader startup timings of STM32 devices

<table>
<tr><th colspan="2">Device</th><th>Minimum bootloader Startup (ms)</th><th>HSE Timeout (ms)</th></tr>
<tr><td colspan="2">STM32F03xx4/6</td><td>1.612</td><td>NA</td></tr>
<tr><td colspan="2">STM32F05xxx and STM32F030x8 devices</td><td>1.612</td><td>NA</td></tr>
<tr><td colspan="2">STM32F04xxx</td><td>0.058</td><td>NA</td></tr>
<tr><td colspan="2">STM32F071xx/072xx</td><td>0.058</td><td>NA</td></tr>
<tr><td rowspan="2">STM32F070x6</td><td>HSE connected</td><td>3</td><td rowspan="2">200</td></tr>
<tr><td>HSE not connected</td><td>230</td></tr>
</table>

Table 140. Bootloader startup timings of STM32 devices (continued)

Device		Minimum bootloader Startup (ms)	HSE Timeout (ms)
STM32F070xB	HSE connected	6	200
	HSE not connected	230	
STM32F09xxx		2	NA
STM32F030xC		2	NA
STM32F10xxx		1.227	NA
STM32F105xx/107xx	PA9 pin low	1.396	NA
	PA9 pin high	524.376	
STM32F10xxx XL-density		1.227	NA
STM32F2xxxx	V2.x	134	NA
	V3.x	84.59	0.790
STM32F301xx/302x4(6/8)	HSE connected	45	560.5
	HSE not connected	560.8	
STM32F302xB(C)/303xB(C)	HSE connected	43.4	2.236
	HSE not connected	2.36	
STM32F302xD(E)/303xD	HSE connected	7.53	NA
	HSE not connected	146.71	NA
STM32F303x4(6/8)/334xx/328xx		0.155	NA
STM32F318xx		0.182	NA
STM32F358xx		1.542	NA
STM32F373xx	HSE connected	43.4	2.236
	HSE not connected	2.36	
STM32F378xx		1.542	NA
STM32F398xx		1.72	NA
STM32F40xxx/41xxx	V3.x	84.59	0.790
	V9.x	74	96
STM32F401xB(C)		74.5	85
STM32F401xD(E)		74.5	85
STM32F410xx		0.614	NA
STM32F411xx		74.5	85
STM32F412xx		0.614	180
STM32F413xx/423xx		0.642	165
STM32F429xx/439xx	V7.x	82	97
	V9.x	74	97

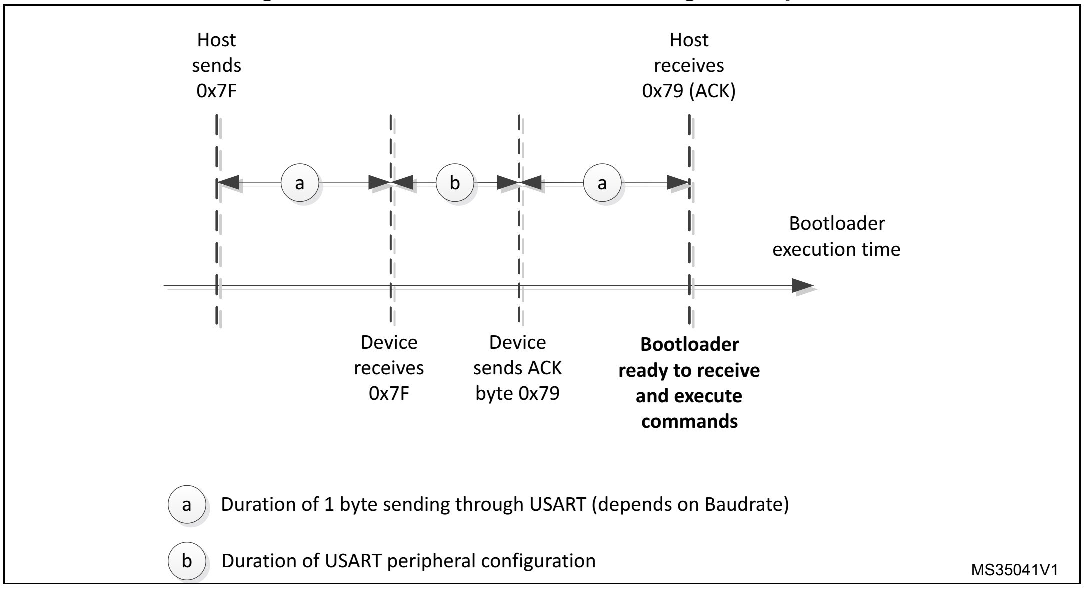
Table 140. Bootloader startup timings of STM32 devices (continued)

Device			Minimum bootloader Startup (ms)	HSE Timeout (ms)
STM32F446xx			73.61	96
STM32F469xx/479xx			73.68	230
STM32F72xxx/73xxx			17.93	50
STM32F74xxx/75xxx			16.63	50
STM32G03xxx/04xxx			0.390	NA
STM32G07xxx/08xxx			0.390	NA
STM32G4xxxx			0.390	NA
STM32H74xxx/75xxx			53.975	2
STM32H7A3xx/B3xx			53.975	NA
STM32L01xxx/02xxx			0.63	NA
STM32L031xx/041xx			0.62	NA
STM32L05xxx/06xxx			0.22	NA
STM32L07xxx/08xxx	V4.x		0.61	NA
	V11.x		0.71	NA
STM32L1xxx6(8/B)A			0.542	NA
STM32L1xxx6(8/B)			0.542	NA
STM32L1xxxC			0.708	80
STM32L1xxxD			0.708	80
STM32L1xxxE			0.708	200
STM32L43xxx/44xxx			0.3335	100
STM32L45xxx/46xxx			50.93	NA
STM32L47xxx/48xxx	V10.x	LSE connected	55	100
		LSE not connected	2560	
	V9.x	LSE connected	55.40	100
		LSE not connected	2560.51	
STM32L412xx/422xx			0.12	NA
STM32L496xx/4A6xx			76.93	100
STM32L4P5xx /Q5xx			NA	NA
STM32L4Rxx/4Sxx			NA	NA
STM32L552xx/562xx			0.390	NA
STM32WB50xx/55xx			0.390	NA
STM32WLE5xx			0.390	NA

65.2 USART connection timing

USART connection timing is the time that the host should wait for between sending the synchronization data (0x7F) and receiving the first acknowledge response (0x79).

Figure 89. USART connection timing description



1. Receiving any other character different from 0x7F (or line glitches) will cause bootloader to start communication using a wrong baudrate. Bootloader measures the signal length between rising edge of first 1 bit in 0x7F to the falling edge of the last 1 bit in 0x7F to deduce the baudrate value
2. Bootloader does not re-align the calculated baudrate to standard baudrate values (ie. 1200, 9600, 115200, ...).

Note: For STM32F105xx/107xx line devices, PA9 pin (USB_VBUS) is used to detect the USB host connection. The initialization of USB peripheral is performed only if PA9 is high at detection phase which means that a host is connected to the port and delivering 5 V on the USB bus. When PA9 level is high at detection phase, more time is required to initialize and shutdown the USB peripheral. To minimize bootloader detection time when PA9 pin is not used, keep PA9 state low during USART detection phase from the moment the device is reset till a device ACK is sent.

Table 141. USART bootloader minimum timings of STM32 devices

Device	One USART byte sending (ms)	USART configuration (ms)	USART connection (ms)
STM32F03xx4/6	0.078125	0.0064	0.16265
STM32F05xxx and STM32F030x8 devices	0.078125	0.0095	0.16575
STM32F04xxx	0.078125	0.007	0.16325
STM32F071xx/072xx	0.078125	0.007	0.16325
STM32F070x6	0.078125	0.014	0.17
STM32F070xB	0.078125	0.08	0.23

Table 141. USART bootloader minimum timings of STM32 devices (continued)

Device		One USART byte sending (ms)	USART configuration (ms)	USART connection (ms)
STM32F09xxx		0.078125	0.07	0.22
STM32F030xC		0.078125	0.07	0.22
STM32F10xxx		0.078125	0.002	0.15825
STM32F105xx/107xx	PA9 pin low	0.078125	0.007	0.16325
	PA9 pin High		105	105.15625
STM32F10xxx XL-density		0.078125	0.006	0.16225
STM32F2xxxx	V2.x	0.078125	0.009	0.16525
	V3.x			
STM32F301xx/302x4(6/8)	HSE connected	0.078125	0.002	0.15825
	HSE not connected			
STM32F302xB(C)/303xB(C)	HSE connected	0.078125	0.002	0.15825
	HSE not connected			
STM32F302xD(E)/303xD		0.078125	0.002	0.15885
STM32F303x4(6/8)/334xx/328xx		0.078125	0.002	0.15825
STM32F318xx		0.078125	0.002	0.15825
STM32F358xx		0.15625	0.001	0.3135
STM32F373xx	HSE connected	0.078125	0.002	0.15825
	HSE not connected			
STM32F378xx		0.15625	0.001	0.3135
STM32F398xx		0.078125	0.002	0.15885
STM32F40xxx/41xxx	V3.x	0.078125	0.009	0.16525
	V9.x		0.0035	0.15975
STM32F401xB(C)		0.078125	0.00326	0.15951
STM32F401xD(E)		0.078125	0.00326	0.15951
STM32F410xx		0.078125	0.002	0.158
STM32F411xx		0.078125	0.00326	0.15951
STM32F412xx		0.078125	0.002	0.158
STM32F413xx/423xx		0.078125	0.002	0.158
STM32F429xx/439xx	V7.x	0.078125	0.007	0.16325
	V9.x		0.00326	0.15951
STM32F446xx		0.078125	0.004	0.16
STM32F469xx/479xx		0.078125	0.003	0.159
STM32F72xxx/73xxx		0.078125	0.070	0.22

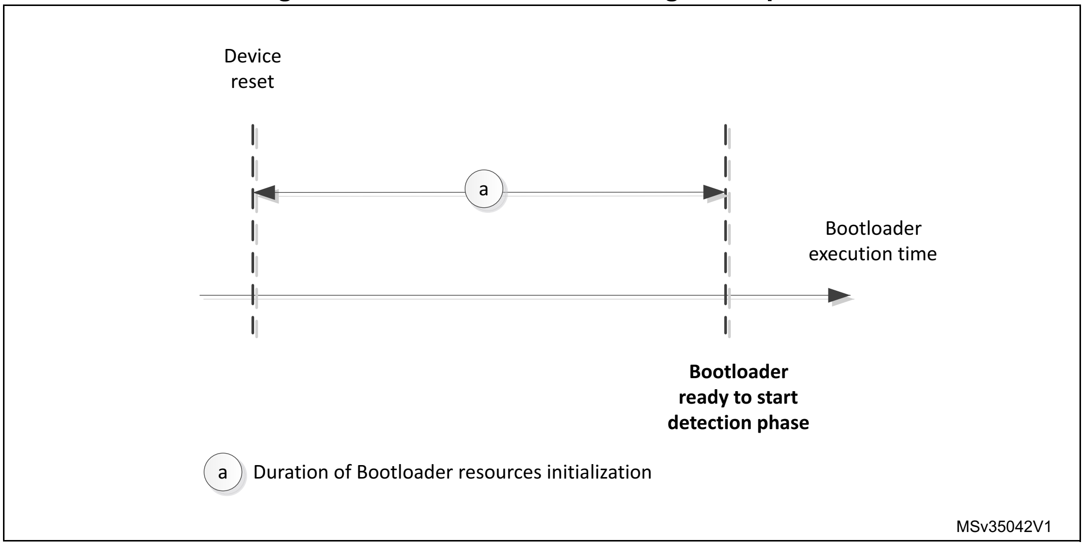
Table 141. USART bootloader minimum timings of STM32 devices (continued)

Device		One USART byte sending (ms)	USART configuration (ms)	USART connection (ms)
STM32F74xxx/75xxx		0.078125	0.065	0.22
STM32G03xxx/04xxx		0.078125	0.01	0.11
STM32G07xxx/08xxx		0.078125	0.01	0.11
STM32G4xxxx		0.078125	0.003	0.159
STM32H74xxx/75xxx		0.078125	0.072	0.22825
STM32H7A3xx/B3xx		0.078125	0.072	0.22825
STM32L01xxx/02xxx		0.078125	0.016	0.17
STM32L031xx/041xx		0.078125	0.018	0.174
STM32L05xxx/06xxx		0.078125	0.018	0.17425
STM32L07xxx/08xxx	V4.x	0.078125	0.017	0.173
	V11.x	0.078125	0.017	0.158
STM32L1xxx6(8/B)A		0.078125	0.008	0.16425
STM32L1xxx6(8/B)		0.078125	0.008	0.16425
STM32L1xxxC		0.078125	0.008	0.16425
STM32L1xxxD		0.078125	0.008	0.16425
STM32L1xxxE		0.078125	0.008	0.16425
STM32L412xx/422xx		0.078125	0.005	0.2
STM32L43xxx/44xxx		0.078125	0.003	0.159
STM32L45xxx/46xxx		0.078125	0.07	0.22
STM32L47xxx/48xxx	V10.x	0.078125	0.003	0.159
	V9.x	0.078125	0.003	0.159
STM32L496xx/4A6xx		0.078125	0.003	0.159
STM32L4Rxx/4Sxx		NA	NA	NA
STM32L4P5xx/4Q5xx		NA	NA	NA
STM32L552xx/562xx		0.078125	0.01	0.11
STM32WB50xx/55xx		0.078125	0.003	0.159
STM32WLE5xx		0.078125	0.001	0.110

65.3 USB connection timing

USB connection timing is the time that the host should wait for between plugging the USB cable and establishing a correct connection with the device. This timing includes enumeration and DFU components configuration. USB connection depends on the host.

Figure 90. USB connection timing description



Note: For STM32F105xx/107xx devices, if the external HSE crystal frequency is different from 25 MHz (14.7456 MHz or 8 MHz), the device performs several unsuccessful enumerations (with connect – disconnect sequences) before being able to establish a correct connection with the host. This is due to the HSE automatic detection mechanism based on Start Of Frame (SOF) detection.

Table 142. USB bootloader minimum timings of STM32 devices

Device		USB connection (ms)
STM32F04xxx		350
STM32F070x6		TBD
STM32F070xB		320
STM32F105xx/107xx	HSE = 25 MHz	460
	HSE = 14.7465 MHz	4500
	HSE = 8 MHz	13700
STM32F2xxxx		270
STM32F301xx/302x4(6/8)		300
STM32F302xB(C)/303xB(C)		300
STM32F302xD(E)/303xD		100
STM32F373xx		300
STM32F40xxx/41xxx	V3.x	270
	V9.x	250
STM32F401xB(C)		250
STM32F401xD(E)		250
STM32F411xx		250
STM32F412xx		380
STM32F413xx/423xx		350

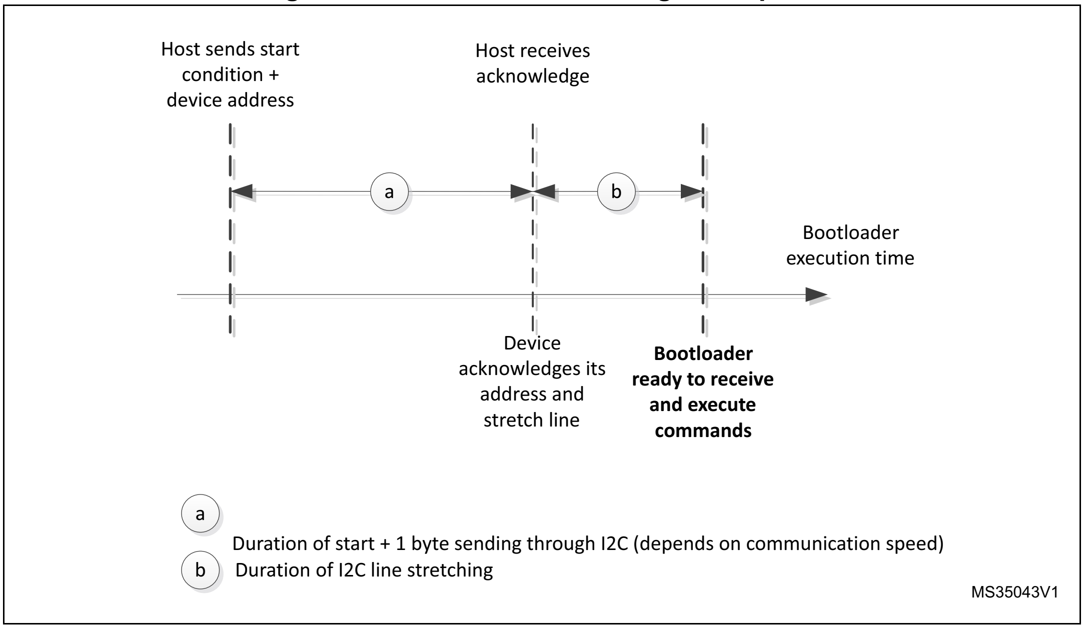
Table 142. USB bootloader minimum timings of STM32 devices (continued)

<table>
<tr><th colspan="2">Device</th><th>USB connection (ms)</th></tr>
<tr><td rowspan="2">STM32F429xx/439xx</td><td>V7.x</td><td rowspan="2">250</td></tr>
<tr><td>V9.x</td></tr>
<tr><td colspan="2">STM32F446xx</td><td>200</td></tr>
<tr><td colspan="2">STM32F469xx/479xx</td><td>270</td></tr>
<tr><td colspan="2">STM32F72xxx/73xxx</td><td>320</td></tr>
<tr><td colspan="2">STM32F74xxx/75xxx</td><td>230</td></tr>
<tr><td colspan="2">STM32G4xxxx</td><td>300</td></tr>
<tr><td colspan="2">STM32H74xxx/75xxx</td><td>53.9764</td></tr>
<tr><td colspan="2">STM32H7A3xx/B3xx</td><td>53.9764</td></tr>
<tr><td colspan="2">STM32L07xxx/08xxx</td><td>140</td></tr>
<tr><td colspan="2">STM32L1xxxC</td><td>849</td></tr>
<tr><td colspan="2">STM32L1xxxD</td><td>849</td></tr>
<tr><td colspan="2">STM32L412xx/422xx</td><td>820</td></tr>
<tr><td colspan="2">STM32L43xxx/44xxx</td><td>820</td></tr>
<tr><td colspan="2">STM32L45xxx/46xxx</td><td>330</td></tr>
<tr><td rowspan="2">STM32L47xxx/48xxx</td><td>V10.x</td><td rowspan="2">300</td></tr>
<tr><td>V9.x</td></tr>
<tr><td colspan="2">STM32L496xx/4A6xx</td><td>430</td></tr>
<tr><td colspan="2">STM32L4P5xx/4Q5xx</td><td>NA</td></tr>
<tr><td colspan="2">STM32L4Rxx/4Sxx</td><td>NA</td></tr>
<tr><td colspan="2">STM32L552xx/L562xx</td><td>300</td></tr>
<tr><td colspan="2">STM32WB50xx/55xx</td><td>300</td></tr>
</table>

65.4 I2C connection timing

I2C connection timing is the time that the host should wait for between sending I2C device address and sending command code. This timing includes I2C line stretching duration.

Figure 91. I2C connection timing description



Note: For I2C communication, a timeout mechanism is implemented and it must be respected to execute bootloader commands correctly. This timeout is implemented between two I2C frames in the same command (eg: for Write memory command a timeout is inserted between command sending frame and address memory sending frame). Also the same timeout period is inserted between two successive data reception or transmission in the same I2C frame. If the timeout period is elapsed a system reset is generated to avoid bootloader crash.

In erase memory command and read-out unprotect command, the duration of flash operation should be taken into consideration when implementing the host side. After sending the code of pages to be erased, the host should wait until the bootloader device performs page erasing to complete the remaining steps of erase command.

Table 143. I2C bootloader minimum timings of STM32 devices

Device	Start condition + one I2C byte sending (ms)	I2C line stretching (ms)	I2C connection (ms)	I2C Timeout (ms)
STM32F04xxx	0.0225	0.0025	0.0250	1000
STM32F070x6	0.0225	0.0025	0.0245	1000
STM32F070xB	0.0225	0.0025	0.0245	1000
STM32F071xx/072xx	0.0225	0.0025	0.0250	1000
STM32F09xxx	0.0225	0.0025	0.0245	1000
STM32F030xC	0.0225	0.0025	0.0250	1000

Table 143. I2C bootloader minimum timings of STM32 devices (continued)

Device		Start condition + one I2C byte sending (ms)	I2C line stretching (ms)	I2C connection (ms)	I2C Timeout (ms)
STM32F303x4(6/8)/334xx/328xx		0.0225	0.0027	0.0252	1000
STM32F318xx		0.0225	0.0027	0.0252	1000
STM32F358xx		0.0225	0.0055	0.0280	10
STM32F378xx		0.0225	0.0055	0.0280	10
STM32F398xx		0.0225	0.0020	0.0245	1500
STM32F40xxx/41xxx		0.0225	0.0022	0.0247	1000
STM32F401xB(C)		0.0225	0.0022	0.0247	1000
STM32F401xD(E)		0.0225	0.0022	0.0247	1000
STM32F410xx		0.0225	0.0020	0.0245	1000
STM32F411xx		0.0225	0.0022	0.0247	1000
STM32F412xx		0.0225	0.0020	0.0245	1000
STM32F413xx/423xx		0.0225	0.0020	0.0245	1000
STM32F42xxx/43xxx	V7.x	0.0225	0.0033	0.0258	1000
	V9.x	0.0225	0.0022	0.0247	1000
STM32F446xx		0.0225	0.0020	0.0245	1000
STM32F469xx/479xx		0.0225	0.0020	0.0245	1000
STM32F72xxx/73xxx		0.0225	0.0020	0.0245	1000
STM32F74xxx/75xxx		0.0225	0.0020	0.0245	500
STM32G03xxx/04xxx		0.0225	0.0020	0.0245	1000
STM32G07xxx/08xxx		0.0225	0.0020	0.0245	1000
STM32G4xxxx		0.0225	0.0020	0.0245	1000
STM32H74xxx/75xxx		0.0225	0.05	0.0725	1000
STM32H7A3xx/7B3xx		0.0225	0.05	0.0745	1000
STM32L07xxx/08xxx		0.0225	0.0020	0.0245	1000
STM32L412xx/422xx		0.0225	0.0020	0.o245	1000
STM32L43xxx/44xxx		0.0225	0.0020	0.0245	1000
STM32L45xxx/46xxx		0.0225	0.0020	0.0245	1000
STM32L47xxx/48xxx	V10.x	0.0225	0.0020	0.0245	1000
	V9.x	0.0225	0.0020	0.0245	1000
STM32L496xx/4A6xx		0.0225	0.0020	0.0245	1000
STM32L4P5xx/4Q5xx		NA	NA	NA	NA
STM32L4Rxx/4Sxx		NA	NA	NA	NA

Table 143. I2C bootloader minimum timings of STM32 devices (continued)

Device	Start condition + one I2C byte sending (ms)	I2C line stretching (ms)	I2C connection (ms)	I2C Timeout (ms)
STM32L552xx/L562xx	0.0225	0.0020	0.0245	1000
STM32WB50xx/55xx	0.0225	0.0020	0.0245	1000

65.5 SPI connection timing

SPI connection timing is the time that the host should wait for between sending the synchronization data (0xA5) and receiving the first acknowledge response (0x79).

Figure 92. SPI connection timing description

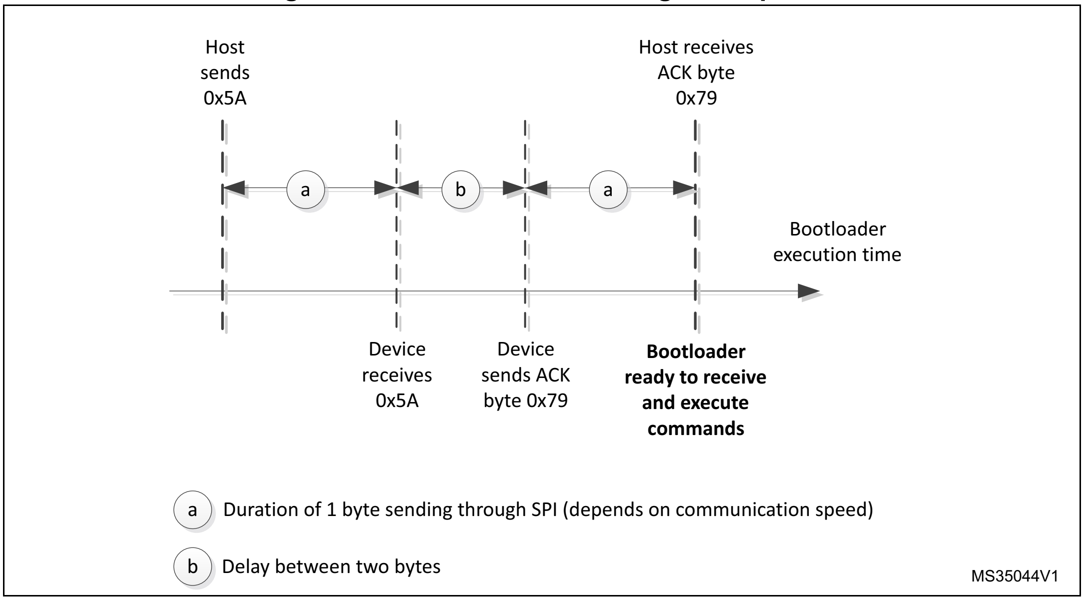


Table 144. SPI bootloader minimum timings of STM32 devices

Device	One SPI byte sending (ms)	Delay between two bytes (ms)	SPI connection (ms)
All products	0.001	0.008	0.01

Appendix A Example of function to use the “ExitSecureMemory” function

```
/**
************************************************************************
****
* @file    main.c
************************************************************************
****
*/

/* Includes ------------------------------------------------------------
---*/
#include "main.h"

/* Private function prototypes ------------------------------------------
---*/
static void ConfigClock(void);

void JUMP_WITHOUT_PARAM(uint32_t jump_address);
void JUMP_WITH_PARAM(uint32_t jump_address, uint32_t magic, uint32_t
applicationVectorAddress);

/* Private functions ----------------------------------------------------
---*/

/**
* @brief  Main program
* @param  None
* @retval None
*/
int main(void)
{
  ConfigClock();

  uint32_t application_address                     = 0x08000800;
  uint32_t exit_secure_memory_address   = 0x1FFF1E00;
  uint32_t magic_number                              = 0x08192A3C;
  uint32_t exit_with_magic_number           = 0x0;

  if (exit_with_magic_number)
  {
    JUMP_WITH_PARAM(exit_secure_memory_address, magic_number,
application_address);
  }
```

```
  else
  {
    JUMP_WITHOUT_PARAM(exit_secure_memory_address);
  }
}

/**
* @brief  ConfigClock
* @param  None
* @retval None
*/
static void ConfigClock(void)
{
  /* Will be developped as per the template of the needed project */
}

/**
* @brief  JUMP_WITHOUT_PARAM
* @param  jump_address
* @retval None
*/
void JUMP_WITHOUT_PARAM(uint32_t jump_address)
{
  asm ("LDR R1, [R0]");     // jump_address
  asm ("LDR R2, [R0,#4]");
  asm ("MOV SP, R1");
  asm ("BX  R2");
}

/**
* @brief  JUMP_WITH_PARAM
* @param  jump_address, magic, applicationVectorAddress
* @retval None
*/
void JUMP_WITH_PARAM(uint32_t jump_address, uint32_t magic, uint32_t
applicationVectorAddress))
{
  asm ("MOV R3, R0");       // jump_address
  asm ("LDR R0, [R3]");
  asm ("MOV SP, R0");
  asm ("LDR R0, [R3,#4]");
  asm ("BX R0");
}
```

```
/************************ (C) COPYRIGHT STMicroelectronics *****END OF
FILE****/
```

66 Revision history

Table 145. Document revision history

Date	Revision	Changes
22-Oct-2007	1	Initial release.
22-Jan-2008	2	All STM32 in production (rev. B and rev. Z) include the bootloader described in this application note. Modified: *Section 3.1: Bootloader activation* and *Section 1.4: Bootloader code sequence*. Added: *Section 1.3: Hardware requirements*, *Section 1.5: Choosing the USART baud rate*, *Section 1.6: Using the bootloader* and *Section:* *Note 2* linked to Get, Get Version & Read Protection Status and Get ID commands in *Table 3: Bootloader commands*, *Note 3* added. Notion of “permanent” (Permanent Write Unprotect/Readout Protect/Unprotect) removed from document. Small text changes. Bootloader version upgraded to 2.0.
26-May-2008	3	Small text changes. RAM and System memory added to *Table : The system clock is derived from the embedded internal high-speed RC, no external quartz is required for the bootloader execution*. *Section 1.6: Using the bootloader on page 8* removed. Erase modified, *Note 3* modified and *Note 1* added in *Table 3: Bootloader commands on page 9*. *Byte 3: on page 11* modified. *Byte 2: on page 13* modified. *Byte 2:*, *Bytes 3-4:* and *Byte 5: on page 15* modified, *Note 3* modified. *Byte 8: on page 18* modified. Notes added to *Section 2.5: Go command on page 18*. *Figure 11: Go command: device side on page 20* modified. Note added in *Section 2.6: Write Memory command on page 21*. *Byte 8: on page 24* modified. *Figure 14: Erase Memory command: host side* and *Figure 15: Erase Memory command: device side* modified. *Byte 3: on page 26* modified. *Table 3: Bootloader commands on page 9*. Note modified and note added in *Section 2.8: Write Protect command on page 27*. *Figure 16: Write Protect command: host side*, *Figure 17: Write Protect command: device side*, *Figure 19: Write Unprotect command: device side*, *Figure 21: Readout Protect command: device side* and *Figure 23: Readout Unprotect command: device side* modified.
29-Jan-2009	4	This application note also applies to the STM32F102xx microcontrollers. Bootloader version updated to V2.2 (see *Table 4: Bootloader versions*).

Table 145. Document revision history (continued)

Date	Revision	Changes
19-Nov-2009	5	IWDG added to *Table : The system clock is derived from the embedded internal high-speed RC, no external quartz is required for the bootloader execution.*. *Note* added. BL changed bootloader in the entire document. Go command description modified in *Table : The system clock is derived from the embedded internal high-speed RC, no external quartz is required for the bootloader execution*. Number of bytes awaited by the bootloader corrected in *Section 2.4: Read Memory command*. Note modified below *Figure 10: Go command: host side*. Note removed in *Section 2.5: Go command* and note added. Start RAM address specified and note added in *Section 2.6: Write Memory command*. All options are erased when a Write Memory command is issued to the Option byte area. *Figure 11: Go command: device side* modified. *Figure 13: Write Memory command: device side* modified. Note added and bytes 3 and 4 sent by the host modified in *Section 2.7: Erase Memory command*. Note added to *Section 2.8: Write Protect command*.
09-Mar-2010	6	Application note restructured. Value line and connectivity line device bootloader added (Replaces AN2662). *Introduction* changed. *Glossary* added.
20-Apr-2010	7	*Related documents*: added XL-density line datasheets and programming manual. *Glossary*: added XL-density line devices. *Table 3*: added information for XL-density line devices. *Section 4.1: Bootloader configuration*: updated first sentence. *Section 5.1: Bootloader configuration*: updated first sentence. Added *Section 6: STM32F10xxx XL-density devices bootloader*. *Table 65*: added information for XL-density line devices.
08-Oct-2010	8	Added information for high-density value line devices in *Table 3* and *Table 65*.
14-Oct-2010	9	Removed references to obsolete devices.
26-Nov-2010	10	Added information on ultralow power devices.
13-Apr-2011	11	Added information related to STM32F205/215xx and STM32F207/217xx devices. Added *Section 32: Bootloader timing*
06-Jun-2011	12	Updated: – *Table 12: STM32L1xxx6(8/B) bootloader versions* – *Table 17: STM32F2xxxx configuration in System memory boot mode* – *Table 18: STM32F2xxxx bootloader V2.x versions* – *Table 20: STM32F2xxxx bootloader V3.x versions*
28-Nov-2011	13	Added information related to STM32F405/415xx and STM32F407/417xx bootloader, and STM32F105xx/107xx bootloader V2.1. Added value line devices in *Section 4: STM32F10xxx devices bootloader* title and overview.

Table 145. Document revision history (continued)

Date	Revision	Changes
30-Jul-2012	14	Added information related to STM32F051x6/STM32F051x8 and to High-density ultralow power STM32L151xx, STM32L152xx bootloader. Added case of BOOT1 bit in *Section 3.1: Bootloader activation*. Updated Connectivity line, High-density ultralow power line, STM32F2xx and STM32F4xx in *Table 3: Embedded bootloaders*. Added bootloader version V2.2 in *Table 8: STM32F105xx/107xx bootloader versions*. Added bootloader V2.2 in *Section 5.3.1: How to identify STM32F105xx/107xx bootloader versions*. Added note related to DFU interface below *Table 15: STM32L1xxxx high-density configuration in System memory boot mode*. Added V4.2 bootloader know limitations and updated description, and added V4.5 bootloader in *Table 16: STM32L1xxxx high-density bootloader versions*. Added note related to DFU interface below *Table 19: STM32F2xxxx configuration in System memory boot mode*. Added V3.2 bootloader know limitations, and added V3.3 bootloader in *Table 20: STM32F2xxxx bootloader V3.x versions*. Updated STM32F2xx and STM32F4xx system memory end address in *Table 21: STM32F40xxx/41xxx configuration in System memory boot mode*. Added note related to DFU interface below *Table 21: STM32F40xxx/41xxx configuration in System memory boot mode*. Added V3.0 bootloader know limitations, and added V3.1 bootloader in *Table 22: STM32F40xxx/41xxx bootloader V3.x version*. Added bootloader V2.1 know limitations in *Table 26: STM32F051xx bootloader versions*. Updated STM32F051x6/x8 system memory end address in *Table 65: Bootloader device-dependent parameters*. Added *Table 75: USART bootloader timings for high-density ultralow power devices*, and *Table 78: USART bootloader timings for STM32F051xx devices*. Added *Table 88: USB minimum timings for high-density ultralow power devices*.

Table 145. Document revision history (continued)

Date	Revision	Changes
24-Jan-2013	15	Updated generic product names throughout the document (see *Glossary*). Added the following new sections: – *Section 8: STM32L1xxxC devices bootloader*. – *Section 13: STM32F031xx devices bootloader*. – *Section 14: STM32F373xx devices bootloader*. – *Section 15: STM32F302xB(C)/303xB(C) devices bootloader*. – *Section 16: STM32F378xx devices bootloader*. – *Section 17: STM32F358xx devices bootloader*. – *Section 18: STM32F427xx/437xx devices bootloader*. – *Section 34.3: I2C bootloader timing characteristics*. Updated *Section 1: Related documents* and *Section 2: Glossary*. Added *Table 79* to *Table 85* (USART bootloader timings). Replaced *Figure 6* to *Figure 16*, and Figures *18*, *19* and *42*. Modified Tables *3*, *5*, *9*, *11*, *17*, *20*, *21*, *22* to *13*, *27*, *29*, *31*, *33*, *35*, *37* and *65*. Removed “X = 6: one USART is used” in *Section 3.3: Hardware connection requirement*. Replaced address 0x1FFFF 8002 with address 0x1FFF F802 in *Section 12.1: Bootloader configuration*. Modified procedure related to execution of the bootloader code in *Note: on page 28*, in *Section 6.2: Bootloader selection* and in *Section 9.2: Bootloader selection*.
06-Feb-2013	16	Added information related to I^2C throughout the document. Streamlined *Table 1: Applicable products* and *Section 1: Related documents*. Modified *Table 3: Embedded bootloaders* as follows: – Replaced "V6.0" with "V1.0" – Replaced "0x1FFFF7A6" with "0x1FFFF796" in row STM32F31xx – Replaced "0x1FFF7FA6" with "0x1FFFF7A6" in row STM32F051xx Updated figures *6*, *9* and *11*. Added *Note:* in *Glossary* and *Note:* in *Section 3.1: Bootloader activation*. Replaced: – "1.62 V" with "1.8 V" in tables*17*, *19*, *19*, *22*, *21*, *27*, *37* and *59* – "5 Kbyte" with "4 Kbyte" in row RAM of *Table 33* – "127 pages (2 KB each)" with "4 KB (2 pages of 2 KB each)" in rows F3 of *Table 65* – "The bootloader ID is programmed in the last two bytes of the device system memory" with "The bootloader ID is programmed in the last byte address - 1 of the device system memory" in *Section 3.3: Hardware connection requirement*. – "STM32F2xxxx devices revision Y" by "STM32F2xxxx devices revision X and Y" in *Section 10: STM32F2xxxx devices bootloader* – “Voltage Range 2” with “Voltage Range 1” in tables *11*, *15* and *26*.

Table 145. Document revision history (continued)

Date	Revision	Changes
21-May-2013	17	Updated: – *Introduction* – *Section 2: Glossary* – *Section 3.3: Hardware connection requirement* – *Section 7: STM32L1xxx6(8/B) devices bootloader* to include STM32L100 value line – *Section 32.2: USART connection timing* – *Section 34.2: USB bootloader timing characteristics* – *Section 34.3: I2C bootloader timing characteristics* – *Table 1: Applicable products* – *Table 3: Embedded bootloaders* – *Table 25: STM32F051xx configuration in System memory boot mode* – *Table 27: STM32F031xx configuration in System memory boot mode* – *Table 65: Bootloader device-dependent parameters* – *Figure 17: Bootloader selection for STM32F031xx devices* Added *Section 19: STM32F429xx/439xx devices bootloader*.
19-May-2014	18	Add: – *Figure 1* to *Figure 5*, *Figure 68*, *Figure 8*, *Figure 27*, *Figure 28*, *Figure 26*, from *Figure 40* to *Figure 88*, *Figure 92* – *Table 4*, *Table 115*, *Table 116*, from *Table 9* to *Table 48*, from *Table 49* to *Table 46*, from *Table 71* to *Table 72*, from *Table* to *Table 144* – *Section 38.4*, *Section 33.2*, *Section 65.1*, *Section 65.5* – *Section 5* ,*Section 23*, *Section 24*, *Section 22*, from *Section 17* to *Section 57* – note under *Figure 1*, *Figure 2*, *Figure 3* and *Figure 4* Updated: – Updated starting from *Section 4* to *Section 7* and *Section 18*, *Section 33* and *Section 33* the chapter structure organized in three subsection: Bootloader configuration, Bootloader selection and Bootloader version. Updated *Section 57* and *Section 65* – Updated block diagram of *Figure 27* and *Figure 22*. – Fixed I2C address for STM32F429xx/439xx devices in *Table 69* – *Table 1*, *Table 2*, *Table 3*, *Table 27*, *Table 109*, *Table 111*, *Table 113*, *Table 31*, *Table 33*, *Table 53*, *Table 139* – from *Figure 16*, to *Figure 30*, *Figure 10*, from *Figure 88* to *Figure 92* – note on *Table 110*

Table 145. Document revision history (continued)

Date	Revision	Changes
29-Jul-2014	19	Updated: – notes under *Table 2* – *Figure 67* and *Figure 68* – *Section 3: Glossary* – replaced any reference to STM32F427xx/437xx with STM32F42xxx/43xxx on *Section 33: STM32F42xxx/43xxx devices bootloader* – replace any occurrence of ‘STM32F072xx’ with ‘STM32F07xxx’ – replace any occurrence of ‘STM32F051xx’ with ‘STM32F051xx and STM32F030x8 devices’. – comment field related to OTG_FS_DP and OTG_FS_DM on *Table 27*, *Table 33*, *Table 53*, *Table 115*, *Table 69*, *Table 71*, *Table 15*, *Table 21*, *Table 57*, *Table 59* and *Table 63* – comment field related to USB_DM on *Table 115*. – replace reference to "STM32F429xx/439xx" by "STM32F42xxx/43xxx” on *Table 3* – comment field related to SPI2_MOSI, SPI2_MISO, SPI2_SCK and SPI2_NSS pins on *Table 71* Added: – note under *Table 2* – reference to STM32F411 on *Table 1*, *Section 3: Glossary*, *Table 140*, *Table 141*, *Table 142*, *Table 143* – *Section 30: STM32F411xx devices bootloader* Removed reference to STM32F427xx/437xx on *Table 3*, *Section 3: Glossary*, *Table 139*, *Table 140*, *Table 141*, *Table 142*
24-Nov-2014	20	Updated: – comment in “SPI1_NSS pin" and "SPI2_NSS pin" rows on *Table 115* and *Table 101* – comment in "SPI1_NSS pin", "SPI2_NSS pin" and "SPI3_NSS pin" rows on *Table 57*, *Table 59* and *Table 63* – *Figure 1*
11-Mar-2015	21	Updated: – *Table 1*, *Table 3*, *Table 25*, *Table 29*, *Table 109*, *Table 31*, *Table 33*, *Table 34*, *Table 53*, *Table 115*, *Table 13*, *Table 14*, *Table 9*, *Table 37*, *Table 69*, *Table 71*, *Table 15*, *Table 16*, *Table 21*, *Table 22*,*Table 35*, *Table 107*, *Table 123*, *Table 139*, *Table 140*, *Table 141*, *Table 142* and *Table 143* – *Figure 76* – *Chapter 3: Glossary* – *Section 4.1* and *Section 4.4* Added: – *Section 57: STM32L47xxx/48xxx devices bootloader* and *Section 34: STM32F446xx devices bootloader*

Table 145. Document revision history (continued)

Date	Revision	Changes
09-Jun-2015	22	Added: – *Section 9: STM32F070x6 devices bootloader* – *Section 10: STM32F070xB devices bootloader* – *Section 12: STM32F09xxx devices bootloader* – *Section 19: STM32F302xD(E)/303xD(E) devices bootloaderSection 25: STM32F398xx devices bootloader* – *Section 36: STM32F72xxx/73xxx devices bootloader* – *Section 57.2: Bootloader V9.x* – Notes 1 and 2 on *Figure 89* Updated: – *Table 1* – *Section 3: Glossary* – *Table 2* – *Table 3* – *Section 4.4: Bootloader memory management* – *Table 139*, *Table 140*, *Table 141*, *Table 142* and *Table 143*
29-Sep-2015	23	Added: – *Section 29: STM32F410xx devices bootloader* – *Section 35: STM32F469xx/479xx devices bootloader* – *Section 46: STM32L031xx/041xx devices bootloader* – *Section 48: STM32L07xxx/08xxx devices bootloader* Updated: – *Table 1* – *Section 3: Glossary* – *Table 3* – *Figure 76*, *Table 125*, *Table 140*, *Table 141*, *Table 142*, *Table 143*
02-Nov-2015	24	Updated: – *Table 1*, *Table 3*, *Table 139*, *Table 140*, *Table 141*, *Table 142*, *Table 143* – *Section 35* Added: – Note on *Section 26.2.1* – *Section 31*
01-Dec-2015	25	Updated: – *Section 4.1*, *Section 48* – *Table 139*
03-Mar-2016	26	Updated: – *Table 1*, *Table 3*, *Table 66*, *Table 104*, *Table 106*, *Table 139* – *Section 3*, *Section 48.1.1*, *Section 48.2.1*, *Section 57* Added: – *Section 45: STM32L01xxx/02xxx devices bootloader* – *Figure 60*, *Figure 62*

Table 145. Document revision history (continued)

Date	Revision	Changes
21-Apr-2016	27	Added: – *Section 38: STM32F76xxx/77xxx devices bootloader*, *Section 55: STM32L43xxx/44xxx devices bootloader*. – Note on: *Section 4.1: Bootloader activation*, *Section 8.1: Bootloader configuration*, *Section 9.1: Bootloader configuration*, *Figure 38: Dual Bank Boot Implementation for STM32F42xxx/43xxx Bootloader V7.x*, *Figure 40: Dual Bank Boot Implementation for STM32F42xxx/43xxx bootloader V9.x* Updated: – *Table 1: Applicable products*, *Table 2: Bootloader activation patterns*, *Table 11: STM32F030xC configuration in system memory boot mode*, *Table 17: STM32F070x6 configuration in system memory boot mode*, *Table 19: STM32F070xB configuration in system memory boot mode*, *Table 23: STM32F09xxx configuration in system memory boot mode*, *Table 35: STM32F301xx/302x4(6/8) configuration in system memory boot mode*, *Table 37: STM32F302xB(C)/303xB(C) configuration in system memory boot mode*, *Table 39: STM32F302xD(E)/303xD(E) configuration in system memory boot mode*, *Table 47: STM32F373xx configuration in system memory boot mode*, *Table 57: STM32F401xB(C) configuration in system memory boot mode*, *Table 59: STM32F401xD(E) configuration in system memory boot mode*, *Table 63: STM32F411xx configuration in system memory boot mode*, *Table 124: STM32L47xxx/48xxx bootloader V10.x versions*, *Table 126: STM32L47xxx/48xxx bootloader V9.x versions*, *Table 139: Bootloader device-dependent parameters* – *Section 3: Glossary*,

Table 145. Document revision history (continued)

Date	Revision	Changes
05-Sep-2016	28	Updated: – *Table 1: Applicable products*, *Table 11: STM32F030xC configuration in system memory boot mode*, *Table 13: STM32F05xxx and STM32F030x8 devices configuration in system memory boot mode*, *Table 15: STM32F04xxx configuration in system memory boot mode*, *Table 17: STM32F070x6 configuration in system memory boot mode*, *Table 19: STM32F070xB configuration in system memory boot mode*, *Table 21: STM32F071xx/072xx configuration in system memory boot mode*, *Table 23: STM32F09xxx configuration in system memory boot mode*, *Table 27: STM32F105xx/107xx configuration in system memory boot mode*, *Table 29: STM32F10xxx XL-density configuration in system memory boot mode*, *Table 31: STM32F2xxxx configuration in system memory boot mode*, *Table 33: STM32F2xxxx configuration in system memory boot mode*, *Table 35: STM32F301xx/302x4(6/8) configuration in system memory boot mode*, *Table 37: STM32F302xB(C)/303xB(C) configuration in system memory boot mode*, *Table 39: STM32F302xD(E)/303xD(E) configuration in system memory boot mode*, *Table 41: STM32F303x4(6/8)/334xx/328xx configuration in system memory boot mode*, *Table 43: STM32F318xx configuration in system memory boot mode*, *Table 45: STM32F358xx configuration in system memory boot mode*, *Table 47: STM32F373xx configuration in system memory boot mode*, *Table 49: STM32F378xx configuration in system memory boot mode*, *Table 51: STM32F398xx configuration in system memory boot mode*, *Table 53: STM32F40xxx/41xxx configuration in system memory boot mode*, *Table 55: STM32F40xxx/41xxx configuration in system memory boot mode*, *Table 57: STM32F401xB(C) configuration in system memory boot mode*, *Table 59: STM32F401xD(E) configuration in system memory boot mode*, *Table 63: STM32F411xx configuration in system memory boot mode*, *Table 69: STM32F42xxx/43xxx configuration in system memory boot mode*, *Table 71: STM32F42xxx/43xxx configuration in system memory boot modeTable 73: STM32F446xx configuration in system memory boot mode*, *Table 75: STM32F469xx/479xx configuration in system memory boot mode*, *Table 79: STM32F74xxx/75xxx configuration in system memory boot mode*, *Table 81: STM32F74xxx/75xxx configuration in system memory boot mode*, *Table 101: STM32L05xxx/06xxx configuration in system memory boot mode*, *Table 107: STM32L1xxx6(8/B)A configuration in system memory boot mode*, *Table 109: STM32L1xxx6(8/B) configuration in system memory boot mode*, *Table 111: STM32L1xxxC configuration in system memory boot mode*, *Table 113: STM32L1xxxD configuration in system memory boot mode*, *Table 115: STM32L1xxxE configuration in system memory boot mode*, *Table 120: STM32L43xxx/44xxx bootloader versions*, *Table 123: STM32L47xxx/48xxx configuration in system memory boot mode*, *Table 139: Bootloader device-dependent parameters* – *Section 55.1: Bootloader configuration*

Table 145. Document revision history (continued)

Date	Revision	Changes
05-Sep-2016	28 (continued)	– *Figure 24: Bootloader selection for STM32F303x4(6/8)/334xx/328xx*, *Figure 25: Bootloader selection for STM32F318xx*, *Figure 27: Bootloader selection for STM32F373xx devices*, *Figure 28: Bootloader selection for STM32F378xx devices*, *Figure 31: Bootloader V9.x selection for STM32F40xxx/41xxx*, *Figure 34: Bootloader V11.x selection for STM32F410xx*, *Figure 36: Bootloader V9.x selection for STM32F412xx*, *Figure 44: Bootloader V9.x selection for STM32F469xx/479xx*, *Figure 49: Bootloader V9.x selection for STM32F76xxx/77xxx*, *Figure 63: Bootloader V11.x selection for STM32L07xxx/08xxx*, *Figure 76: Bootloader V10.x selection for STM32L47xxx/48xxx*
07-Dec-2016	29	Updated: – *Table 1: Applicable products*, *Section 3: Glossary*, *Section 4.1: Bootloader activation*, *Table 3: Embedded bootloaders*, *Table 12: STM32F09xxx devices bootloader*, *Table 14: STM32F105xx/107xx devices bootloader*, *Table 15: STM32F10xxx XL-density devices bootloader*, *Table 16: STM32F2xxxx devices bootloader*, *Table 17: STM32F301xx/302x4(6/8) devices bootloader*, *Table 18: STM32F302xB(C)/303xB(C) devices bootloader*, *Table 20: STM32F303x4(6/8)/334xx/328xx devices bootloader*, *Table 22: STM32F358xx devices bootloader*, *Table 25: STM32F398xx devices bootloader*, *Table 29: STM32F410xx devices bootloader*, *Table 32: STM32F413xx/423xx devices bootloader*, *Table 59: STM32F401xD(E) configuration in system memory boot mode*, *Section 14.3.1: How to identify STM32F105xx/107xx bootloader versions*, *Section 28.1: Bootloader configuration*, *Table 61: STM32F410xx configuration in system memory boot mode*, *Table 63: STM32F411xx configuration in system memory boot mode*, *Table 65: STM32F412xx configuration in system memory boot mode*, *Section 30.1: Bootloader configuration*, *Table 70: STM32F42xxx/43xxx bootloader V7.x versions*, *Table 72: STM32F42xxx/43xxx bootloader V9.x versions*, *Table 83: STM32F76xxx/77xxx configuration in system memory boot mode*, *Table 84: STM32F76xxx/77xxx bootloader V9.x versions*, *Table 98: STM32L01xxx/02xxx bootloader versions*, *Table 106: STM32L07xxx/08xxx bootloader V11.x versions*, *Table 119: STM32L43xxx/44xxx configuration in system memory boot mode*, *Table 120: STM32L43xxx/44xxx bootloader versions*, *Table 124: STM32L47xxx/48xxx bootloader V10.x versions*, *Table 139: Bootloader device-dependent parameters*, *Table 140: Bootloader startup timings of STM32 devices*, *Table 142: USB bootloader minimum timings of STM32 devices*, *Table 142: USB bootloader minimum timings of STM32 devices*, *Table 143: I2C bootloader minimum timings of STM32 devices* Added: – *Section 32: STM32F413xx/423xx devices bootloader*

Table 145. Document revision history (continued)

Date	Revision	Changes
13-Mar-2017	30	Updated: – *Table 1: Applicable products*, *Table 3: Embedded bootloaders*, *Table 14: STM32F05xxx and STM32F030x8 devices bootloader versions*, *Table 15: STM32F04xxx configuration in system memory boot mode*, *Table 16: STM32F04xxx bootloader versions*, *Table 18: STM32F070x6 bootloader versions*, *Table 20: STM32F070xB bootloader versions*, *Table 21: STM32F071xx/072xx configuration in system memory boot mode*, *Table 22: STM32F071xx/072xx bootloader versions*, *Table 23: STM32F09xxx configuration in system memory boot mode*, *Table 24: STM32F09xxx bootloader versions*, *Table 35: STM32F301xx/302x4(6/8) configuration in system memory boot mode*, *Table 38: STM32F302xB(C)/303xB(C) bootloader versions*, *Table 84: STM32F76xxx/77xxx bootloader V9.x versions*, *Table 97: STM32L01xxx/02xxx configuration in system memory boot mode*, *Table 120: STM32L43xxx/44xxx bootloader versions*, *Table 139: Bootloader device-dependent parameters*, *Table 125: STM32L47xxx/48xxx configuration in system memory boot mode*, *Table 140: Bootloader startup timings of STM32 devices*, *Table 141: USART bootloader minimum timings of STM32 devices*, *Table 142: USB bootloader minimum timings of STM32 devices*, *Table 143: I2C bootloader minimum timings of STM32 devices*, *Table 144: SPI bootloader minimum timings of STM32 devices* – *Section 3: Glossary*, *Section 6.1: Bootloader configuration*, *Section 14.3.3: USART bootloader Get-Version command returns 0x20 instead of 0x22*, RPN reference in *Section 55: STM32L43xxx/44xxx devices bootloader* and in *Section 57: STM32L47xxx/48xxx devices bootloader* Added *Section 36: STM32F72xxx/73xxx devices bootloader* and *Section 58: STM32L496xx/4A6xx devices bootloader*

Table 145. Document revision history (continued)

Date	Revision	Changes
04-Jul-2017	31	Updated: – *Table 1: Applicable products*, *Table 2: Bootloader activation patterns*, *Table 3: Embedded bootloaders*, *Table 28: STM32F105xx/107xx bootloader versions*, *Table 33: STM32F2xxxx configuration in system memory boot mode*, *Table 37: STM32F302xB(C)/303xB(C) configuration in system memory boot mode*, *Table 45: STM32F358xx configuration in system memory boot mode*, *Table 47: STM32F373xx configuration in system memory boot mode*, *Table 49: STM32F378xx configuration in system memory boot mode*, *Table 55: STM32F40xxx/41xxx configuration in system memory boot mode*, *Table 57: STM32F401xB(C) configuration in system memory boot mode*, *Table 59: STM32F401xD(E) configuration in system memory boot mode*, *Table 63: STM32F411xx configuration in system memory boot mode*, *Table 69: STM32F42xxx/43xxx configuration in system memory boot mode*, *Table 73: STM32F446xx configuration in system memory boot mode*, *Table 75: STM32F469xx/479xx configuration in system memory boot mode*, *Table 77: STM32F72xxx/73xxx configuration in system memory boot mode*, *Table 79: STM32F74xxx/75xxx configuration in system memory boot mode*, *Table 81: STM32F74xxx/75xxx configuration in system memory boot mode*, *Table 93: STM32H74xxx/75xxx configuration in system memory boot mode*, *Table 111: STM32L1xxxC configuration in system memory boot mode*, *Table 113: STM32L1xxxD configuration in system memory boot mode*, *Table 115: STM32L1xxxE configuration in system memory boot mode*, *Table 121: STM32L45xxx/46xxx configuration in system memory boot mode*, *Table 139: Bootloader device-dependent parameters*, *Table 140: Bootloader startup timings of STM32 devices*, *Table 141: USART bootloader minimum timings of STM32 devices*, *Table 142: USB bootloader minimum timings of STM32 devices*, *Table 143: I2C bootloader minimum timings of STM32 devices* – *Introduction*, *Section 3: Glossary* – *Figure 72: Bootloader V9.x selection for STM32L43xxx/44xxx* Added: – *Section 43: STM32H74xxx/75xxx devices bootloader*, *Section 56: STM32L45xxx/46xxx devices bootloader*
16-Feb-2018	32	Updated *Table 3: Embedded bootloaders*, *Table 94: STM32H74xxx/75xxx bootloader version*, *Table 127: STM32L496xx/4A6xx configuration in system memory boot mode*, *Table 128: STM32L496xx/4A6xx bootloader version*, *Table 139: Bootloader device-dependent parameters*, *Table 140: Bootloader startup timings of STM32 devices*, *Table 141: USART bootloader minimum timings of STM32 devices*, *Table 142: USB bootloader minimum timings of STM32 devices*, *Table 143: I2C bootloader minimum timings of STM32 devices*. Added *Section 60: STM32L4Rxxx/4Sxxx devices bootloader*
07-Aug-2018	33	Updated *Note:* in *Section 8.1: Bootloader configuration*, *Note:* in *Section 9.1: Bootloader configuration*

Table 145. Document revision history (continued)

Date	Revision	Changes
05-Nov-2018	34	Updated *Table 1: Applicable products*, *Table 54: STM32F40xxx/41xxx bootloader V3.x versions*, *Table 56: STM32F40xxx/41xxx bootloader V9.x versions*, *Table 58: STM32F401xB(C) bootloader versions*, *Table 60: STM32F401xD(E) bootloader versions*, *Table 62: STM32F410xx bootloader V11.x versions*, *Table 64: STM32F411xx bootloader versions*, *Table 66: STM32F412xx bootloader V9.x versions*, *Table 68: STM32F413xx/423xx bootloader V9.x versions*, *Table 70: STM32F42xxx/43xxx bootloader V7.x versions*, *Table 72: STM32F42xxx/43xxx bootloader V9.x versions*, *Table 74: STM32F446xx bootloader V9.x versions*, *Table 76: STM32F469xx/479xx bootloader V9.x versions*, *Table 78: STM32F72xxx/73xxx bootloader V9.x versions*, *Table 80: STM32F74xxx/75xxx bootloader V7.x versions*, *Table 82: STM32F74xxx/75xxx bootloader V9.x versions*, *Table 84: STM32F76xxx/77xxx bootloader V9.x versions*, *Table 139: Bootloader device-dependent parameters*, *Table 140: Bootloader startup timings of STM32 devices*, *Table 141: USART bootloader minimum timings of STM32 devices*, *Table 142: USB bootloader minimum timings of STM32 devices*. Added *Section 54: STM32L412xx/422xx devices bootloader*
06-Dec-2018	35	Updated *Table 1: Applicable products*, *Section 3: Glossary*, *Table 140: Bootloader startup timings of STM32 devices*, *Table 141: USART bootloader minimum timings of STM32 devices*, *Table 143: I2C bootloader minimum timings of STM32 devices*. Added *Section 40: STM32G07xxx/08xxx device bootloader*
21-Feb-2019	36	Updated *Table 1: Applicable products*, *Section 3: Glossary*, *Table 3: Embedded bootloaders*, *Table 139: Bootloader device-dependent parameters*, *Table 140: Bootloader startup timings of STM32 devices*, *Table 141: USART bootloader minimum timings of STM32 devices*, *Table 142: USB bootloader minimum timings of STM32 devices*, *Table 143: I2C bootloader minimum timings of STM32 devices*. Added *Section 62: STM32WB50xx/55xx devices bootloader*
06-May-2019	37	Updated *Table 1: Applicable products*, *Section 3: Glossary*, *Table 139: Bootloader device-dependent parameters*, *Table 140: Bootloader startup timings of STM32 devices*, *Table 141: USART bootloader minimum timings of STM32 devices*, *Table 142: USB bootloader minimum timings of STM32 devices*, *Table 143: I2C bootloader minimum timings of STM32 devices*. Added *Section 41: STM32G431xx/441xx devices bootloader*, *Section 42: STM32G47xxx/48xxx devices bootloader*

Table 145. Document revision history (continued)

Date	Revision	Changes
08-Jul-2019	38	Updated: – *Table 1: Applicable products*, *Table 2: Bootloader activation patterns*, *Table 3: Embedded bootloaders*, *Table 67: STM32F413xx/423xx configuration in system memory boot mode*, *Table 93: STM32H74xxx/75xxx configuration in system memory boot mode*, *Table 94: STM32H74xxx/75xxx bootloader version*, *Table 99: STM32L031xx/041xx configuration in system memory boot mode*, *Table 120: STM32L43xxx/44xxx bootloader versions*, *Table 121: STM32L45xxx/46xxx configuration in system memory boot mode*, *Table 128: STM32L496xx/4A6xx bootloader version*, *Table 136: STM32WB50xx/55xx bootloader versions*, *Table 139: Bootloader device-dependent parameters*, *Table 140: Bootloader startup timings of STM32 devices*, *Table 141: USART bootloader minimum timings of STM32 devices*, *Table 142: USB bootloader minimum timings of STM32 devices*, *Table 143: I2C bootloader minimum timings of STM32 devices* – *Section 3: Glossary*, *Section 4.1: Bootloader activation*, *Section 39.1: Bootloader configuration*, *Section 41.1: Bootloader configuration* – *Figure 55: Bootloader V9.x selection for STM32H74xxx/75xxx*, *Figure 83: Dual bank boot implementation for STM32L4Rxxx/STM32L4Sxxx bootloader V9.x* Added *Note:* in *Section 4.2*, *Note:* in *Section 13.3*, *Note:* in *Section 43.1*, *Note:* in *Section 45.1*, *Section 39: STM32G03xxx/ STM32G04xxx devices bootloader*
16-Sep-2019	39	Updated: – *Table 1: Applicable products*, *Table 2: Bootloader activation patterns*, *Table 3: Embedded bootloaders*, *Table 86: STM32G03xx/04xxx bootloader versions*, *Table 118: STM32L412xx/422xx bootloader versions*, *Table 120: STM32L43xxx/44xxx bootloader versions*, *Table 122: STM32L45xxx/46xxx bootloader versions*, *Table 124: STM32L47xxx/48xxx bootloader V10.x versions*, *Table 126: STM32L47xxx/48xxx bootloader V9.x versions*, *Table 128: STM32L496xx/4A6xx bootloader version*, *Table 130: STM32L4P5xx/4Q5xx bootloader versions*, *Table 139: Bootloader device-dependent parameters*, *Table 140: Bootloader startup timings of STM32 devices*, *Table 141: USART bootloader minimum timings of STM32 devices*, *Table 142: USB bootloader minimum timings of STM32 devices*, *Table 143: I2C bootloader minimum timings of STM32 devices* – *Section 3: Glossary*, *Section 4.2: Bootloader identification* Added *Figure 54: Dual bank boot implementation for STM32G47xxx/48xxx bootloader V13.x*, *Section 61: STM32L552xx/STM32L562xx devices bootloader*, note in *Section 62.3: Bootloader version*
03-Oct-2019	40	Updated *Table 3: Embedded bootloaders*, *Table 134: STM32L552xx/562xx bootloader versions*, *Table 136: STM32WB50xx/55xx bootloader versions*

Table 145. Document revision history (continued)

Date	Revision	Changes
25-Oct-2019	41	Updated: – *Table 78: STM32F72xxx/73xxx bootloader V9.x versions*, *Table 80: STM32F74xxx/75xxx bootloader V7.x versions*, *Table 82: STM32F74xxx/75xxx bootloader V9.x versions*, *Table 84: STM32F76xxx/77xxx bootloader V9.x versions*, *Table 85: STM32G03xxx/G04xxx configuration in system memory boot mode*, *Table 94: STM32H74xxx/75xxx bootloader version*, *Table 130: STM32L4P5xx/4Q5xx bootloader versions*, *Table 133: STM32L552xx/562xx configuration in system memory boot mode*, *Table 140: Bootloader startup timings of STM32 devices*, *Table 141: USART bootloader minimum timings of STM32 devices*, *Table 143: I2C bootloader minimum timings of STM32 devices* – *Section 16: STM32F2xxxx devices bootloader*
05-Dec-2019	42	Updated: – *Table 1: Applicable products*, *Table 2: Bootloader activation patterns*, *Table 3: Embedded bootloaders*, *Table 139: Bootloader device-dependent parameters*, *Table 140: Bootloader startup timings of STM32 devices*, *Table 141: USART bootloader minimum timings of STM32 devices*, *Table 142: USB bootloader minimum timings of STM32 devices*, *Table 143: I2C bootloader minimum timings of STM32 devices* – *Section 3: Glossary* Added: *Section 44: STM32H7A3xx/B3xx devices bootloader*, *Section 59: STM32L4P5xx/4Q5xx devices bootloader*, *Section 63: STM32WLE5xx devices bootloader*

Table 145. Document revision history (continued)

Date	Revision	Changes
15-Jun-2020	43	Updated: – *Table 1: Applicable products*, *Table 2: Bootloader activation patterns*, *Table 3: Embedded bootloaders*, *Table 89: STM32G431xx/441xx configuration in system memory boot mode*, *Table 91: STM32G47xxx/48xxx configuration in system memory boot mode*, *Table 92: STM32G47xxx/48xxx bootloader version*, *Table 94: STM32H74xxx/75xxx bootloader version*, *Table 96: STM32H7A3xx/7B3xx bootloader version*, *Table 130: STM32L4P5xx/4Q5xx bootloader versions*, *Table 133: STM32L552xx/562xx configuration in system memory boot mode*, *Table 134: STM32L552xx/562xx bootloader versions*, *Table 135: STM32WB50xx/55xx configuration in system memory boot mode*, *Table 139: Bootloader device-dependent parameters* – *Section 3: Glossary*, *Section 37: STM32F74xxx/75xxx devices bootloader*, *Section 39.1: Bootloader configuration*, *Section 40.1: Bootloader configuration*, *Section 41.1: Bootloader configuration*, *Section 42.1: Bootloader Configuration*, *Section 43.1: Bootloader configuration* Added: – *Section 4.5: Bootloader UART baudrate detection*, *Section 4.6: Flash Programming constraints:*, *Section 4.7: “ExitSecureMemory” feature* – *Note:* in: *Section 26.1.1: Bootloader configuration*, *Section 26.2.1: Bootloader configuration*, *Section 27.1: Bootloader configuration*, *Section 28.1: Bootloader configuration*, *Section 30.1: Bootloader configuration*, *Section 31.1: Bootloader configuration*, *Section 32.1: Bootloader configuration*, *Section 33.1.1: Bootloader configuration*, *Section 33.2.1: Bootloader configurationSection 34.1: Bootloader configuration*, *Section 35.1: Bootloader configuration*, *Section 36.1: Bootloader configuration*, *Section 37.1.1: Bootloader configuration*, *Section 37.2.1: Bootloader configuration*, *Section 38.1: Bootloader configuration* – *Figure 71: Dual bank boot Implementation for STM32L3x2xx/44xxx bootloader V9.x*, *Figure 73: Dual bank boot Implementation for STM32L45xxx/46xxx bootloader V9.x*, *Figure 79: Dual bank boot Implementation for STM32L496xx/4A6xx bootloader V9.x* – *Appendix A: Example of function to use the “ExitSecureMemory” function* Deleted Figure 48. Access to securable memory area from the bootloader for STM32G03xxx/G04xxx, Figure 50. Access to securable memory area from the bootloader for STM32G07xxx/G08xxx, Figure 52. Access to securable memory area, Figure 54. Access to securable memory area