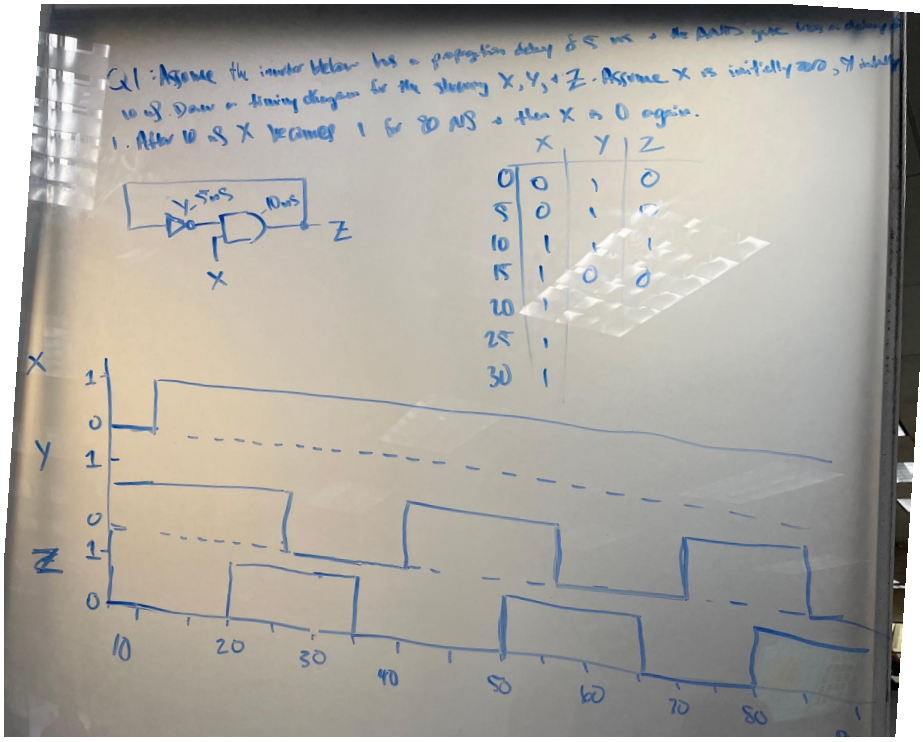
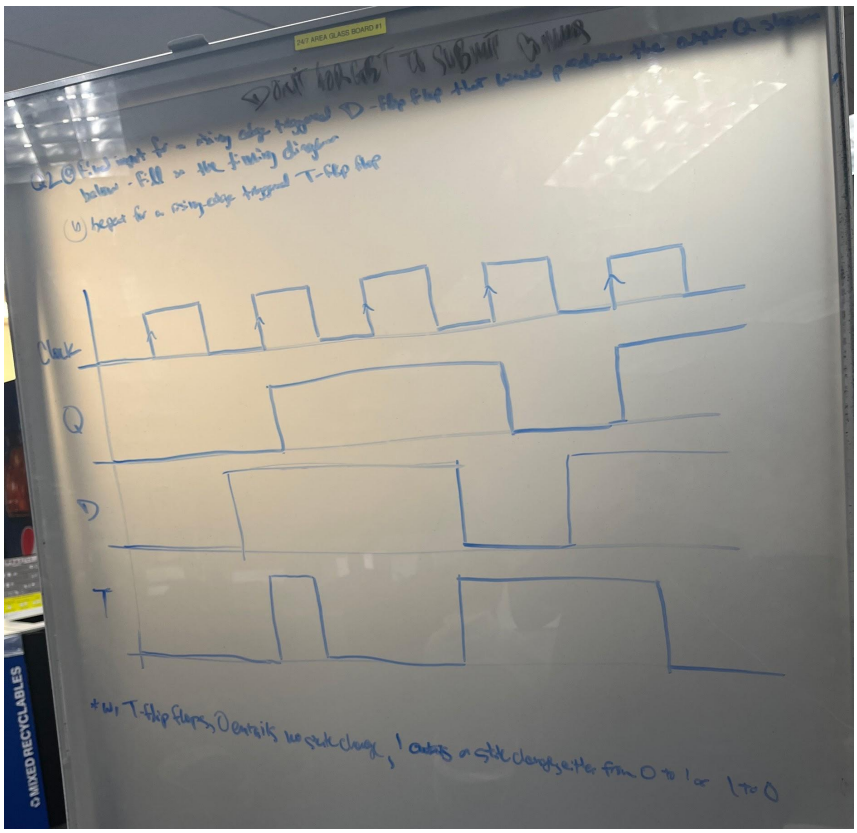
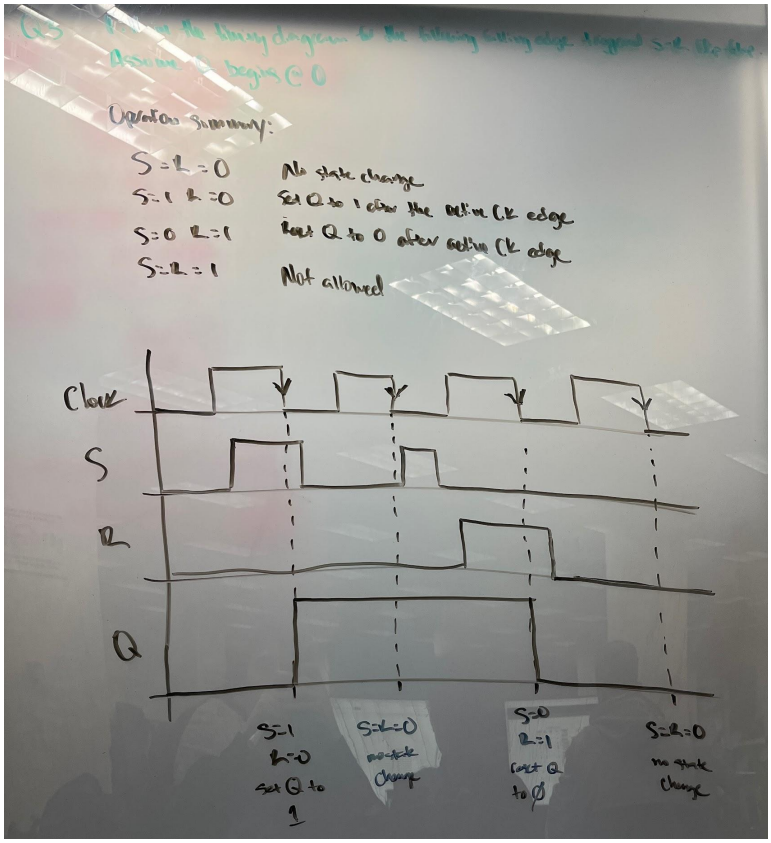
(1)


Q1 : Assume the inverter below has a propagation delay of 5 ns
10 ns. Draw a timing diagram for the signals X, Y, & Z. Assume X is initially zero, Y initially
1. After 0 ns X becomes 1 for 30 ns & then X is 0 again.
X
Y
Z
10
20
30
40
50
60
70
80

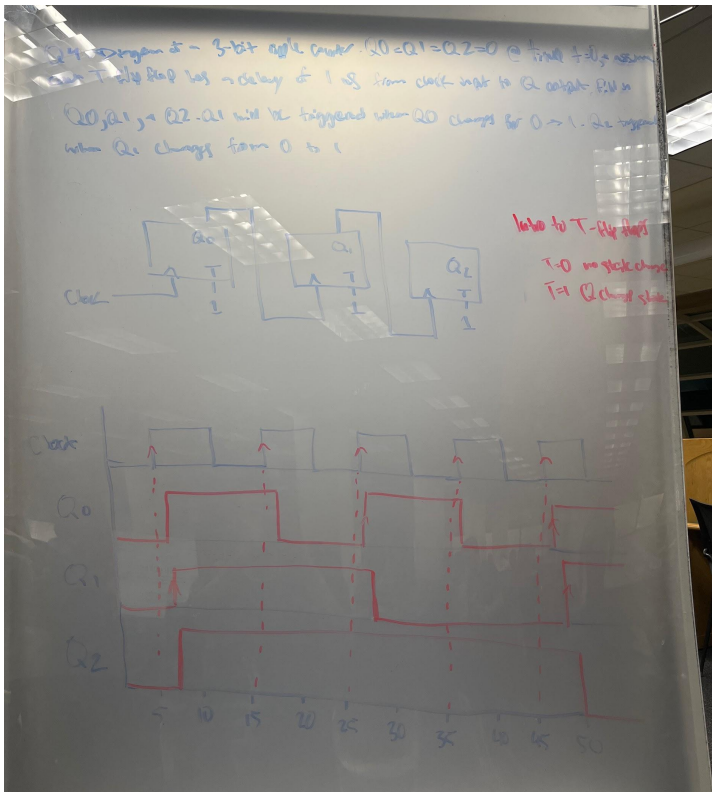
(2)


Clock
Q
D
T
*If T-flip flops, 0 entails no state change, 1 entails a state change either from 0 to 1 or 1 to 0

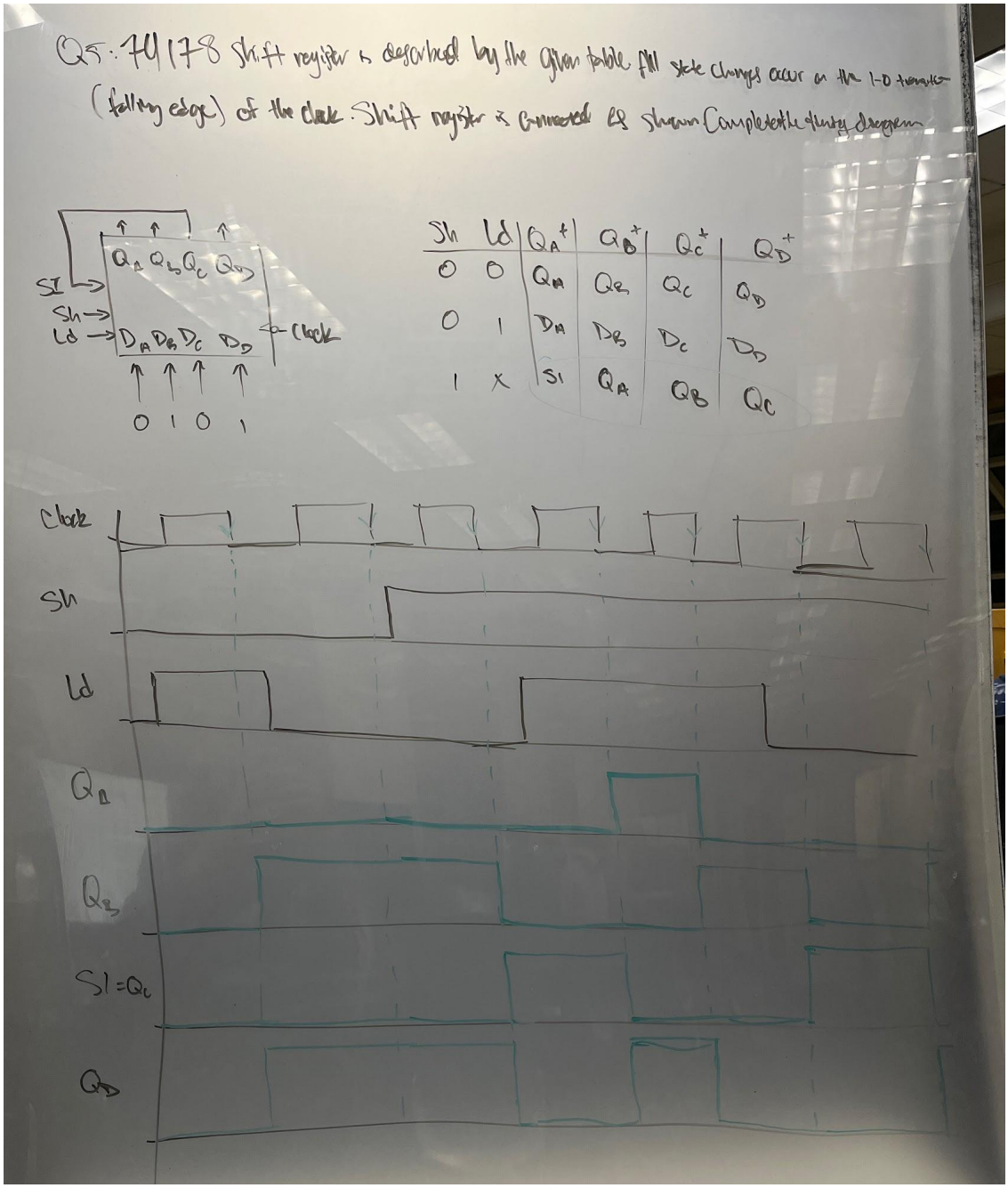
(3)


Operation Summary:
S=R=0
No state change
S=1 R=0
Set Q to 1 after the next Clk edge
S=0 R=1
Reset Q to 0 after next Clk edge
S=R=1
Not allowed
Clock
S
R
Q
S=1
R=0
Set Q to
1
S=R=0
no state
change
S=0
R=1
reset Q
to 0
S=R=0
no state
change

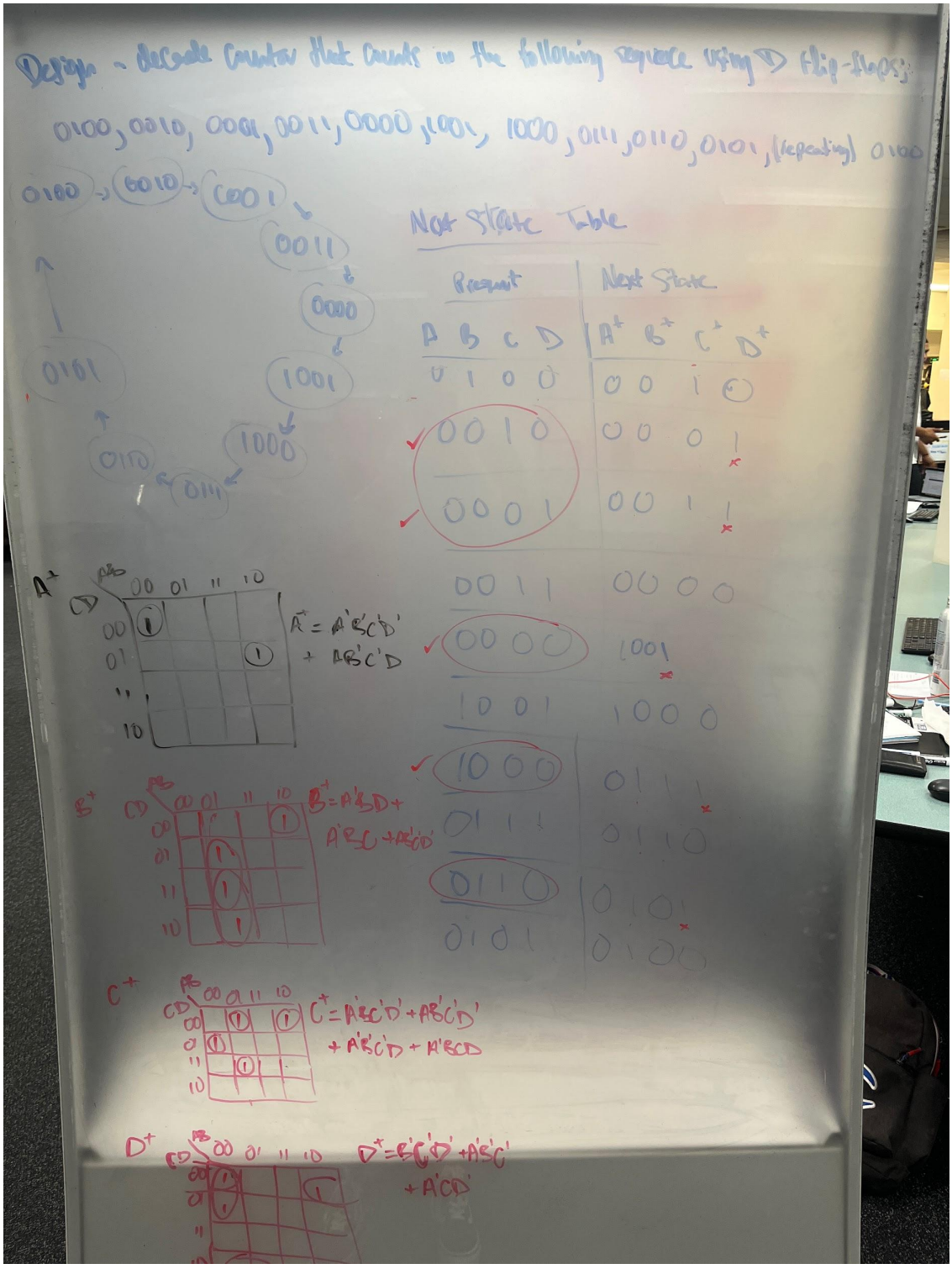
(4)


Clock
Q0
Q1
Q2
5
10
15
20
25
30
35
40
45
50

(5)


Q5: 74178 Shift register is described by the given table. All state changes occur on the 1-0 transition (falling edge) of the clock. Shift register is connected as shown. Complete the timing diagram.
SI
Sh
Ld
Clock
0 1 0 1
Sh Ld Q_A^+ Q_B^+ Q_C^+ Q_D^+
0 0 Q_A Q_B Q_C Q_D
0 1 D_A D_B D_C D_D
1 X SI Q_A Q_B Q_C
Clock
Sh
Ld
Q_A
Q_B
SI = Q_C
Q_D

(6)

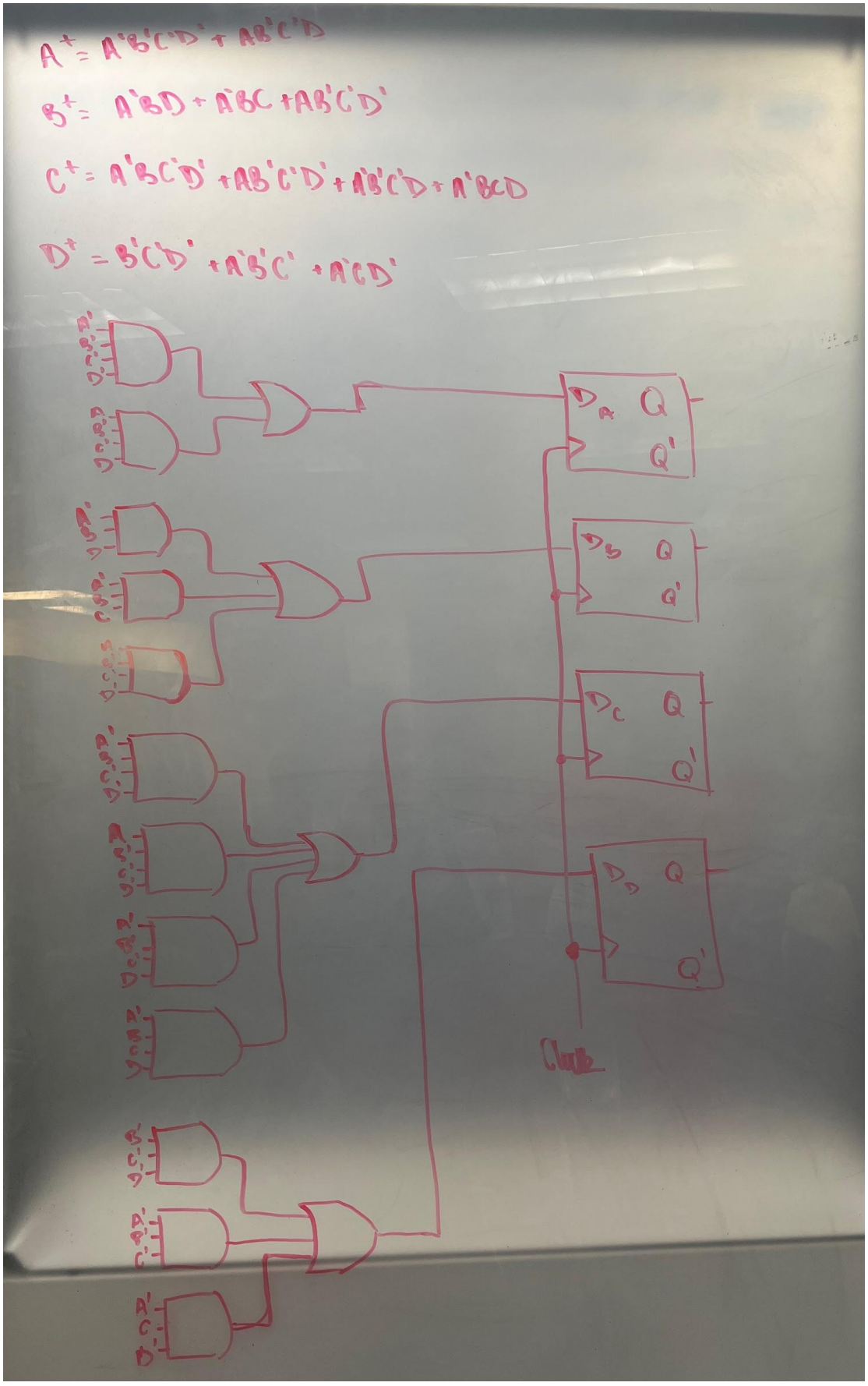

Design a decade Counter that counts in the following sequence using D flip-flops:
0100, 0010, 0001, 0011, 0000, 1001, 1000, 0111, 0110, 0101, (repeating) 0100
Next State Table
Present
Next State
A B C D
A+ B+ C+ D+
A+ = A'B'C'D' + AB'C'D
B+ = A'B'D + A'BC + AB'C'
C+ = A'B'C'D' + AB'C'D' + A'B'C'D + A'BCD
D+ = B'C'D' + A'B'C' + A'C'D'

$A^+ = A'B'C'D' + AB'C'D$

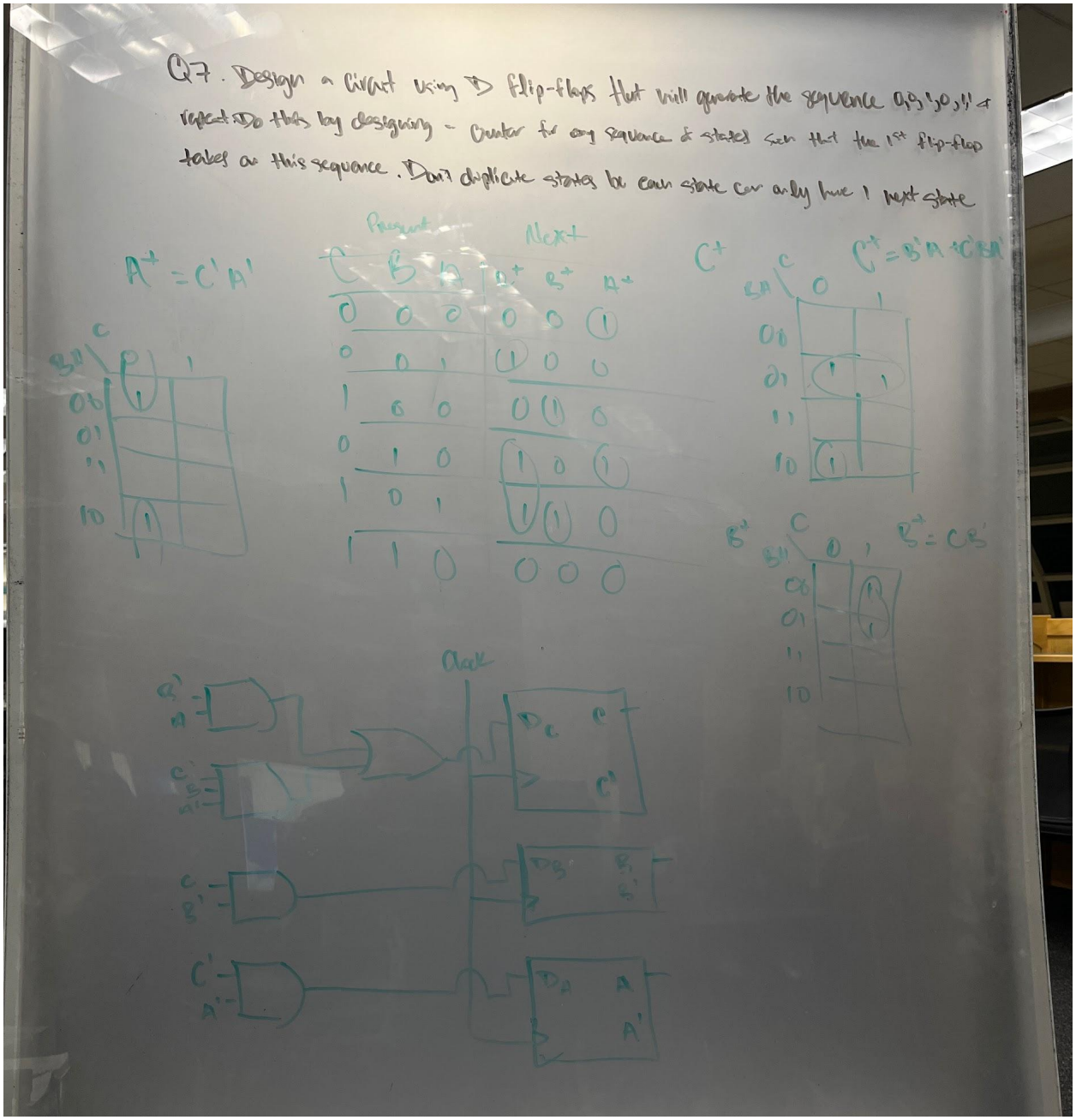
$B^+ = A'BD + A'BC + AB'C'D'$

$C^+ = A'BC'D' + AB'C'D' + A'B'C'D + A'BCD$

$D^+ = B'C'D' + A'B'C' + A'CD'$



(7)


Q7. Design a circuit using D flip-flops that will generate the sequence 0,3,1,0,1,1 & repeat. Do this by designing a Counter for any sequence & states such that the 1st flip-flop takes on this sequence. Don't duplicate states be each state can only have 1 next state
Present
Next
$A^+ = C'A'$
$C^+ = B'A + CB'$
$B^+ = CB'$
Clock

(8)

Q8. Design a decade Counter which counts from 0-9 using the excess 3-code for decimal digits

Decimal	Excess-3
0	0011
1	0100
2	0101
3	0110
4	0111
5	1000
6	1001
7	1010
8	1011
9	1100

Present State				Next State			
A	B	C	D	A^+	B^+	C^+	D^+
0	0	1	1	0	1	0	0
0	1	0	0	0	1	0	1
0	1	0	1	0	1	1	0
0	1	1	0	0	1	1	1
0	1	1	1	1	0	0	0
1	0	0	0	1	0	0	1
1	0	0	1	1	0	1	0
1	0	1	0	1	0	1	1
1	0	1	1	1	1	0	0
1	1	0	0	0	0	1	1

A^+

CD \ AB	00	01	11	10
00				1
01				1
11		1		1
10				1

$A^+ = AB^+ + A'BCD$

B^+

CD \ AB	00	01	11	10
00		1		
01		1		
11	1			1
10		1		

$B^+ = A'BD' + A'BC' + B'CD$

C^+

CD \ AB	00	01	11	10
00			1	
01		1		1
11				
10	1			1

$C^+ = ABC'D' + A'BC'D + AB'C'D + A'BCD' + AB'CD'$

D^+

CD \ AB	00	01	11	10
00		1		1
01				
11				
10	1			1

$D^+ = AB'D' + ACD' + A'BD'$

$A^+ = AB' + A'BCD$ ✓

$B^+ = A'BD' + A'BC' + B'CD$

$C^+ = ABC'D + A'BCD + ABC'D + A'BCD' + AB'CD'$

$D^+ = AB'D' + ACD' + A'BD'$