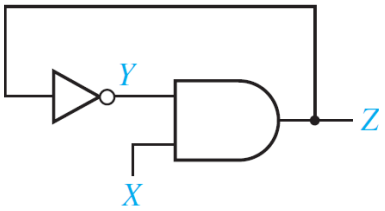
Homework 10-11

First Name:
Last Name:
Red ID#:

Q1

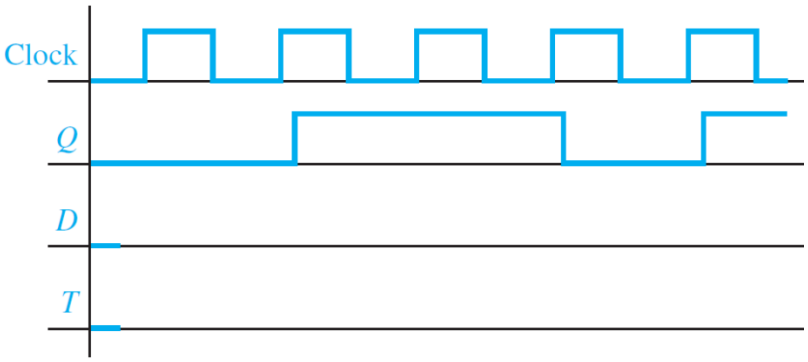
Assume that the inverter in the given circuit has a propagation delay of 5 ns and the AND gate has a propagation delay of 10 ns. Draw a timing diagram for the circuit showing *X*, *Y*, and *Z*. Assume that *X* is initially 0, *Y* is initially 1, after 10 ns *X* becomes 1 for 80 ns, and then *X* is 0 again.



Q2

(a) Find the input for a ***rising***-edge-triggered D flip-flop that would produce the output *Q* as shown below. Fill in the timing diagram.

(b) Repeat for a ***rising***-edge-triggered T flip-flop.

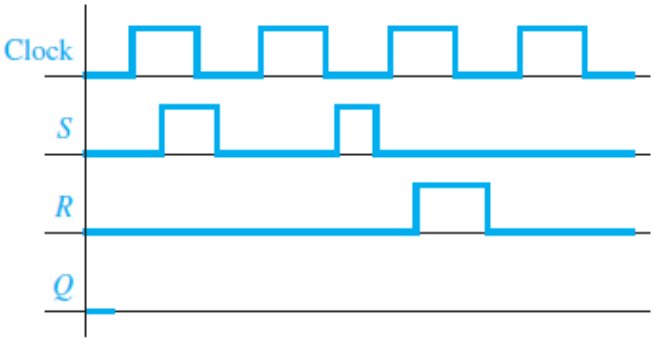


Q3

Fill in the timing diagram for the following ***falling***-edge-triggered S-R flip-flop. Assume Q begins at 0.

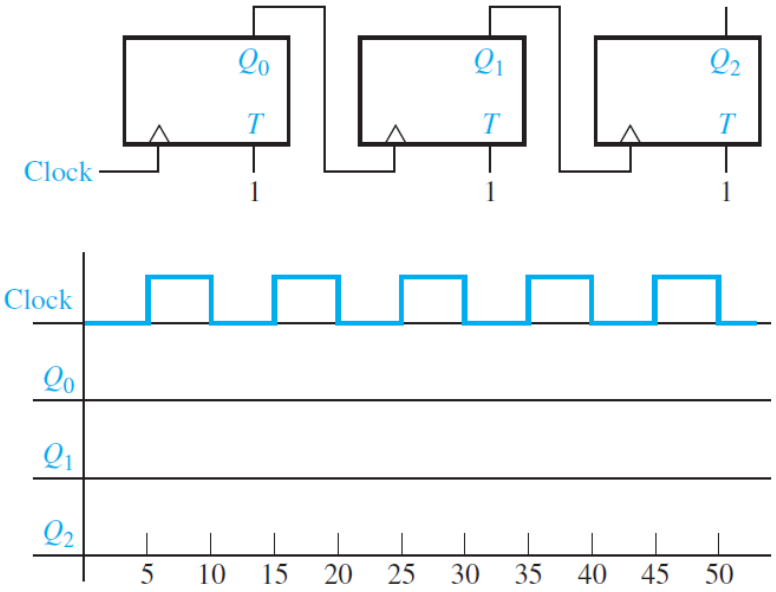
Operation summary:

$S = R = 0$	No state change
$S = 1, R = 0$	Set Q to 1 (after active Ck edge)
$S = 0, R = 1$	Reset Q to 0 (after active Ck edge)
$S = R = 1$	Not allowed



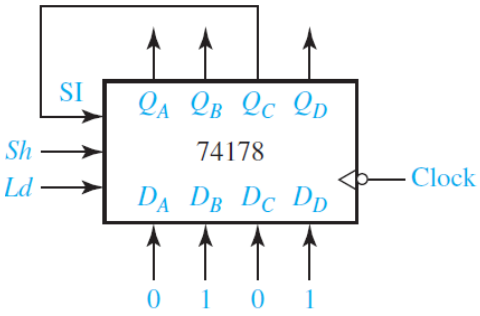
Q4

Here is the diagram of a 3-bit ripple counter. Assume $Q_0 = Q_1 = Q_2 = 0$ at $t = 0$, and assume each T flip-flop has a delay of 1 ns from the clock input to the Q output. Fill in Q_0, Q_1, and Q_2 of the timing diagram. The flip-flop Q_1 will be triggered when Q_0 changes from 0 to 1. The flip-flop Q_2 will be triggered when Q_1 changes from 0 to 1.

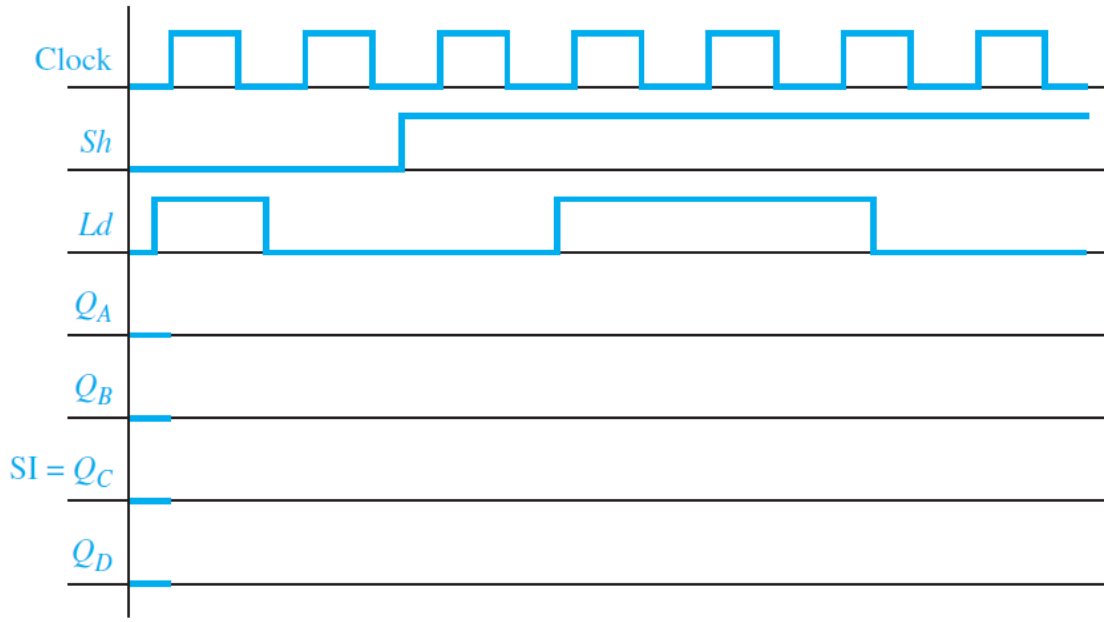


Q5

A 74178 shift register is described by the given table. All state changes occur on the 1-0 transition (falling edge) of the clock.The shift register is connected as shown. Complete the timing diagram.



Sh	Ld	Q_A^+	Q_B^+	Q_C^+	Q_D^+
0	0	Q_A	Q_B	Q_C	Q_D
0	1	D_A	D_B	D_C	D_D
1	X	SI	Q_A	Q_B	Q_C



Q6

Design a decade counter which counts in the following sequence using D flip-flops:
0100, 0010, 0001, 0011, 0000, 1001, 1000, 0111, 0110, 0101, (repeating) 0100…

Q7

Design a circuit using D flip-flops that will generate the sequence 0, 0, 1, 0, 1, 1 and repeat. Do this by designing a counter for any sequence of states such that the first flip-flop takes on this sequence. There are many correct answers, but do not duplicate states, because each state can have only one next state.

Q8
Design a decade counter which counts from 0 to 9 using the excess-3 code for decimal digits.