Lab1 Assignment

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COMPE 270 : Digital Systems

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Introduction

In this experiment, we will attempt to create logic circuits for a half-subtractor and for a full subtractor. This will be completed via truth tables, with logic expressions being derived from these tables with the help of Karnaugh maps. From there, these logic expressions will be converted into Verilog code, with this Verilog code in turn being used to create timing diagrams for the respective circuits.

Theoretical Preparation

1. Half-Subtractor

AB	D	B
00	0	0
01	1	1
10	1	0
11	0	0

D = A'B + AB' = A XOR B
B = A'B

2. Full-Subtractor

A	B	Bin	D	Bout
0	**0**	**0**	0	0
0	**0**	**1**	1	1
0	**1**	**0**	1	1
0	**1**	**1**	0	1
1	**0**	**0**	1	0
1	**0**	**1**	0	0
1	**1**	**0**	0	0
1	**1**	**1**	1	1

D = (A XOR B) XOR Bin
Bout = A'Bin + A'B + BBin

Experimental Setup

1. Half-subtractor

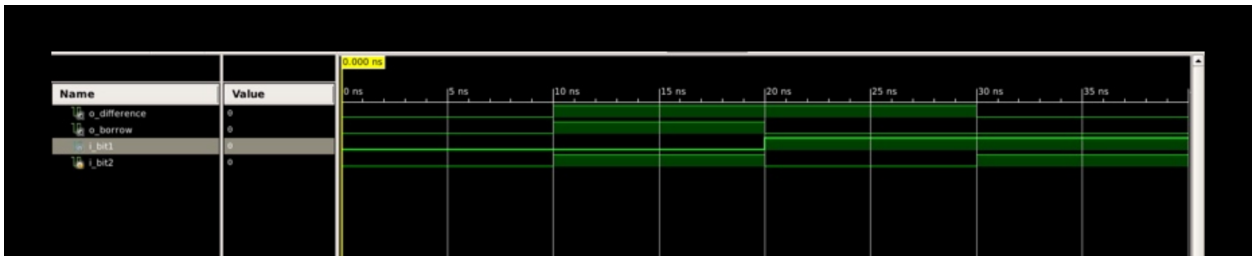
```
‘timescale lns / lps
module HA (
        i_bit1,
        i_bit2,
        o_D,
        o_B
         );

input i_bit1;
input i_bit2;
output o_D;
output o_B;

assign o_D = i_bit1 ^ i_bit2;
assign o_B = !(i_bit1) & i_bit2;

endmodule
```

2. Full-subtractor

```
‘timescale lns / lps
module HA (
        A,
        B,
        o_D,
        o_B;
          );

input A;
input B;
input Bin;
output o_D;
output o_B;

assign o_D = A ^ B ^ Bin;
assign o_B = (-A & B) | (-A & Bin) | (B & Bin);

endmodule
```

Experimental Results

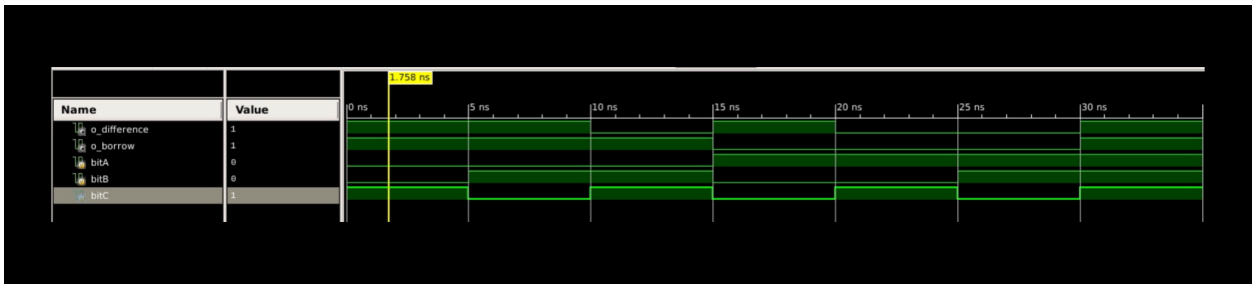
1. Half-subtractor



The timing diagram for a half subtractor circuit shows the relationship between the input signals and the output signals over time. The circuit has two inputs, A and B, and two outputs, D and B(which is different from the input B).
Since the input signals are stable at their initial values before changing, the timing diagram for each input combination will show the response of the output signals D and Bout over time.
For example, consider the input combination A=1 and B=0. The timing diagram would show the following:

- At time t=0, all input signals are stable at their initial values (A=1, B=0).
- At time t=1, the input signal A changes from 1 to 0. This change will cause the output signal D to change from 1 to 0, and the output signal Bout to remain at 0.
- At time t=2, the input signal B changes from 0 to 1. This change will cause the output signal D to change from 0 to 1, and the output signal Bout to change from 0 to 1.

2. Full-subtractor



The timing diagram for a full subtractor circuit shows how the input signals move through the circuit and how the output signals change. It displays the timing relationship between the input and output signals, and can be used to verify that the circuit is working correctly and meeting its design requirements.

In the case of a full subtractor circuit, there are three input signals: A (the minuend), B (the subtrahend), and Bin (the borrow in). There are also two output signals: D (the difference) and Bout (the borrow out).

The Verilog timing diagram shows the input signals as well as the output signals. Each input signal and output signal is plotted against time on a common time axis, with the horizontal axis representing time and the vertical axis representing the voltage level of the signal.

At the start of the timing diagram, all input signals are held constant at their initial values. As time progresses, the input signals change according to the design of the circuit. The timing diagram will show how these changes affect the output signals.

For example, if A, B, and Bin are held constant at their initial values, and then A changes from 0 to 1, the timing diagram will show how D and Bout respond to this change. D will change from 0 to 1 if B is 0 or from 1 to 0 if B is 1, and Bout will change from 0 to 1 if B is 1 and Bin is 0.

For example, consider the input combination A=1, B=0, and Bin=0. The timing diagram would show the following:

- At time t=0, all input signals are stable at their initial values (A=1, B=0, Bin=0).
- At time t=1, the input signal A changes from 1 to 0. This change will cause the output signal D to change from 1 to 0, and the output signal Bout to change from 0 to 1.
- At time t=2, the input signal B changes from 0 to 1. This change will cause the output signal D to change from 0 to 1, and the output signal Bout to remain at 1.
- At time t=3, the input signal Bin changes from 0 to 1. This change will cause the output signal D to change from 1 to 0, and the output signal Bout to remain at 1.

Conclusions

In conclusion, in this lab we designed a half subtractor and full subtractor. We began the design by creating truth tables. The truth table for the half subtractor had four possible combinations since there are two input variables (2^2 = 4), and the truth table for the full subtractor had eight possible combinations (2^3 = 8). From there, karnaugh maps were designed to derive the logic expressions for the half and full subtractors, and finally these logic expressions were converted to Verilog in order to obtain the half and full subtractor circuits' respective timing diagrams.