NICHOLAS LINDSAY

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EDUCATION

Yale University | August 2019 – Present Advisor: Professor Abhishek Bhattacharjee
Ph. D. Computer Science (expected May 2026).
M.Sc. Computer Science (awarded May 2024).

University of Glasgow | September 2015 – June 2019
B. Eng. First Class Honours. Electronic and Electrical Engineering.
Awarded Howe Prize (for Excellence in Lecture and Laboratory Coursework) and George Young Bursary.

PROJECTS

Deciphering Microarchitecture with Hardware Performance Counters | September 2024 – Present
- Invented a structured modelling framework for extracting microarchitectural features from performance counters. Developed project from theoretical conception to full software implementation, which includes a custom language with parser, graph visualization, integration with linear programming solver, and end-to-end data processing stack.
- As a case study, profiled large set of benchmarks on modern x86 microprocessor in controlled experimental environment, using *perf* to collect millions of data points. Using dataset discovered and characterized underspecified features related to virtual memory including TLB prefetching, MSHRs, and page table walk cache microarchitecture.

Future Virtual Memory Architectures | August 2019 – May 2024
- Experimentally determined on real hardware that address translation performance overhead often scales $\sim \log m$ with memory footprint. Proposed new metric that predicts address translation overhead from individual components.
- Profiled custom benchmarks on modified Linux kernel to evaluate overheads relating to page table management.
- Contributed to NAPOT virtual memory extension adopted by RISC-V standard. Released an open source software tool for simplifying operating system related studies.

Hardware Software Codesign for Brain Computer Interfaces | August 2019 – May 2020
- Worked with team to prototype brain-computer interface chip that operates under strict power constraints. Designed custom configuration bus interface and implemented in Verilog RTL. Chip currently taped out and under test.

PUBLICATIONS

CounterPoint: Using Hardware Event Counters to Refute and Refine Microarchitectural Assumptions.
ASPLOS 2026 (to appear). Nick Lindsay, Caroline Trippel, Anurag Khandelwal, Abhishek Bhattacharjee.

Understanding Address Translation Scaling Behaviours Using Performance Counters.
IISWC 2024. Nick Lindsay, Abhishek Bhattacharjee.

HALO: A Hardware-Software Co-Designed Processor for Brain-Computer Interfaces.
IEEE MICRO 2021. Karageorgos, Ioannis, Karthik Sriram, Xiayuan Wen, Ján Veselý, Nick Lindsay, Michael Wu, Lenny Khazan. Raghavendra Pothukuchi, Rajit Manohar and Abhishek Bhattacharjee.

EXPERIENCE

Yale Ph. D. Researcher | August 2019 – Present
- Conducted independent research on advanced computer architecture topics relating to virtual memory and hardware performance counters using experimental, statistical and theoretical methods and models.
- Published academic papers and delivered conference talk (ASPLOS, IISWC).
- Teaching Fellow for Introductory (CPSC323) and Advanced (CPSC420) Computer Architecture class. Created and delivered new tutorials on Verilog RTL design. Designed and delivered a new "Linker and Loader" programming assignment. Coordinated room bookings, held regular office hours, and prepared/graded assignments and exams.
- Mentored graduate and undergraduate students on various projects including workload characterization and gem5 simulator modelling. Regularly exchanged results and ideas with colleagues through meetings and reading groups.
- Configured and maintained experimental infrastructure including multiple workstation and server machines.

AMD Ph. D. Intern | June 2024 – August 2024
- Evaluated novel optimizations for state-of-the-art CPU cores. Employed range of tools from trace analysis to detailed microarchitectural simulators with complex codebases. Disseminated results to fellow researchers and engineers.

Arm Research Scientist Intern | June 2018 – August 2018
- Explored and evaluated implementations of proposed architectural feature. Evaluated prototypes using *gem5*. Discovered, documented and mitigated unexpected performance bug. Delivered department-wide presentation.

SKILLS

Concepts: computer architecture, microarchitecture, virtual memory, performance profiling, statistics, optimization
Languages/Tools: python, C, C++, bash, gem5, perf, git, numpy, scipy, matplotlib, pulp, seaborn, CMake, Jira, vscode