FPGA Development for the LHCb Vertex Locator Upgrade

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Abstract

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Contents

1 Introduction

1.1 The Standard Model of Particle Physics

Central to the modern age particle physics is the standard model,

The standard model, shown in equation **??**, is a quantum field theory that discribes the fundermental particles and how they interact. While this essay does require, or attempt, to understand the intricate detail of the stardard model; the aim of many particle physics experiments is to Test, measure and varify the model. Dispite being the current best theory to explain particle interactions, the model is not complete. There are many undescribed phemimina, such as the matter domination in the universe, that require physics behond the standard model. To that end, major international efforts, namely in the form of the Large Hardrom Collider, aim to further knowledge and understanding of the underlying physics of the universe. [**?**]

1.2 The LHCb Experiment

One such Experiment and the Large Hadrom Colider is Large Hadron Colider beauty (LHCb).

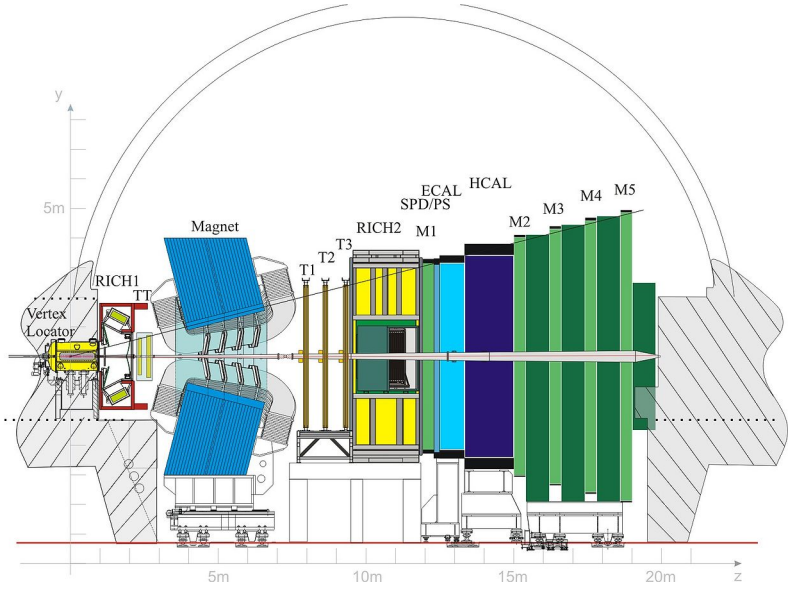

Figure 1: The LCHb Detector along the bending plane.

1.2.1 The Detector

1.2.2 Physics Studied at LHCb

1.2.3 VELO Upgrade

1.3 FPGAs in Particle Detectors

1.3.1 Field Programable Gate Arrays

1.3.2 The Role of FPGA's in the VELO Upgrade

2 Scrambling Algorithms

Due to radiation levels inside the detector chamber, the main data processing takes place in a concrete bunker away from the detector, minimising radiation damage to the hardware. To facilitate this, optical linkes, 20 per modual, are used to transfer the data from the front end VELO to the Data Aquizition FPGA (DAQ). When comunicating data digitaly, the tranfering modual (TX) and the recieving modual (RX) must have syncrinised clocks. When achieving this, there are three main approunches:

I. Syncinize both the TX and RX from a single central clock.

II. Transmit the TX clock to the RX modual.

III. Use bit-changes in the data to coninuesly sycnronise the RX clock.

The two former of these options, although the most convienient, are not appropriate for the VELO as they are suseptable to unforseens delays that could cause desyncronisation. The latter, while less suseptable to delays, requires data with a high density of tranitions to reduce the likelyhood of a desyncronisation event. Becuase delays in the data are possible, the latter option has been selected.

2.1 The Role of Scrambling Data in the VELO

For the reasons described in Section 2, it is nessesary to ensure that the data has large density of transitions before being transmitted from the front-end detector to the DAQ modual. However, as the majority of SP hitmaps are empty, the data has a large bais towards 0s. This reduces the frequancy of transitions in the data - increasing the probability of a desyncronisation event. It is therefor nesseccary to scramble the data pria to transmition and descramble the data in the DAQ FPGA.

Scrambleing and later descrambleing the data is not a trivial exercise. The scrambleing (TX) modual and descrambling (RX) modual must use a sycronised *'key'*, derived from the previous states of the data. There are two options when generating this *'key'*:

Additive The *'key'* is generated by evolving the previous *'key'* at each itteration of data using the incoming frame.

Multiplicative The *'key'* is generated from the previos n frames. (Here n is a variable specific to the algorithm).

2.2 Scrambler Options

Three scrambling algorithums have been concidered:

Additive Scrambler
This algoritum is simple and easy to use, however has the drawback of time dependance. If a desyncronisation event occours, all subsequent data is rendered unrecoverable untill such time as a global reset signal is sent. Further adding to the drawbacks, if a data packet is not sent from the TX during any clock cycle the RX descrambler will still evolve its descramble key - the TX sccrambler, however, will not. This will ofcourse desyncronise the *'keys'*, and as before all subsequent data is lost.

Intermediate Scrambler
Deriving its name from being the second algorithum under concideration, the Intermediate Scrambler is a **multiplicative** algorithm. The *'key'* is generated from the current incoming frame and the previous frame. Therefor, in the event of desyncronisation, only two frames are lost before the *'key'* is automatically recovered. This is a significant improvment over the Additive Scrambler.

VeloPix Scrambler
Named as, at the time of the start of the project *(September 2015)*, this algorithum is the current preffered option by the VeloPix team; this too is a **multiplicative** algorithm. The *'key'* is, again like the Intermediate Scrambler, generaged from the currect and previous data frame. The VeloPix Scrambler differse from the Intermediate scrambler as it aims to more effeciently scramble the data.

2.3 Algorithm Analysis

2.3.1 Messurements of the Algorithms

2.3.2 Results of Analysis

2.4 Conclusion

3 Event Isolation Flagging

3.1 Motivation

3.2 Time Sorting Data

3.3 Bubble Sorting

3.4 Isotation Checking

3.5 Conclusion

4 Future Development

4.1 LHCb 2020 Upgrade

4.2 Further Development of FPGA's in the VELO

5 Conclusion

6 Acknoledgments

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