Elec 413 Project Report

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Date here

Abstract

Tbd

GitHub for Chip 1: https://github.com/farnkjin/openEBL-2025-02/blob/main/submissions/ELEC413_FrankJin.gds

GitHub for Chip 2: https://github.com/SiEPIC/UBC-ELEC413-2025/tree/main/submissions

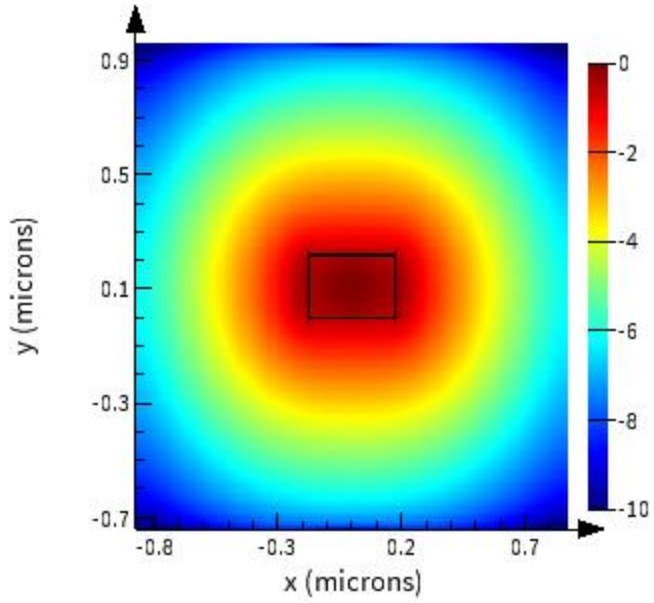
Introduction

TBD

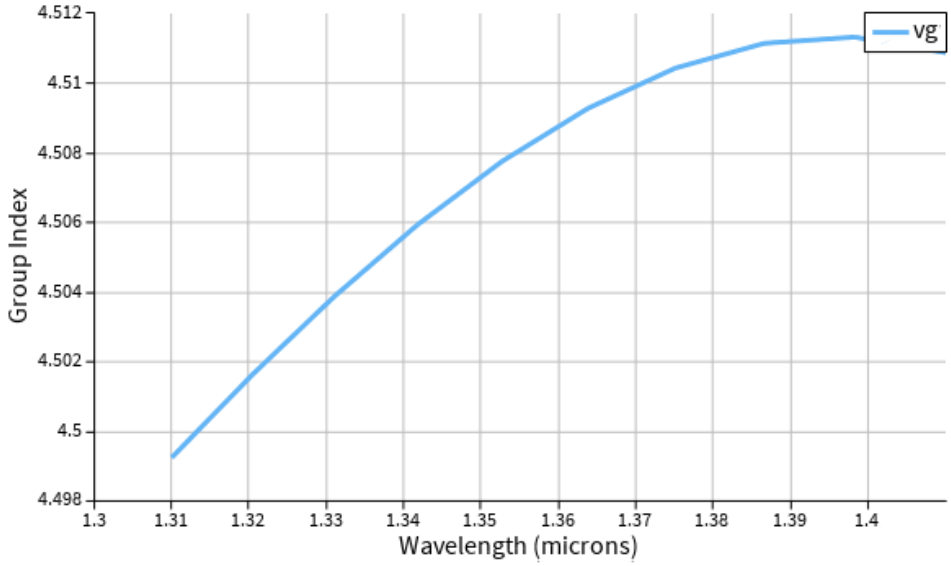
Theory

Modelling

I first use Lumerical MODE to simulate the waveguide

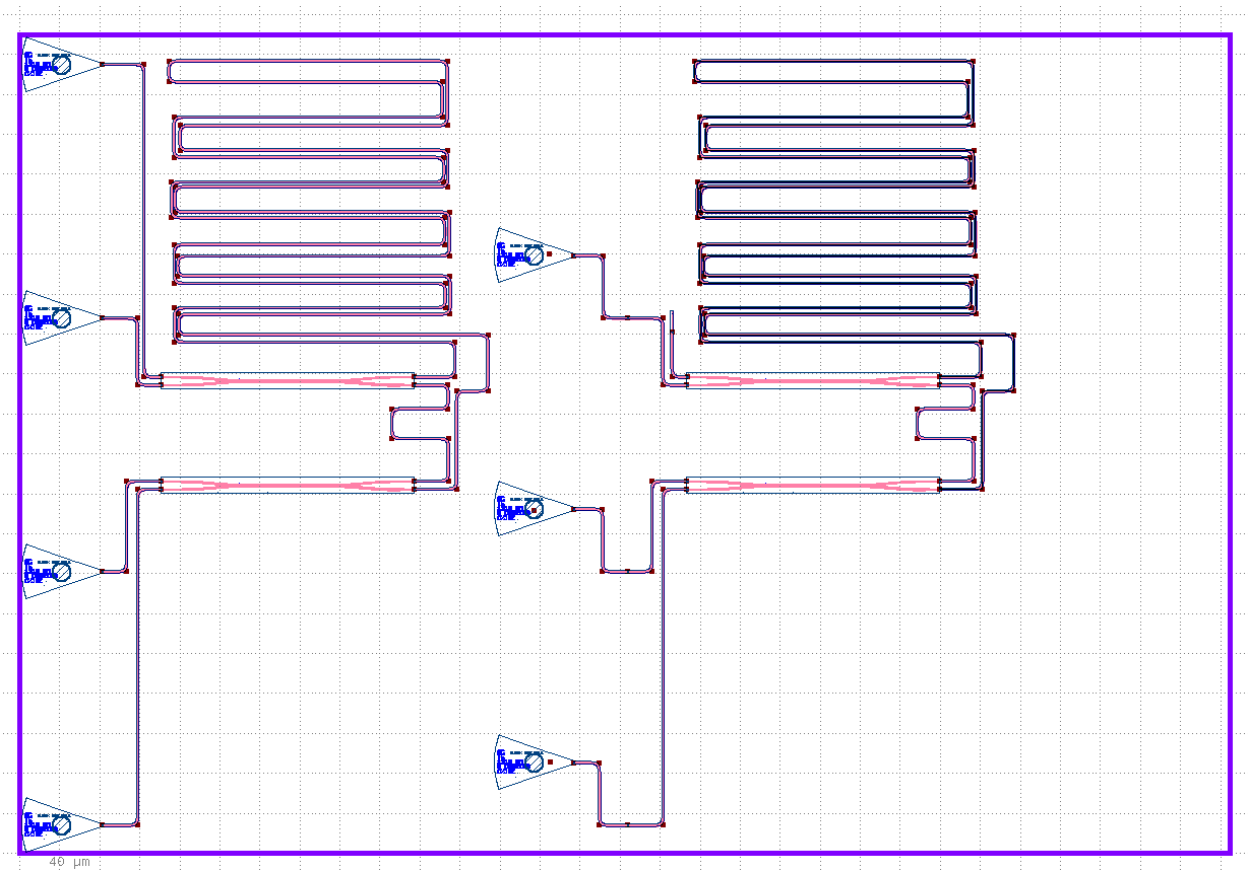


Then, doing a frequency sweep I obtained the group index n_g at 1310nm, which was around 4.435.

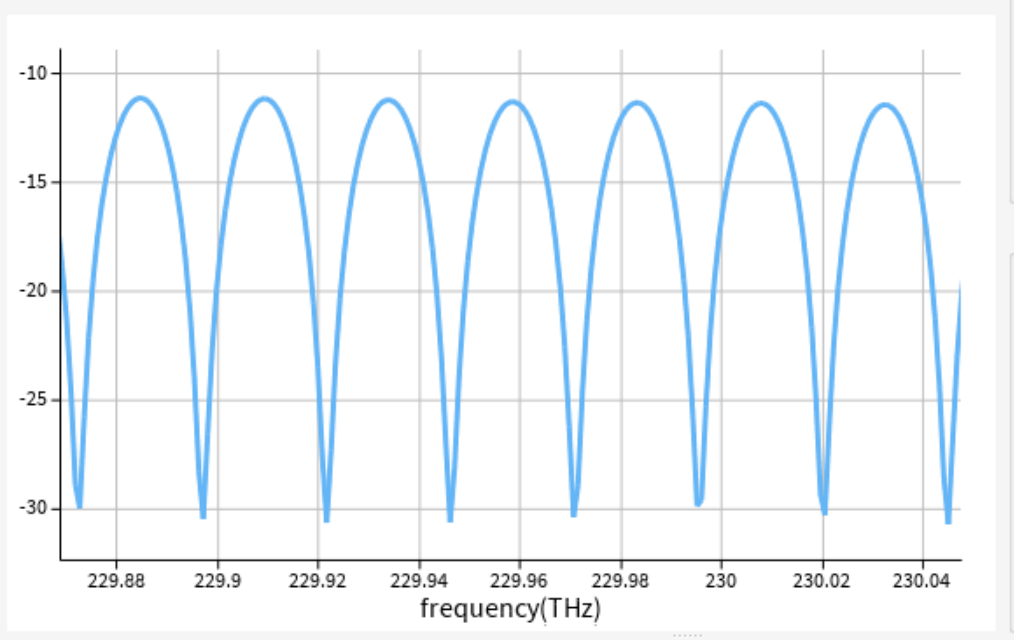


Using this and the equation FSR = cLng I was able to calculate the path length difference which was around 2.705mm.

Then, using KLayout I created 2 structures, one with a waveguide width of 350nm and one with a width of 335nm to account for manufacturing error.



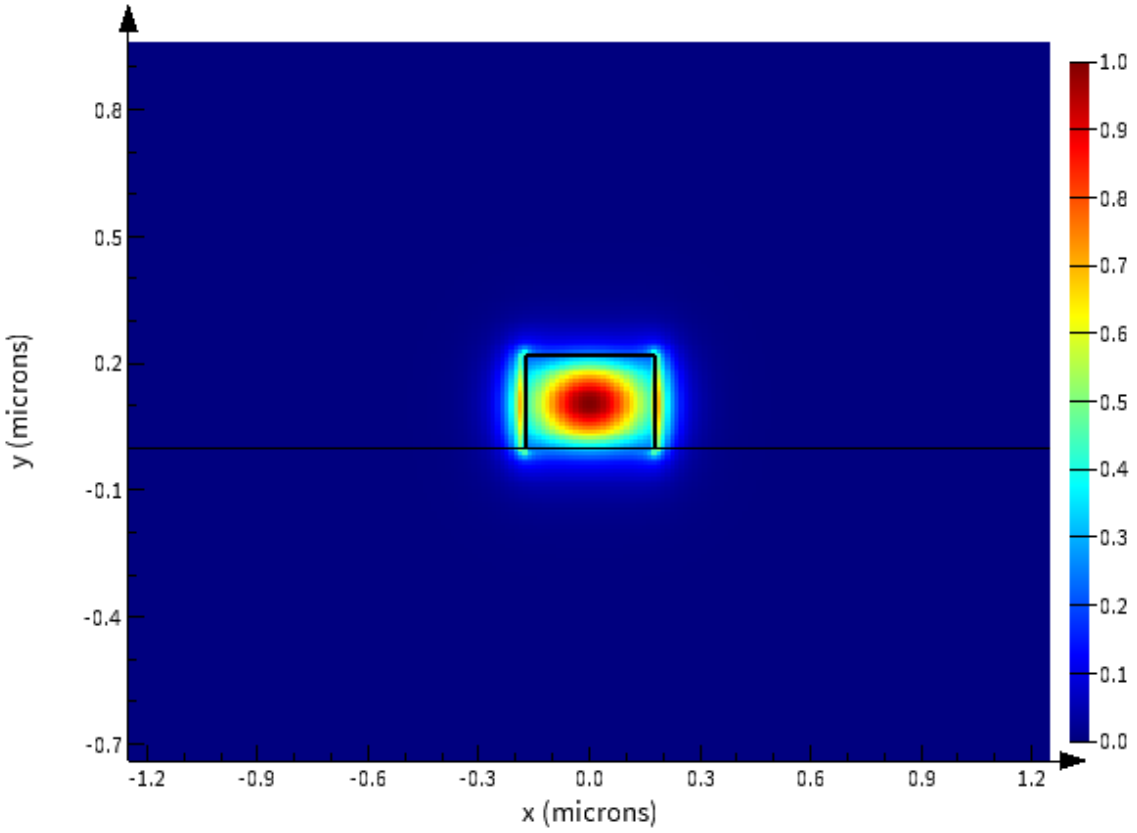
I then simulated this circuit in Lumerical Interconnect to verify an FSR of 25GHz.



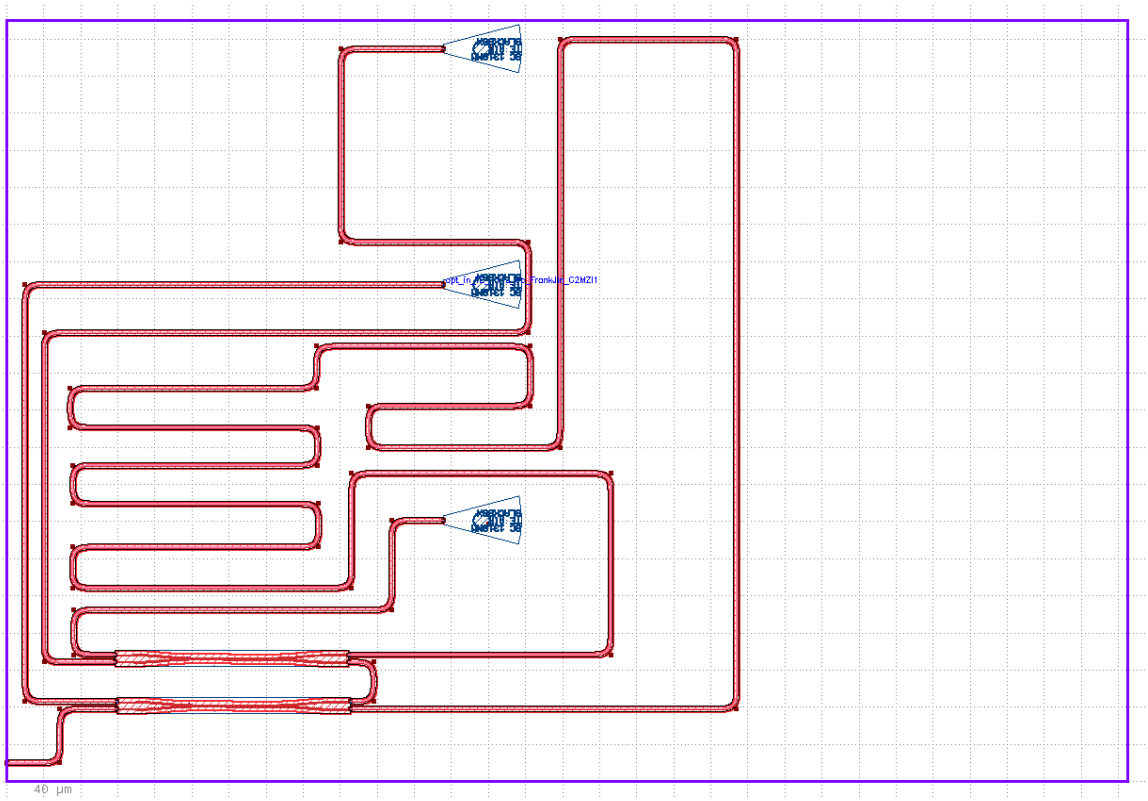
By looking at the distance between peaks, we can calculate the FSR to be aroun 24.5GHz.

Chip 2

Simulated waveguide using MODE with an air cladding.



Obtained a group index of 4.7696 and calculated dL to be 2.5159mm.



Simulating this circuit on interconnect, we can get the transmission plot and calculate the FSR to be around 24.49 GHz