A Study on Mach-Zehnder Interferometer

Sherwin Tiu
Department of Electrical and Computer Engineering
University of British Columbia, Vancouver, BC V6T 1Z4, Canada

***Abstract*—**

I. INTRODUCTION

The URL for the Github repository of my Chip 2 can be found here: https://github.com/SherwinTiu/UBC-ELEC413-2025

The following information combines (incomplete) aspects of my Chip 1 and Chip 2 designs.

II. THEORY

A. Background

III. DESIGN

A. Waveguide Design

From fabrication bias requirements and the availability of componenets in the SiEPIC PDK, the waveguide has a design of 350 nm × 220 nm strip waveguide. This was simulated in Lumerical MODE Solutions using the Palik dataset of materials at λ = 1310 nm, with results of the model seen in Figure 1. A wavelength sweep was performed from 1.31 μm to 1.36 μm, and the Effective Index vs Wavelength plot was curve-fitted into a second-order Taylor series expansion in Equation 1, and the resulting plot can be found in Figure 2.

Through the simulation, we can get the effective index, n_{eff}, and the group index, n_g. For the TE mode and λ = 1310 nm, n_{eff} = 2.84185 and n_g = 4.4991. For the TM mode, n_{eff} = 2.04889 and n_g = 4.6196. These parameters were used in the design of a MZI Chip, to be referred to as Chip 1.

$$n(\lambda) = 2.43114 - 1.57892(\lambda - 1.31) - 0.0723265(\lambda - 1.31)^2 \quad (1)$$

B. MZI Circuit Model

Using n_g gained from designing the waveguide, we use Equation 2 to get the difference in length between the two waveguides, ΔL = 2.667 mm. Also gained from the simulation is the propagation loss, α, which is used to calculate for the propagation constant in Equation 3. The transfer function for the circuit model is obtained through equation 4.

$$FSR = \Delta\lambda = \frac{\lambda^2}{\Delta L n_g} \quad (2)$$

$$\beta(\lambda) = \frac{2\pi n_{eff}(\lambda)}{\lambda} + i\frac{\alpha}{2} \quad (3)$$

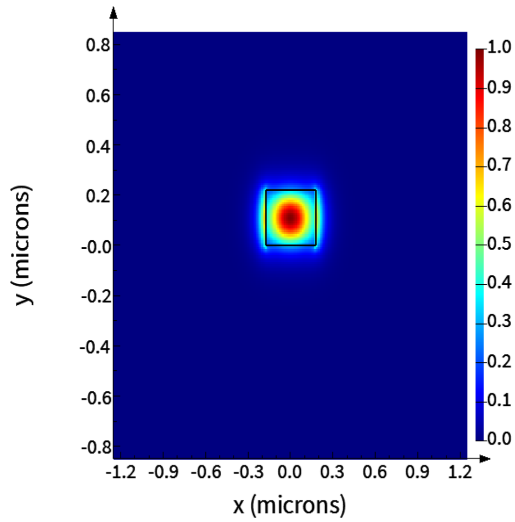

Fig. 1. The 1st mode profile with 98% TE polarization for the 350 nm $times$ 220 nm SiO_2-cladded waveguide at λ = 1310 nm, calculated using Lumerical MODE Solutions.

Fig. 2. The plot of the single waveguide modeled through a second-order Taylor series expansion.

$$T_{MZI}(\lambda) = \frac{1}{4}|e^{-i\beta L_1} + e^{-i\beta L_2}|^2 \approx \frac{1}{4}|1 + e^{-i\beta \Delta L}|^2 \quad (4)$$

C. Laser Integration to Chip 2

In the previous section, the circuit was designed with a SiO_2-cladded waveguide. In this section, a new circuit, to be called Chip 2, will have an air-cladded waveguide.

In Figure 3, the results of the mode calculation for an air-cladded waveguide can be seen. For the TE mode and λ = 1310 nm, n_{eff} = 2.31881 and n_g = 4.90580, with a loss of 0.00078613 dB/cm. For the TM mode, n_{eff} = 1.59873 and n_g = 6.19578, with a loss of 0.00086512 dB/cm.

Another wavelength sweep was performed with the plot curve-fitted using a second-order Taylor series expansion in Equation 5, with the resulting plot seen in Figure 4.

$$n(\lambda) = 2.31879 - 1.97127(\lambda - 1.31) - 0.872847(\lambda - 1.31)^2 \quad (5)$$

Using Equation 2, ΔL = 2.446 mm. The propagation loss for this circuit is $\alpha_{\mu m^{-1}} = 17.115 \times 10^{-9}$, giving $\beta(\lambda) = 11.122 \times 10^6 + 8.558 \times 10^{-9} i$ from Equation 3. Using Equation 4, the transfer function is then calculated to be $T_{MZI}(\lambda) = 0.99981$.

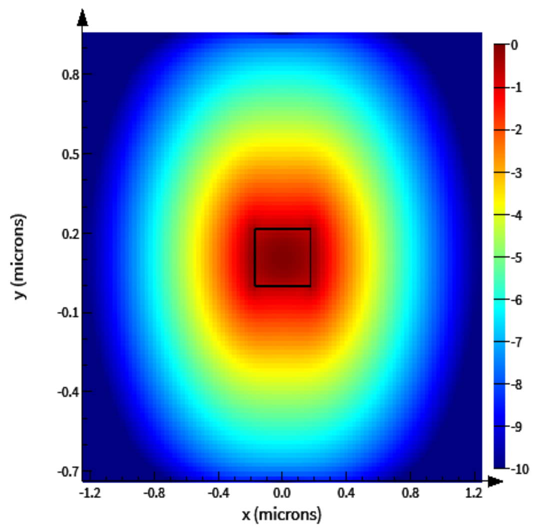

Fig. 3. The 1st mode profile with 97% TE polarization for the 350 nm *times* 220 nm air-cladded waveguide at λ = 1310 nm, calculated using Lumerical MODE Solutions.

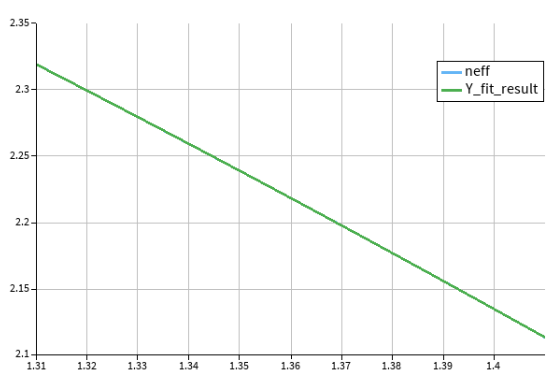

Fig. 4. The plot of the single waveguide for Chip 2 modeled through a second-order Taylor series expansion.

D. Mask Layout

Four iterations of Chip 1 were placed in Figure 3. The first layout with ΔL = 2792.22 μm is designed with spiral waveguides. The second waveguide with ΔL = 2446.09 μm is designed in a square spiral paperclip pattern. The third design uses an elongated spiral paperclip. The three designs were made to be compact so that more layout iterations can be done on a single chip. This will also lower propagation loss compared to the final design, which maximizes the remaining chip space. This fourth iteration is designed to allow for phase accumulation, although this will mean longer propagation time and an increased sensitivity to temperature variations.

For Chip 2, the design was chosen so as to reduce the number of bends beyond those already present in the spiral paperclip.

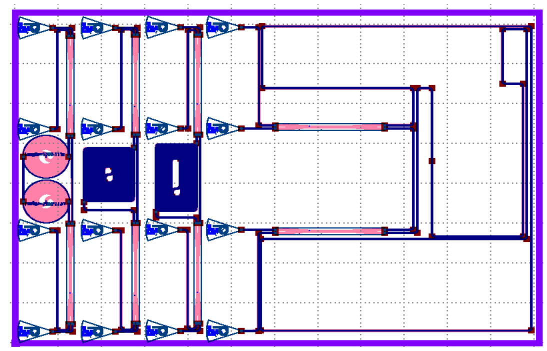

Fig. 5. Mask layout for Chip 1

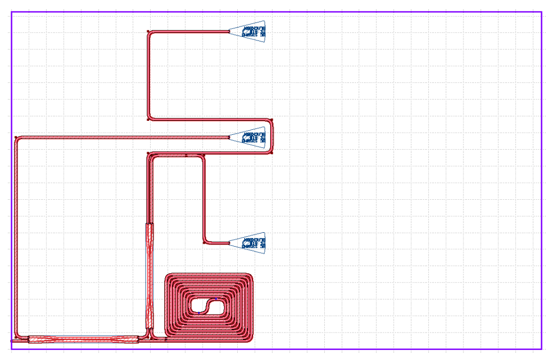

Fig. 6. Mask layout for Chip 2

IV. Conclusions

References