ELEX 7660: Lab 1

7-Segment LED Decoder

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Table of Contents

Table of Figures

1 Modules

1.1 Decode2

```
// decode2.sv - ELEX 7660 - 2 to 4 decoder. Selects which digit of the 7-segment
LED Display to enable.
// Nicholas Huttemann 2018-01-12
module decode2 ( input logic [1:0] digit,
                 output logic [3:0] ct);

always_comb
      case(digit)
            0 : ct = 4'b0001;
            1 : ct = 4'b0010;
            2 : ct = 4'b0100;
            3 : ct = 4'b1000;
      endcase
endmodule
```

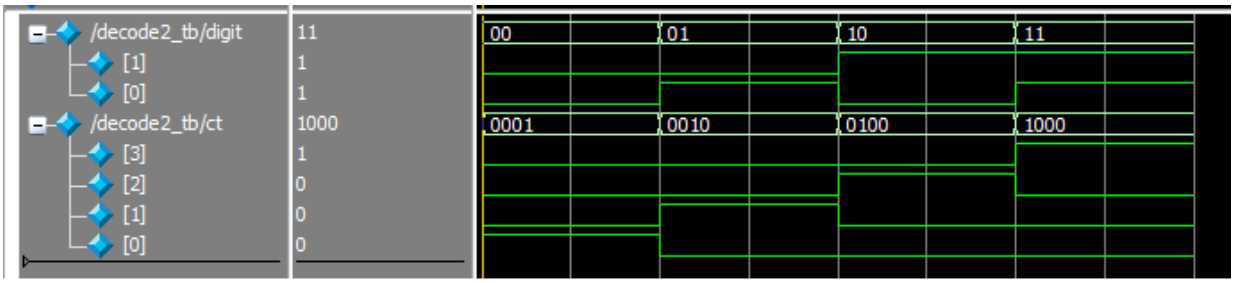

Figure 1: Decode2 Waveform

1.2 Bcitid

```
// bcitid.sv - ELEX 7660 - Module that selects and stores the last 4 digits of my
student ID
// Nicholas Huttemann 2018-01-12
module bcitid ( input logic [1:0] digit,
                output logic [3:0] idnum);

always_comb
      case(digit)
            3 : idnum = 0;
            2 : idnum = 4;
            1 : idnum = 3;
            0 : idnum = 9;
      endcase
endmodule
```

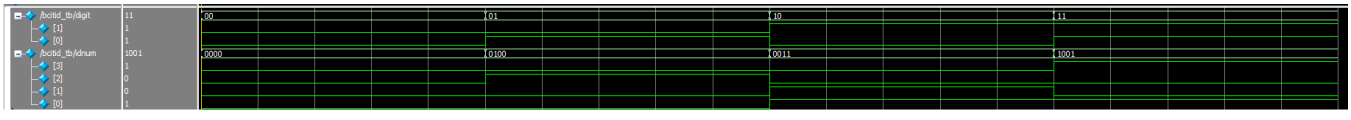

Figure 2: Bcitid Waveform

1.3 Decode7

```
// decode7.sv - ELEX 7660 - Converts 'num', a decimal integer 0 - 9 (10 for DP),
into an 8-bit vector 'leds' that will light up corresponding segments on a 7-
segment LED.
// Nicholas Huttemann 2018-01-12
module decode7 ( input logic [3:0] num,
                 output logic [7:0] leds);

always_comb
      case(num)
            0 : leds = 8'b11000000;
            1 : leds = 8'b11111001;
            2 : leds = 8'b10100100;
            3 : leds = 8'b10110000;
            4 : leds = 8'b10011001;
            5 : leds = 8'b10010010;
            6 : leds = 8'b10000010;
            7 : leds = 8'b11111000;
            8 : leds = 8'b10000000;
            9 : leds = 8'b10010000; //Updated to new style of 9
            10: leds = 8'b01111111;
      endcase
endmodule
```

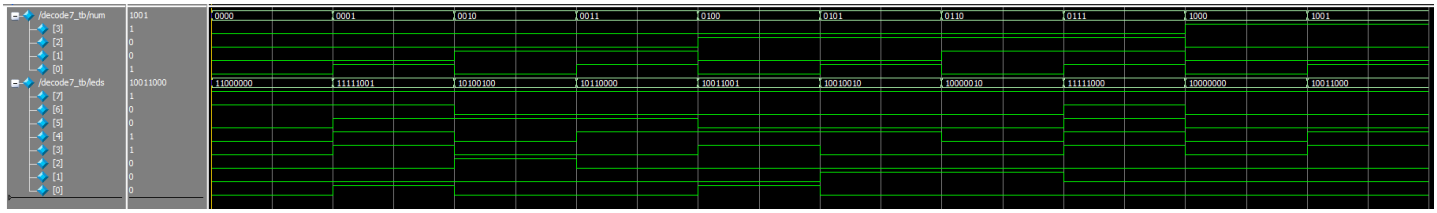

Figure 3: Decode7 Waveform

1.4 Schematic

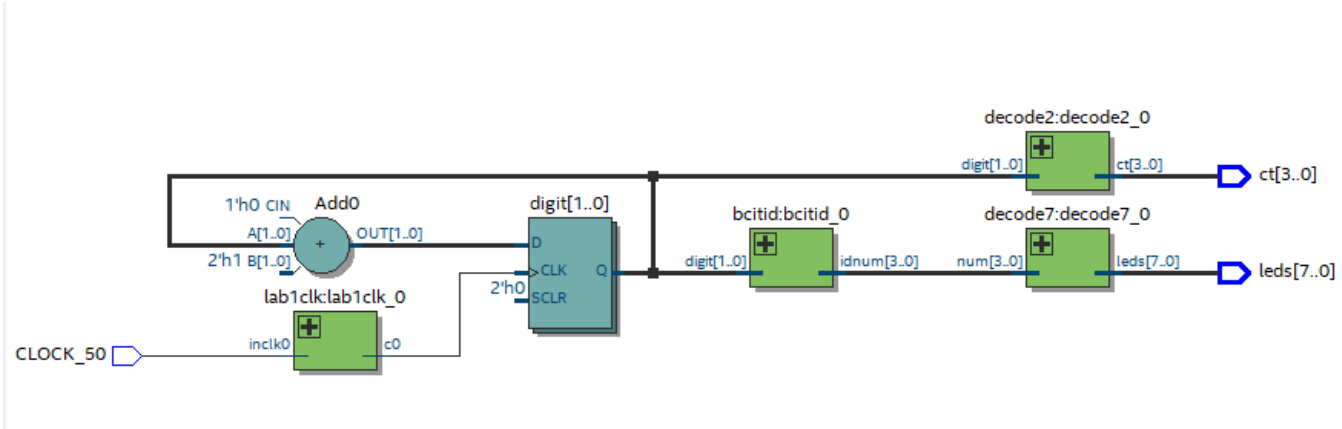

Figure 4: Circuit schematic created by Quartus

1.5 Compilation Report

Flow Status	Successful - Fri Jan 18 08:51:31 2019
Quartus Prime Version	18.0.0 Build 614 04/24/2018 SJ Lite Edition
Revision Name	Lab1
Top-level Entity Name	lab1
Family	Cyclone IV E
Device	EP4CE22F17C6
Timing Models	Final
Total logic elements	7 / 22,320 (< 1 %)
Total registers	2
Total pins	13 / 154 (8 %)
Total virtual pins	0
Total memory bits	0 / 608,256 (0 %)
Embedded Multiplier 9-bit elements	0 / 132 (0 %)
Total PLLs	1 / 4 (25 %)

Figure 5: Compilation Report