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Computer Architecture
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Deliverable 1:

Way 1 [Gated Clock]   Way 2 ["Good Practice"]

d[i] → [box] → q[i]   d[i] → [box] → q[i]

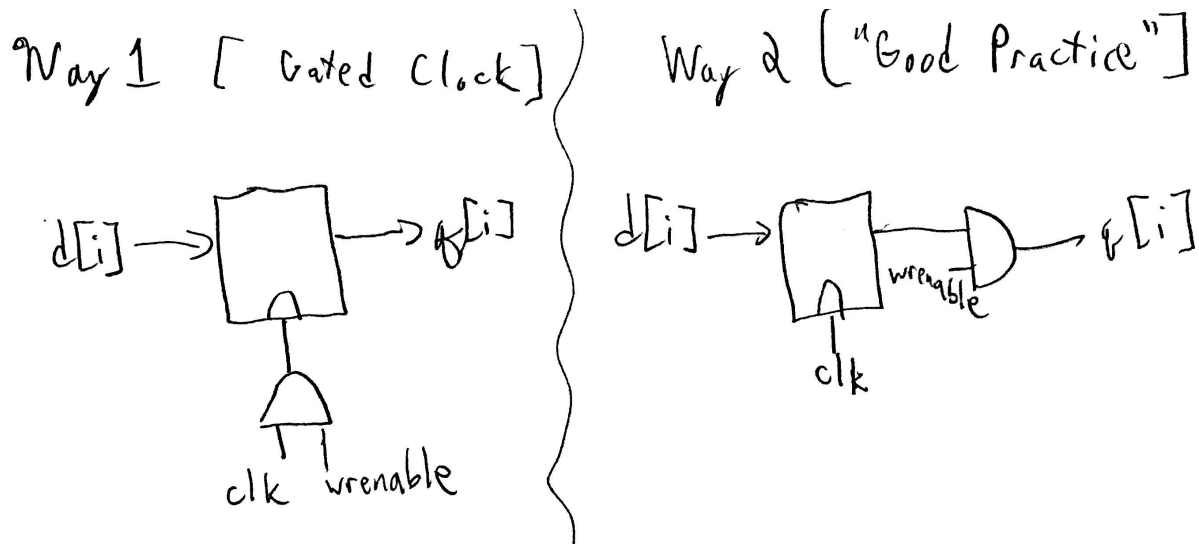clk wrenable   clk

Deliverable 6:

The decoder module, as given in HW4, works by taking in an "enable" of whether or not anything should be written, and an address, which gives the location of the output that should be changed. What happens is that "enable" is shifted by the number of bits denoted in "address" (up to 31 positions). This occurs because the << operator is a "shift left" operation, which means that it will be shifted and select the correct register file. This will then allow the code to function as a decoder.