# ECEC 471 Lab 2

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# 1 Introduction

## 1.1 Overview

This lab is meant to guide us through the tools while designing an inverter as well as using the built-in analysis tools to decide on the best width to get a symmetric inverter. CMOS circuits are designed by tying the outputs of a pull down and pull up network together. The pull up network in this lab is a singular pmos tied to voltage high, or Vdd, and the pull down network is an nmos tied to voltage low, or ground. An inverter takes whatever signal it is given and flips it, causing a one to become a zero and a zero to become a one. Rise time and fall time are the time it takes for the ouput to rise from 10% to 90% of the total voltage or fall from 90% to 10% of the total voltage. Propagation delay is the time it takes for the output to appear after the input, usually measured by taking the difference of the 50% marks of the input and output.

## 1.2 Symmetric Inverters

A symmetric inverter is an inverter whose rise and fall times are the same. In other words, the input and output voltage cross the half point of Vdd at the same time. We get a symmetric inverter by keeping one of the transistor widths constant and changing the other.

# 2 Simulation and Analysis

## 2.1 Schematic Design

Figure 1 shows the transistor-level schematic of the inverter before the ideal width for the pmos was found. The initial width of both transistors was 90nm and the length of both transistors is 50nm. Figure 2 shows the simula-

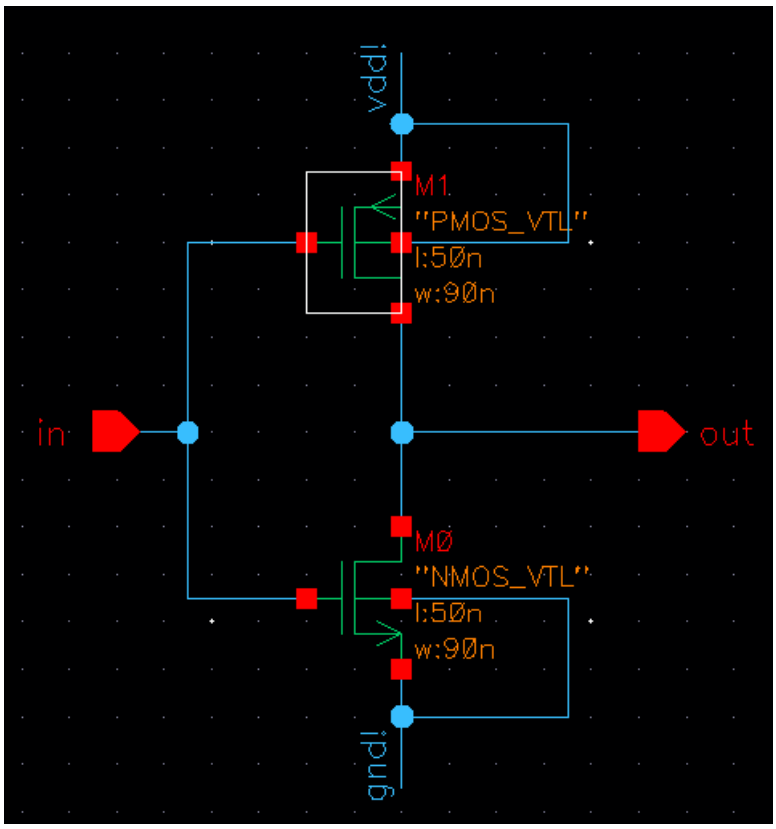


Figure 1: Transistor-level Non-symmetric Inverter Schematic

tion schematic with the source and load. A pulse is used so we can measure the rise and fall times as well as the propagation delay. The pulse has an amplitude of 1.2V, a period of 100ns, a rise time of 10ps, 1 fall time of 10ps and a pulse width of 50ns. A 5fF capacitor was tied to the output to get it closer to a realistic model where the inverter would have some capacitance. The transient analysis and DC response of the circuit are shown in Figure 3

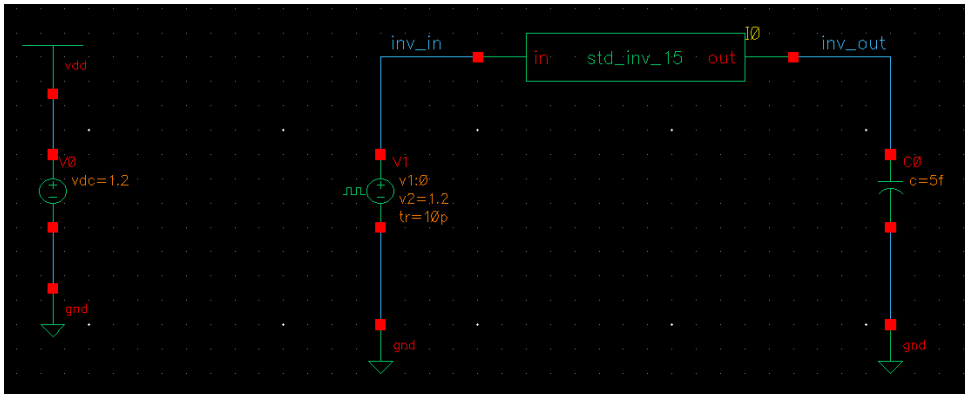


Figure 2: Simulation Schematic

and Figure 4 respectively. Using the transient analysis graphs a rise time of 29.94ps, a fall time of 51.82ps, and propragation delay of 25.68ps were all easily found. The switching voltage was found to be 538.739mV using the DC response graph which is not the desired 0.6V we want for a symmetric inverter. To find the desired width of the pmos transistor, we used para-

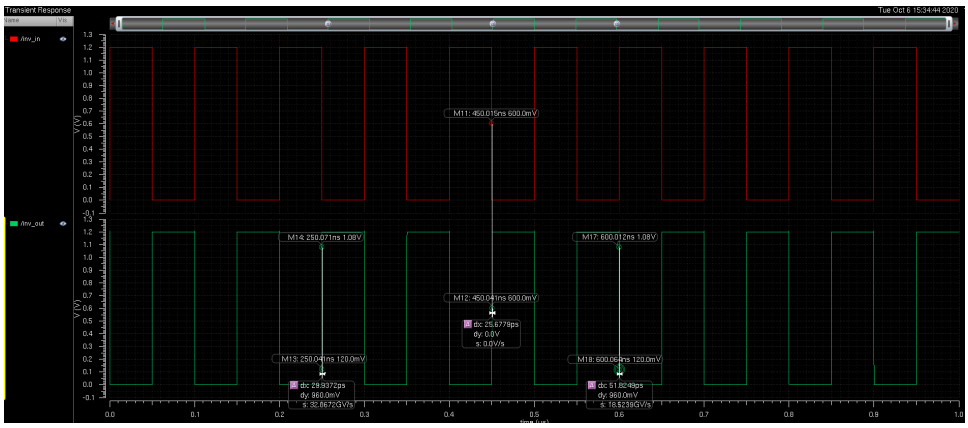


Figure 3: Transient Analysis

metric analysis to get Figure 5 and found that a width of 142.9412nm gave us a switching voltage of about 0.6V. The schematic was updated to use the new width in Figure 6 and DC response was simulated and graphed again to give us Figure 7 which shows a switching voltage of about 0.6V.

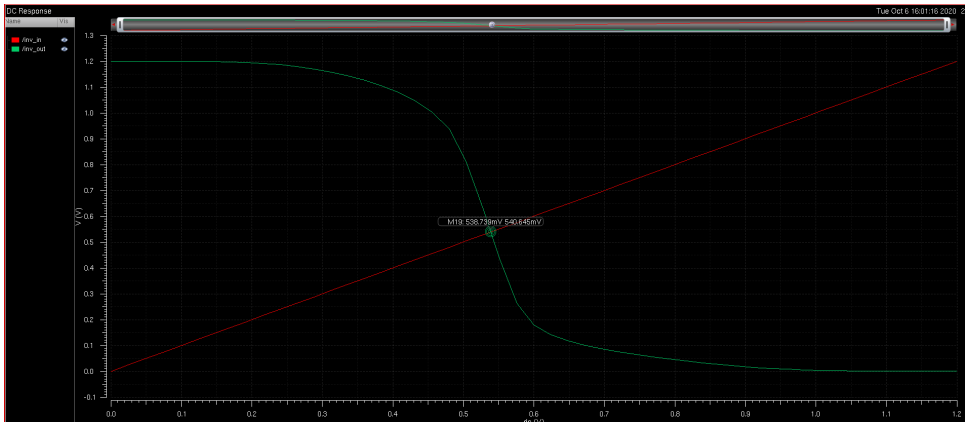


Figure 4: DC Response of an Asymmetric Inverter

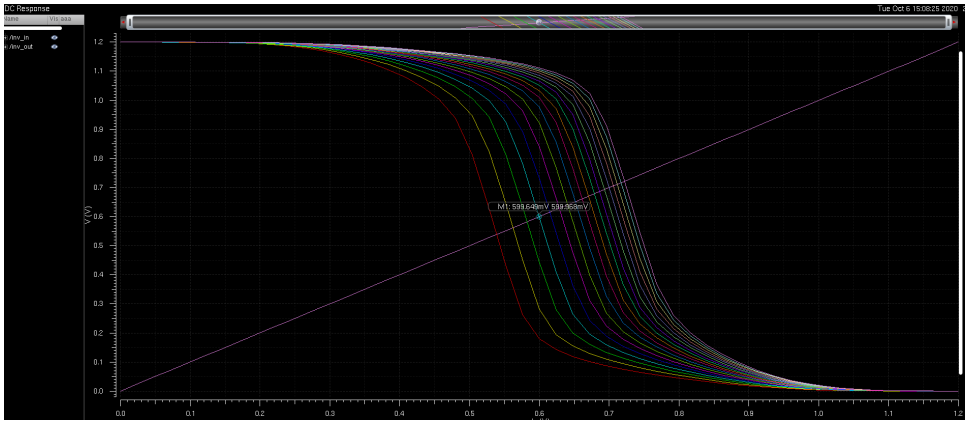


Figure 5: Parametric Analysis

## 2.2 Layout Design

After the schematic was finished with it designed to be a symmetric inverter, layout was done. The pmos and nmos were built first, taking special care to make sure the width of the transistors match the schematic. The pmos and nmos are shown in Figure 8 and Figure 9 respectively. Afterwards, the Vdd and ground rails were added to the design as shown in Figure 10. Lastly, design rule checking(DRC) is used to make sure that no design rules are being violated and everything is fixed very painstakingly. The results can be seen in Figure 11 After that layout versus schematic(LVS) was used to make

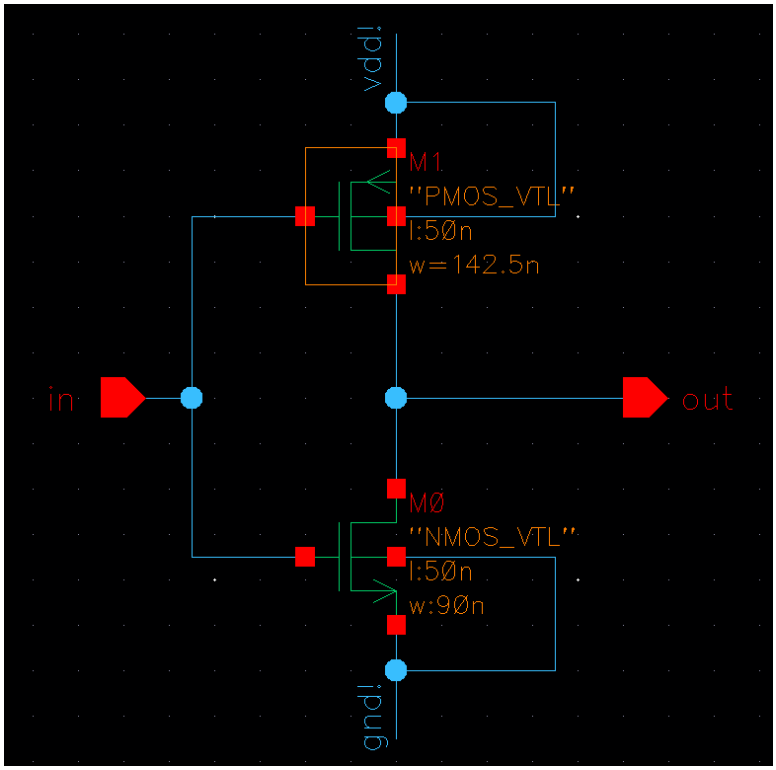


Figure 6: Symmetric Inverter Schematic

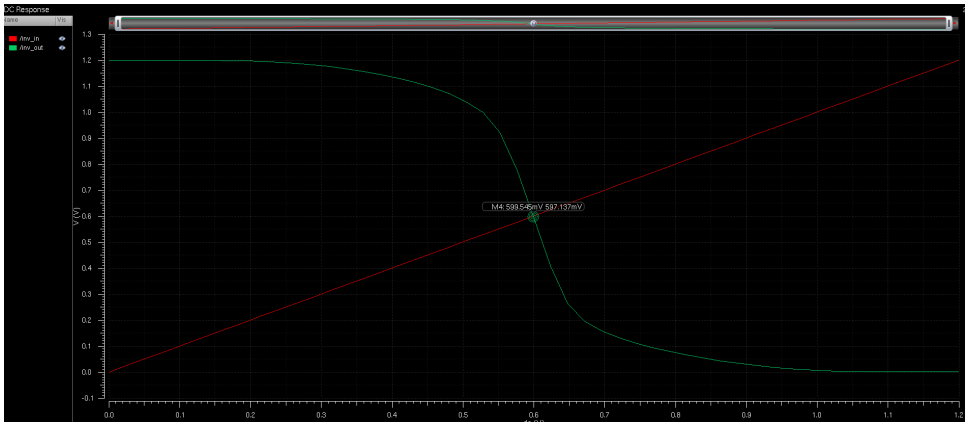


Figure 7: DC Response of a Symmetric Inverter

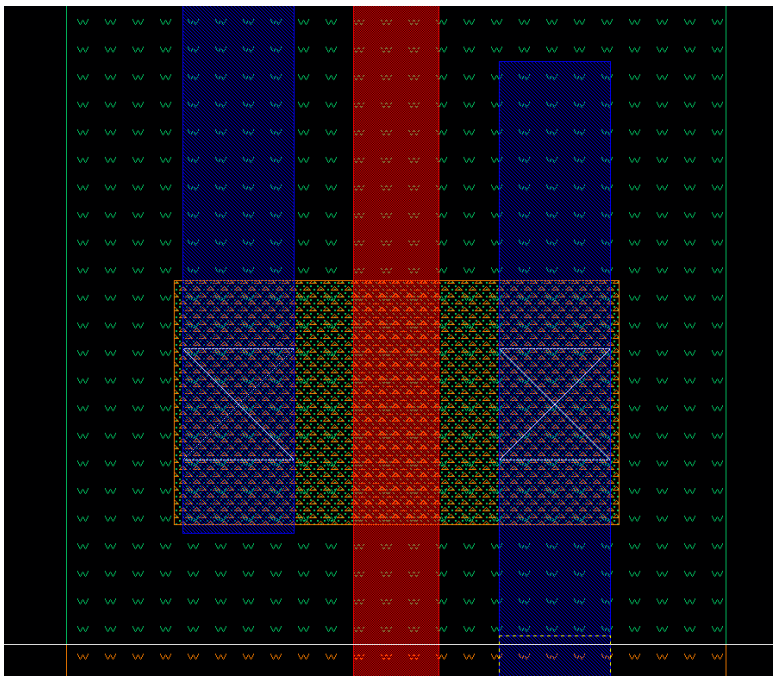

Figure 8: pMOS Layout

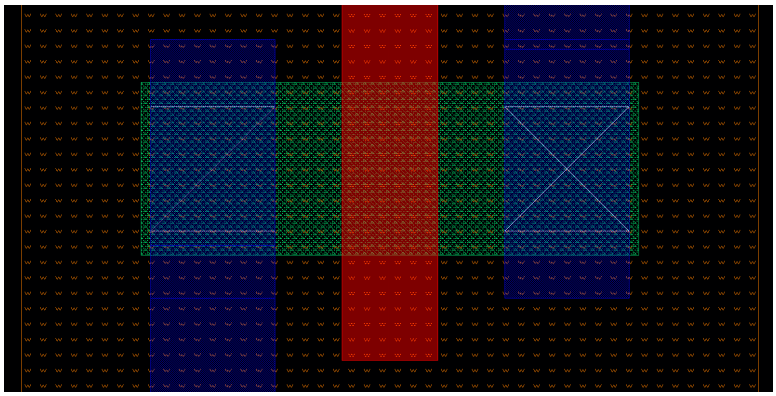

Figure 9: nMOS Layout

sure our layout matches the design we modeled with the schematic and can be seen in Figure 12.

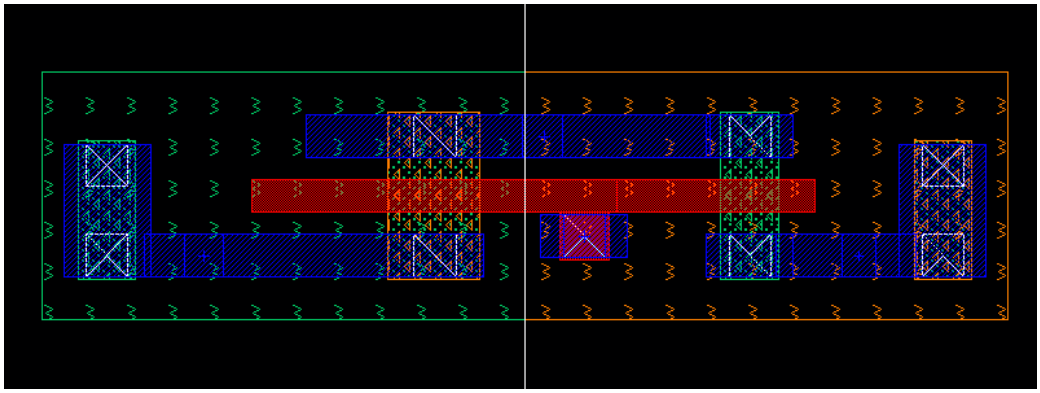

Figure 10: Inverter Layout

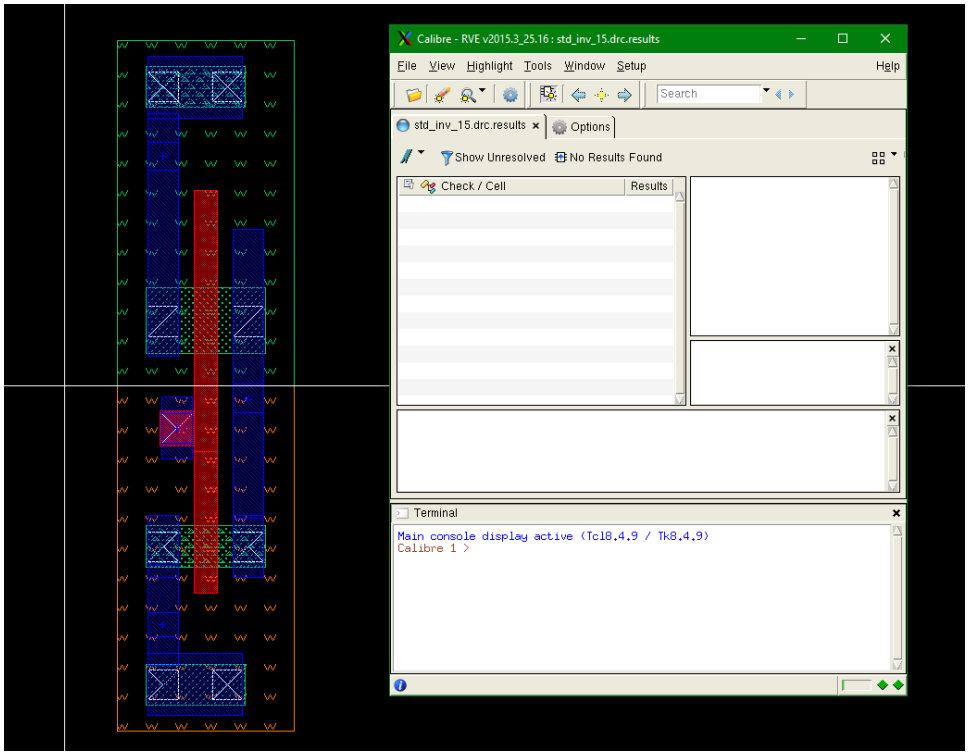


Figure 11: DRC Results

# 3 Conclusion

The lab was a very good way to work through building a schematic and deriving a layout from that schematic. It helped me get used to the tools

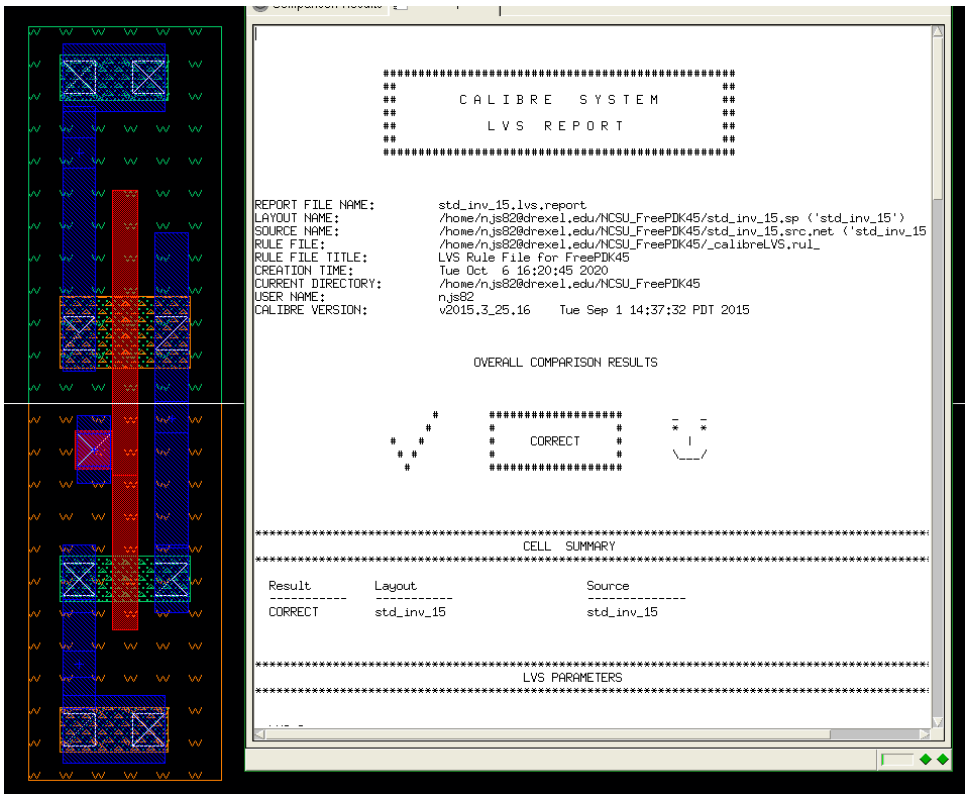


Figure 12: LVS Results

and use them extensively to fine tune my design and make sure everything was working as it should. It also helped me get a deeper understanding of the underlying technologies. The only thing I wish I could change is making it easier to find the correct value for a symmetric inverter. Right now, it is a lot of try, check, and revise to get the perfect value.