ECEC 471 Lab 4

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1 Introduction

1.1 Overview

1.2 Invert Chain

An inverter chain is, like the name implies, a chain of inverters used to reduce propagation delay by setting the number of stages to be able to efficiently run the circuit, given a certain input and ouput capacitance. If there are too many stages, the inverter chain could end up doing more harm than help. Using Equation**??** and using the value of 0.5 for p_{inv} we can solve for ρ. Then using Equation**??** we can solve for the best number of stages for the inverter chain. The number that was achieved by this method for ρ was about 3.181. The best number of stages was about 3.381 which was rounded to three.

$$p_{inv} + \rho(1 - \ln \rho) = 0 \tag{1}$$

$$N = \log_{\rho} \frac{C_{out}}{C_{in}} \tag{2}$$

1.3 Ring Oscillator

A ring oscillator is a chain of inverters with the input and output tied together. A ring oscillator is used in digital logic to deliver a clock signal to the circuit. The period of a signal is the time it takes for one cycle to pass. It usually is ideal to get the time it takes for a bunch of cycles to pass and divide by the number of cycles you took.

2 Simulation and Analysis

2.1 Schematic Design

Figure **??** shows the transistor-level schematic of the inverter chain. It was a straight-forward schematic with just the number of inverters, three. Fig-

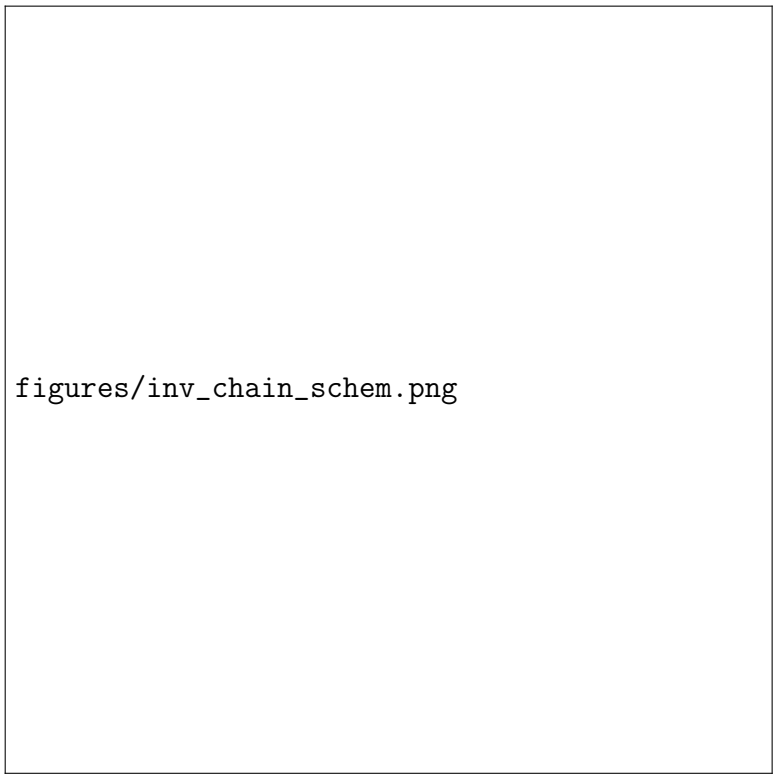

Figure 1: Transistor-level Inverter Chain Schematic

ure **??** shows the simulation schematic with the source and load. A pulse is used so we can measure the rise and fall times as well as the propagation delay. The pulse has an amplitude of 1.2V, a period of 2ns, a rise time of 5ps, a fall time of 5ps and a pulse width of 1ns. A 5fF capacitor was tied to the output to get it closer to a realistic model where the output of the nor gate would have some capacitance. The transient analysis and DC response of the circuit are shown in Figure **??** and Figure **??** respectively. Using the transient analysis graphs a rise time of 98.88, a fall time of 17.99ps, and propagation delay of 13.70ps were all easily found. The switching voltage

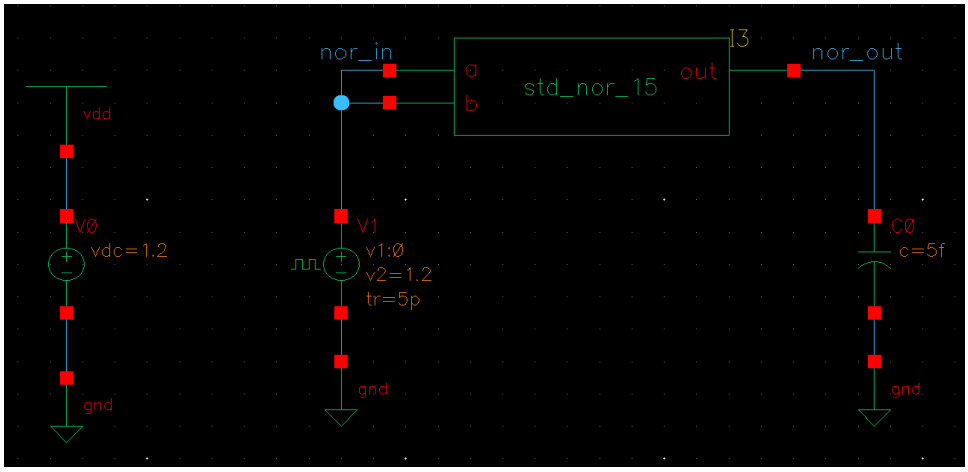

Figure 2: NOR Simulation Schematic

was found to be 412.29mV using the DC response graph which is not the desired 0.6V we want for a symmetric nor gate. To find the desired width of

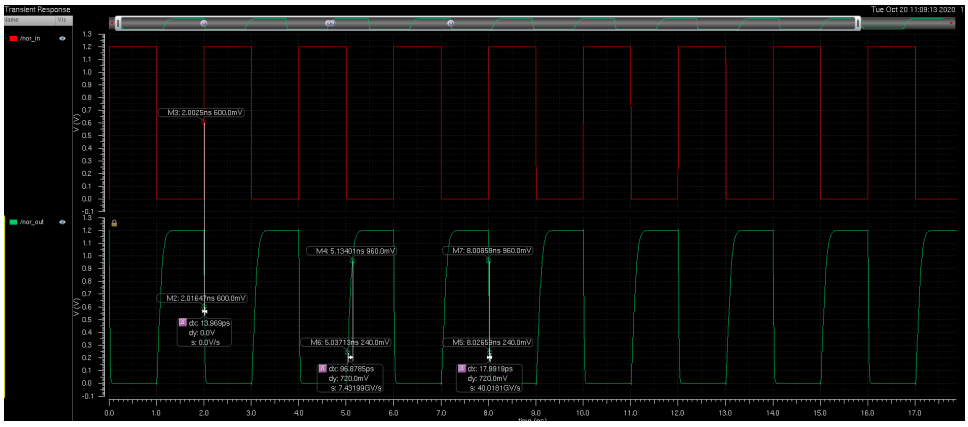

Figure 3: NOR Transient Analysis

the pmos transistor, we used parametric analysis to get Figure **??** and found that a width of 547.5nm gave us a switching voltage of about 0.6V. After the schematic was updated to use the new width, DC response was simulated and graphed again to give us Figure **??** which shows a switching voltage of about 0.6V, which is desired.

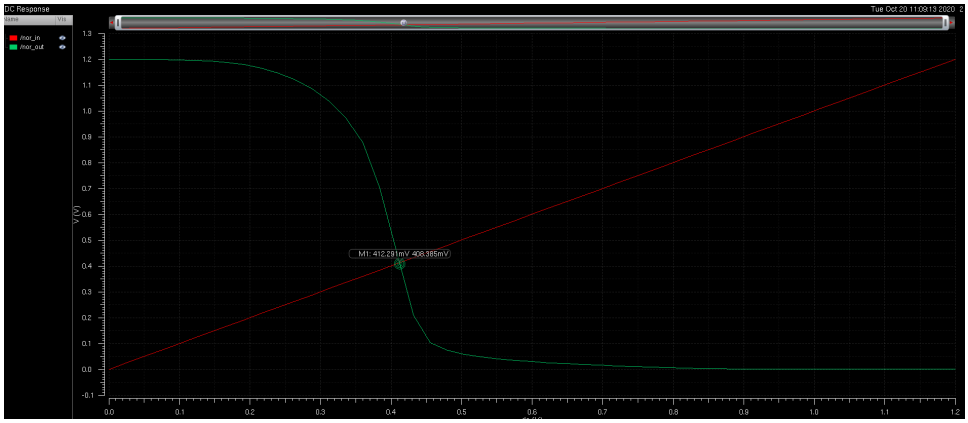

Figure 4: DC Response of an Asymmetric NOR Gate

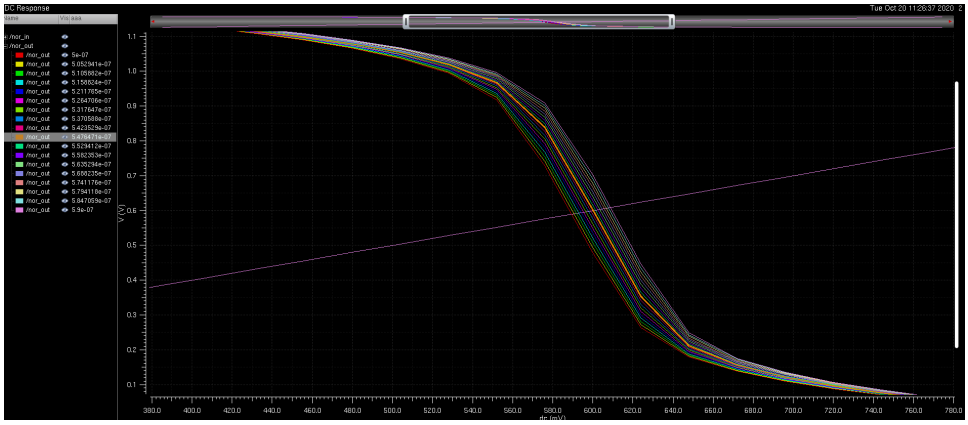

Figure 5: NOR Parametric Analysis

2.2 Layout Design

After the respective gate's schematic was finished, layout was done. The pmos and nmos were built first, taking special care to make sure the width of the transistors match the schematic. The pmos and nmos circuits were built first with the Vdd and ground rails being added to the design after as shown in Figure **??**. The same was done for the nor layout and is shown Figure **??**. Lastly, design rule checking(DRC) is used to make sure that no design rules are being violated and everything is fixed very painstakingly. The results for the nand and nor gate can be seen in Figure **??** and Figure **??**, respectively After that layout versus schematic(LVS) was used to make sure

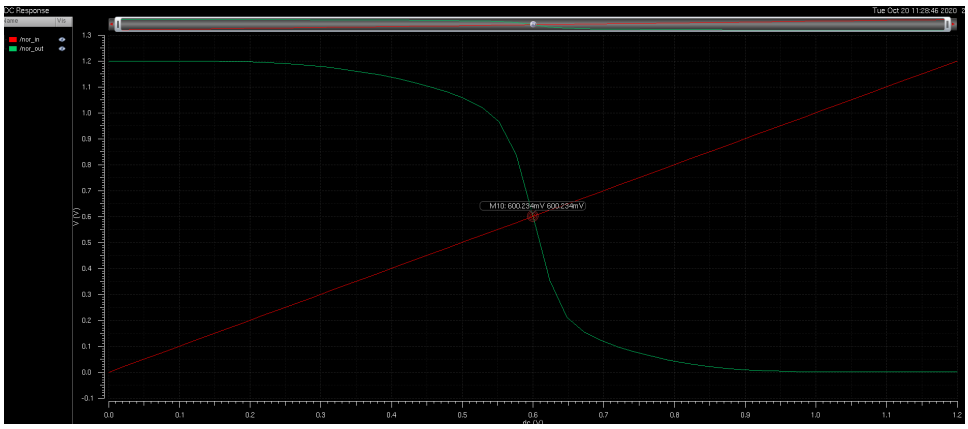

Figure 6: DC Response of a Symmetric NOR Gate

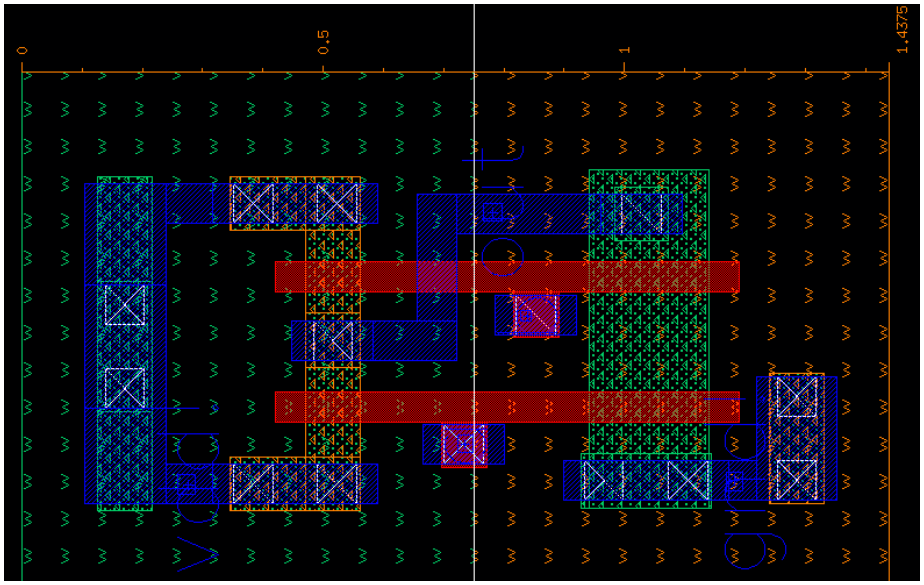

Figure 7: NAND Layout

our layout matches the design we modeled with the schematic and can be seen in Figure **??** and Figure **??**, respectively.

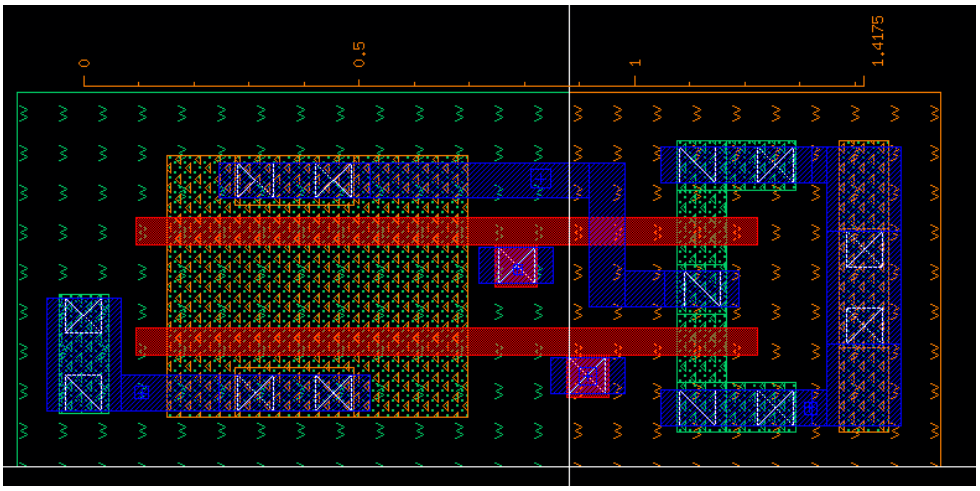

Figure 8: NOR Layout

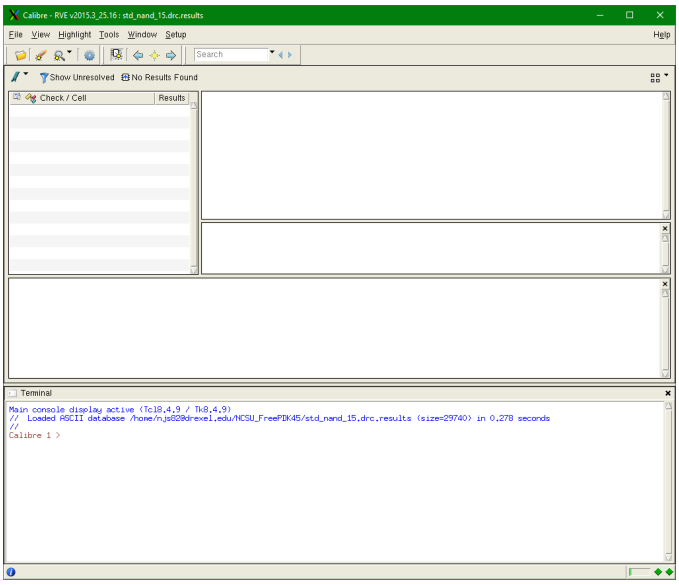

Figure 9: NAND DRC Results

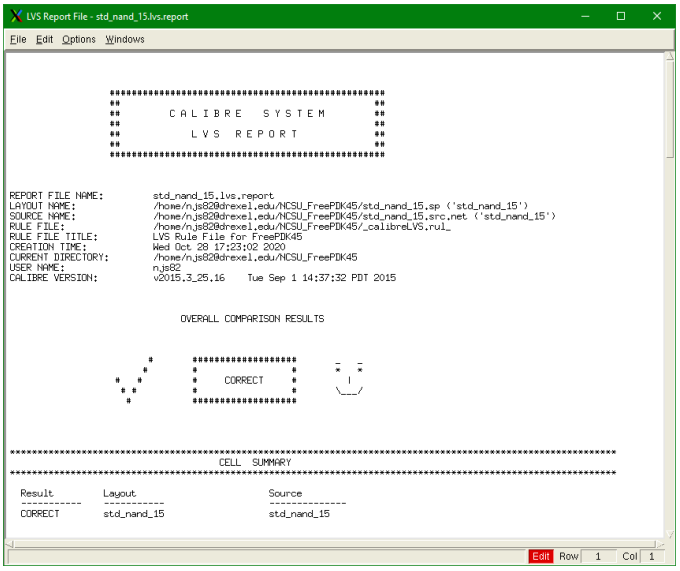

Figure 10: NAND LVS Results

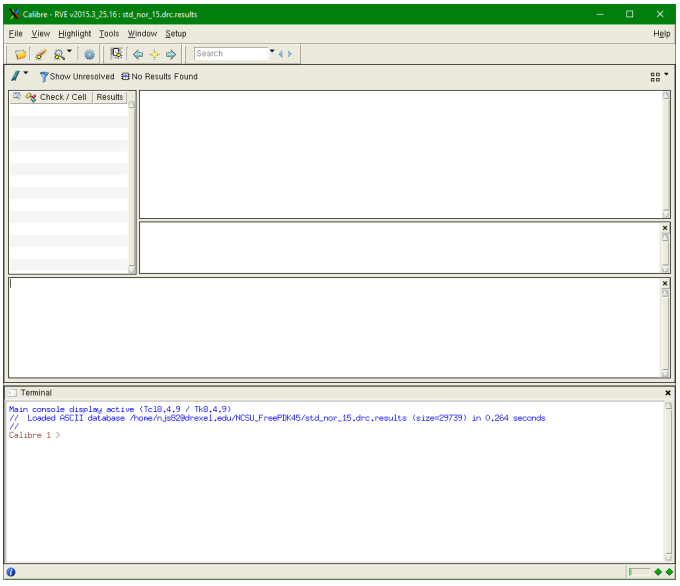

Figure 11: NOR DRC Results

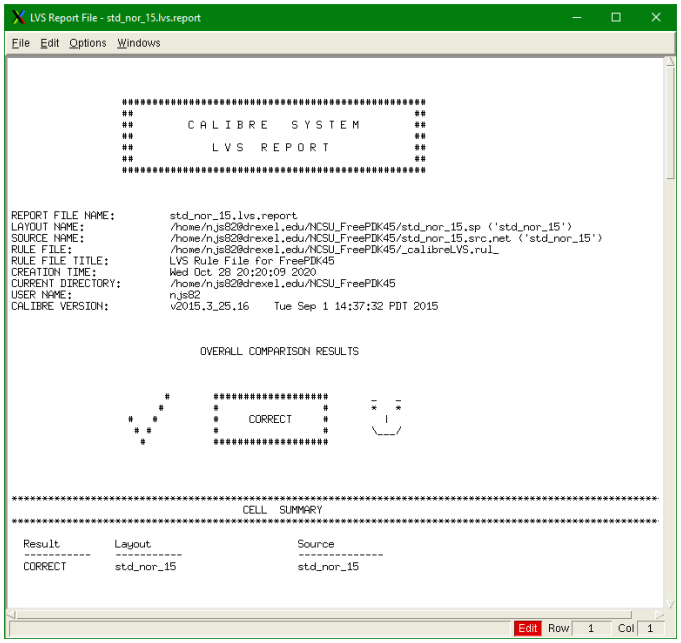

Figure 12: NOR LVS Results

3 Conclusion

The lab was a very good way to cement the fundamentals we picked up in lab two by creating two essential gates in any digital designers toolkit. It helped me further get used to the tools and use them extensively to fine tune my design and make sure everything was working as it should. It also helped me get a deeper understanding of the underlying technologies. The only thing I wish I could change is making it easier to find the correct value for a symmetric gate, which was made a bit easier to tell if the value was correct by the methods we learned in class. Still, though, it is a lot of try, check, and revise to get the perfect value.