Literature Review of Nanowire Interconnects

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***Abstract*—As devices continue to decrease in size, new technologies are being explored as alternatives to the traditional interconnects. Among these are nanowire, optical, and graphene interconnects are the three biggest contenders as a replacement. In this survey paper, nanowire interconnects and their relation to the other options will be explored as well as other uses that can be exploited from them.**

I. Introduction

While scaling down CMOS designs, researchers are looking for the best material to use for the interconnects of the device. Every material brings different, interesting properties to the table and many researchers are looking for alternatives to the traditional copper interconnect [1], while others are seeing what they can do with copper or really most nanowire materials. Nanowire interconnects provide significant improvements in power and performance when using them for 3-D CMOS design as opposed to the traditional approach [2]. They also allow for new technologies to be released, like ASICs that can self-repair [3], or even building logic right into the interconnects [4]. The first section will discuss the biggest alternative to copper, ruthenium, and how it compares to copper when used as a nanowire interconnect. The section will also discuss methods in which placing metal interconnects will not be as wasteful, thus using less of the more expensive metals. The next section will discuss advancements in 3-D CMOS fabrication due to nanowire interconnects and a whole method that was designed with nanowire interconnects. The second to last section will talk about configurable interconnects and replacing vias with transistors made out of nanowires. Lastly, research into self-repairing circuits made from nanowire interconnects, memristors and permanent components which allow the speed of an ASIC while being able to fix faulty sections of the circuit will be looked at.

II. Ruthenium Nanowire Interconnects

The big contenders in alternative metals when it comes to replacing copper are platinum-group metals or more specifically, ruthenium [1]. The biggest advantage of ruthenium over copper is the current carrying capability of the metal [1]. As shown in Fig. 1, ruthenium has a current carrying capability between 530 and 720MA/cm^2. This beats coppers carrying capacity of 100MA/cm^2 greatly and shows the biggest gain when it comes to ruthenium [1]. Ruthenium also did not break down when the temperature changed which proved it could be used in very hot environments without any issue when it comes to the circuit functioning correctly. The biggest tradeoff of a metal like ruthenium is its cost. It is due to the cost of ruthenium and other metals similar to it that methods of saving material while placing them are being researched heavily. The most promising method is gas-phased electrodeposition and the general method involves using an inert gas to transfer nanoparticles from a spark to where the metal is intending to go. The general steps of placing a nanowire using gas-phased electrodeposition is shown in Fig. 3 while the old method is shown in Fig. 4. The old method had a yield of about 53% [1] while the new method has a yield of about 95% [5] when it came to the amount of metal used. The new method of placing nanowires also allows for the self alignment of pads, which allows for the pads to not have to be perfectly lined up to create a connection between the two. This method also allows for two arbitrary points of a design to be connected without any modification to the layout which could lead to further design improvements.

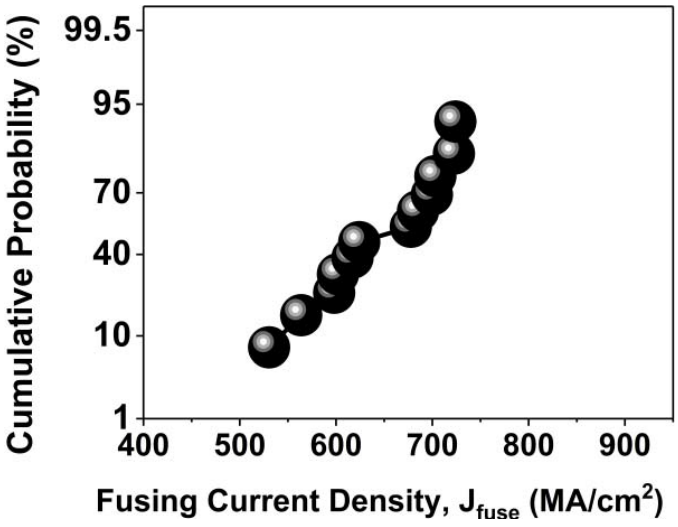

Fig. 1. Fusing current density of Ru nanowires [1].

III. Nanowire 3-D CMOS Fabrication

The use of nanowires causes 3-D CMOS design to improve dramatically, but causes a lot of what is expected to change in the process. The 3-D CMOS approach researched is called stacked horizontal nanowire-based 3-D CMOS approach, or SN3D. This 3-D CMOS approach allows for higher density packing, fine-grained routing, reduced interconnect lengths, and better control of transistors in which the gate is surrounding them [2]. Fig. 2 shows the basic structure of different parts of the CMOS fabric. The idea of using a nanowire as a transistor, which is done in this method, is discussed in greater detail in the next section. A bunch of different designs were created and the new 3-D CMOS method was found to have a way smaller area, less power consumption, and a shorter

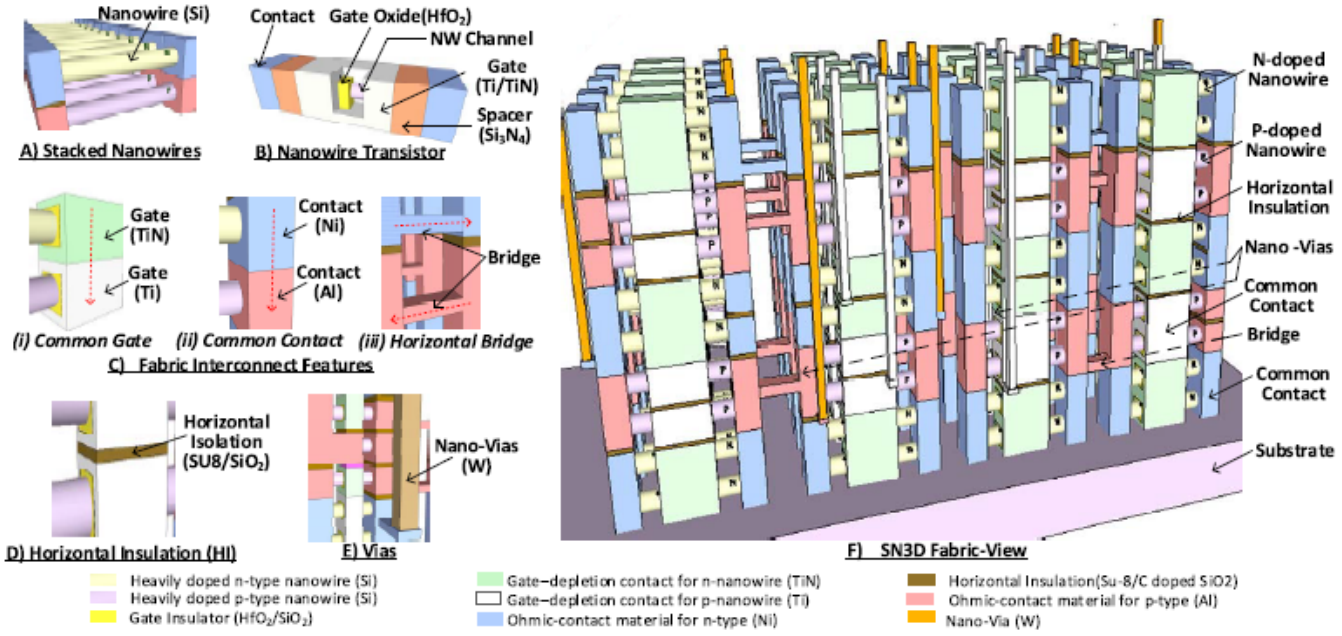

Fig. 2. SN3D fabric core components. (A) stacked nanowires. (B) Junction-less transistor surrounded by gate. (C) Different Interconnects (D) Horizontal isolation. (E) Vias. (F) Fabric of all components [2].

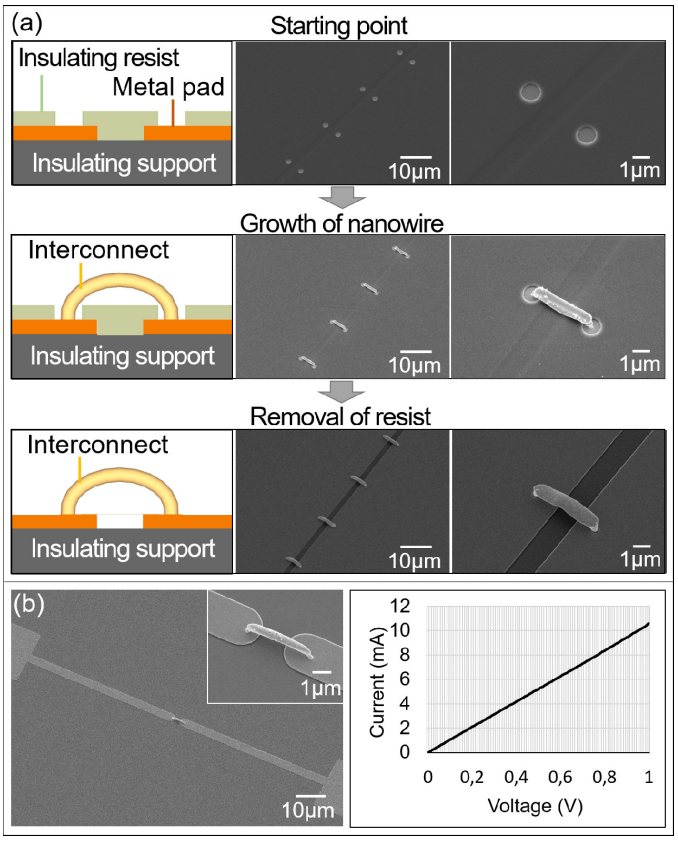

Fig. 3. (a) shows the phases in electrodeposition of nanowire materials (b) shows the current-voltage characteristic of a single bridge [5].

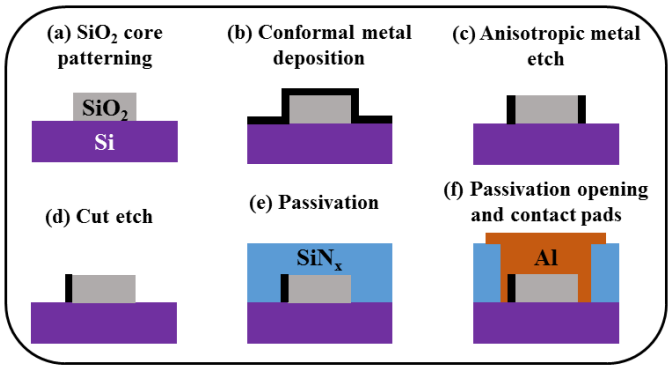

Fig. 4. Flow to fabricate nanowires [1].

delay when it came to a two input NAND, a full adder, and a four bit adder. It also maintained this lead even when the sizing of the transistors changed, only being beat in area at the 45nm node. The fabrication of these designs is radically different because a lot of the nanowire needs to be placed on air, which is an issue due to nothing holding the nanowire up.

IV. Reconfigurable Interconnects

Vias in a 3-D CMOS design are used to connect different layers of the design together and even allow for 3-D CMOS designs to be realized in a more condensed form. Fig. 5 shows a nanowire transistor inserted where a via would be. The general method of creating these reconfigurable interconnects is to grow silicon and put a metal on the tips. Gold would be best, but is generally avoided by semiconductor manufacturers

which leads to research into alternatives, most notably copper [4]. The use of these silicon nanowire interconnects can possibly allow designers to disable areas of their device by using it like a transistor. Nanowire transistors are even used in the 3-D CMOS fabrication research discussed in the previous section.

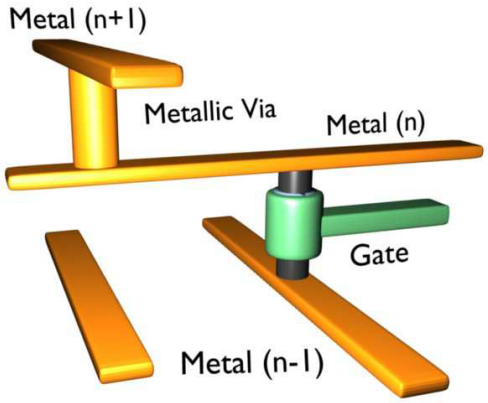

Fig. 5. Nanowire transistor in interconnect [4].

V. Self-Repairing Interconnects

The idea behind self-repairing interconnects builds off a field programmable nanowire interconnect(FPNI) which is basically an field programmable gate array(FPGA) built using nanowires. Fig. 6 shows the basic layout of an FPNI device. Self-repair usually occurs in several steps. The first step being the device identifies faulty areas, next isolates them by putting switching elements in, and finally replaces them with a working unit. The device has a permanent layer and an FPNI layer connected using memristors. As the device identifies areas that need to be replaced, the FPNI layer reconfigures itself to use different paths between the permanent parts of the design which allows for the faulty areas to be avoided [3]. The device gets the speed and performance of an ASIC while maintaining the ability to use different pathways in case of a fault in the current one.

VI. Conclusion

There is much discussion and research when it comes to nanowire interconnects as the best material needs to be chosen going forward as an industry standard. This issue will only get more prominent as the devices grow smaller and smaller due to the limits of materials already being used as interconnects. The discovery of different properties different materials have as well as different technologies the materials enable will likely lead to certain industries leaning towards using certain materials. The impact of the interconnect is a huge one and it is important that the trade-offs of every material is closely examined as to make the right choice. The improvements discussed by a 3-D CMOS fabrication process using nanowire

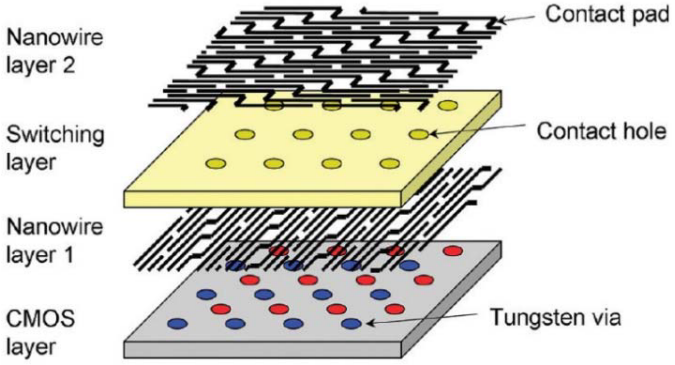

Fig. 6. FPNI technology [3].

interconnects is also promising and could allow for faster and more compact designs. Given the adoption of new materials and methods to not use so much of the expensive materials, integrated circuits could get a lot faster and smaller, given that nanowire interconnects are adopted.

References

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