# ECEC 471 Lab 3

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## 1 Introduction

### 1.1 Overview

This lab is meant to use the knowledge gained in lab 2 to build a symmetric version of the nand and nor gates. CMOS circuits are designed by tying the outputs of a pull down and pull up network together. For the nand gate, the pull up network is two pmos transistors in parallel tied to voltage high, or Vdd, and the pull down network is two nmos transistors in series tied to voltage low, or ground. The nor gate has the pull-up and pull-down networks swapped. A nand outputs a zero when both inputs are high and a one otherwise, while a nor outputs a zero when either input is high and a zero otherwise. Rise time and fall time are the time it takes for the ouput to rise from 10% to 90% of the total voltage or fall from 90% to 10% of the total voltage. Propagation delay is the time it takes for the output to appear after the input, usually measured by taking the difference of the 50% marks of the input and output.

### 1.2 Symmetric Gates

A symmetric gate is a gate whose worst case rise and fall times are the same. In other words, the input and output voltage cross the half point of Vdd at the same time. We get a symmetric gate by keeping the non-worst case path constant and changing the other. The path usually kept constant in simple gate is the path with the parallel transistors, while the series transistors are changed. This is the pull-down network for the nand and the pull-up network for the nor in this lab.

# 2 Simulation and Analysis

## 2.1 NAND Schematic Design

Figure 1 shows the transistor-level schematic of the nand gate after the ideal width for the nmos transistors was found. The initial width of every transistor in the circuit was 90nm before the change and the length of every transistor in the circuit is 50nm. After the change, the width of the nmos transistors became 200nm. Figure 2 shows the simulation schematic with the

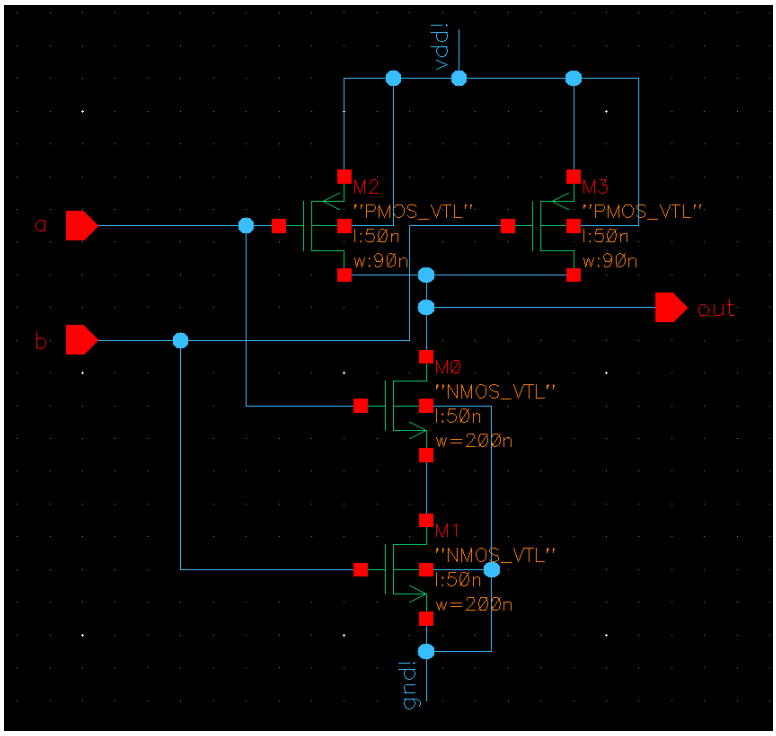


Figure 1: Transistor-level Symmetric NAND Schematic

source and load. A pulse is used so we can measure the rise and fall times as well as the propagation delay. The pulse has an amplitude of 1.2V, a period of 2ns, a rise time of 5ps, a fall time of 5ps and a pulse width of 1ns. A 5fF capacitor was tied to the output to get it closer to a realistic model where the output of the nand gate would have some capacitance. The transient analysis and DC response of the circuit are shown in Figure 3 and Figure 4 respectively. Using the transient analysis graphs a rise time of 28.67ps, a

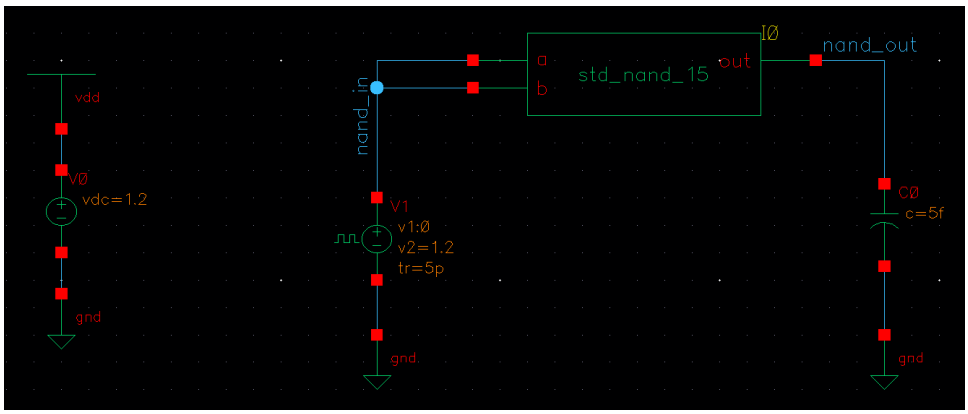


Figure 2: NAND Simulation Schematic

fall time of 27.70ps, and propagation delay of 9.49ps were all easily found. The switching voltage was found to be 696.338mV using the DC response graph which is not the desired 0.6V we want for a symmetric nand gate. To


Figure 3: NAND Transient Analysis

find the desired width of the pmos transistor, we used parametric analysis to get Figure 5 and found that a width of 200nm gave us a switching voltage of about 0.6V. After the schematic was updated to use the new width, DC response was simulated and graphed again to give us Figure 6 which shows a switching voltage of about 0.6V, which is desired.

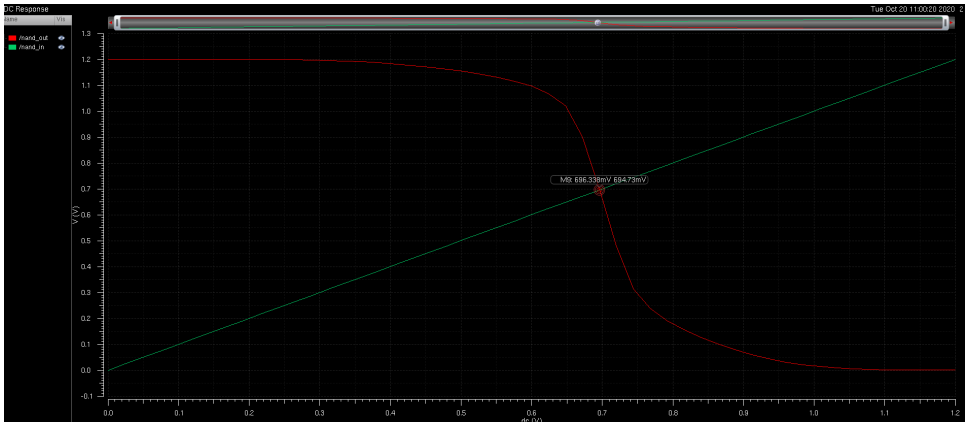


Figure 4: DC Response of an Asymmetric NAND Gate

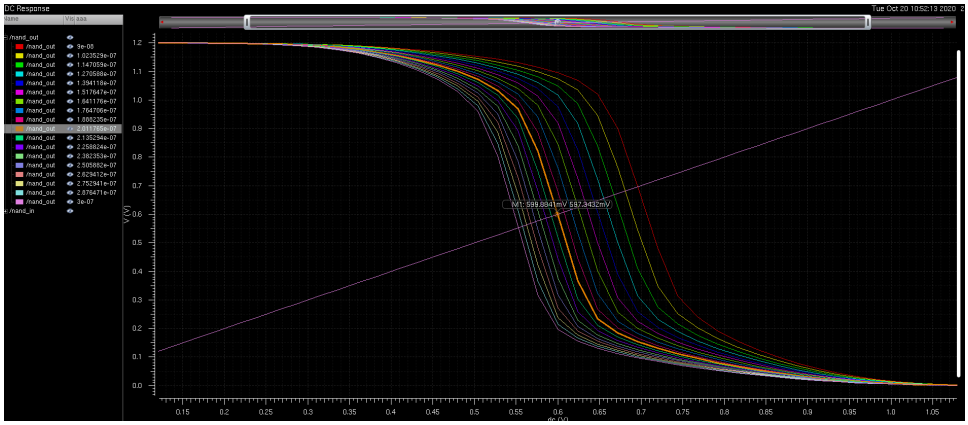


Figure 5: NAND Parametric Analysis

## 2.2 NOR Schematic Design

Figure 7 shows the transistor-level schematic of the nor gate after the ideal width for the nmos transistors was found. The initial width of every transistor in the circuit was 90nm before the change and the length of every transistor in the circuit is 50nm. After the change, the width of the nmos transistors became 547.5nm. Figure 8 shows the simulation schematic with the source and load. A pulse is used so we can measure the rise and fall times as well as the propagation delay. The pulse has an amplitude of 1.2V, a period of 2ns, a rise time of 5ps, a fall time of 5ps and a pulse width of 1ns.

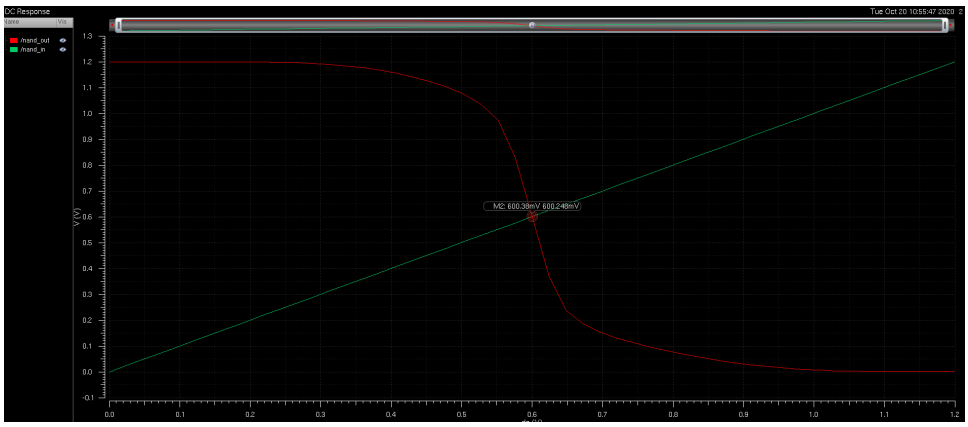


Figure 6: DC Response of a Symmetric NAND Gate

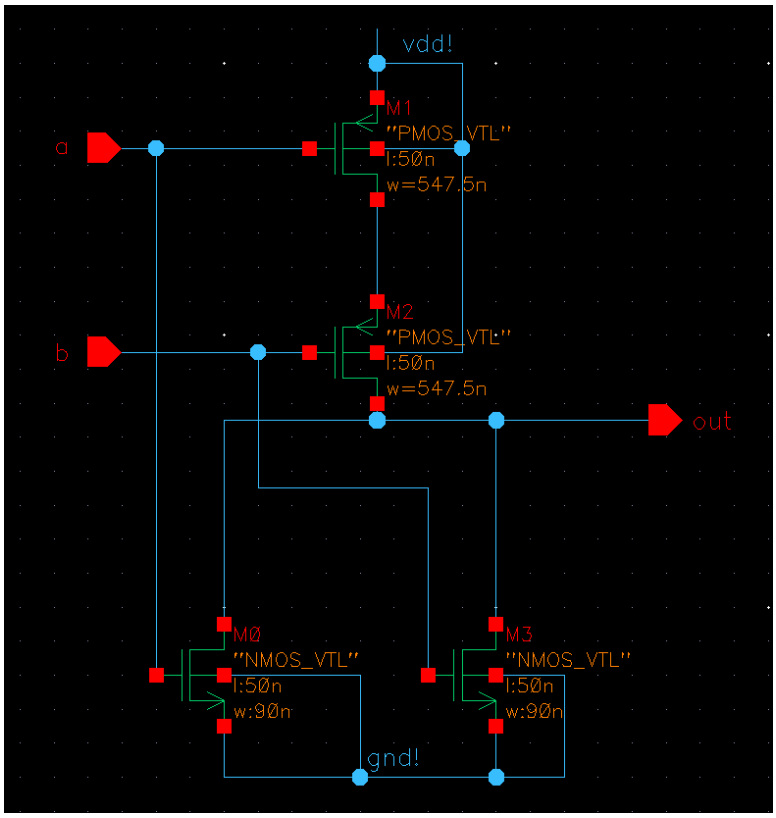


Figure 7: Transistor-level Symmetric NOR Schematic

A 5fF capacitor was tied to the output to get it closer to a realistic model where the output of the nor gate would have some capacitance. The transient

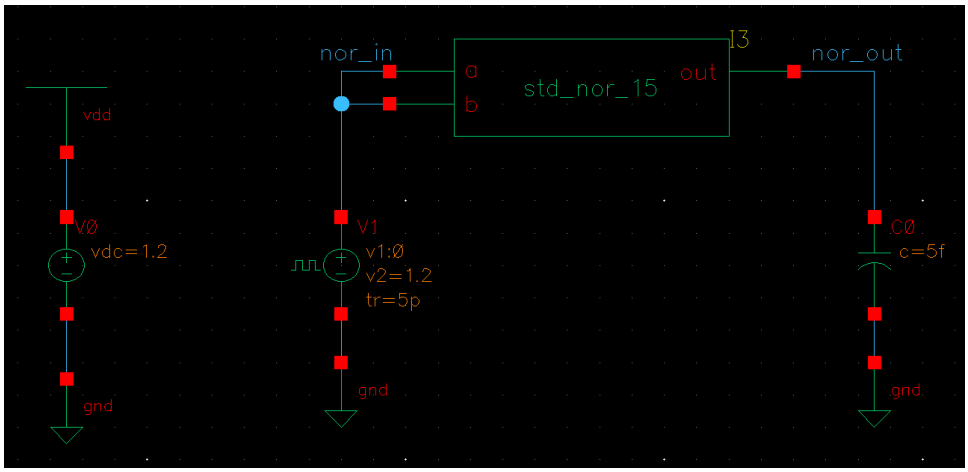


Figure 8: NOR Simulation Schematic

analysis and DC response of the circuit are shown in Figure 9 and Figure 10 respectively. Using the transient analysis graphs a rise time of 98.88, a fall time of 17.99ps, and propagation delay of 13.70ps were all easily found. The switching voltage was found to be 412.29mV using the DC response graph which is not the desired 0.6V we want for a symmetric nor gate. To find

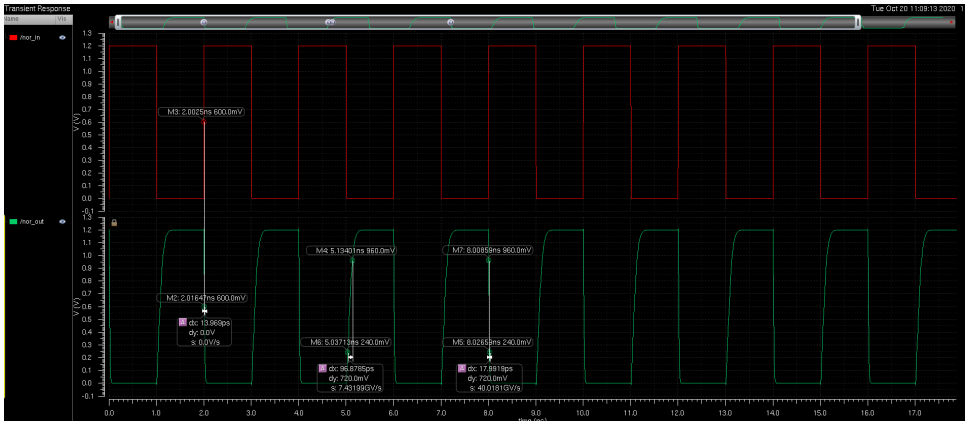


Figure 9: NOR Transient Analysis

the desired width of the pmos transistor, we used parametric analysis to get

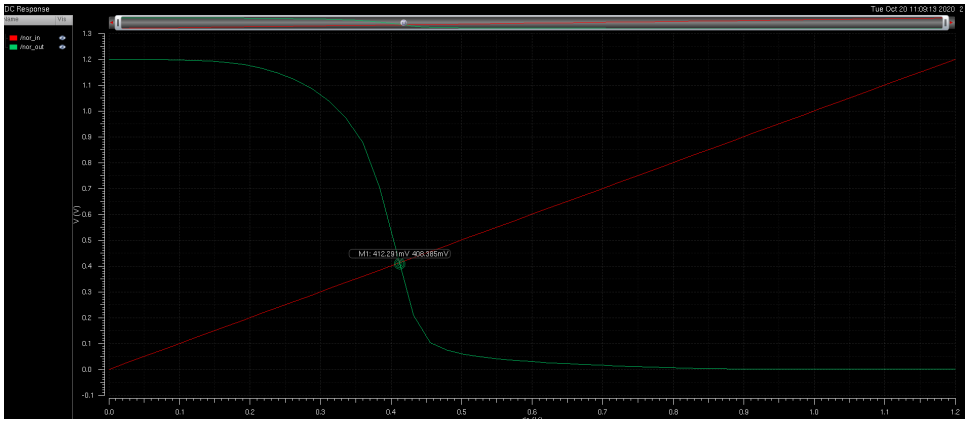


Figure 10: DC Response of an Asymmetric NOR Gate

Figure 11 and found that a width of 547.5nm gave us a switching voltage of about 0.6V. After the schematic was updated to use the new width, DC

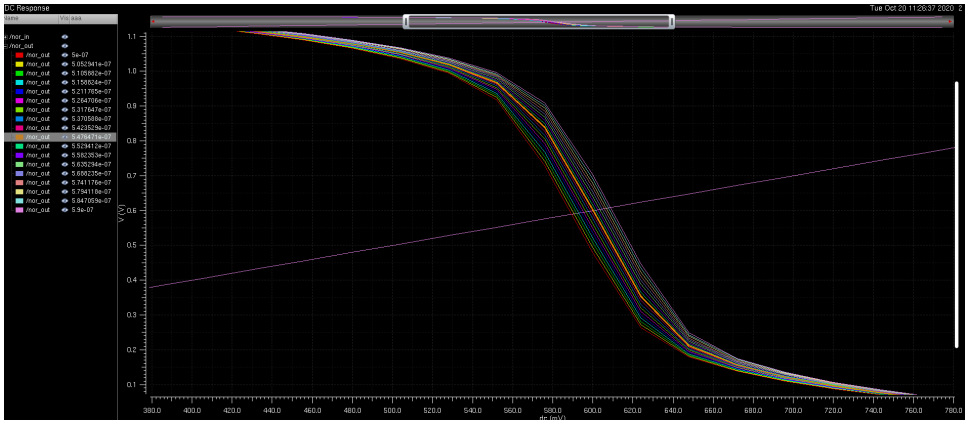


Figure 11: NOR Parametric Analysis

response was simulated and graphed again to give us Figure 12 which shows a switching voltage of about 0.6V, which is desired.

## 2.3 Layout Design

After the respective gate's schematic was finished, layout was done. The pmos and nmos were built first, taking special care to make sure the width

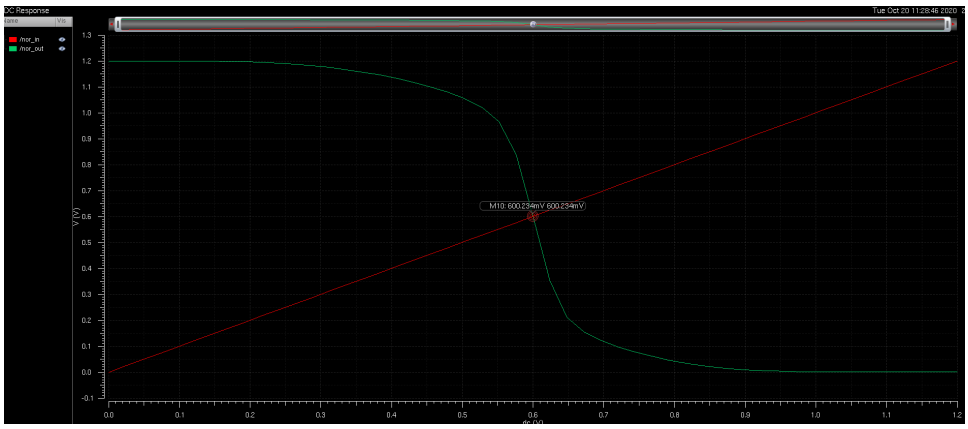


Figure 12: DC Response of a Symmetric NOR Gate

of the transistors match the schematic. The pmos and nmos circuits were built first with the Vdd and ground rails being added to the design after as shown in Figure 13. The same was done for the nor layout and is shown Figure 14. Lastly, design rule checking(DRC) is used to make sure that

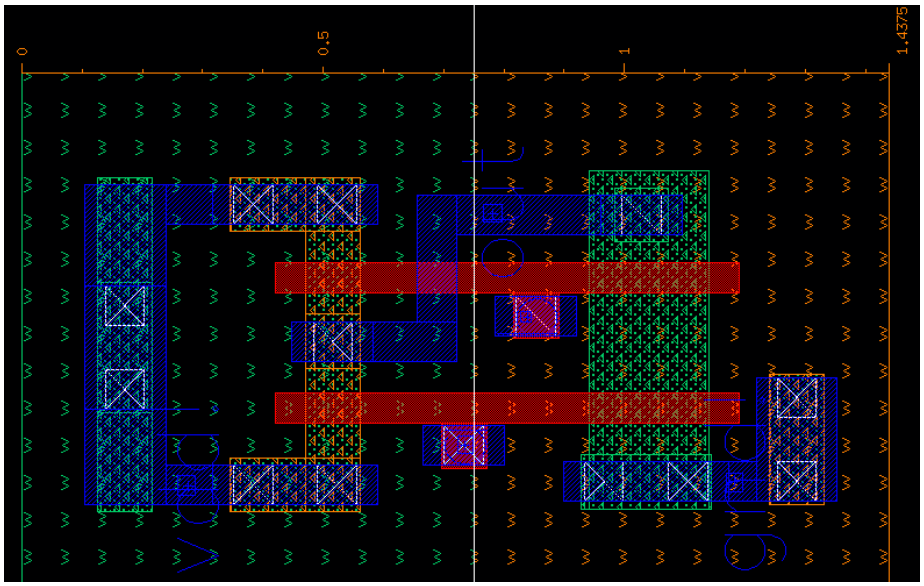


Figure 13: NAND Layout

no design rules are being violated and everything is fixed very painstakingly.

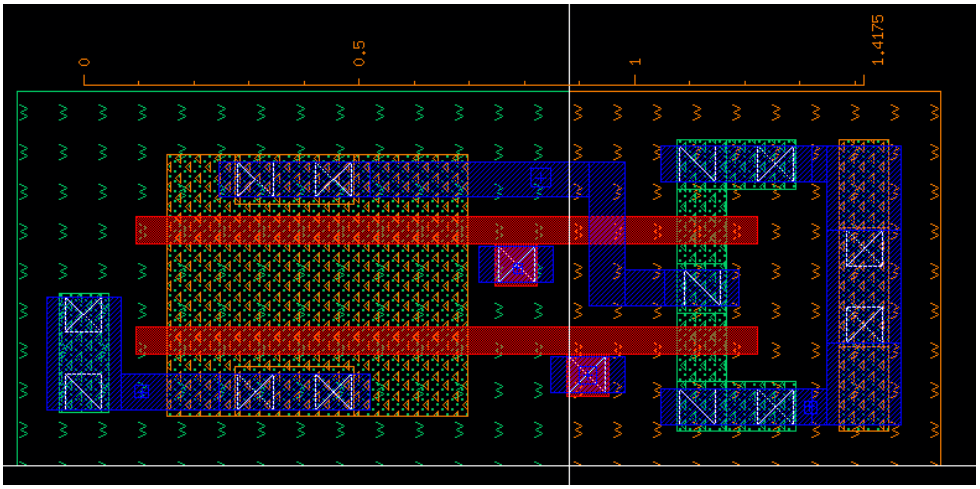


Figure 14: NOR Layout

The results for the nand and nor gate can be seen in Figure 15 and Figure 17, respectively After that layout versus schematic(LVS) was used to make sure our layout matches the design we modeled with the schematic and can be seen in Figure 16 and Figure 18, respectively.

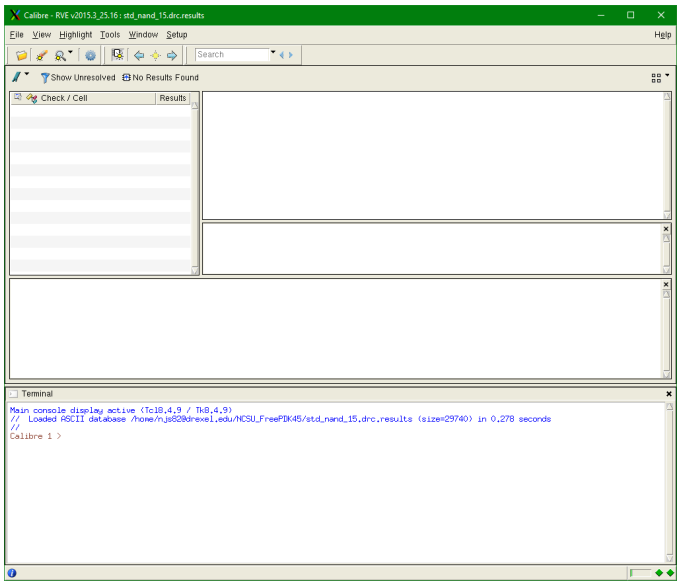


Figure 15: NAND DRC Results

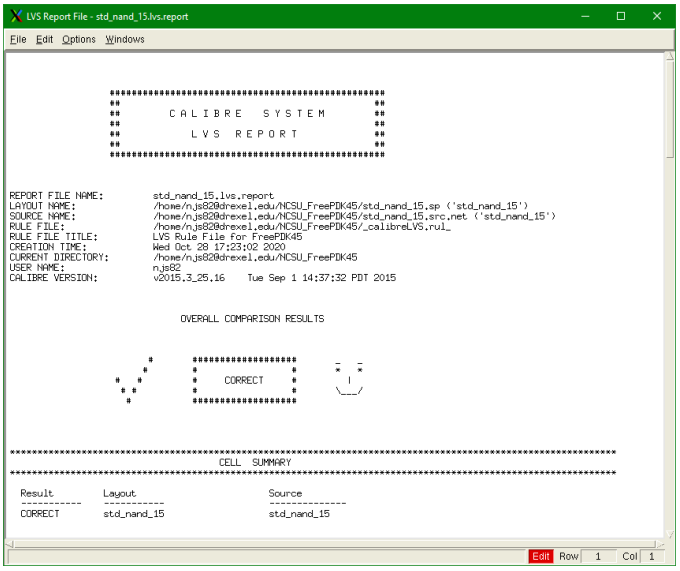


Figure 16: NAND LVS Results

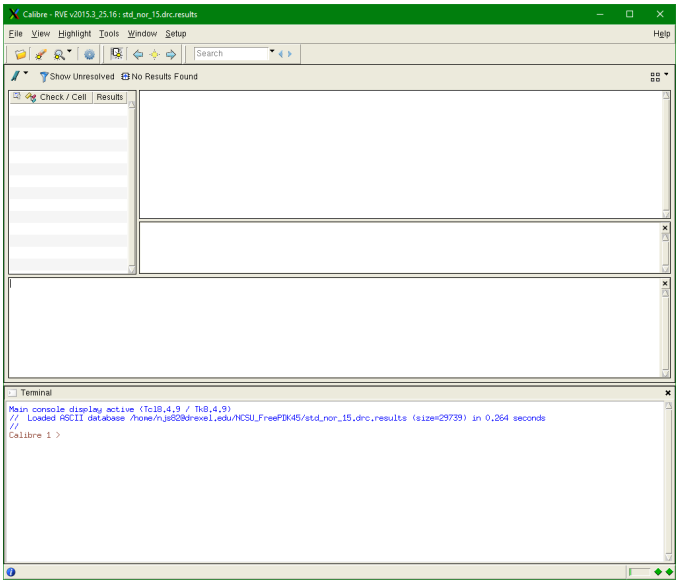


Figure 17: NOR DRC Results

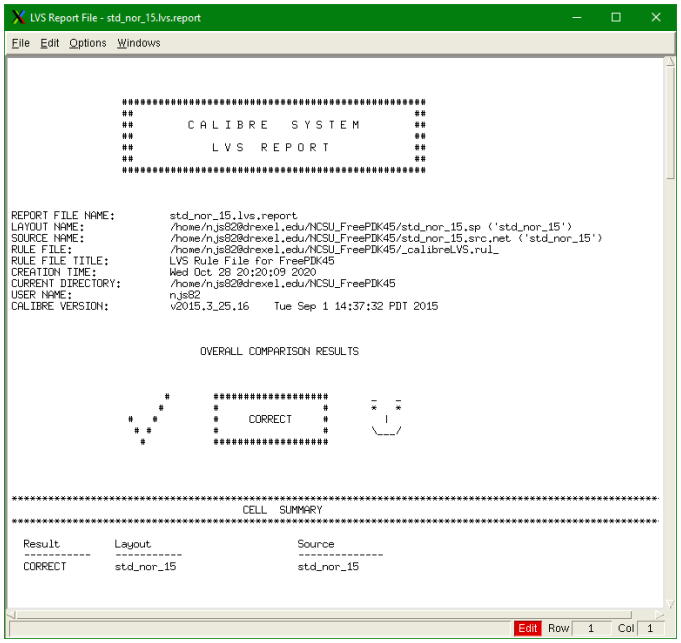


Figure 18: NOR LVS Results

# 3 Conclusion

The lab was a very good way to cement the fundamentals we picked up in lab two by creating two essential gates in any digital designers toolkit. It helped me further get used to the tools and use them extensively to fine tune my design and make sure everything was working as it should. It also helped me get a deeper understanding of the underlying technologies. The only thing I wish I could change is making it easier to find the correct value for a symmetric gate, which was made a bit easier to tell if the value was correct by the methods we learned in class. Still, though, it is a lot of try, check, and revise to get the perfect value.