ECEC 471 Lab 4

Nicholas Sica

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1 Introduction

1.1 Overview

1.2 Invert Chain

An inverter chain is, like the name implies, a chain of inverters used to reduce propagation delay by setting the number of stages to be able to efficiently run the circuit, given a certain input and ouput capacitance. If there are too many stages, the inverter chain could end up doing more harm than help. Using Equation 1 and using the value of 0.5 for p_{inv} we can solve for ρ. Then using Equation 2 we can solve for the best number of stages for the inverter chain. The number that was achieved by this method for ρ was about 3.181. The best number of stages was about 3.381 which was rounded to three.

$$p_{inv} + \rho(1 - \ln \rho) = 0 \tag{1}$$

$$N = \log_{\rho} \frac{C_{out}}{C_{in}} \tag{2}$$

Working backwards using Figure 3 The output and input capacitances for each stage can be found which leads us to multiply th previous stage transistor widths by 3.69 to get the transistor sizes for the current stage.

$$C_{in} = \frac{C_{out} \times g}{\hat{f}} \tag{3}$$

1.3 Ring Oscillator

A ring oscillator is a chain of inverters with the input and output tied together. A ring oscillator is used in digital logic to deliver a clock signal to the circuit. The period of a signal is the time it takes for one cycle to pass. It usually is ideal to get the time it takes for a bunch of cycles to pass and divide by the number of cycles you took.

2 Simulation and Analysis

2.1 Schematic Design

Figure 1 shows the transistor-level schematic of the inverter chain. It was a straight-forward schematic with just the number of inverters needed for minimum delay, three in this case. Figure 2 shows the simulation schematic with the source and load of 0.1fF and 5fF as specified in the lab. A pulse is used so we can measure the propagation delay of each inverter in the chain as well as the propagation delay of the whole chain. The pulse has an amplitude of 1.2V, a period of 20ns, a rise time of 10ps, a fall time of 10ps and a pulse width of 10ns.

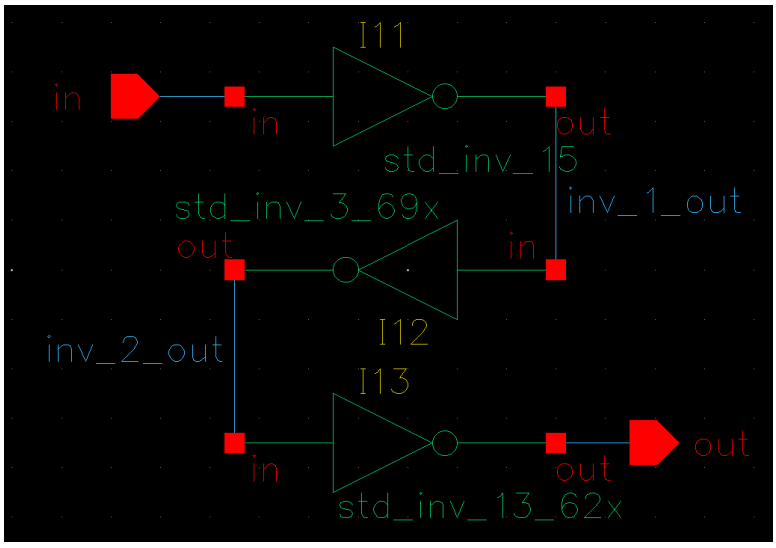

Figure 1: Transistor-level Inverter Chain Schematic

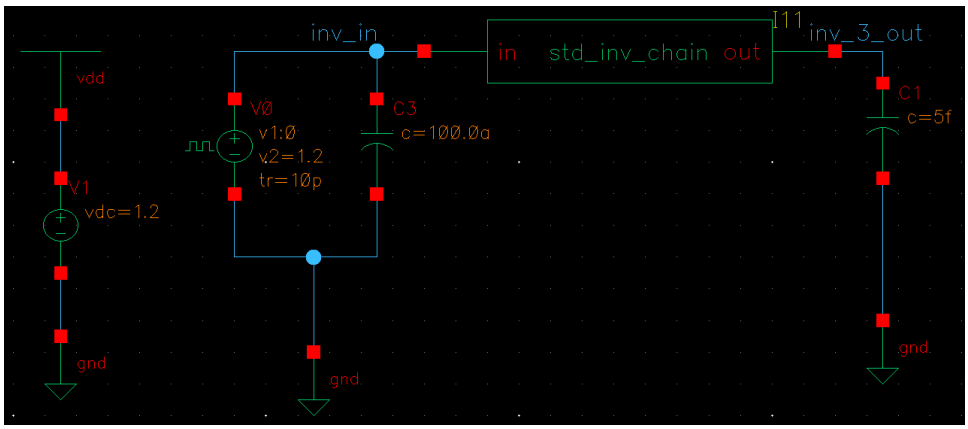

Figure 2: Inverter Chain Simulation Schematic

The transient analysis of the circuit is shown in Figure 3. Using the transient analysis graphs, the propagation delay of the entire chain was found to be 25.05ps, while each the first, second, and third inverters' propagation delays are 8.95ps, 10.47ps, and 5.63ps, respectively. In lab two, the propagation delay was found to be 25.68ps which is a bit larger than the propagation delay of our inverter chain.

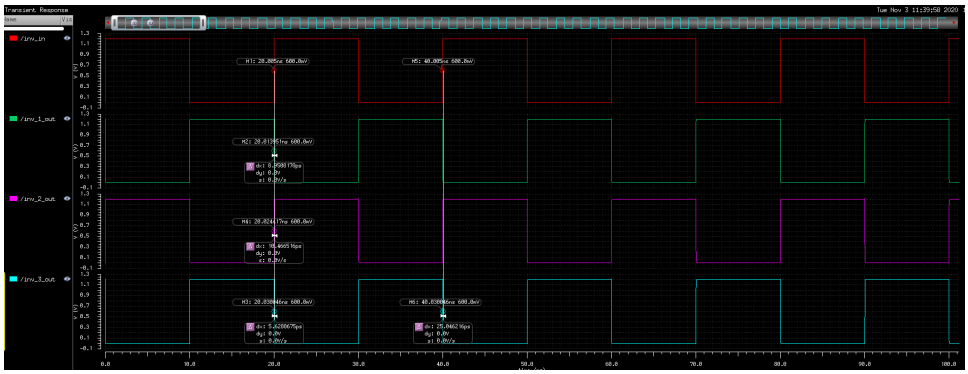

Figure 3: Inverter Chain Transient Analysis

After layout was done, parasitic extraction was done and simulation was re-run with the parasitics factored in. Figure 4 was used to find the propagation delay at all stages is about 2ps longer while the entire chain is about 6ps longer.

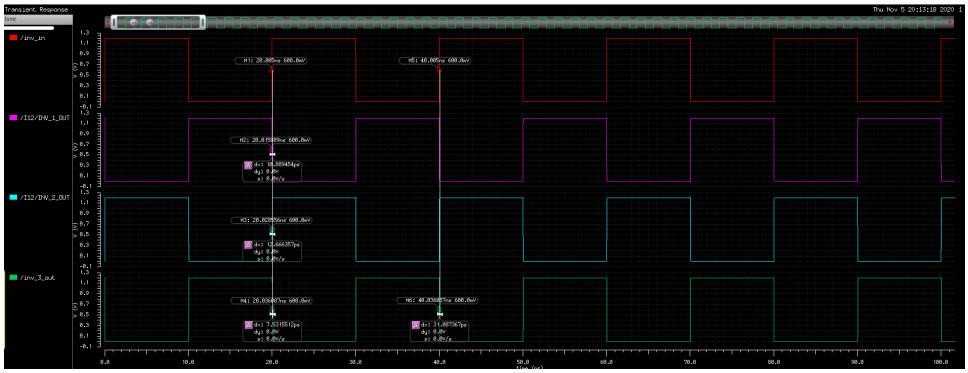

Figure 4: Inverter Chain Post-Layout Transient Analysis

The ring oscillator schematic is shown in Figure 5 and is simply twenty-one inverters with the output tied to the input of the entire chain. Afterwards, simulation was setup as shown in Figure 6 and is similar to the layout of all the other simulations.

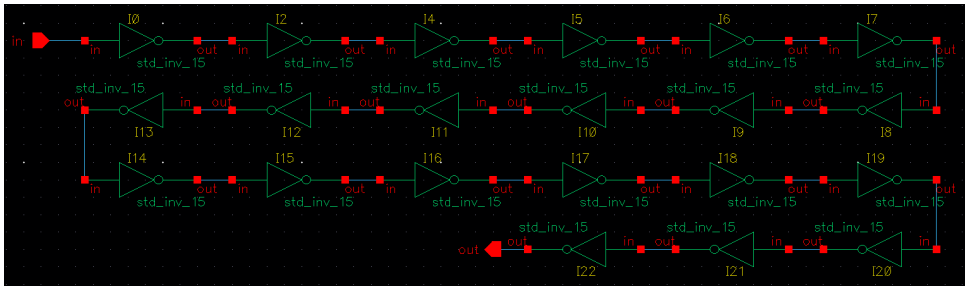

Figure 5: Transistor-level Ring Oscillator Schematic

Lastly, simulation was run and Figure 7 was obtained. With this we were able to count twenty-nine cycles and get a delay of 7.81ns over those twenty-nine cycles. Using that information, a frequency of 3.71GHz or a period of 0.27ns was obtained.

2.2 Inverter Chain Layout Design

After the inverter chain's schematic was finished, layout was done as shown in Figure 8. This time, the pitch of each sized inverter was matched to ensure smooth integration into the inverter chain. In order to achieve this, "fingers"

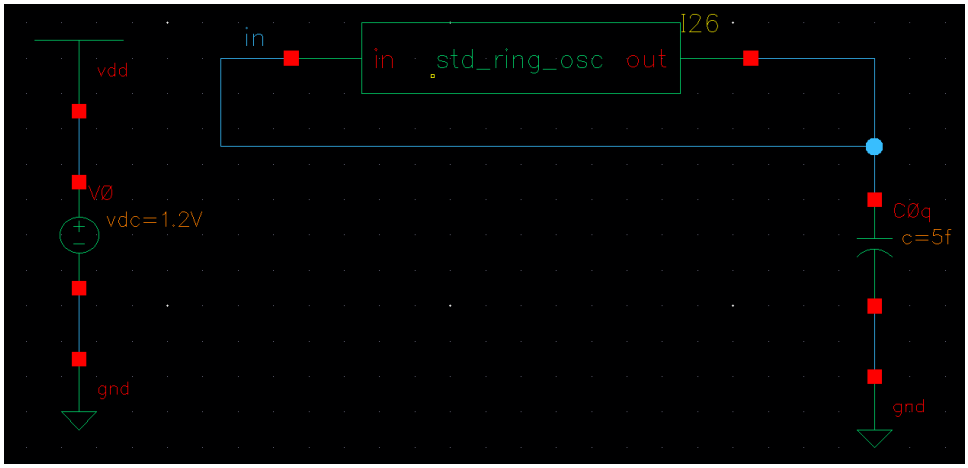

Figure 6: Ring Oscillator Simulation

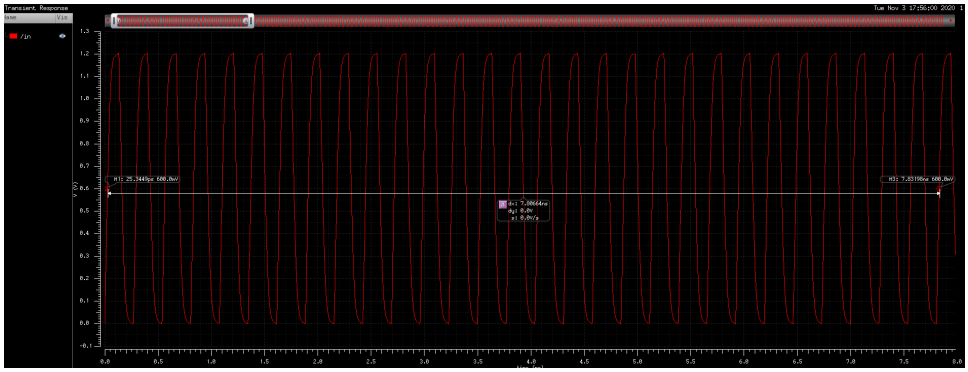

Figure 7: Ring Oscillator Transient Analysis

were used to allow for a smaller implant width, but still keep the desired width intact.

Lastly, design rule checking(DRC) is used to make sure that no design rules are being violated and everything is fixed very painstakingly. The results for the DRC can be seen in Figure 9 After that layout versus schematic(LVS) was used to make sure our layout matches the design we modeled with the schematic and can be seen in Figure 10. Once LVS was done, we used parasitic extraction to get the parasitics of the circuit and do post-layout simulation.

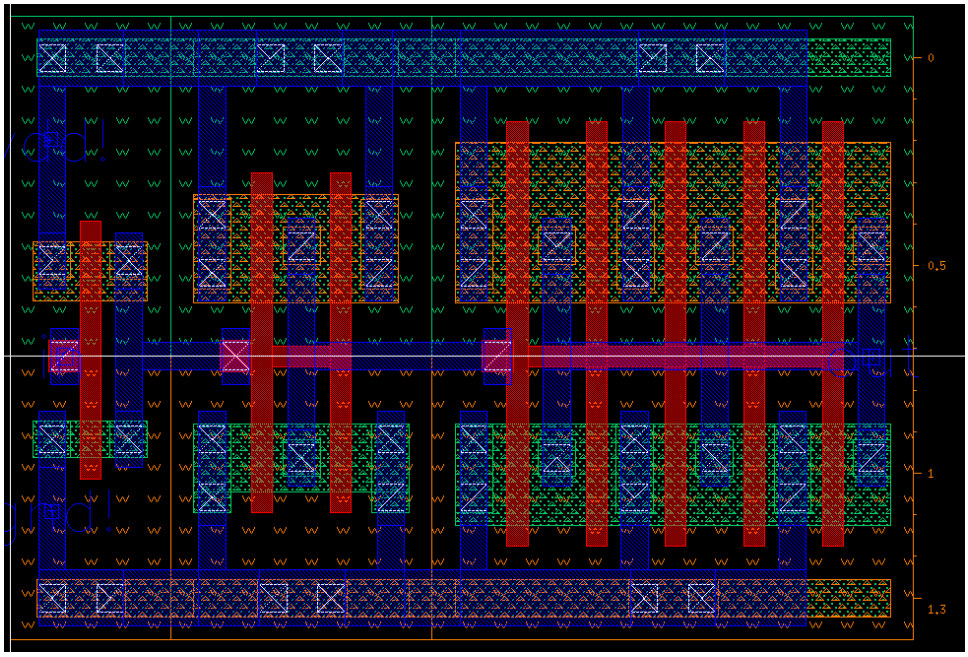

Figure 8: Inverter Chain Layout

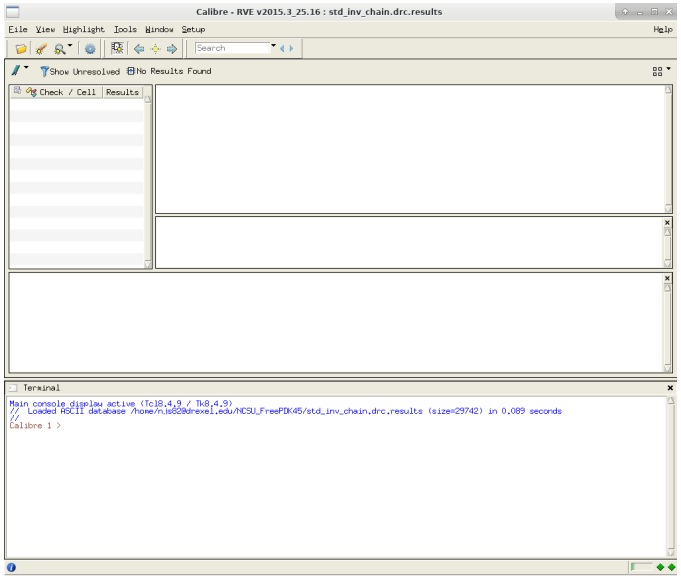

Figure 9: DRC Results

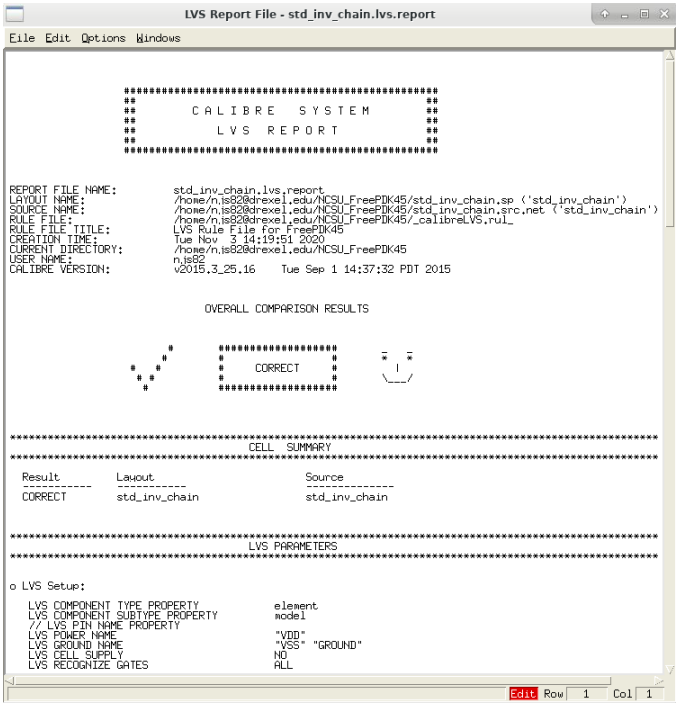

Figure 10: LVS Results

3 Conclusion

The lab helped the class figure out how to currectly size gates to achieve minimum delay and work through the issues of pitch matching to get all the pieces of a circuit to fit together nicely. The parasitic extraction tool was a pain to wrestle with, mostly due to a bug on Cadence's end. Everything came out as expected with the inverter chain speeding up the circuit a bit.