Spiking Neural Network on an FPGA

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Abstract

Individuals of every demographic may be affected by sleep apnea, an affliction causing irregular or halted breathing during periods of sleep. Those afflicted must obtain diagnoses by participating in polysomnography (PSG) lab tests to determine their treatment options. Lab tests use an array of sensors that measure quantities not limited to blood oxygen level, cardiac rhythm signals, brain electrical activity, and eye motion [1]. In-lab tests offer the greatest accuracy in exchange for greater cost and the need to relocate patients from their preferred resting environments. Contrarily, in-home tests require less sensors, correspondingly less cost, and no need for relocation. A disadvantage of a portable test is a reduced number of sensors measuring only blood oxygen content and most often airway pressure [1]. The reduced sensor count provides fewer measurements and results in less accuracy than the in-lab tests except for the most severe of cases. Additionally, the need to return the measuring devices has the potential to delay test results and treatment prescriptions such as a continuous positive airway pressure (CPAP) machine. Medical professionals and patients alike would benefit most from a solution providing the accuracy of in-lab tests at the cost and comfort of in-home tests.

The proposed solution that aims to reduce the gap between in-lab and in-home sleep study tests implements a spiking neural network (SNN) machine learning model on a field-programmable gate array (FPGA). Using this SNN model, impulse-train representations of input signals such as blood oxygen level and respiratory pressure are mapped to predictions of future apnea states and their severity. The implementation augments the in-home sleep studies to provide real-time monitoring and levels of accuracy not normally characteristic of portable tests. The SNN's ability to encode time-dependent feature characteristics and to conduct asynchronous activation propagation in addition to the FPGA's efficiency for high-frequency switching and rapid re-programmability will facilitate low-power, high-speed operation. As opposed to using a more general computational device, such as a graphics processing unit (GPU), the FPGA offers a smaller form factor, and at the same time is not as permanent as application-specific integrated circuits (ASICs) which allows for rapid development. SNNs are less complex and sparsely connected compared to related long short-term memory (LSTM) recurrent

neural networks (RNNs), which makes them feasible to implement on power- and memory-constrained devices like the FPGA.

The project makes extensive use of open-source solutions for most of the development and makes use of a granted Xilinx FPGA board for the physical implementation. Python is used to develop the SNN software golden model. Vivado is used to develop the hardware description of the FPGA and generate a programmable bitstream. SymbiYosys is used for formal verification of the hardware design. Provided proprietary data as well as openly available data from the PhysioNet Apnea-ECG Database is used for determining software accuracy and error [2], [3]. Following hardware synthesis, a power test is conducted to determine efficiency of the implemented FPGA solution.

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2.1 Concepts

An FPGA is the changeable version of a CPU or GPU. It allows you to create digital logic that can be easily changed and is usually what chip makers use to prototype a CPU or GPU before it is turned into an ASIC. A designer can take an FPGA and mold it to fit the criteria of a specific application and therefore give speed advantages over a CPU or GPU since it is not general purpose. The downside of the FPGA is that it is very difficult to program and changes to it require a lot more time than that of a GPU or CPU. A CPU is great for tasks that happen one after the next but suffers in tasks that require parallelization which is where the GPU thrives. Price is a bit tricky with all the devices and will be discussed when the three are compared in the next section.

2.2 Concept Evaluation

The type of device to use could make or break the implementation of the neural network. Traditionally CPUs and GPUs were the two main choices due to their ease of programming. GPUs were preferred over CPUs because of their highly parallelizable nature. An FPGA allows a designer to custom fit the low level logic to work a lot faster since it only has to do one task whereas a CPU or GPU has to support a great number of instructions to

be multipurpose. If a designer wants even faster speeds, they can turn to designing an ASIC, but that causes the design to be permanent and not easily changeable. It is also significantly more difficult to design an ASIC. Price is also a big limiting factor. Since CPUs are typically not great at all for neural networks they will not be discussed. High-end GPUs are typically in the range from $500-$700 while an FPGA has a price range from $60 to $10,000. The price usually lands around the $3,000 mark, although it is hard to say exactly where due to the FPGA being scaled to how many logic elements are needed. This may cause you to immediately pick the GPU, but GPU improvements generally cause the consumer to buy new ones sometimes on a yearly basis if the improvements are needed. FPGAs, on the other hand, can be reprogrammed on the fly and even incorporate these improvements especially if the top of the market chip is being used. It will be relevant and up to date a lot longer than a GPU would be.

2.3 Detailed Design

3 Context and Impact

3.1 Economic Analysis

The anticipated impact of the FPGA SNN implementation is to bridge the gap between the high-accuracy, high-cost, in-lab PSG tests and the low-accuracy, low-cost, in-home sleep studies. The solution must showcase greater accuracy than in-home tests at a cost lower than that of in-lab tests. There exist four types of sleep study test with type I tests requiring the largest number of sensors, constant supervision, and relocation, and type IV tests allowing for portability and requiring at least one sensor [1]. Recent estimates project that type III tests, a single level of complexity above type IV tests, can cost on average about $1,000.00[11], which is more than double the price of the $400.00[12] rate for type IV tests [4]. These prices are on par with the expected rates to pay out-of-pocket for tests of these levels. The solution must be able to use whatever signals are provided by type III or type

[1]This value was first adjusted for November 2017 british pound conversion (1 GBP = 1.3478 USD)

[1]Rounded up from $991.98 (original price was 736 GBP)

[2]Rounded up from $431.30 (original price 320 GBP)

IV tests and improve accuracy for all severities while incurring no significant costs.

The greatest cost incurred by the solution remains the FPGA integrated circuit that implements the SNN. The market price for different chips can range anywhere from $60 to a chip with a low density of logic elements to $10,000 for a chip with hundreds of thousands of logic elements. The most cost effective chip to buy would have to be chosen after the design is made to pick a chip that just barely fits the design with a little bit of wiggle room. Software and formal verification utilize open-source technologies, thereby incurring no additional price on project development. Additional costs from power consumption are minimal since the implementation respects the constraints of a low-power, efficient solution. To prevent additional consequences from hardware integration with present type III or type IV tests, the design uses signals already produced from test kits. This avoids the additional costs of more sensors and designates the FPGA solution as a near plug-and-play add-on to readily available testing options.

3.2 Environmental Impact Analysis

Unintentional environmental effects because of the project implementation are avoided by considering the potential for lead free circuit devices. The FPGA manufacturer, Xilinx designates that the part number XC7VX485T-2FFG1761C of project device corresponds to a RoHS 6/6 "with Exemption 15" with only enough lead content to ensure proper connection between internal die wire and package pins [5], [6]. Since the software model is configurable to various hardware constraints, compliant devices that offer further restrictions than the device used for development continue to have the potential for drop-in replacement.

3.3 Social Impact Analysis

Sleep apnea is a condition that affects all demographics without regard for socioeconomic status, and tests providing accurate and reliable results should be made available to everyone who may be afflicted. Reducing the financial gap for in-home tests allows for quicker access to diagnostics on sleep apnea severity and correspondingly quicker administration for treatment. Out-of-pocket expenses for in-home tests are not billed as such unless a patient's insurance provider preapproves the testing option and subsidizes the total

cost for treatment. Unfortunately, existing low-cost solutions may not provide the accuracy necessary for insurance coverage thereby gating the option of a cheaper test type to those with comprehensive healthcare coverage. Augmenting existing low-cost testing kits with minimal hardware that significantly increases prediction accuracy may lead to wider insurance approval and thereby greater accessibility for patients of all walks of life.

Such requirements deemed necessary for test and treatment approval depends on the type of insurance. Federal healthcare determines coverage based on reliability and necessity standards dictated by laws on Social Security and confirmed by the U.S. Food and Drug Administration (FDA) [7]. Private healthcare institutions provide coverage based on internally decided criteria. The proposed implementation addresses such criteria, like those required by the Blue Cross and Blue Shield Association (BCBSA). The BCBSA determines coverage based on how the experimental technology satisfies five criteria [7]. Technology must be approved by government authorities, backed up by scientific evaluations, positively effective on health, at least as effective as alternative solutions, and expandable beyond its original research setting.

Accuracy tests to be delivered upon project completion address the evidence-based criteria and effectiveness-based criteria of such private insurance solutions. Augmenting type III and type IV tests with greater accuracy provides a greater positive effect for affected populations and increases effectiveness of already available solutions. Some tests are already portable, and the addition of the small formfactor FPGA, will not significantly change a testing kit's size, thereby preserving the tests portability. Following the results of both accuracy and efficiency tests, if the solution deems to be beneficial in all regards, the potential for further approval may be explored. By aiming to satisfy various insurance requirements, such concerns as financial availability may be addressed by the implementation allowing for greater accessibility for all social levels.

3.4 Ethical Analysis

Reliability is the greatest concern, as its absence reduces all faith in the project's design. The implementation must ensure high accuracy, minimize false negatives, and minimize false positives. High accuracy results from the proper configuration of the software golden model and the accurate implementation of the model and training rules on the FPGA. Multiple verification tests quantify the accuracy of the implementation by reporting minimized er-

ror metrics such as least mean squares (LMS) error and mean squared error (MSE). A false positive reading corresponds to the implementation incorrectly determining the severity of sleep apnea to be more severe than is correctly determined. False positive readings by the model are to be avoided because any falsities decrease the viability of the solution and may indicate inconsistent results. A false negative reading corresponds to the implementation incorrectly determining the severity of sleep apnea to be less severe than is correctly determined. False negative readings may detriment an individual by providing proof for a treatment that insufficiently mitigates the sleep apnea affliction. In some cases, these types of decisions may lead to insufficient enough treatment as to have irreversible, detrimental effects on the patient. Since a low level of reliability may lead to permanent harm of an otherwise healthy individual, the absolute minimization of all false readings is pursued.

4 Approach

4.1 CAD/CAM

4.2 Animations

4.3 Simulations

4.4 Numerical Modeling

5 Materials/Resources

5.1 Hardware

5.2 Software

6 Project Management

6.1 Team Organization

All team members are responsible for the tasks they have volunteered for. Team members choices correspond to the strengths and focus areas that they

study. Member Cameron Calv who majors in electrical engineering and computer engineering focuses on the formal verification of hardware, software development of the testbench, and the implementation efficiency analysis. Member Neel Jagad who majors in computer engineering leads software design implementing the SNN golden model and conducting experimental data analysis and feature selection. Member Nick Sica who majors in computer engineering and minors in computer science leads hardware designing performing the development of the hardware Verilog for the FPGA, synthesizing the programmable bitstream, and assisting in final analysis and verification. The faculty member advising the team is Dr. Anup Das.

Group tasks will be assigned using a Kanban project management board allowing for accurate planning of deadlines and compartmentalization of responsibilities. Code flow including that for software models and hardware descriptions is facilitated using Git version control and code storage on GitHub.

6.2 Schedule and Milestones

Project progress is conducted in a six-month time frame split up into three academic terms. The initial month of progress determines familiarity with sleep apnea datasets and obtaining access authorization for proprietary data once familiarity is established. Following the feature selection from available data the software golden model of the SNN is developed as well as the initial architecture layout on the FPGA. Much of the winter season is spent on configuring the model and developing the hardware framework. Connection between the hardware and software will be facilitated with a software testbench. Following the connection of the hardware and the software, prediction accuracy tests will be conducted to determine how, if at all, the model needs to be tuned. Concluding progress are the final efficiency tests for the FPGA implementing the SNN following the synthesis of the hardware bitstream. The following chart showing the time dedicated to each design goal and the relative participation of each team member to the goal is provided below.

6.3 Project Budget

The total cost of all materials consists only of the expenses incurred by the hardware design choice. The FPGA provided by Xilinx must be programmed and developed upon using the Vivado HLx program which incurs a licensing cost of $3,500. All other technologies used are open-source or publicly

licensed databases.

6.4 Success Benchmarks

Performance metrics such as the MSE and LSM error will give accuracy results from the software and hardware implemented model. Efficiency tests run on the hardware give a method of quantifying the total energy cost of the implementation which must remain as low as possible.

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Appendices

A Detailed Project Management

B Programming Source Code and Drawings

C Teamwork Contract