Project Title: Finite State Device

Course: ELET 1210 – DIGITAL EELECTRONICS 1

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Introduction

This report will be discussing Flip Flops, specifically a J-K Flip Flop. Flip flops are the most basic memory devices used for information storage in sequential circuits. There are 1-bit memory devices where the output depends not only on the present value of the input, but the previous value as well. In this lab a synchronous finite state device will be designed based on a sequence using a J-K flip flop. The J-K flip flop device will then be analysed through tables, diagrams, and circuits to check and verify it cycles through its sequence correctly and is self-correcting.

Description of Experimental Setup/List of Equipment Used

The equipment used for this experiment include, a power supply, DIP switch, 2 breadboards, wires, resistors, push button, 7 segment display and ICs.

Required IC's:

74HC73 Dual J-K Flip Flop – 2

74HC32 Quad 2 – Input OR

Logic Diagram

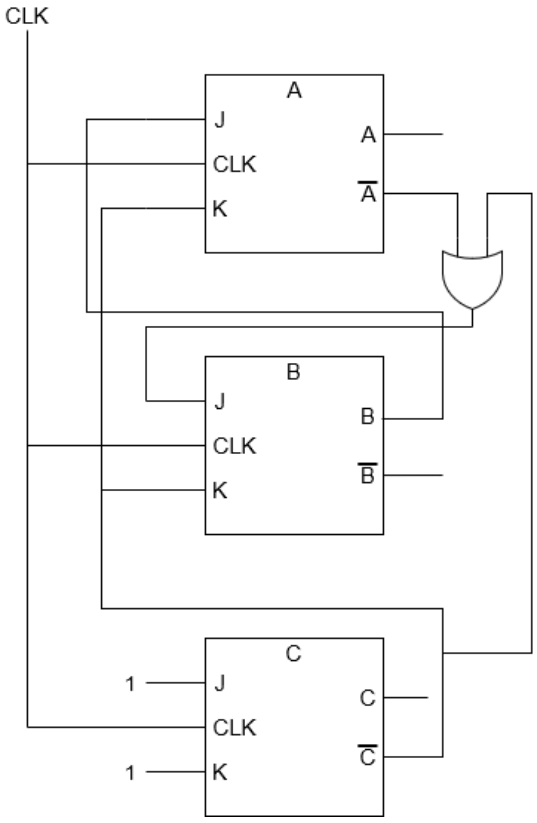


Figure A: Logic Diagram of Finite State Device using J-K Flip Flop

Pictorial Diagram

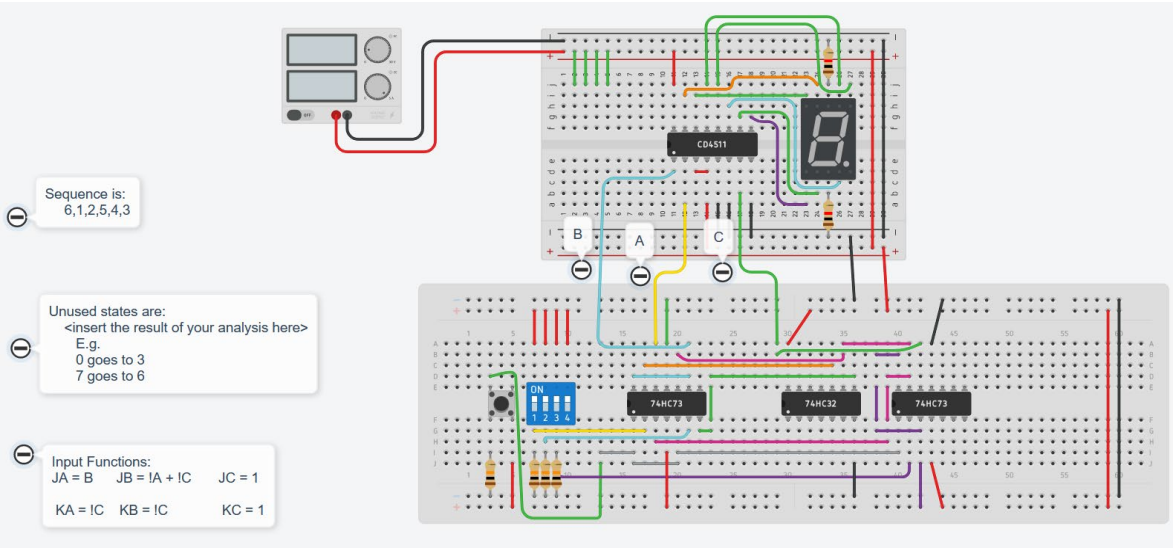


Figure B: Pictorial Diagram of Finite State Device using J-K Flip Flop

IC Positions: 1- 73HC73, 2- OR 3-73HC73

State Diagram

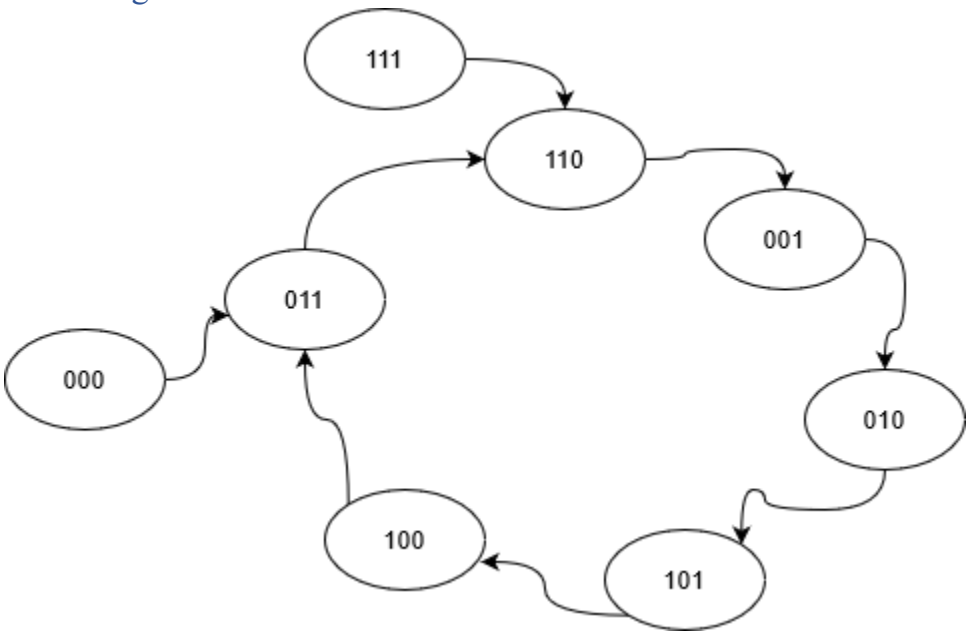


Figure C: State Diagram of Finite State Device using J-K Flip Flop

Procedure/Method

A count sequence was given and used to produce tables D-K. The input functions resulting from the tables were then used to create the diagrams from Figure A and C. The circuit template was used and then implemented based on the input functions calculated and IC positions given. The circuit was set up as shown in figure B. The device was tested by turning on the power supply, setting the inputs on the DIP switch to on and the pushbutton was pressed to cycle through numbers in a sequence that was displayed on the 7-segment display. After different inputs were checked and the sequence was verified the power supply was turned off.

Results

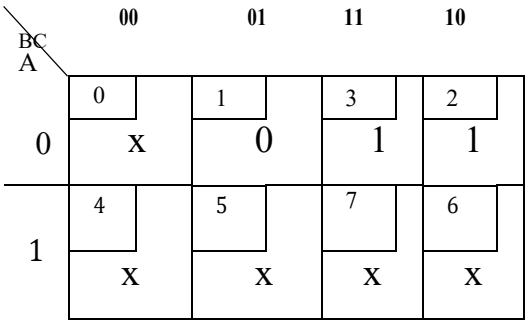
Sequence – 6,1,2,5,4,3

Type of flip Flop = J-K

State Table													
Present State					Next State				Flip Flop Functions					
sequence	A	B	C		A	B	C		J_A	K_A	J_B	K_B	J_C	K_C
6	1	1	0		0	0	1		X	1	X	1	1	X
1	0	0	1		0	1	0		0	X	1	X	X	1
2	0	1	0		1	0	1		1	X	X	1	1	X
5	1	0	1		1	0	0		X	0	0	X	X	1
4	1	0	0		0	1	1		X	1	1	X	1	X
3	0	1	1		1	1	0		1	X	X	0	X	1

Figure D

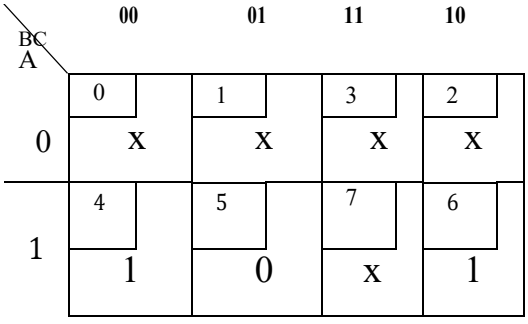
Simplify the function of each input:



Present State					Flip Flop Function
	A	B	C		J_A
6	1	1	0		X
1	0	0	1		0
2	0	1	0		1
5	1	0	1		X
4	1	0	0		X
3	0	1	1		1

$J_A = B$

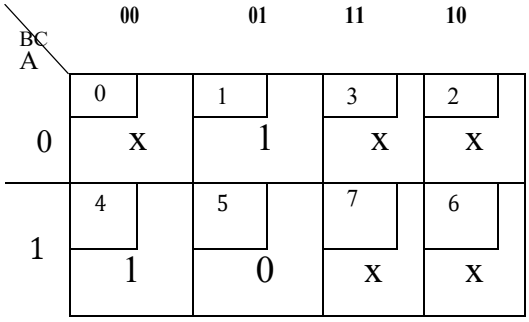
Figure E



Present State					Flip Flop Function
	A	B	C		K_A
6	1	1	0		1
1	0	0	1		X
2	0	1	0		X
5	1	0	1		0
4	1	0	0		1
3	0	1	1		X

$K_A = \overline{C}$

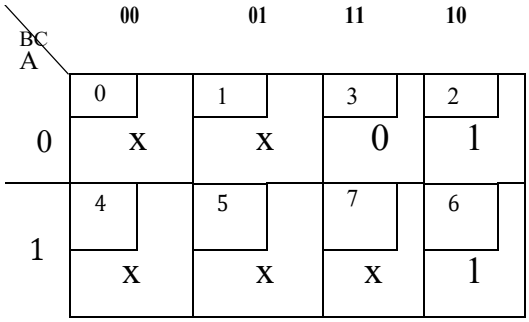
Figure F



$J_B = \overline{A} + \overline{C}$

Present State					Flip Flop Function
	A	B	C		J_B
6	1	1	0		X
1	0	0	1		1
2	0	1	0		X
5	1	0	1		0
4	1	0	0		1
3	0	1	1		X

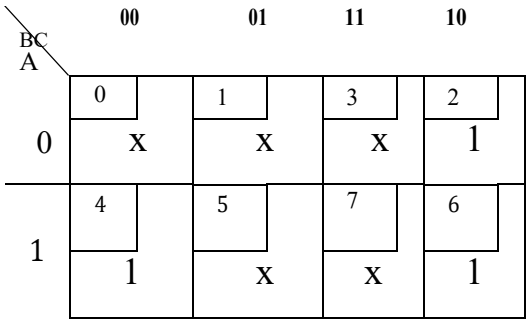
Figure G



Present State					Flip Flop Function
	A	B	C		K_B
6	1	1	0		1
1	0	0	1		X
2	0	1	0		1
5	1	0	1		X
4	1	0	0		X
3	0	1	1		0

$K_B = \overline{C}$

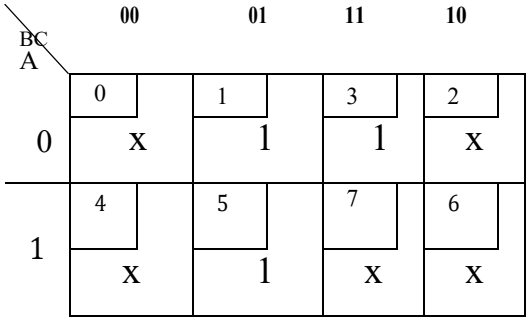
Figure H



Present State					Flip Flop Function
	A	B	C		J_C
6	1	1	0		1
1	0	0	1		X
2	0	1	0		1
5	1	0	1		X
4	1	0	0		1
3	0	1	1		X

$J_C = 1$

Figure I



Present State					Flip Flop Function
	A	B	C		K_C
6	1	1	0		X
1	0	0	1		1
2	0	1	0		X
5	1	0	1		1
4	1	0	0		X
3	0	1	1		1

$K_C = 1$

Figure J

Input Functions

$J_A = B$ $J_B = \overline{A} + \overline{C}$ $J_C = 1$

$K_A = \overline{C}$ $K_B = \overline{C}$ $K_C = 1$

Analyzing unused state

	Present State									Next State			
	A	B	C	J_A	K_A	J_B	K_B	J_C	K_C	A	B	C	
0	0	0	0	0	1	1	1	1	1	0	1	1	3
7	1	1	1	1	0	0	0	1	1	1	1	0	6

Figure K

Discussion and Conclusion

To conclude, nothing unusual was shown and results were shown as expected. A synchronous finite state device using J-K Flip Flops was designed based on a given sequence and implemented. The sequence was used to show the state table, input functions, state diagram and logic diagram and then proved to work through a circuit. The circuit proved the device sequence cycled correctly and showed it was self-correcting.