Project Title: MINIMIZATION & THE ADDER

Course: ELET 1210 – DIGITAL EELECTRONICS 1

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Introduction

This report discusses minimization and adders. Minimization is the process of simplifying the algebraic expression of a Boolean function. Minimization is important because it minimizes the logic gates used in an expression without changing the output of a Boolean expression. An adder is a digital circuit that performs addition of numbers. There are two types of adders, a full adder, and a half adder. A full adder can be constructed using two half adders. In this lab function minimization will be proved and two half adders will be used to construct a full adder with basic gates.

Description of Experimental Setup/List of Equipment Used

Equipment Used:

The equipment used for this experiment include, a breadboard, power supply, wires, a DIP switch, resistors, 2 LEDs, and ICs.

Required IC's:

74LS04 Hex Inverter

74LS32 Quad 2 – Input OR

74LS11 Triple 3-Input AND

74LS08 Quad 2-Input AND

Logic Diagram Experiment 1

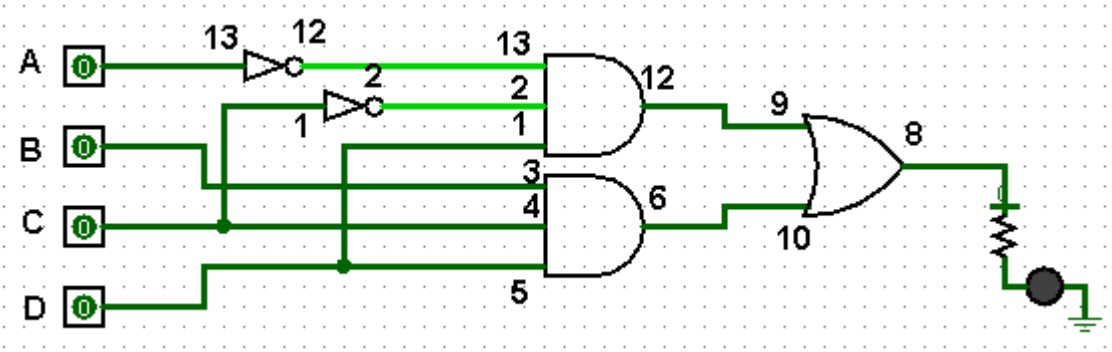

Figure A : Example of a Logic Diagram for a $DBC + D\overline{A}\,\overline{C}$

Pictorial Diagram Experiment 1

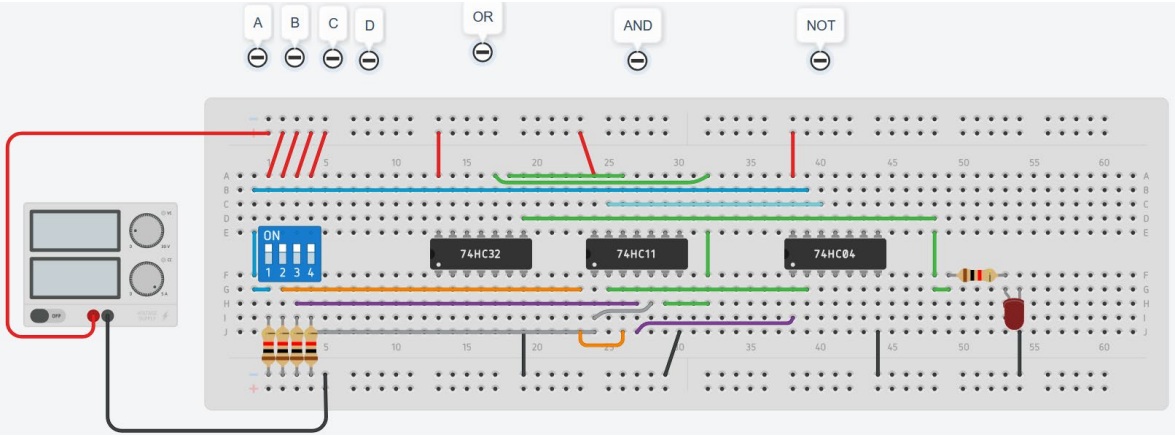

Figure B : Example of Pictorial Diagram for $DBC + D\overline{A}\,\overline{C}$

Logic Diagram Experiment 2

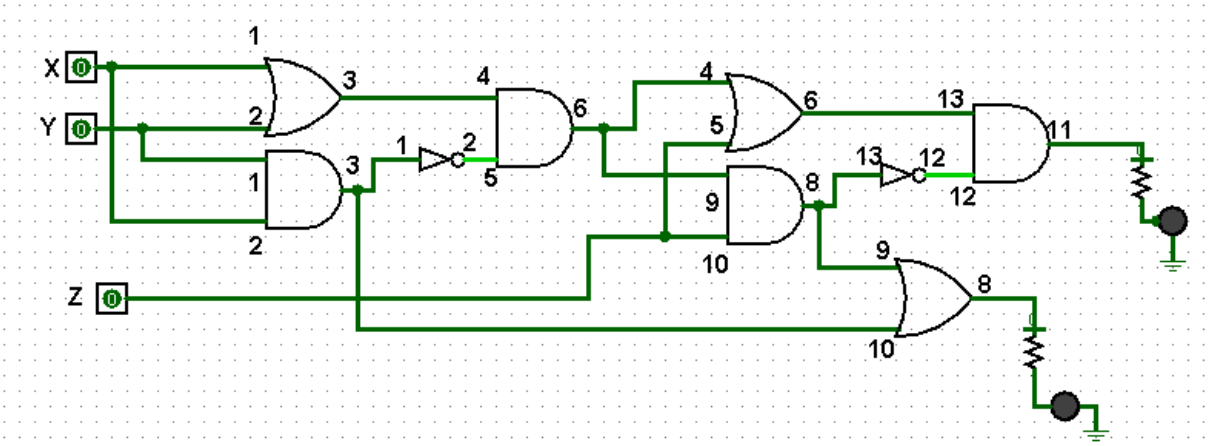

Figure C : Example of Logic Diagram for Full Adder

Pictorial Diagram Experiment 2

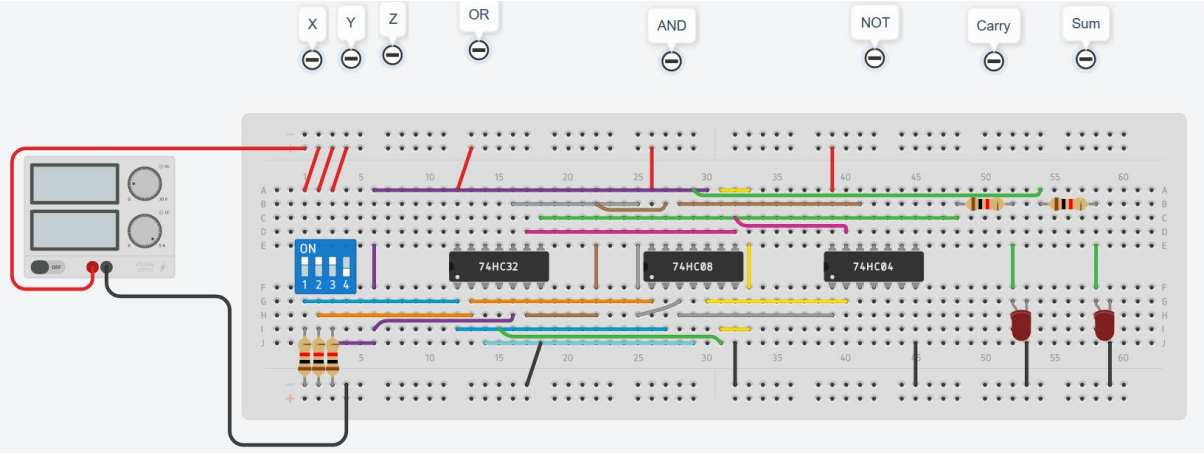

Figure D : Example of Pictorial Diagram for Full Adder

Procedure/Method

All equipment was gathered, and setup as showed in the pictorial diagrams, figures B and D. The power supply was turned on and the DIP switch was then used to put in different input from the truth tables and output was showed in the LEDs. The LED being on signified an output of 1 and the LED being offed signified off. In Experiment 1 16 different inputs were used and the outputs were recorded. In experiment 2 8 different inputs were used and two outputs were recorded. The two outputs recorded were the sum and the carry of the full adder. Finally, after inputs were entered for each experiment the power supply was turned off.

Results

Table for Experiment 1

Table for expression: $(D+\overline{B}D)(\overline{B}+B\overline{C}+BC)(BC+\overline{A}\,\overline{C})$							
A	B	C	D	$D+\overline{B}D$	$\overline{B}+B\overline{C}+BC$	$BC+\overline{A}\,\overline{C}$	F
0	0	0	0	0	1	1	0
0	0	0	1	1	1	1	1
0	0	1	0	0	1	0	0
0	0	1	1	1	1	0	0
0	1	0	0	0	1	1	0
0	1	0	1	1	1	1	1
0	1	1	0	0	1	1	0
0	1	1	1	1	1	1	1
1	0	0	0	0	1	0	0
1	0	0	1	1	1	0	0
1	0	1	0	0	1	0	0
1	0	1	1	1	1	0	0
1	1	0	0	0	1	0	0
1	1	0	1	1	1	0	0
1	1	1	0	0	1	1	0
1	1	1	1	1	1	1	1

$(D+\overline{B}D)(\overline{B}+B\overline{C}+BC)(BC+\overline{A}\,\overline{C})$

Simplified:

$(D+\overline{B}D)(\overline{B}+\overline{C}+BC)(BC+\overline{A}\,\overline{C})$

$(D)(\overline{B}+\overline{C}+B)(BC+\overline{A}\,\overline{C})$

$(D)(\overline{B}+B+\overline{C})(BC+\overline{A}\,\overline{C})$

$(D)(1+\overline{C})(BC+\overline{A}\,\overline{C})$

$(D)(BC+\overline{A}\,\overline{C})$

$DBC+D\overline{A}\,\overline{C}$

Table for Experiment 1 Simplified

Table for expression: $DBC + D\overline{A}\,\overline{C}$						
A	B	C	D	DBC	$D\overline{A}\,\overline{C}$	F
0	0	0	0	0	0	0
0	0	0	1	0	1	1
0	0	1	0	0	0	0
0	0	1	1	0	0	0
0	1	0	0	0	0	0
0	1	0	1	0	1	1
0	1	1	0	0	0	0
0	1	1	1	1	0	1
1	0	0	0	0	0	0
1	0	0	1	0	0	0
1	0	1	0	0	0	0
1	0	1	1	0	0	0
1	1	0	0	0	0	0
1	1	0	1	0	0	0
1	1	1	0	0	0	0
1	1	1	1	1	0	1

Table for Experiment 2

Table of Full Adder					
	Previous Carry	Addend	Augend	Sum	Carry
	X	Y	Z	S	C
0	0	0	0	0	0
1	0	0	1	1	0
2	0	1	0	1	0
3	0	1	1	0	1
4	1	0	0	1	0
5	1	0	1	0	1
6	1	1	0	0	1
7	1	1	1	1	1

Discussion and Conclusion

In conclusion, nothing unusual was shown and results were shown as expected in experiment 1 and 2. In experiment 1 the simplified algebraic expression showed the same results as the regular expression. Minimization was proven to be very useful by significantly reducing the expression and was displayed through the truth tables and circuit. In experiment 2 the full adder was built and showed through circuits and basic logic gates. The outputs of the full adder were also successfully

shown in the circuit. To sum up, both experiments were successful to show the implantation of minimization and full adder.