Construction of a Digital Voice Recorder System

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Executive summary

The aim of this project is to design and evaluate a digital voice recoding system using the Teensy 2.0 microcontroller. This report focuses on developing a condition circuitry to enable the Teensy board to process and play back input signals from a microphone.

The design goal for the integrated circuitry is to produce high-quality audio recording such that it can be utilized in a personal voice recording unit. This is achieved by having low audio distortion between frequencies of 280hz to 7kHz. The conditioning circuitry was split into three main sections, the microphone interfacing stage, the filter stage, and amplification stage. The microphone interfacing stage offsets the AC component of the microphone output to be centered at 2.5V. The filter stage has a target attenuation of at least 48.16dB above 7813Hz while minimizing distortion within the passband and maximizing the passband. This is to ensure the significant does not experience anti-aliasing. The final amplification stage aimed to achieve a signal close to 5Vpp with a dc offset of 2.5V.

These stages will be designed and integrated into the conditioning circuitry for the TeensyboBv2. To achieve this, multiple programs were used including MATLAB, excel and LTspice. The circuitry was then built and tested. Both the microphone and amplification stages 1 and 3 were demeaned to be adequate for a high-quality audio application. The filter stage however displayed a large range of variation within the gain of the passband. This would result in significant distortion in an output sound.

Because limitations posed by capacitor and resistor tolerances hindered the production of high-quality audio recording software. As a result, further investigation is recommended to explore the potential advantages of implementing potentiometers with calibrated resistances or high accuracy resistors. These approaches have the potential to reduce gain variations within the passband near the cutoff frequency. A higher sampling rate microcontroller could also be used to increase the stopband frequency. These strategies would result in a design to record and play back high-quality audio within further designs.

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Project Description

Project Aim

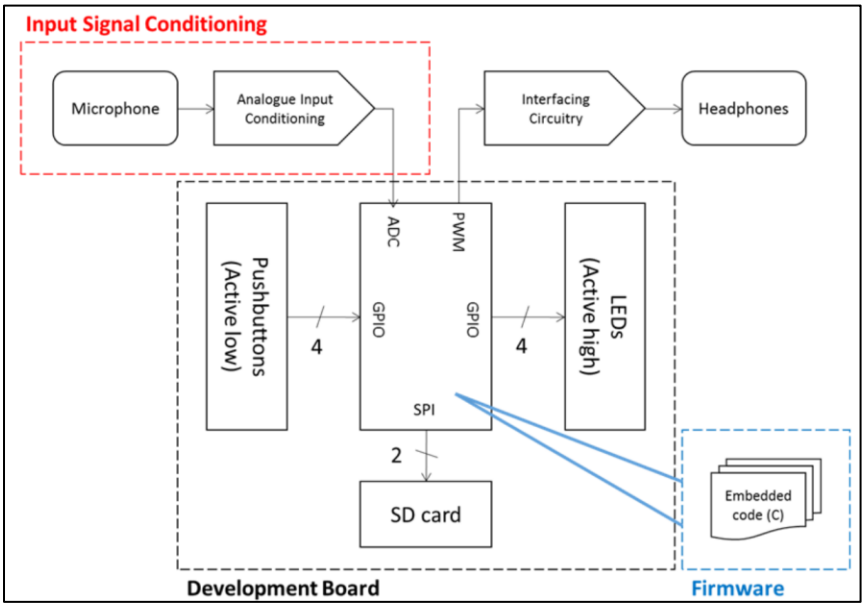


Figure 1: The Block diagram of the DVR system. The signal condition system is indicated in red.

The aim of this project is to design, implement and evaluate a digital voice recording system. As seen in figure 1, the final stages of digital voice recorder (DVR) system have been provided. This includes a microcontroller which was to process and save an input such that it can be played back using a headphone

jack. The microcontroller supplied for this project is the Teensy 2.0 microcontroller, which will be exclusively utilized within the scope of this design report.

Therefore, the primary focus of this report is to develop, implement and evaluate conditioning circuity for the Teensy 2.0. The circuity must condition the input signal from a supplied electret condenser microphone enable it to be processed successfully by a microcontroller. Developing input conditioning circuitry is the crucial step which will enable the operation of the digital voice recording system. This paper aims to methodically construct circuity that seamlessly integrates with the provided microcontroller enabling the successful operation of the digital voice recorder system.

Design goals

The design goal of the input circuitry is high-quality audio recording capabilities. To accomplish this, the input signal circuitry should reduce the effect of background noise. The input from the microphone must maintain its accuracy throughout the processing chain of the analogue input condition circuity. By prioritizing these aspects, the circuitry aims to deliver an optimal audio recording experience, ensuring the captured voice remains accurate to the original source with minimal artifacts or degradation.

Considering that the DVR is to be used by humans, the frequency of human speech should be considered. It was generally known that a common speech frequency band used by telephone carries typically extends from 280hz to 3.3khz [1]. However, it was determined using the PAMS (perceptual analysis measurement system) that an upper bound of 7khz can provide a significant improvement when compared to 3.3khz [2]. Within the design constructed it is required to have frequencies ranging from 280hz to 3.3khz, however an upper bound of 7khz is desired for a high-quality audio recording device.

The range of input signal frequencies between 280hz and 7khz must remain scaled uniformly to avoid distorted sound. The sound perceived as barely perceptual to the human ears is <1 dB under ideal circumstances. An average listener would be expected to hear a change in dB greater than 3db [3, p. 325]. Therefore, the design must ensure that the frequencies between 280hz and 7khz must have a maximum dB change of less than 3 dB to ensure no audio distortion. This should be further extended to be equal to less than 1.5dB. This is to ensure statistically the average listeners will not be able to perceive any change or distortion within the played back sound. The circuity will meet specifications if the maximum deviation is less than 3dB, with an ideal deviation of 1.5dB, throughout the frequency audio hearing range from 280hz to 7khz.

In summary, the design goals for this report, the primary objective is to create input circuitry that enables high-quality audio recording capabilities. This involves reducing background noise and maintaining the accuracy of the input signal throughout the entire processing chain. The desired frequency range for the audio recording device extends from 280Hz to 7kHz, ensuring compatibility with human speech frequencies and providing an improvement in audio quality when compared to the typical 300Hz to 3.3kHz speech bandwidth. The circuitry must ensure consistent scaling of frequencies within this range to avoid non-uniform sound. The maximum deviation in dB should be less than 3dB, with an ideal deviation of 1.5dB, throughout the frequency range of 280Hz to 7kHz. By meeting these specifications, the designed circuitry will provide exceptional audio recording, delivering accurate and distortion-free playback that is imperceptible to the average listener.

Design Specifications

The microcontroller used to process and input signal is the Teensy 2.0 microcontroller board (TeensyboBv2). The Teensy is capable of supplying 5V from a traditional USB power supply to the input signal conditioning circuity. The Teensy board's analogue to digital converter (ADC) peripheral to save the input signal. To achieve maximum volume the input signal supplied to the Teensy board should be as close to 5 volts peak to peak (Vpp) centered around 2.5 volts. The Teensy also has an 8-bit resolution within the ADC peripheral. There are only 256 quantization levels which range from 0 to 255 which represents max.

The TeensyboBv2 has a sample rate of 15625Hz which heavily limits the capabilities of the DVR system. This is because of Nyquist-Shannon sample theorem [4], which states that the maximum accurately represented frequency that results in no aliasing is half of the sampling rate. Since the calculated sampling rate is:

$$15625Hz/2 = 7812.5Hz.$$

The frequency cutoff for the output of the signal conditioning circuitry is then strictly required to be less than 7812.5Hz. If an input signal above this frequency limit is fed into the Teensy board, the high-frequency signal gets processed into a lower frequency range resulting in significant distortion within the audible output signal. To prevent frequencies above 7812.5Hz from reaching the microcontroller, it is crucial to ensure that the input circuitry effectively filters out any signals beyond this threshold. Due to the limited 256 quantization levels, frequencies beyond 7812.5Hz need to be attenuated to a level below the first quantization level to ensure the signal is not captured by the microcontroller. As a result, the circuitry must attenuate any frequencies above 7812.5Hz by at least a factor of 256. This represented in dB is:

$$20 * \log_{10}(256) = 48.16dB$$

It can be said that a critical requirement of the design must attenuate frequencies above 7812.5Hz to a minimum factor of 48.16dB when compared to the passband frequencies.

For the construction of this circuit design, we have been provided access to TL974 op amps, CMA-6542TF-K electret condenser microphone as well as E12(10% tolerance) capacitors and E24 (5% tolerance) resistors. These components will be exclusively used throughout this report do the accessibility in construction. These components must be utilized effectively to ensure optimal performance of the design.

The specifications are summarized include:

- Maximum dB variation is less than 3dB, ideally less than 1.5dB.
- The AC signal must be offset by 2.5V.
- The AC signal must be close to 5Vpp.
- Frequencies above 7812.5Hz must be attenuated by a minimum of 48.16dB.
- Components are limited to E12 capacitors and E24 resistors.
- The microphone used is the CMA-6542TF-K electret condenser microphone.
- The op amps available are the TL974 op amps.

Adhering to these specifications is crucial to functional, high performance DVR system.

Design Process

Design Approach

Through research on existing microphone interfacing circuitry, it was discovered that the circuit can be divided into three primary stages: microphone interfacing, filtering, and final amplification [5] [6] [7]. By utilizing op-amps in each stage, the output signals can be buffered, enabling the independent construction of each stage while ensuring consistent operation when combined.

The first stage of microphone interfacing involves capturing and processing the microphone signal to prepare it for the subsequent filter stage. The op-amps supplied have a common-mode input range when supplied with 0V to 5V of 1.15V to 3.85V. The output directly from the microphone does not fall within this range as it has dc offset removed within a typical application circuit [8]. To avoid distortion the output signal from the microphone interfacing stage into the filter stage should be centered around 2.5V and not exceed the range from 1.15V to 3.85V.

The second stage, which is the filter stage, will be used to ensure that frequencies above 7813Hz are attenuated to at least 48.16dB when compared to the passband frequencies. The passband frequencies should not be significantly affected by the filter stage. This is to ensure there is no distortion above 1.5dB within the passband of the output signal.

The existing solutions typically use the Sallen-Key topology for filtering the microphone input. This topology is favored due to its ability to cascade of multiple Sallen-Key filters which facilitates the construction of higher order filters to achieve response characteristics required by the filter stage. Furthermore, the Sallen-Key filters are beneficial because they are reasonably tolerant of component variations [9]. As such the Sallen-Key topology will be incorporated within the filter stage.

The third stage within the conditioning circuity is amplification. This stage will simply manipulate the signal from the filter stage to ensure the signal is close to 5Vpp and has a dc offset of 2.5V. The amplification required will depend on the gains in stage 1 and 2 as well as the microphone's typically peak-to-peak output voltage. An inverting op-amp circuit will be used to amplify the signal to meet specifications.

To summarize, in stage 1, the signal will first be output by a typical microphone configuration. A dc of 2.5V will be added using an op-amp. In stage 2, the signal will then be processed by the filter stage to ensure an attenuation of approximately 48dB at frequencies beyond 7813Hz while guaranteeing audio quality. Afterwards the amplification stage will ensure the signal is centered around 2.5V and has close to 5Vpp during typical speaking conditions. These individual blocks will be designed separately and combined to form the input conditioning circuity for the TeensyboBv2.

Design Circuitry Blocks

Microphone Interfacing

The microphone was set up with 1.5k Ω resistor and 1 µF as these values are supplied within the data sheet for the CMA-6542TF-K electret condenser microphone. This microphone was then tested as seen in appendix 1 to confirm a working circuit and to determine the maximum Vpp of 135mV when counting from 1 to 50. To optimize the microphone's capability to capture the speaker's voice while minimizing background noise, the microphone was positioned close (approximately a 5cm gap) to the speaker. This practice is commonly observed in the use of commercial voice recorders. This 135mVpp is not close to

clipping the common mode input range of the TL974 op-amp once centered around 2.5V. The output from the microphone just must be dc offset to 2.5V. This can be achieved using an inverting op with a voltage bias at the non-inverting terminal [10].

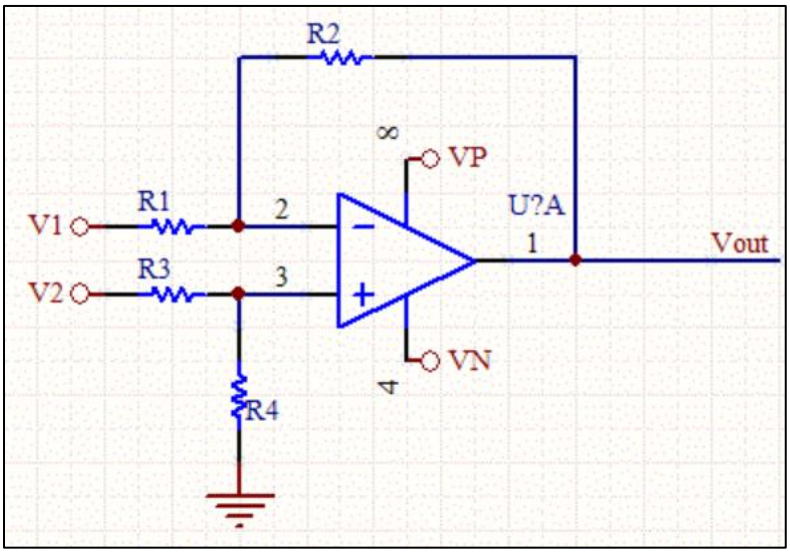


Figure 2: The circuit required to add dc offset to the microphone signal, V1 is input signal, V2 is power supply voltage.

In our design, we have chosen to eliminate the need for gain within stage 1, resulting in equal resistors (R1 = R2). This was done to ensure the common mode input range for the op-amps would not be exceeded Additionally, to properly account for input bias current, we have set R3 to be equal to R1. Because Vcc is 5V and the inverting terminal requires Vref at 2.5V, we have selected R4 to be equal to R3, effectively acting as a 50% voltage divider. Adding both the microphone circuit together with the dc offset circuit finalizes the first microphone interfacing stage.

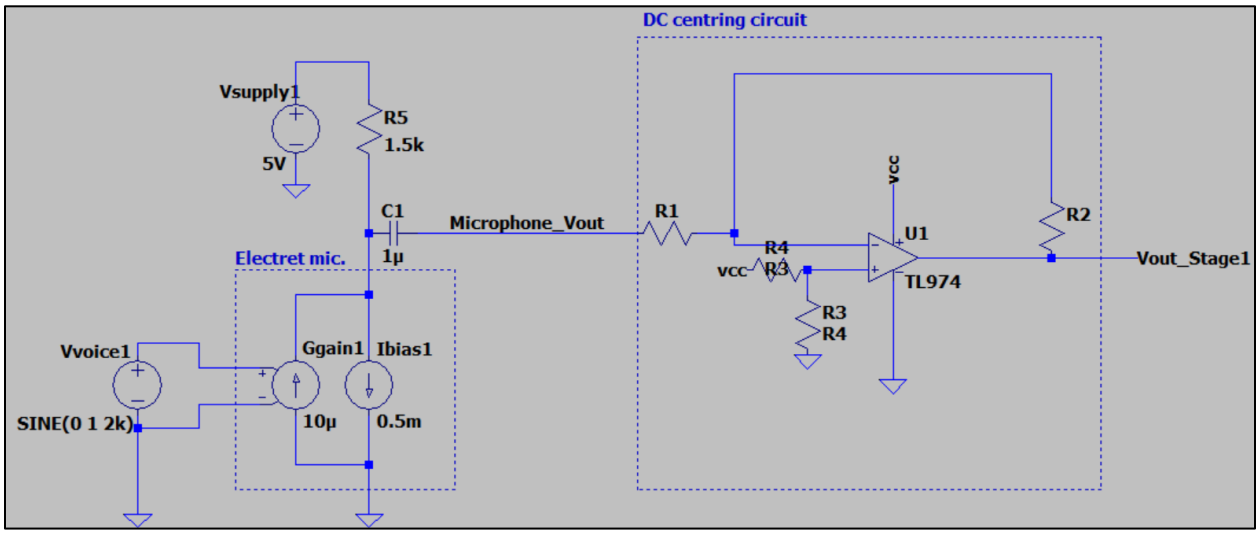


Figure 3: The current iteration microphone interfacing circuitry

As seen in figure 3, the C1 capacitor and R1 resistor form a passive high pass filter. The cutoff frequency for this high pass filter is shown to be sufficiently low such that it does not attenuate the passband. This can be achieved by setting R1 within the circuit diagram in figure 3 to be 10kΩ. This results in a cutoff frequency of 15Hz which is low enough to have no effect on the passband frequencies. This in return results in R2=R1 and R4=R3=R1. Therefore, the microphone interfacing stage is complete.

Filter Stage

The filter stage is the most critical stage to ensure the quality of audio remains intact. To develop an effective solution, MATLAB analysis was performed to determine the characteristics of the entire filter stage. The initial deductions made from the MATLAB analysis was that the design goal of a passband ranging to 7000Hz was unachievable as seen in appendix 2. A 15th order Chebyshev filter or 58th order Butterworth filter was required to achieve specifications which are not efficient or compact enough for use in portable recorder. Furthermore, it was determined that the Chebyshev filter is better suited due to its faster roll off attenuation passed the cutoff frequency, which is attributed to its second-order transfer function. Therefore, it will be exclusively used throughout the rest of the report.

The passband cutoff frequencies range from 2800Hz, 4450Hz and 5650Hz(appendix 1 to 3) for a 4th order, 6th order and 8th order Chebyshev filter respectively. Since the 2800Hz filter simply does not meet the minimum specifications, it will not be implemented. The 6th order barely meets specifications, however, due to the use of a total of five op-amps (1 for dc-centering, 1 for amplification and 3 for filtering) an additional TL974 will be required within the design. This is because the TL974 is limited to only 4 op-amps. Therefore, only ¼ of this additional unit will be utilized which is efficient. To reduce this inefficiency a higher order filter is either 8th,10th or 12th order to ensure exceptional audio quality while maintaining the use of two TL974 units. Both the 10th and 12th order filters get close to the specification set therefore further analysis will be done to determine their viability (appendix 4 to 6).

MATLAB has an inbuilt function called chev1(draws values from cheb1ord as well) which can calculate the poles and zeroes of the transfer function for a given set of parameters. The Sallen-Key transfer function for the give Sallen-Key low-pass filter can be seen in figure 4.

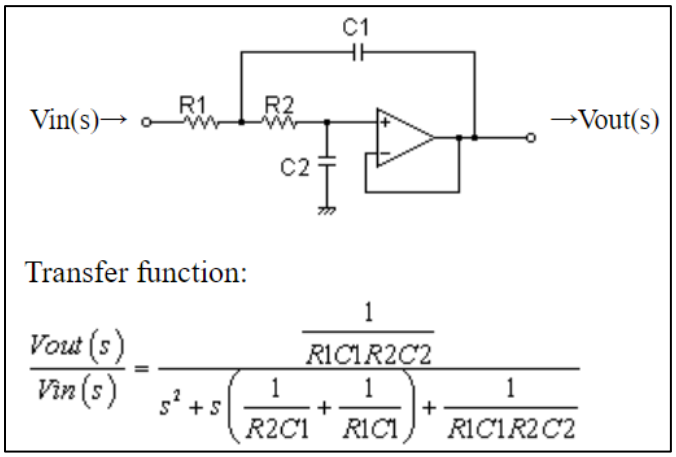


Figure 4: Sallen-Key low-pass filter and its associated transfer function [11].

$$\frac{V_{o(s)}}{V_{in(s)}} = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

Figure 5: The standard second-order form of a transfer function. [11]

$$(s - p_1)(s - p_2) = s^2 - (p_1 + p_2)s + p_1 p_2$$

Figure 6: The calculated MATLAB poles calculated into standard form [12].

Therefore, it should be clear to see the parallel format between the denominators of figure 4 to figure 6. From figures 4 to 6 equations 1 and 2 can be constructed from the like terms within the denominator. Let the damping ratio be equal to Q.

$$p_1 p_2 = w_n^2 = \frac{1}{R_1 R_2 C_1 C_2} \quad (1)$$

$$-(p_1 + p_2) = 2Qw_n = \left(\frac{1}{R_2 C_1} + \frac{1}{R_1 C_!}\right) \quad (2)$$

To simplify the transfer function let:

$$C_1 = 1 * 10^{-9} F$$

$$C_2 = nC_1$$

$$R = R_1 = R_2$$

Therefore equation 1 becomes;

$$p_1 p_2 = w_n^2 = \frac{1}{RRC_1 nC_1}$$
$$p_1 p_2 = w_n^2 = \frac{1}{R^2 nc_1^2}$$
$$\sqrt{p_1 p_2} = w_n = \frac{1}{\sqrt{n} RC_1}$$

And equation 2 becomes:

$$-(p_1 + p_2) = 2Qw_n = \left(\frac{1}{\mathrm{R}C_1} + \frac{1}{\mathrm{R}C_1}\right)$$

$$-(p_1 + p_2) = 2Qw_n = \frac{2}{RC_1}$$

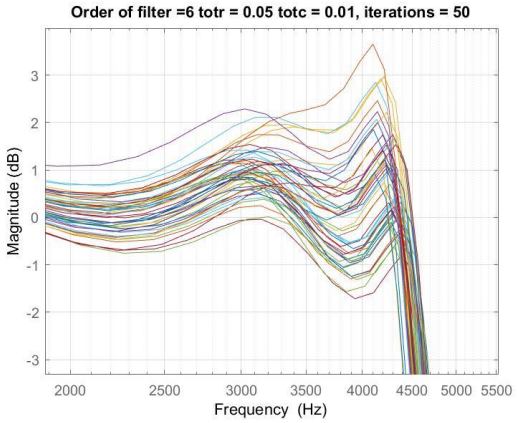
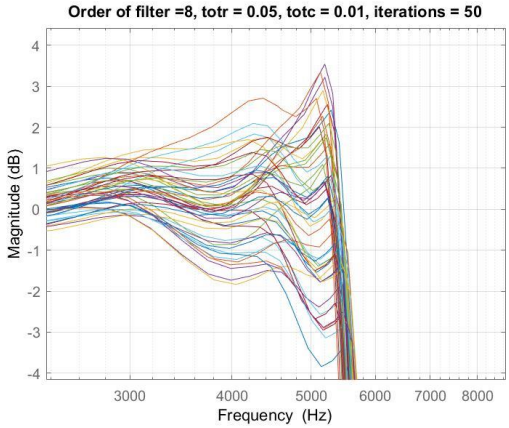
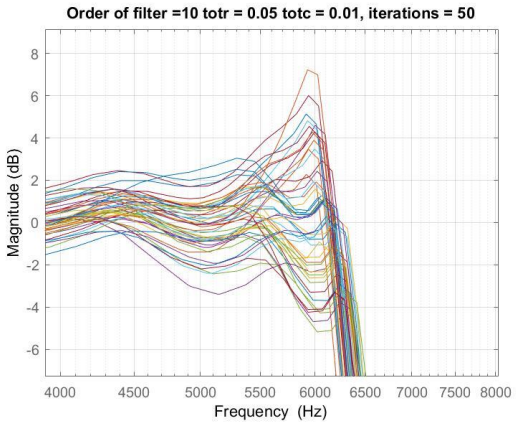
$$-\frac{(p_1 + p_2)}{2} = Qw_n = \frac{1}{\mathrm{R}C_1}$$

Now we have the required equations to turn the poles of p1 and p2 into first w_n, then Q and R. These can then be used to calculated n and subsequently C_2. As a result the 4 unknown component values have been exactly determined for the two complex conjugate poles supplied. These calculations are implemented into the MATLAB function as seen in Appendix 8. The code turns a set of two poles into released values resistor and capacitor values for the circuit diagram shown in figure 4 assuming $R_1 = R_2$, and $C_1 = 1nF$. Another MATLAB function was created (Appendix 9) which turns returns realized values back into a transfer function. MATLAB code was created to turn all poles into realized values, run 50 iterations of randomized values with the tolerances of the E12 capacitors and E24 resistors (appendix 10).

The tolerances are causing a massive variation in potential values for maximum passband gain. The inaccuracy of the registered values of the E12 range capacitors results in a cumulative effect as each additional filter order is implemented. This effect is evident in the significant deviation from the expected bode plot, as shown in Appendix 11 in especially the 10th and 12th order filters. To mitigate this, for the sake of results, the capacitors will be carefully measured and only accepted if their total deviation from the desired value is within 1%. This reduces the theoretical tolerance of the capacitors to 1%.

This reduction in capacitor tolerance had a significant effect on the design allowing the 6th order transfer function to almost obtain an absolute maximum passband gain of less of approximately 4dB (appendix 12). However, after restricting the capacitors used, the 12th order filter still exhibits a substantial deviation far greater than 3dB. As a result, the 12th order filter is not suitable for the design outlined in this report. An additional modification that will reduce the attention of the passband is setting Amax lower within the MATLAB code (maximum gain within the passband lower). This is in attempt to reduce the peak ripple at the edge of the passband caused because of the Chebyshev filter. To further improve the design, stopband attenuation was increased to -49dB to ensure sufficient over-attenuation and prevent any potential anti-aliasing effects.

Table 1: The final iterations of the 3 potential filter designs

Potential filter orders to be chosen	Bode plots for a range of tolerance values, Test condition 3 Amax = 1, totr = 0.05, totc1, totc2 = 0.1, amin=49 (within MATLAB code)
6th order MATLAB Condition: Fp=4550	
8th order Fp= 5400	
10th order Fp= 6200	

Due to the limitations of tolerances values, some leniency must be given to this design. Despite not strictly less that 3dB the entire passband, the 8th order filter performs the best when compared against the 6th and 10th order filter. The 10th order filter still has too significant of gang within the passband frequencies as thus is not suitable. The 6th order filter has 2dB located within the critical speech intelligibility range. Therefore, design having potential higher gain peaks and a more complex design, the 8th order filter does achieve the highest quality in voice. This can be seen in table 1.

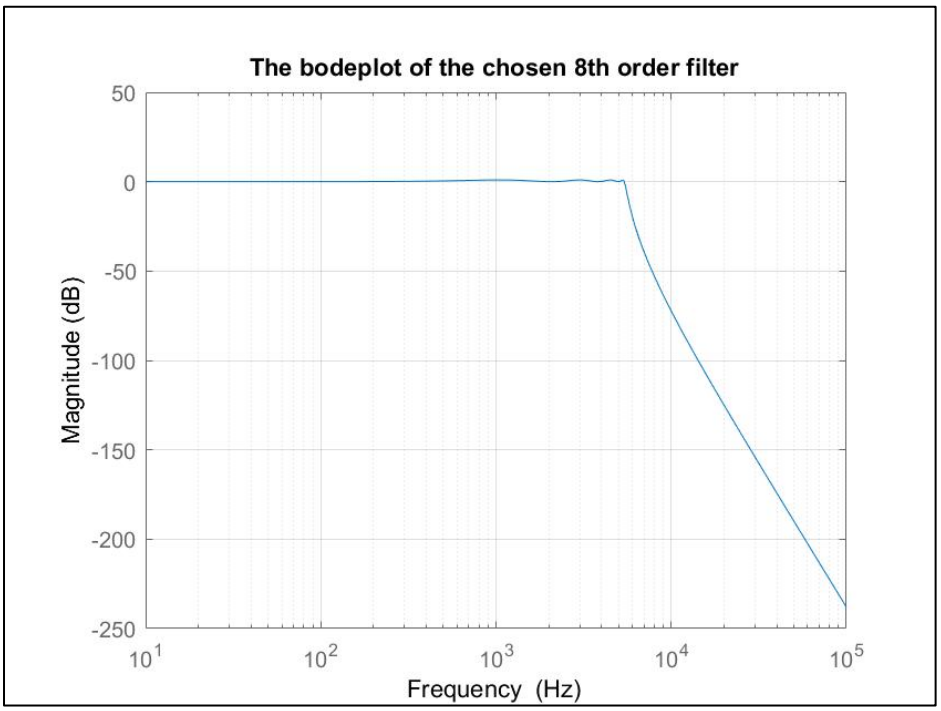


Figure 7: The overall bode plot of the chosen 8th order filter (params, Fp=5400, Amin=49, Amax=1).

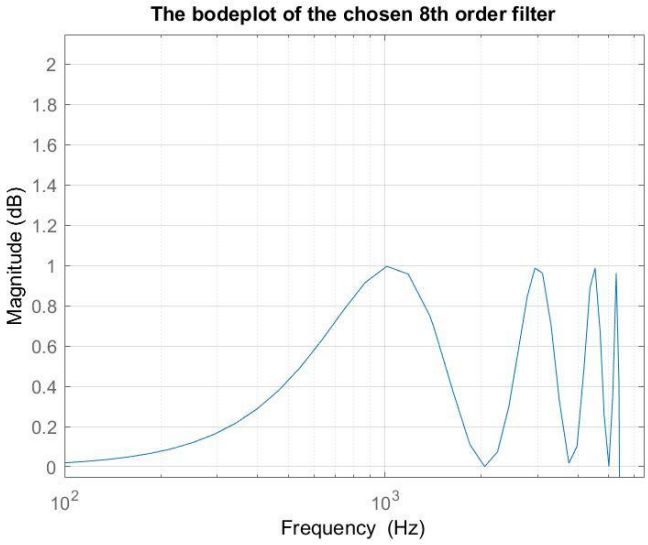


Figure 8: The passband for the bode plot for the chosen 8th order filter design.

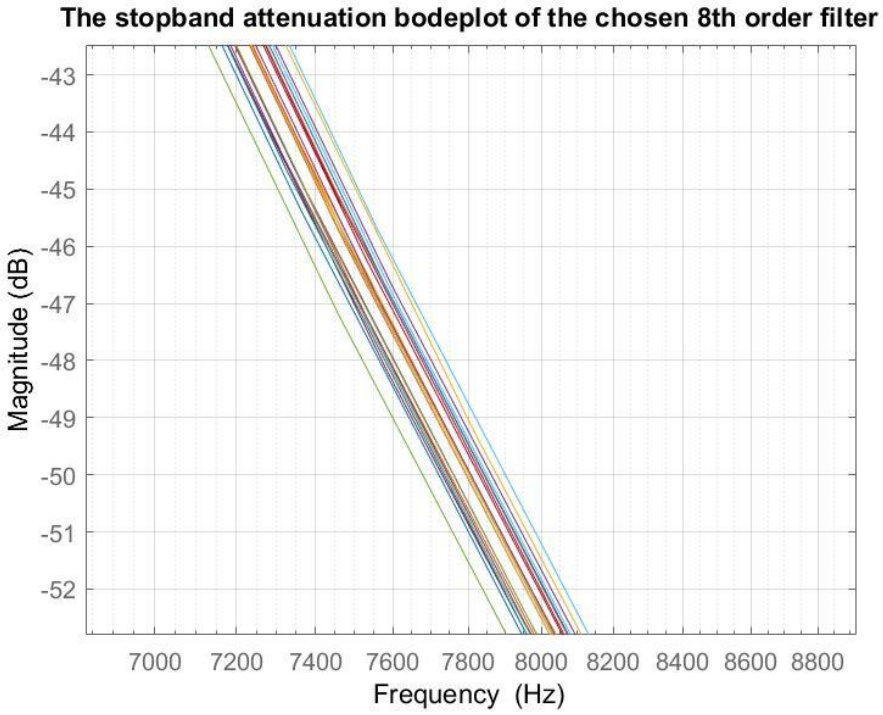


Figure 9: The magnitude of attenuation achieved, including the effects of tolerances.

Component Selection

The component values required for the design shown in figures 7 and 8 are provided. These values must be assigned to realized E12 capacitors and E24 resistors. To achieve this an excel spreadsheet was utilized to calculate the optimum corresponding E12 capacitors and E24 resistors. The results of this analysis are shown below in table 2.

Table 2: The value of capacitors and resistors deemed most optimum, the actual required to produce a perfect design, and the measured values of components used in protype design.

Filter Stage 1 (lowest Q value)			
	c2	r1	r2
Value	3.9nF	27k	120k
Required	3.89	26200	121500
Measured	3.8	26980	118430
Filter Stage 2			
	c2	r1	r2
Value	27nf	3.9k	22k
Required	29.86nf	3900	22000
Measured	28.12nf	3.84	21936
Filter Stage 3			
	c2	r1	r2
Value	150nF	1.1k	6.8k

Required	152	1130	7000
Measured	147.5nf	1.18k	6.8k
Filter Stage 4 (highest Q Value)			
	c2	r1	r2
Value	820nF	910ohm	1.1k
Required	818.66	940	1140
Measured	838nf	0.808	1.176

Therefore, the filter design stage is complete. The filter stage will be a series of four filter stages as shown in figure 4 which are the values specified in table 2. Capacitor 1 is set to 1nF and found to be accurate to less than a percent. This circuit should achieve slightly greater than 48dB attenuation at the stopband with its optimum. However due to the constraints of the tolerances of components there is a chance for the design to have greater than 3dB of gain within the passband. We deem our solution the filter design to be an optimal solution given the limiting constraints of the design specifications. Just to ensure the design did not significantly change due to these values, a simple bode plot analysis was performed on LTspice using the circuit to ensure its still meeting specifications. The circuit diagram, and critical values found are shown below.

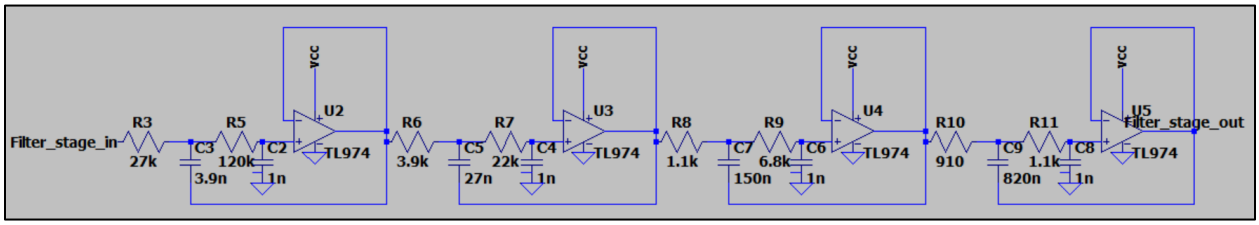


Figure 10: The filter Stage circuitry, showing the fourth separate filter stages.

```
* D:\simulation\measure.mout
Rp: PP(mag(V(Vout)))=(1.88268dB,0°) FROM 1 TO 5400
Amin: MAX(mag(V(Vout)))=(-48.2086dB,0°) FROM 7813 TO 10000
```

Figure 11: The critical values for circuit design.

Amplifier Stage

To quantify the gain required at the final amplifier stage, the maximum output from the microphone must be calculated. The average microphone peak to peak was determined via taking the average of set of individual sound samples. This was conducted over a set of 50 individual samples as seen below in table 3.

Table 3: The millivoltage measured peak to peak of the output signal of the electric condenser microphone.

Trail runs	Set 1	Set 2	Set 3	Set 4	Set 5
1	124	98	84	53	69
2	177	113	79	75	86
3	77	143	72	65	71

4	96	87	85	90	74
5	77	114	136	168	108
6	138	82	200	44	56
7	61	92	80	68	69
8	65	80	126	71	50
9	120	130	130	67	71
10	179	75	64	59	154
Total Average					95.0399
Total STD					36.867

As seen in table 3, the average voltage peak to peak produced by the microphone is 95mV. To ensure even statically anomalies will not get clipped by the TeensyBob, a safety factor of 3 standard deviations will be used. Thus, it can said, that the 99 percentile of speech will result in less than a 205mVpp out from the microphone. To reach 5 volts from peak to peak, a gain of 24.4-fold increase must be achieved within this final amplifier stage. This can be simply achieved by constructing an inverting op-amp gain circuit. An additional feature can be added to ensure the ac signal has exactly 2.5V of dc offset. This is achieved identically to the initial microphone interfacing circuitry. The same circuity will be used as shown in the dc centering circuit as shown in figure 3; however, a gain of 22-fold will be incorporated using a 10k Ω and a 120k Ω resistor. This circuit will recenter the dc around 2.5V to correct for any drift amongst the filter phase and amplify the signal to the absolute maximum of 5Vpp. The final circuit design for the DC recentering and amplifying can be seen below in figure 12.

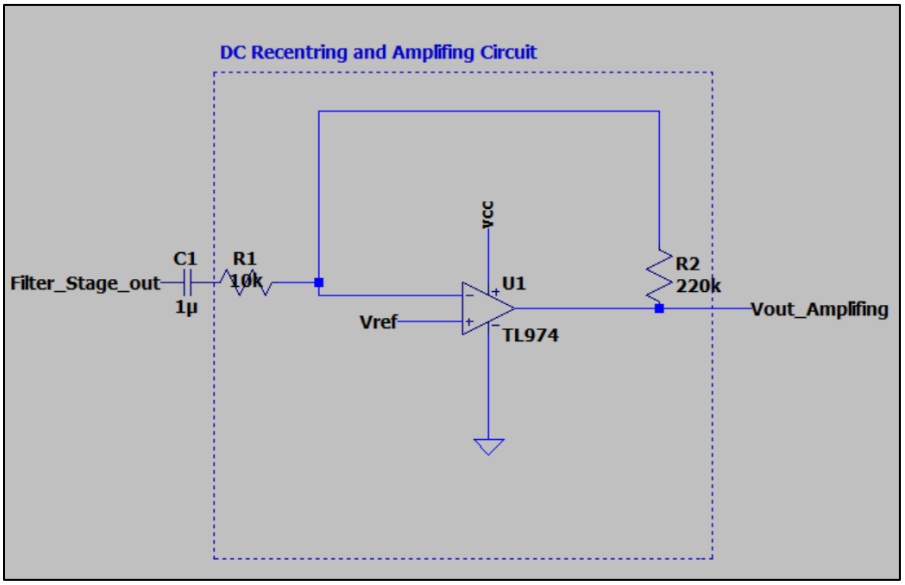


Figure 12: The final dc recentering and amplifying circuit that will interface with the Teensy board.

Total Circuit Diagram

The total circuit diagram is easily constructed by combining the three total stages to form the complete input conditioning circuitry. The total circuit schematic is shown in figure 13 below.

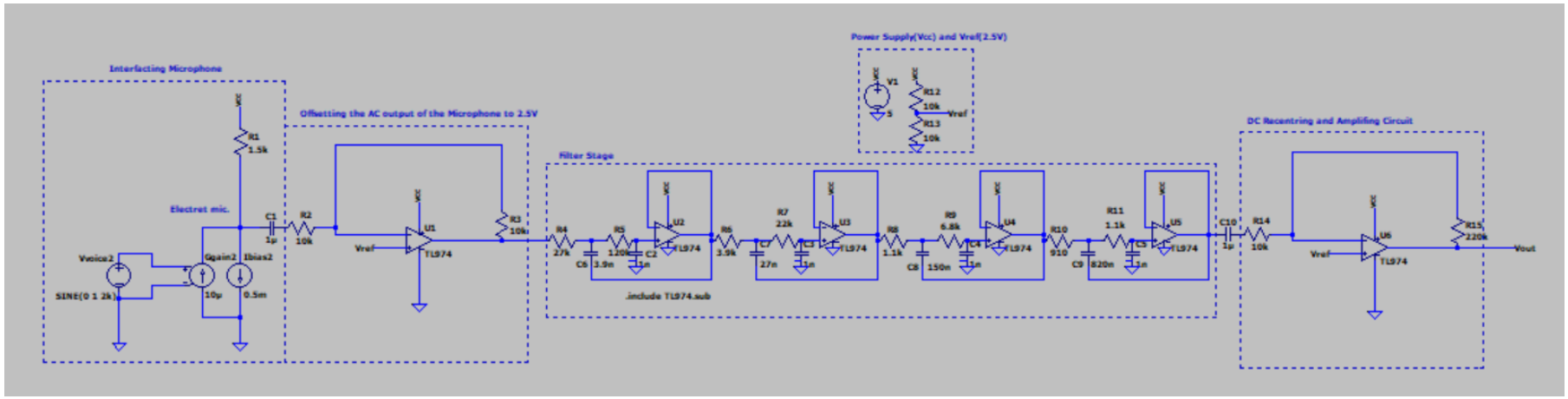


Figure 13: Complete circuit diagram for the input condition hardware

Prototyping of Design

The design was then constructed according to the circuit schematic found in figure 13. It should be noted that every component placed within the filter stage was measured and recorded table 2 as “measured values”. These measured values differ from the circuit schematic due to the tolerances of the components and thus were recorded to compare simulated data to experimental data. It should be noted that one small change was made to the microphone resistor. The 1.5KΩ was swapped to a 6.8kΩ. This has no consequential effect on the rest of the circuitry as the dc bias is immediately removed. Additionally, no iterations other changes were made to the protype circuit from the schematic.

Prototype photos

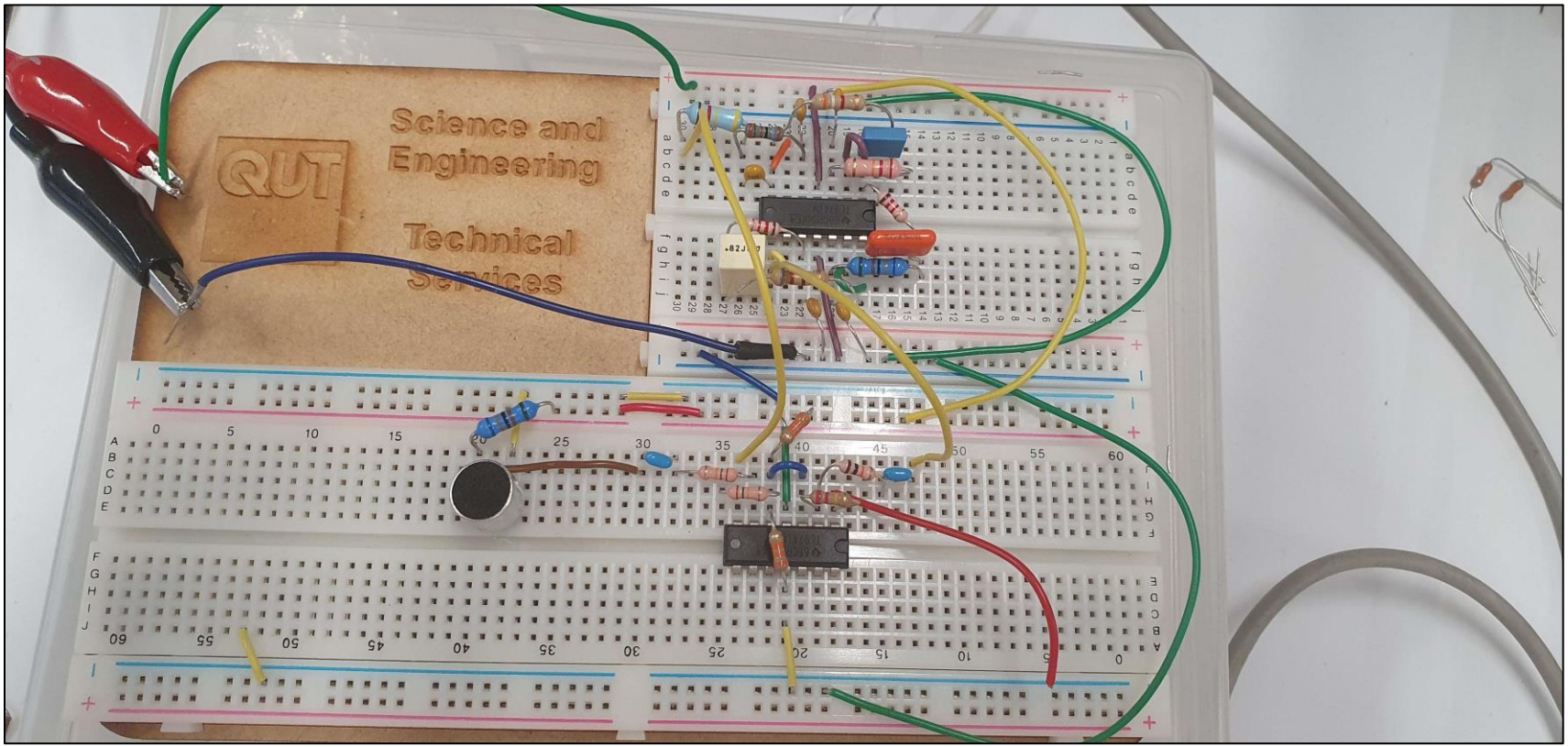


Figure 14: Completed Prototype Circuit according to the schematic in figure 13.

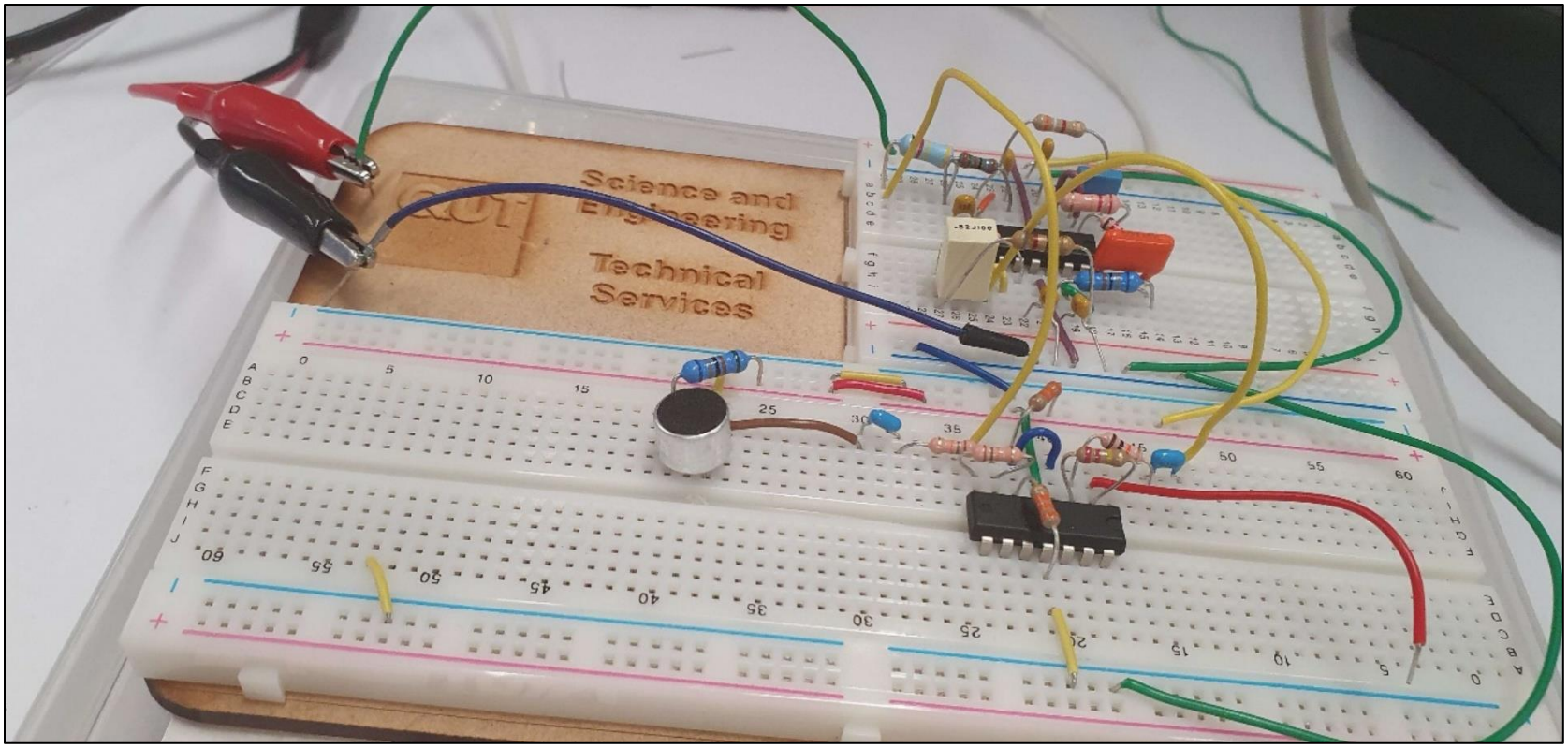


Figure 15: Another angle of the built prototype of the circuit

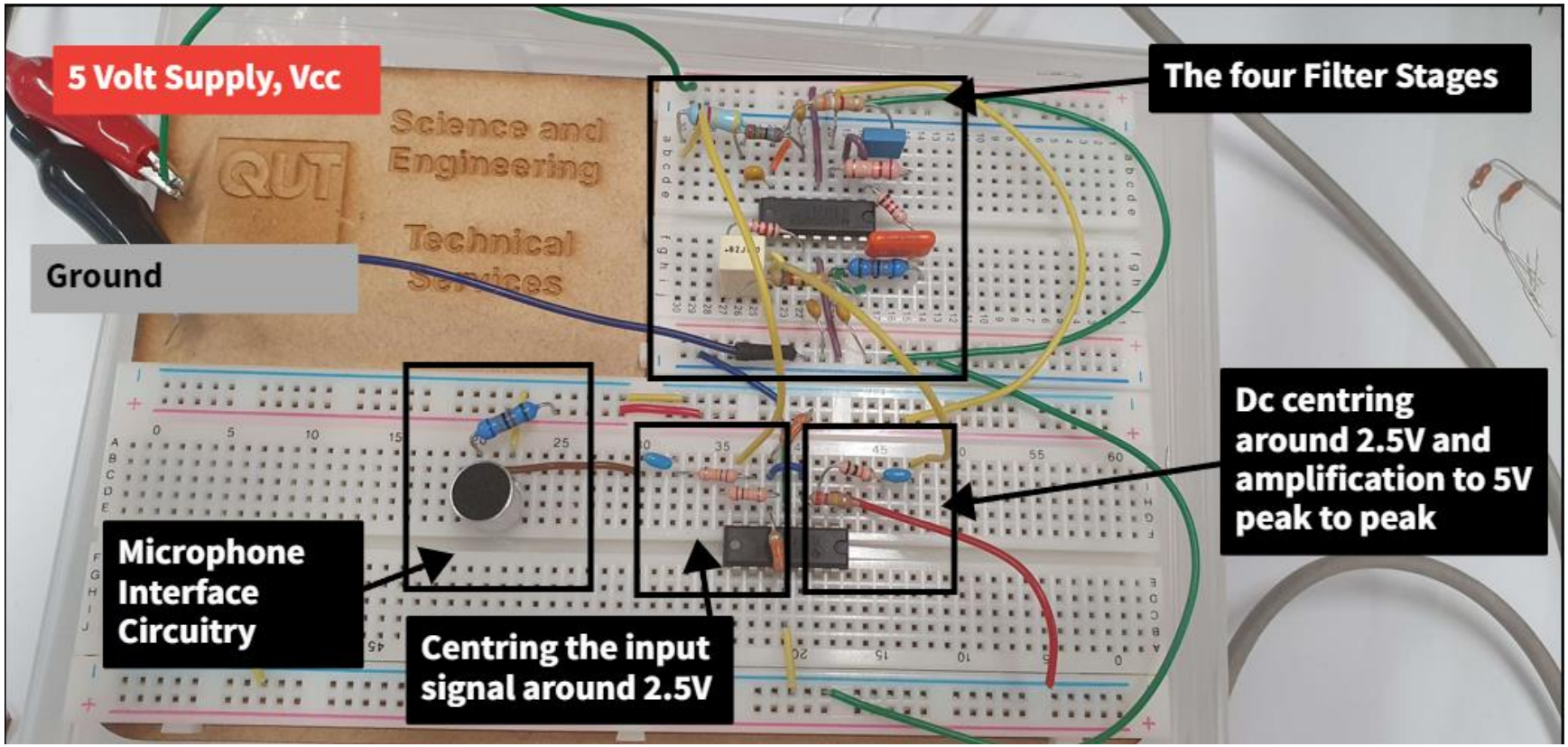


Figure 16: Annotated Realized prototype of circuitry

Simulation Results

Simulation Setup

Three individual sections are required to be analyzed, the DC offset of the microphone, the effectivity of the filter and the gain within the final amplifier stage. These circuits can be seen in figure 3,10 and 12. The net code for these circuits is provided within the appendix.

Simulation Results and Analysis

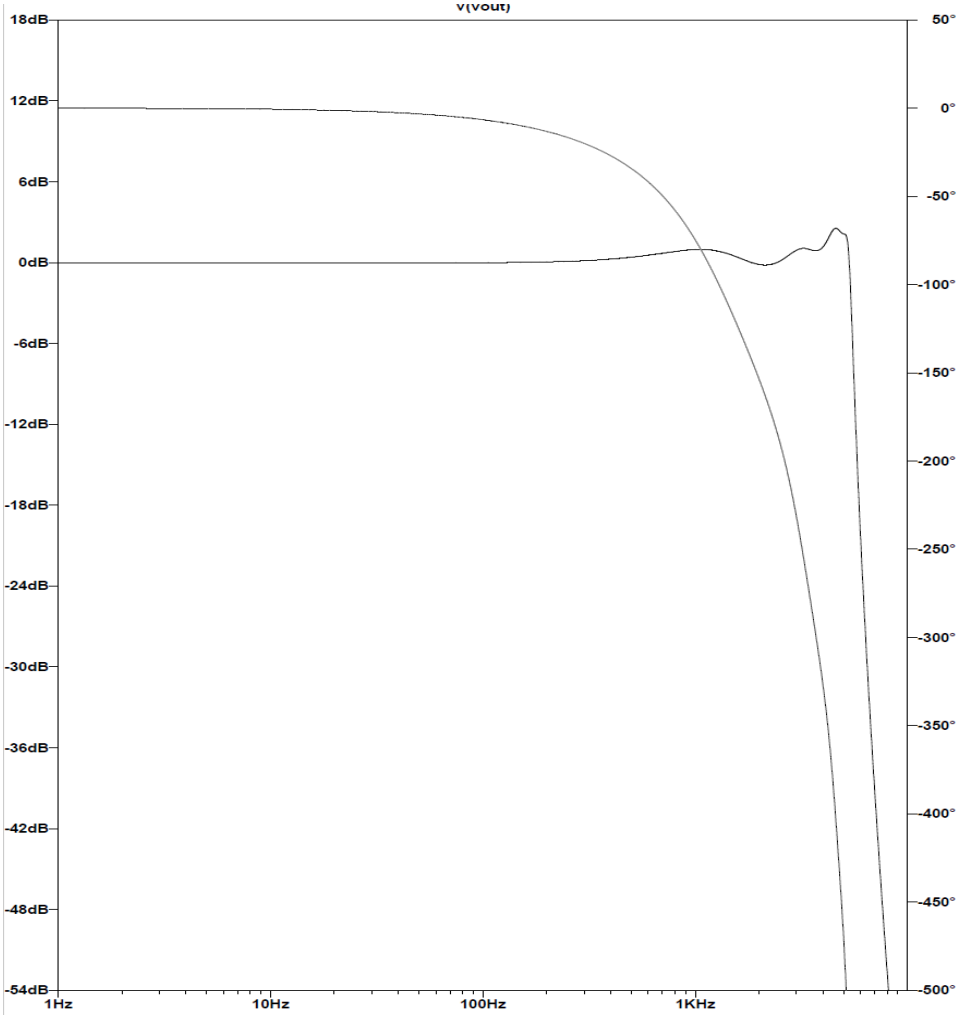


Figure 17: Bode Plot of the filter stage shown within this report

```
Rp: PP(mag(V(Vout)))=(4.92993dB,0°) FROM 1 TO 5400
Amin: MAX(mag(V(Vout)))=(-50.246dB,0°) FROM 7813 TO 10000
```

Figure 18: Maximum gain within the passband as well as the attenuation achieved at the stopband.

The filter stage's bode plot (figure17) reveals a nearly flat gain curve up to 3kHz, indicating consistent signal amplification. However, a noticeable ripple appears within the end passband. The simulated circuit shares similar parameters with the prototype circuit, suggesting that the actual filter stage's performance will align with the simulation.

Analyzing the components used, it was determined that the filter stage achieved a total gain of 4.929dB within the passband. While this gain change is noticeable, it is important to note that it occurs at frequencies beyond the critical sound profile for speech intelligibility. Therefore, the slight deviation in gain should not significantly affect speech intelligibility. However, this is not to say that this is an ideal outcome from the design. This is caused because of component tolerance. A similar effect should be seen within the experimental results of this report.

Looking at figure 18, the Amin requirement of greater than 48 dB of attention was achieved. This means the circuitry effectively prevents anti-antialiasing. Overall, the filter stage demonstrates satisfactory performance, providing effective signal amplification within the desired frequency range, despite the observed ripple in the passband.

```
GainDB: MAX(mag(V(Vout)))=(26.6519dB,0°) FROM 1 TO 10000
```

Figure 19: Maximum gain achieved by the final amplifier circuit seen in figure 12.

Figure 19 shows the simulated results of the gain achieved by the final amplifier circuit. It is shown to be 26.651dB. This corresponds to a linear increase by a factor of 21.5 from the input to the output of this circuit. With a maximum input signal of 0.205Vpp, this causes the circuit to be 4.407Vpp after the final amplifier stage.

Experimental Results

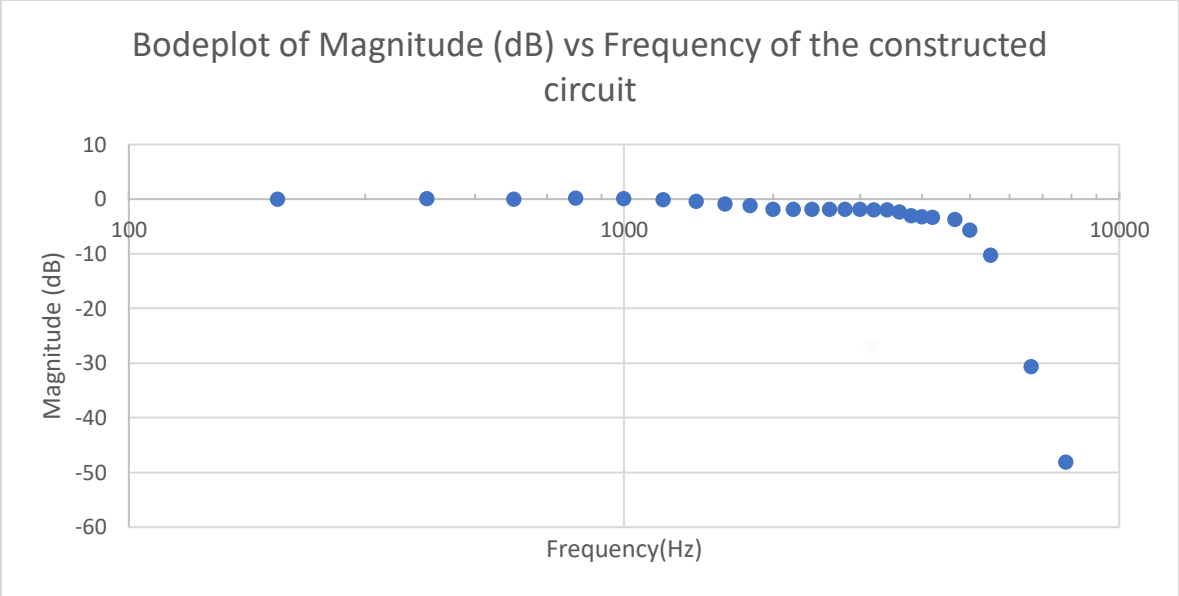


Figure 20: The calculated Bode plot using gain calculated at 26 individual points.

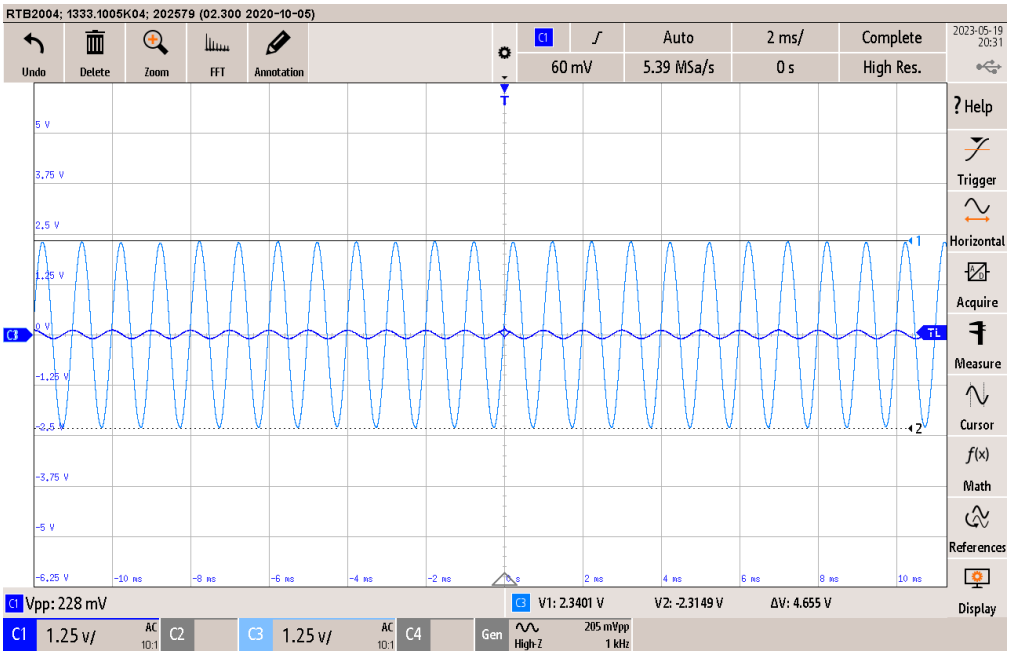


Figure 21: The input signal getting raised to the 5Vpp required to supply Teensy Board and maximum 205mVpp microphone output.

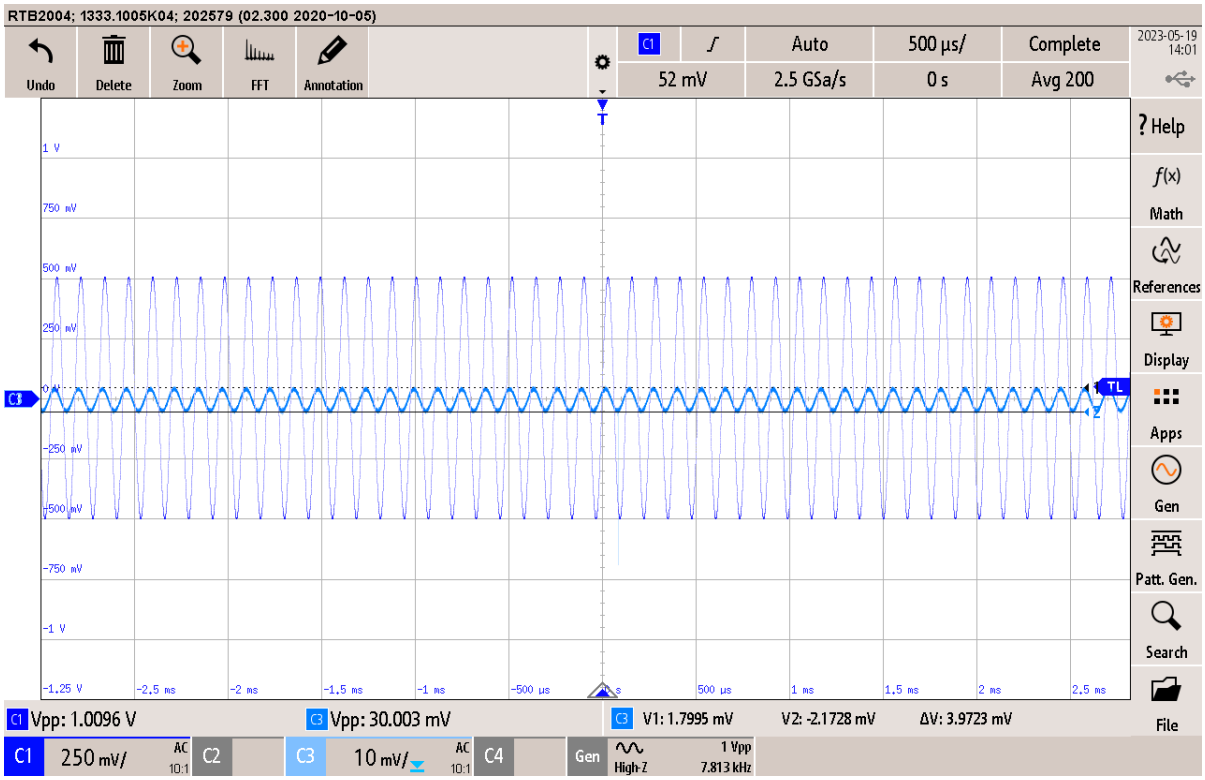


Figure 22: The attenuation achieved at the stopband frequency 7.8kHz (dark blue scalded at 250mV), light blue scale shown(10mV).

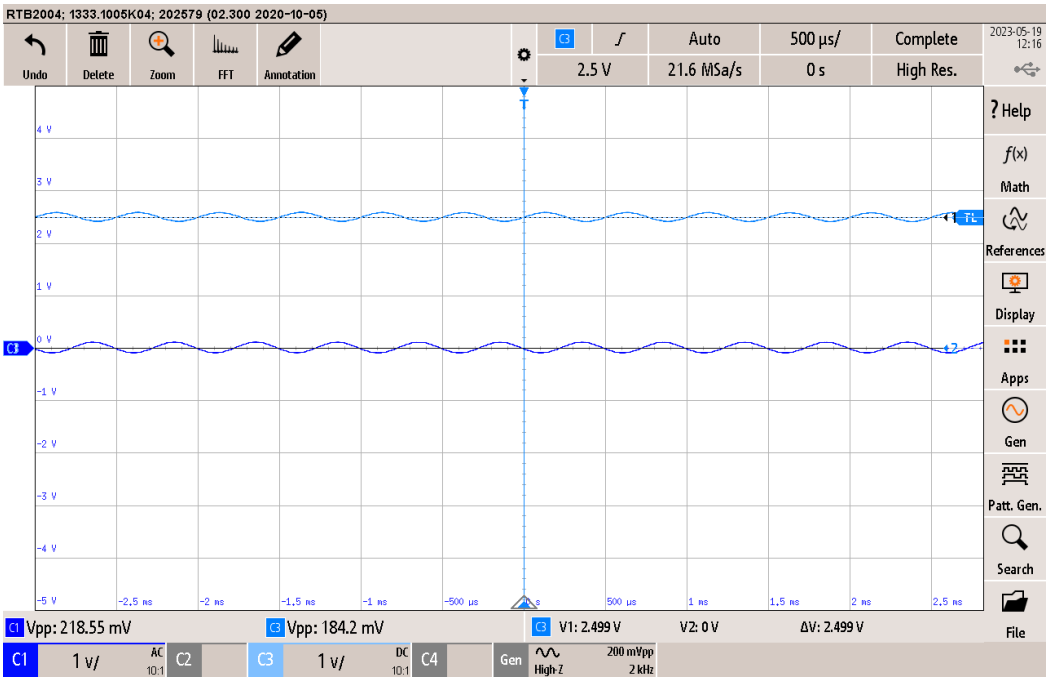


Figure 23: The input signal (AC coupled) and the output of the DC offset circuitry with the microphone interfacing stage.

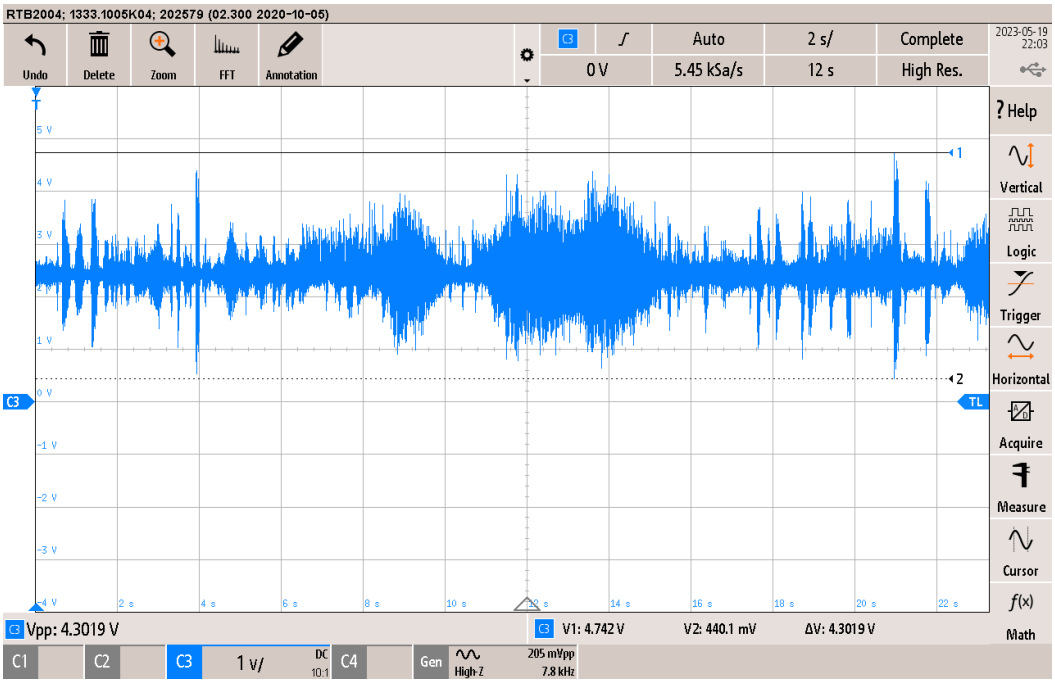


Figure 24: The entire circuit with audio playing into the microphone, the output that will be interfaced by the Teensyboard.

Results Analysis

The results collected seem to display many critical functions of the design. Figure 20 shows the overall effect of the filter stage and demonstrates its ability to attenuate at higher frequencies. Figure 21 specifically shows the absolute maximum peak to peak voltage through the filter and amplifier stage of the circuit. Figure 23 directly highlights the attenuation achieved at 7.813kHz. Figure 24 demonstrates the added dc off-set to the unaffected microphone signal.

DVR system's circuit implementation is evident from its operation stages. This is because all stages are in operational order. The maximum peak to peak attenuation at the passband was found to be 5.7 dB at the ripple. Figure 20 shows the distortion of frequencies from the range of 2kHz to 5.4kHz. This is not ideal for a high-quality audio recording system.

The amplifier circuitry performed highly as it was able to provide a maximum 4.6Vpp without clipping anywhere amongst. This can be confirmed by as a 1kHz a relatively peak is seen in within the bode plot of figure 20. The output signal was perfected centered on 2.499V.

The attenuation achieved by the filter was found to be effective. The 2030mV source was attenuated down to 9.737mv. This means the source was attenuated by:

$$20 * \left|\log_{10} \frac{1009.6}{3.972}\right| = 48.2dB$$

This means the filter will successfully ensure no antialiasing will occur from the Teensy board. Another part of the circuit that was successfully implemented was the microphone interfacing. As seen in figure 23, where the signal is offset but not distorted. The amplification of the overall circuit seems to be well set at it achieves close to 5Vpp however does not clip as shown in figure 24.

Evaluation

The analysis from the circuit simulations and experiments are similar. Both the simulated circuit and tested circuit have a maximum ripple in the bandpass of approximately 5dB. It can also be seen that figures 17 and 20 have an increased ripple at the passband when compared to the ideal values within figures 7 and 8. The figures both have large ripples at starting at 2kHz and extending to the edge of the stopband. This is due to inaccuracies in resistor and capacitor tolerances.

The simulated results of the dB gain of the found that a gain of 26.5dB should be achieved through this final stage. Within the prototype design this was calculated to be $20 * \left|\log_{10} \frac{4655}{228}\right| = 26.2dB$. For the final stage three of the input conditioning circuitry, was very similar to the simulated results.

Performance Evaluation against Design Specifications

The design constructed was able to achieve most of the design specifications set. The design was able to be audio out was able to offset at close to 2.5V and have maximum peak to peak output voltage close to 5V. it successfully attenuated a minion of 48.16dB from the peak seen within the bandwidth. The design was ability to be made with E12 capacitors, E24 resistors, Cma-6542TF-K microphone and the Tl974 op amps However, the design to deliver on the most important design goal which was to ensure a peak-to-peak dB width of less than 3dB achieving a result of 5.7dB for the prototype design. This was the result of the massive limitations set within this project.

Limitations

The two most restricting limitations that reduce the efficacy of the design were the very wide tolerance of resistors and the sampling rate of the TeensyboBv2 board. This significantly limited the capabilities of the design in which was able to be achieved.

The largest limitation was the inaccuracy of resistors. It was found that even with capacitors tolerances low, the resistor tolerances played a crucial role in the accuracy of the filter stage. To improve upon this limitation by either using potentiometers or lower tolerance resistors. The design would be significantly improved at the ripple at the stopband would be significantly reduced.

Another limitation identified was the relatively slow sampling rate of 15.625kHz. According to the Nyquist–Shannon sampling theorem even a perfect filter, an absolute maximum passband frequency would be 7812kHz. This is to ensure that anti-aliasing doesn't occur. Because perfect filters don't exist, this either pushes the cutoff frequency away from this 7812kHz or requires increased filter complexity to provide a sharper roll of frequency.

Another limitation of the report was the required use of ceramic capacitors. Ceramic capacitors are not ideal in frequency-based applications due to their sensitivity of vibrations. However due to the limited supply of available film capacitors it was decided to reduce overall circuit complexity by using ceramic capacitors.

Conclusion

The objective of this project report was to construct input conditioning circuitry that would enable the Teensy board to effectively process the signal. While several aspects of the design specifications were successfully achieved, the limitations imposed by capacitor and resistor tolerances prevented the production of a high-quality audio recording sound software. Therefore, further investigations should be conducted to explore the potential benefits of utilizing potentiometers calibrated to the ideal resistance or employing higher tolerance resistors. These measures could potentially minimize the gain variation within the passband near the cutoff frequency.

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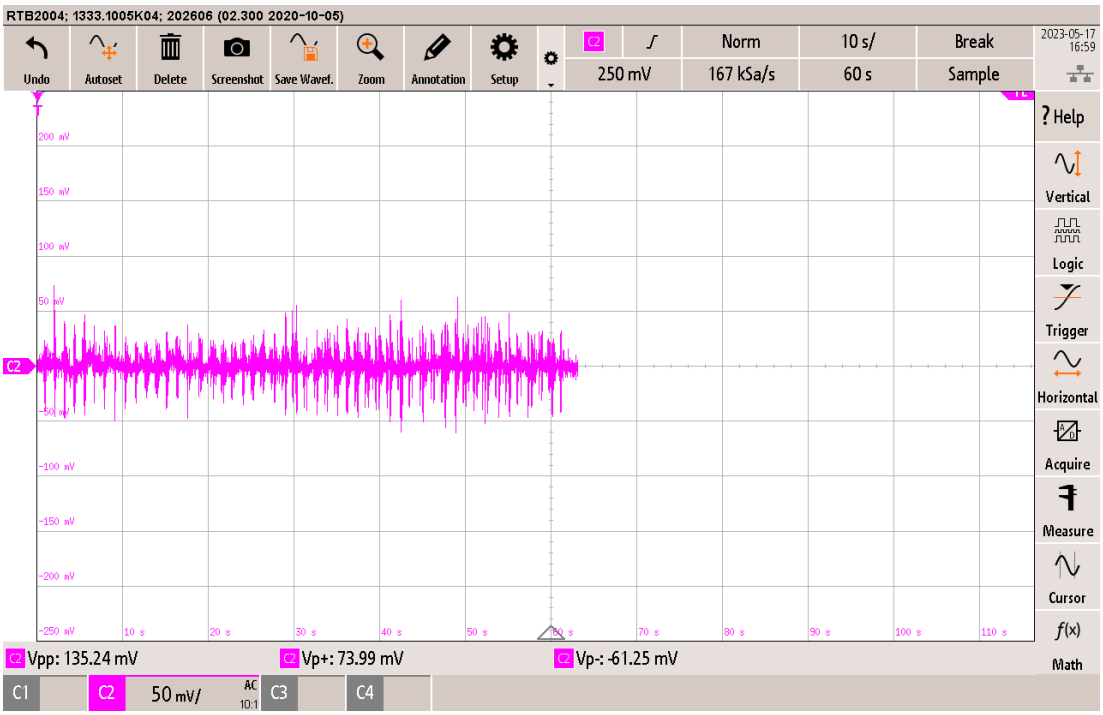
Appendices



Appendix 1: Microphone output, Peak to Peak voltage, identified counting 1 to 50 with 1.5KΩ resistor and 1µF capcitor.

```
n_butt =

    55


wn_butt =

   4.4380e+04


nchev =

    14


wnchev =

   4.3982e+04

>>
```

```
%Initilisation
fsamp = 15625;
fs=fsamp/2;
fp=7000; % Passband Frequency
ws=2*pi*fs; %Frequency to angular velocity
wp=2*pi*fp; %Frequency to angular velocity
amin= 48.16; %Required attentuation at stopband
amax=1.5; %Maximum attentuation in the passband

[n_butt, wn_butt]=buttord(wp,ws,amax,amin,"s") %Calculate required order to meet spec
[nchev, wnchev] = cheb1ord(wp,ws,amax,amin,'s') %Calculate required order to meet spec
```

Appendix 2: Initial MATLAB calculates to determine the order of Sallen-Key topography active filters to achieve specifications.

```
nchev =

     8


wnchev =

   3.5500e+04

>>
```

```
1   %Initilisation
2   fsamp = 15625;
3   fs=fsamp/2;
4   fp=5650; % Passband Frequency
5   ws=2*pi*fs; %Frequency to angular velocity
6   wp=2*pi*fp; %Frequency to angular velocity
7   amin= 48.16; %Required attentuation at stopband
8   amax=1.5; %Maximum attentuation in the passband
9
10  [nchev, wnchev] = cheb1ord(wp,ws,amax,amin,'s') %Calculate required order to meet spec
```

Appendix 3: The maximum low pass frequency cutoff to achieve an 8th order design. (fp =5650)

```
nchev =

     6


wnchev =

   2.8588e+04

>>
```

```
1   %Initilisation
2   fsamp = 15625;
3   fs=fsamp/2;
4   fp=4550; % Passband Frequency
5   ws=2*pi*fs; %Frequency to angular velocity
6   wp=2*pi*fp; %Frequency to angular velocity
7   amin= 48.16; %Required attentuation at stopband
8   amax=1.5; %Maximum attentuation in the passband
9
10  [nchev, wnchev] = cheb1ord(wp,ws,amax,amin,'s') %Calculate required order to meet spec
```

Appendix 4: The maximum low pass frequency cutoff to achieve a 6th order design. (fp =4550)

```
nchev =

     4


wnchev =

   1.7593e+04

>>
```

```
1   %Initilisation
2   fsamp = 15625;
3   fs=fsamp/2;
4   fp=2800; % Passband Frequency
5   ws=2*pi*fs; %Frequency to angular velocity
6   wp=2*pi*fp; %Frequency to angular velocity
7   amin= 48.16; %Required attentuation at stopband
8   amax=1.5; %Maximum attentuation in the passband
9
10  [nchev, wnchev] = cheb1ord(wp,ws,amax,amin,'s') %Calculate required order to meet spec
```

Appendix 5: The maximum low pass frequency cutoff to achieve a 4th order design.(fp = 2800)

```
nchev =

    10


wnchev =

   3.9741e+04

>>
```

```
1   %Initilisation
2   fsamp = 15625;
3   fs=fsamp/2;
4   fp=6325; % Passband Frequency
5   ws=2*pi*fs; %Frequency to angular velocity
6   wp=2*pi*fp; %Frequency to angular velocity
7   amin= 48.16; %Required attentuation at stopband
8   amax=1.5; %Maximum attentuation in the passband
9
10  [nchev, wnchev] = cheb1ord(wp,ws,amax,amin,'s') %Calculate required order to meet spec
```

Appendix 6: The maximum low pass frequency cutoff to achieve a 10th order design.(fp = 6350)

```
nchev =

    12


wnchev =

   4.2254e+04

>>
```

```
%Initilisation
fsamp = 15625;
fs=fsamp/2;
fp=6725; % Passband Frequency
ws=2*pi*fs; %Frequency to angular velocity
wp=2*pi*fp; %Frequency to angular velocity
amin= 48.16; %Required attentuation at stopband
amax=1.5; %Maximum attentuation in the passband

[nchev, wnchev] = cheb1ord(wp,ws,amax,amin,'s') %Calculate required order to meet spec
```

Appendix 7: The maximum frequency passband cutoff to achieve a 12th order design(fp = 6725)

```
function [r1, r2, c1, c2,Q,wn] = polestovalues(p1, p2)
%  POLESTOVALUES Turns poles given by the cheby1 function into released
% resistor and capcitor values as well as the damping ratio and natural
% frequency
a1 = -p1-p2;
a2 = p1*p2;
wn = sqrt(a2);
Q = wn/a1;
n = (2*Q)^2;
c1 = 1e-9;
c2 = n*c1;
r1 = 1/(wn * c1 * sqrt(n));
r2 = r1;
end
```

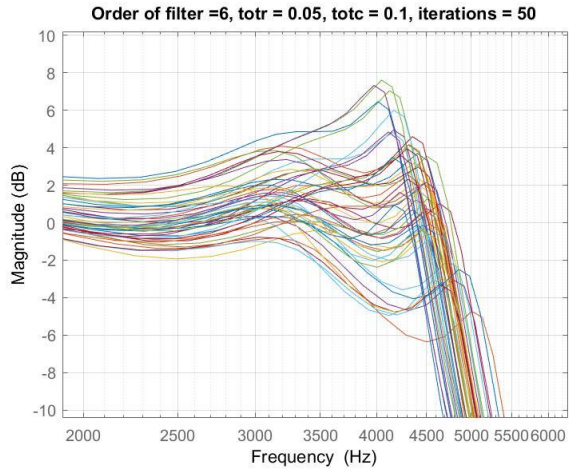
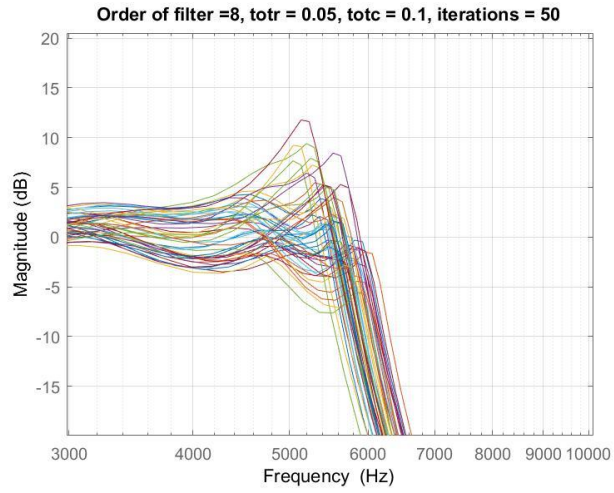
Appendix 8: MATLAB function to turn polestovalues given two poles, assumes c1 = 1nF and returns the 4 values required to release that transfer function in real life.

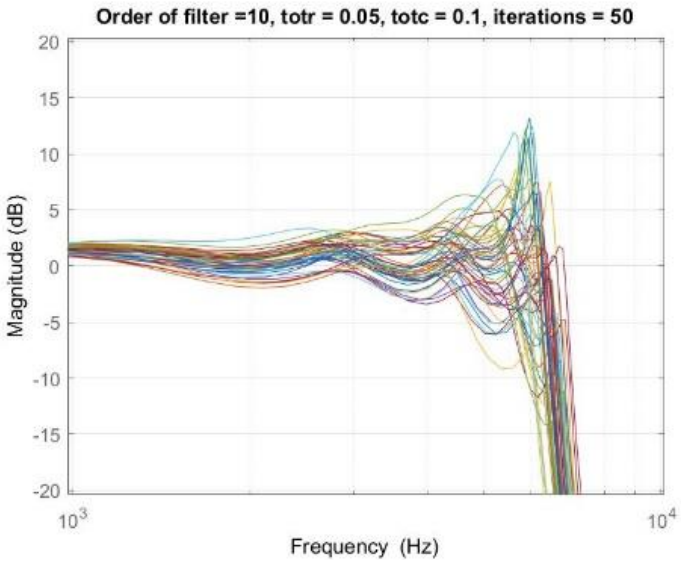
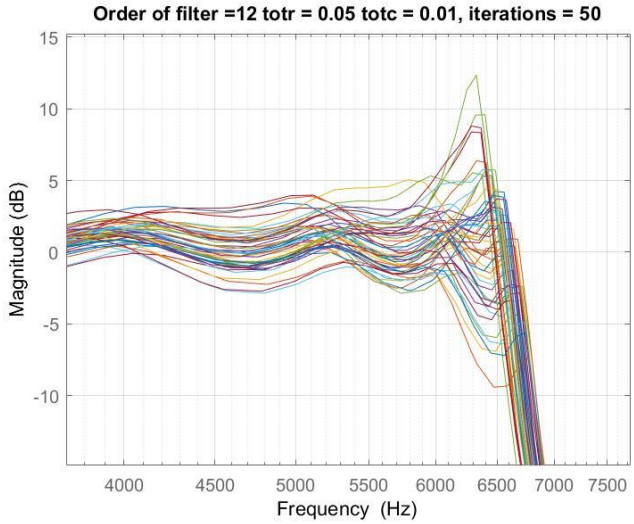
```
function HtestA = valuestotransfer(R1A, R2A, C1A,C2A)
%  VALUESTOTRANSFER This turns values into a transfer function that can thenbe ploted in matlab
K1test = 1;
numA = [0 0 K1test/(R1A*R2A*C1A*C2A)];                                          % numerator
denA = [1 (1/(R1A*C2A) + 1/(R2A*C2A) + (1-K1test)/(R2A*C1A)) 1/(R1A*R2A*C1A*C2A)];    % denominator
HtestA = tf(numA,denA);
end
```

Appendix 9: MATLAB function to turn actual values into a transfer function which can be visualized within MATLAB.

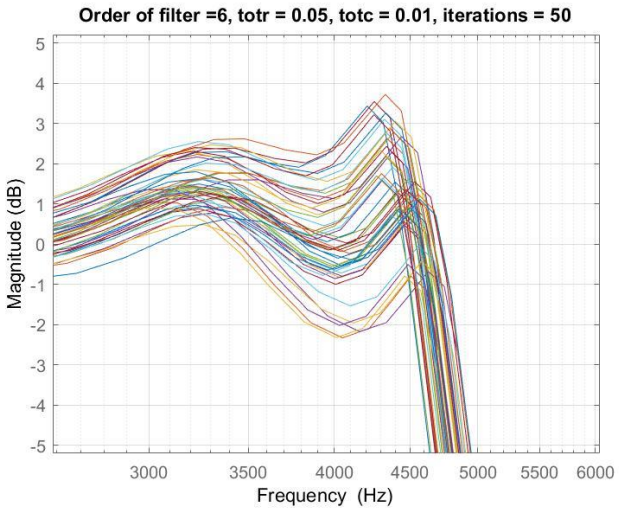
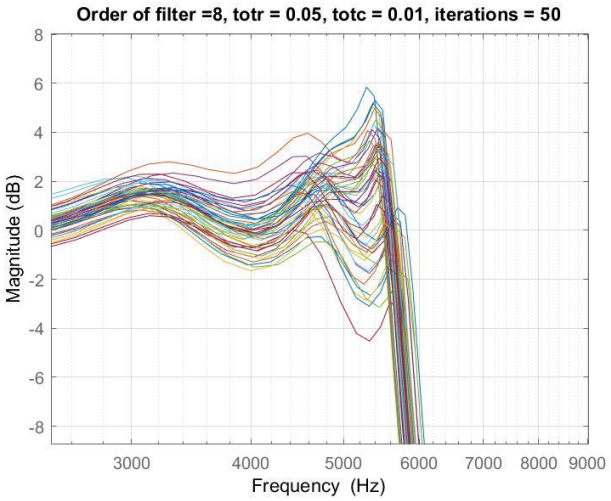
```
%Initilisation
fsamp = 15625;
fs=fsamp/2;
fp=6200; % Passband Frequency
ws=2*pi*fs; %Frequency to angular velocity
wp=2*pi*fp; %Frequency to angular velocity
amin= 49; %Required attentuation at stopband
amax=1; %Maximum attentuation in the passband
itn=50; %Number of iterations to run tolerance testing on
totr=0.04;
totc1=0.01;
totc2=0.01;
allbodes=[]
[nchev, wnchev] = cheblord(wp,ws,amax,amin,'s') %Calculate required order to meet spec
[z,p,k] = cheby1(nchev,amax,wnchev,"low",'s'); %Calculate poles
% Turn the calculated poles into circuit values
lenp= length(p)
if rem(lenp,2)==1;
    error('Code only deals with even filter orders')
end
 if lenp>=2 % Set the appropriate amount of poles to values
[r1A,r2A,c1A,c2A,Q1,WnA]=polestovalues(p(1),p(2))
 end
 if lenp >= 4
[r1B,r2B,c1B,c2B,Q2,WnB]=polestovalues(p(3),p(4))
 end
 if lenp >=6
[r1C,r2C,c1C,c2C,Q3,WnC]=polestovalues(p(5),p(6))
 end
 if lenp >=8
[r1D,r2D,c1D,c2D,Q4,WnD]=polestovalues(p(7),p(8))
 end
 if lenp>=10
[r1E,r2E,c1E,c2E,Q5,WnE]=polestovalues(p(9),p(10))
 end
 if lenp>=12
[r1F,r2F,c1F,c2F,Q6,WnF]=polestovalues(p(11),p(12))
 end
hold off

for i = 1:itn % No time to trip code, code is determining the transfer function at incorporating randomised tolerances values.
    a=rand([1 24]);
    ab=(randn([1 24])>0)*-2;
    ab = ab+1;
    a=a.*ab;
    if lenp==2
    A=valuestotransfer(r1A+r1A*totr*a(1),r2A+r2A*totr*a(2),c1A+c1A*totc1*a(3),(c2A) +(c2A)*totc2*a(4));
    Htest = A;
    allbodes = [allbodes, Htest];
    elseif lenp==4
    A=valuestotransfer(r1A+r1A*totr*a(1),r2A+r2A*totr*a(2),c1A+c1A*totc1*a(3),(c2A) +(c2A)*totc2*a(4));
    B=valuestotransfer(r1B+r1B*totr*a(5),r2B+r2B*totr*a(6),c1B+c1A*totc1*a(7),(c2B) +(c2B)*totc2*a(8));
    Htest = A*B;
    allbodes = [allbodes, Htest];
    elseif lenp==6
    A=valuestotransfer(r1A+r1A*totr*a(1),r2A+r2A*totr*a(2),c1A+c1A*totc1*a(3),(c2A) +(c2A)*totc2*a(4));
    B=valuestotransfer(r1B+r1B*totr*a(5),r2B+r2B*totr*a(6),c1B+c1A*totc1*a(7),(c2B) +(c2B)*totc2*a(8));
    C=valuestotransfer(r1C+r1C*totr*a(9),r2C+r2C*totr*a(10),c1C+c1A*totc1*a(11),(c2C) +(c2C)*totc2*a(12));
    Htest = A*B*C;
    allbodes = [allbodes, Htest];
    elseif lenp==8
    A=valuestotransfer(r1A+r1A*totr*a(1),r2A+r2A*totr*a(2),c1A+c1A*totc1*a(3),(c2A) +(c2A)*totc2*a(4));
    B=valuestotransfer(r1B+r1B*totr*a(5),r2B+r2B*totr*a(6),c1B+c1A*totc1*a(7),(c2B) +(c2B)*totc2*a(8));
    C=valuestotransfer(r1C+r1C*totr*a(9),r2C+r2C*totr*a(10),c1C+c1A*totc1*a(11),(c2C) +(c2C)*totc2*a(12));
    D=valuestotransfer(r1D+r1D*totr*a(13),r2D+r2D*totr*a(14),c1D+c1A*totc1*a(15),(c2D) +(c2D)*totc2*a(16));
    Htest = A*B*C*D;
    allbodes = [allbodes, Htest];
    elseif lenp==10
    A=valuestotransfer(r1A+r1A*totr*a(1),r2A+r2A*totr*a(2),c1A+c1A*totc1*a(3),(c2A) +(c2A)*totc2*a(4));
    B=valuestotransfer(r1B+r1B*totr*a(5),r2B+r2B*totr*a(6),c1B+c1A*totc1*a(7),(c2B) +(c2B)*totc2*a(8));
    C=valuestotransfer(r1C+r1C*totr*a(9),r2C+r2C*totr*a(10),c1C+c1A*totc1*a(11),(c2C) +(c2C)*totc2*a(12));
    D=valuestotransfer(r1D+r3D*totr*a(13),r2D+r2D*totr*a(14),c1D+c1A*totc1*a(15),(c2D) +(c2D)*totc2*a(16));
    E=valuestotransfer(r1E+r1E*totr*a(17),r2E+r2E*totr*a(18),c1E+c1E*totc1*a(19),(c2E) +(c2E)*totc2*a(20));
    Htest = A*B*C*D*E;
    allbodes = [allbodes, Htest];
    elseif lenp==12
    A=valuestotransfer(r1A+r1A*totr*a(1),r2A+r2A*totr*a(2),c1A+c1A*totc1*a(3),(c2A) +(c2A)*totc2*a(4));
    B=valuestotransfer(r1B+r1B*totr*a(5),r2B+r2B*totr*a(6),c1B+c1A*totc1*a(7),(c2B) +(c2B)*totc2*a(8));
    C=valuestotransfer(r1C+r1C*totr*a(9),r2C+r2C*totr*a(10),c1C+c1A*totc1*a(11),(c2C) +(c2C)*totc2*a(12));
    D=valuestotransfer(r1D+r1D*totr*a(13),r2D+r2D*totr*a(14),c1D+c1A*totc1*a(15),(c2D) +(c2D)*totc2*a(16));
    E=valuestotransfer(r1E+r1E*totr*a(17),r2E+r2E*totr*a(18),c1E+c1E*totc1*a(19),(c2E) +(c2E)*totc2*a(20));
    F=valuestotransfer(r1F+r1F*totr*a(21),r2F+r2F*totr*a(22),c1F+c1F*totc1*a(23),(c2F) +(c2F)*totc2*a(24));
    Htest = A*B*C*D*E*F;
    allbodes = [allbodes, Htest];
    end
end
figure('Visible','on')
for i=1:itn
    h=bodeplot(allbodes(1,i));
    hold on
end                                 % display bode plot
setoptions(h,'FreqUnits','Hz');                     % change units to Hz
setoptions(h,'FreqUnits','Hz','PhaseVisible','off');  % remove phase plot
grid on;
title(append('Order of filter =',num2str(lenp),' totr = ' ,num2str(0.05),' totc = ',num2str(totc2), ', iterations = ', num2str(itn)))
hold off;
```

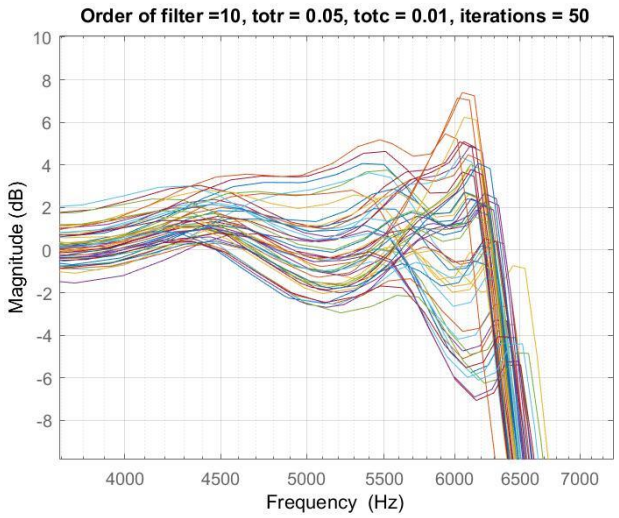
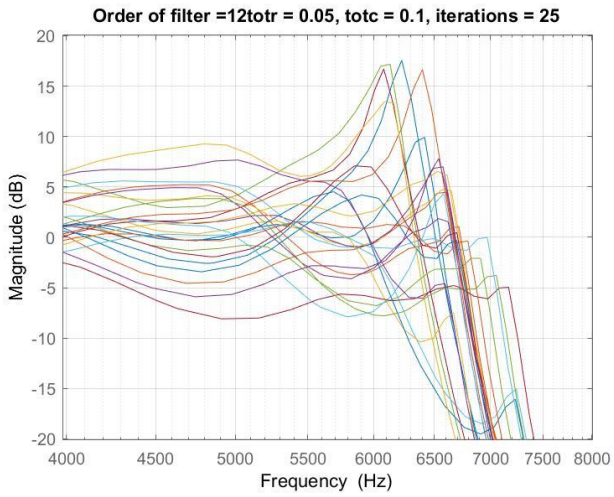
Appendix 10: Raw code that was used to generate figure to estimate tolerance issues.

Potential orders to be chosen	Bode plots for a range of tolerance values, test conditions 1 Expected conditions: Amax = amin, totr = 0.05, totc1, totc2 = 0.1, amin=48.16
6th order Conditions	
8th order	

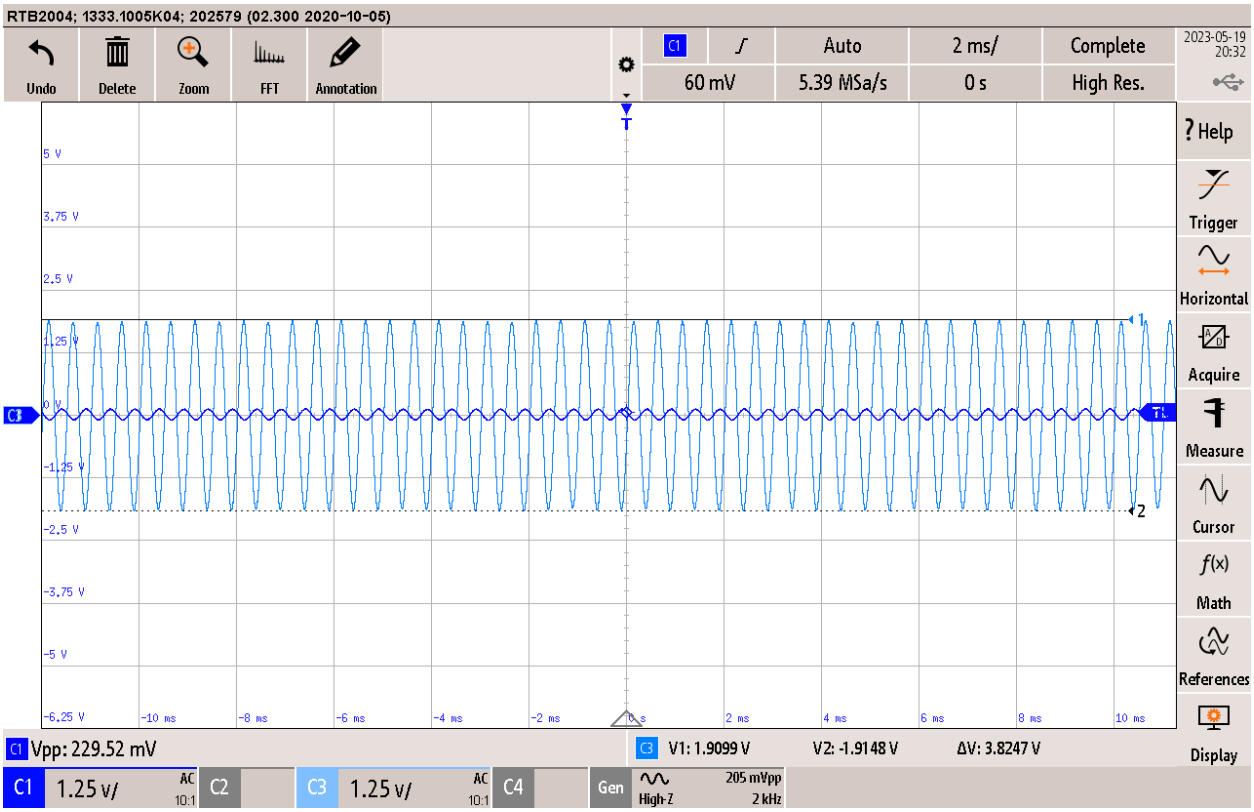
10th order	
12th order	

Appendix 11: The bode plots of 6 to 12 order filters including the effects of E12 capacitor tolerances and E24 resistor tolerances.

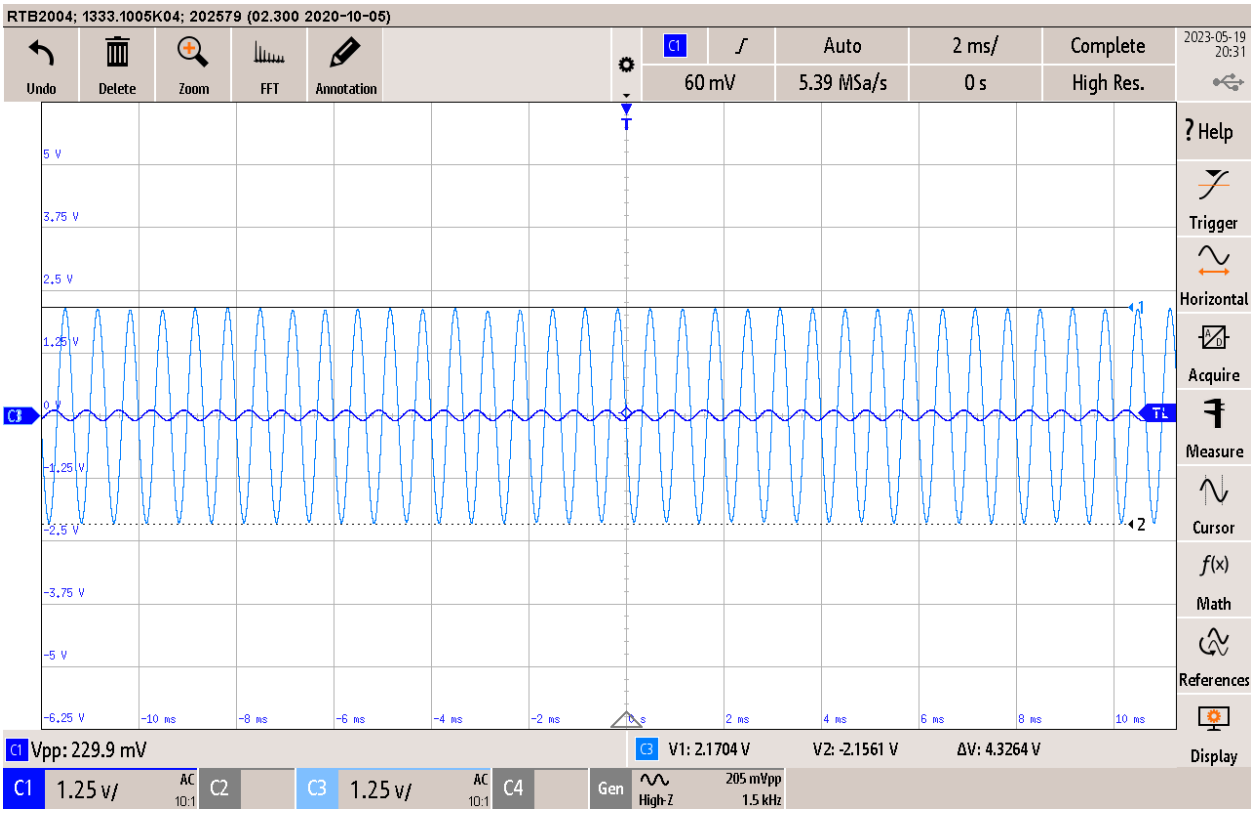
Potential orders to be chosen	Bode plots for a range of tolerance values, Test conditions 2 Expected conditions however capacitor tolerances reduced Totc1=0.01, totc2=0.01
6th order	
8th order	

10th order	
12th order	

Appendix 12: Bode plots for reduce range of capacitor values for 6th to 12th order filters.



Appendix 13: Full microphone circuit tested at 2kHz



Appendix 14: Full microphone circuit tested at 1.5kHz

```
XU1 N002 N001 vcc 0 Vout
TL974
R2 N001 Vout 220k
R1 N001 P001 10k
C1 P001 Vin 1µ
V1 Vin 0 SINE(2.5 95mV 2k)
AC 1 0
V2 vcc 0 5
R3 N002 0 10k
R4 N002 vcc 10k
.include TL974.sub
.ac dec 1000 1 10000
;tran 0 15m 0
* DC Recentring and
Amplifing Circuit
.backanno
.end
```

Appendix 15: Net code required for the LT spice model in figure 12.

```
R4 N005 N004 26980
R5 N006 N005 118430
XU2 N006 N001 vcc 0 N001 TL974
C2 N006 0 1n
C6 N005 N001 3.8n
R6 N007 N001 3.84k
R7 N008 N007 21936
XU3 N008 N002 vcc 0 N002 TL974
C3 N008 0 1n
C7 N007 N002 28.12n
R8 N009 N002 1.18k
R9 N010 N009 6.8k
XU4 N010 N003 vcc 0 N003 TL974
C4 N010 0 1n
C8 N009 N003 147.5n
R10 N011 N003 940
R11 N012 N011 1140
XU5 N012 Vout vcc 0 Vout TL974
C5 N012 0 1n
C9 N011 Vout 838n
R12 vcc Vref 10k
R13 Vref 0 10k
V1 vcc 0 5
V2 N004 0 SINE(2.5 205m 2k) AC 1 0
.include TL974.sub
* Filter Stage
* Power Supply(Vcc) and Vref(2.5V)
.ac dec 1000 1 10k
.MEAS AC Rp PP mag(V(Vout)) TO 5400
.MEAS AC Amin MAX mag(V(Vout)) FROM 7813
.backanno
.end
```

Appendix 16: Net code required for Figure 10 circuit.