

Week 2 Application Assignment: Mission 004

Overview

The goal of this assignment is learn how to use the Quartus Prime tool to create an example design. The student should be following the video instructions and creating the example as they go along. Their progress is checked at milestones by presenting screenshots which are matched to the solution screenshots to verify their work. Milestones checked are design schematic creation, design compilation, RTL viewing, timing analysis and simulation.

This assignment is required. Peers must review 3 submissions to pass the assignment.

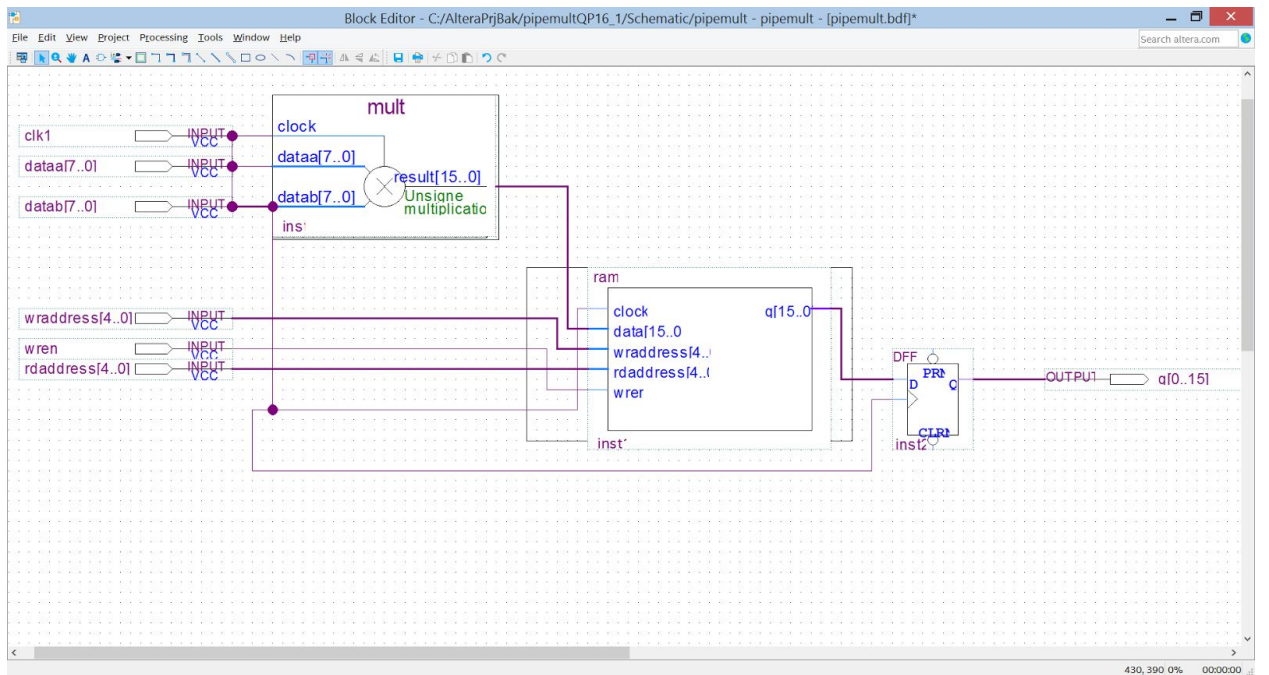
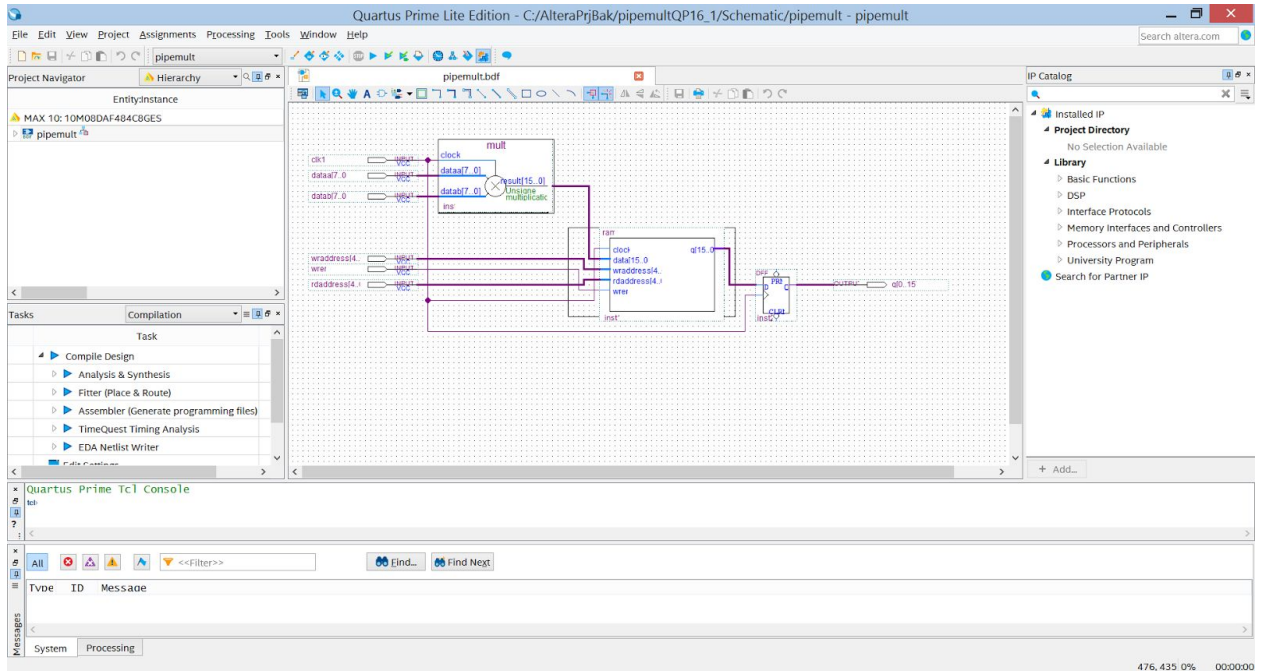
Submit screenshots (Format: .jpg) of:

- 1) The completed pipemult schematic after Video #6
- 2) The Compilation Report after Video #7 showing Fmax and % utilization
- 3) A high level RTL view after Video #8
- 4) The Compilation Report at the end of Video #10 showing Fmax and % utilization
- 5) The ModelSim Simulation waveform window at the end of Video #11

Solutions:

Submit screenshots (Format: .jpg) of:

- 1) The completed pipemult schematic after Video #6



2) The Compilation Report after Video #7 showing Fmax and % utilization

Quartus Prime Lite Edition - C:/AlteraPrj/pipemultQP16_1/Schematic/pipemult - pipemult2

File Edit View Project Assignments Processing Tools Window Help

Search altera.com

Project Navigator

Entity Instance

MAX 10: 10M08DAF484C8GES

pipemult

Table of Contents

Flow Summary

Flow Status

Quartus Prime Version

Revision Name

Top-level Entity Name

Family

Device

Timing Models

Total logic elements

Total registers

Total pins

Total virtual pins

Total memory bits

Embedded Multiplier 9-bit elements

Total PLLs

UFM blocks

ADC blocks

Successful - Sun Mar 26 23:41:17 2017

16.1.0 Build 196 10/24/2016 S.J. Lite Edition

pipemult2

MAX 10

10M08DAF484C8GES

Preliminary

6 / 8,064 (< 1 %)

21

44 / 250 (18 %)

0

512 / 387,072 (< 1 %)

1 / 48 (2 %)

0 / 2 (0 %)

0 / 1 (0 %)

0 / 1 (0 %)

IP Catalog

Installed IP

Project Directory

No Selection Available

Library

Basic Functions

DSP

Interface Protocols

Memory Interfaces and Controllers

Processors and Peripherals

University Program

Search for Partner IP

Tasks

Compilation

Task

Compile Design

Analysis & Synthesis

Fitter (Place & Route)

Assembler (Generate programming files)

TimeQuest Timing Analysis

EDA Netlist Writer

Quartus Prime Tcl Console

Tcl

Find

Find Next

Messages

System

Processing

0% 00:00:00

Quartus Prime Lite Edition - C:/AlteraPrj/pipemultQP16_1/Schematic/pipemult - pipemult

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Project Navigator

Entity Instance

MAX 10: 10M08DAF484C8GES

pipemult

multinst

raminst1

Table of Contents

Slow 1200mV 85C Model Fmax Summary

	Fmax	Restricted Fmax	Clock Name	Note
1	162.26 MHz	162.26 MHz	clk1	

This panel reports FMAX for every clock in the design, regardless of the user-specified clock periods. FMAX is only computed for paths where the source and destination registers or ports are driven by the same clock. Paths of different clocks, including generated clocks, are ignored. For paths between a clock and its inversion, FMAX is

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Find Next

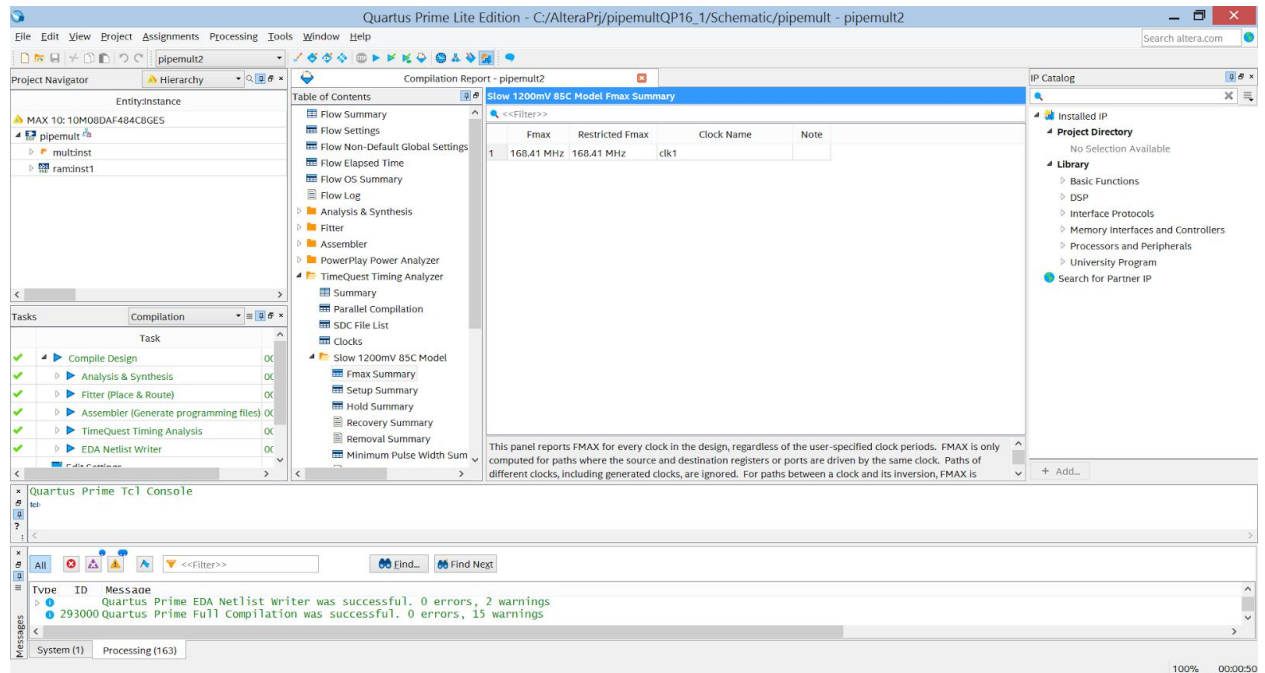
Messages

System

Processing

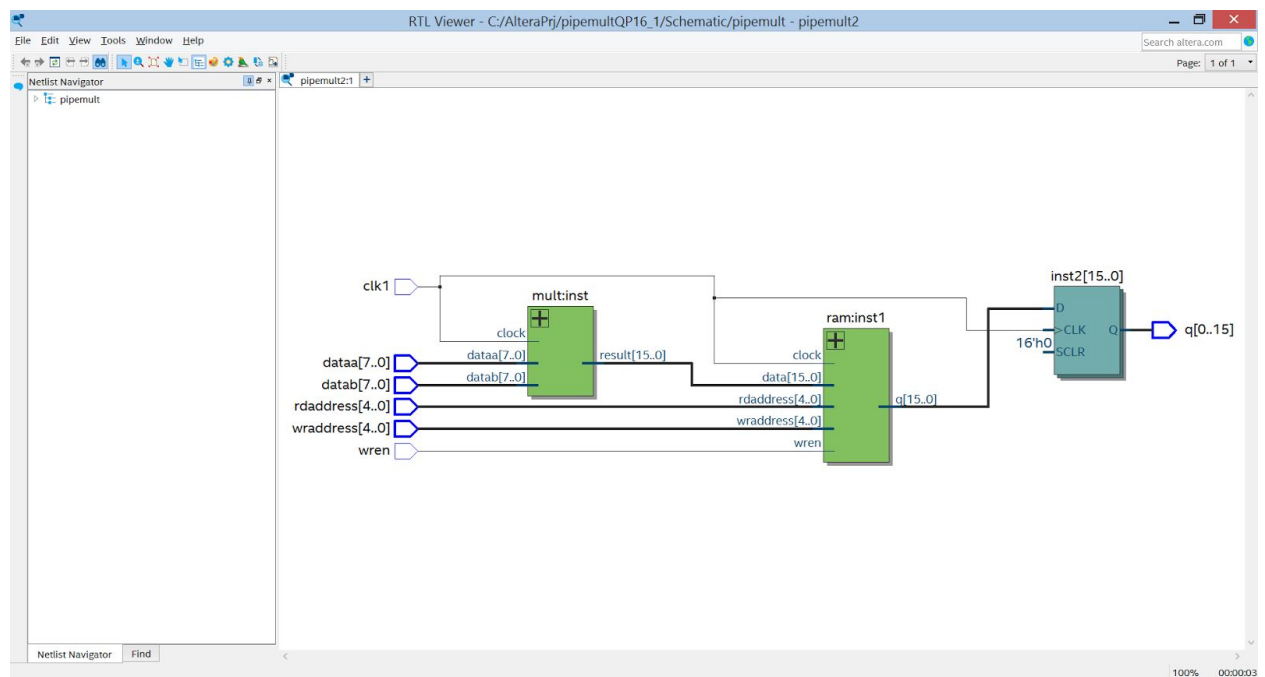
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Revision 1 Fmax

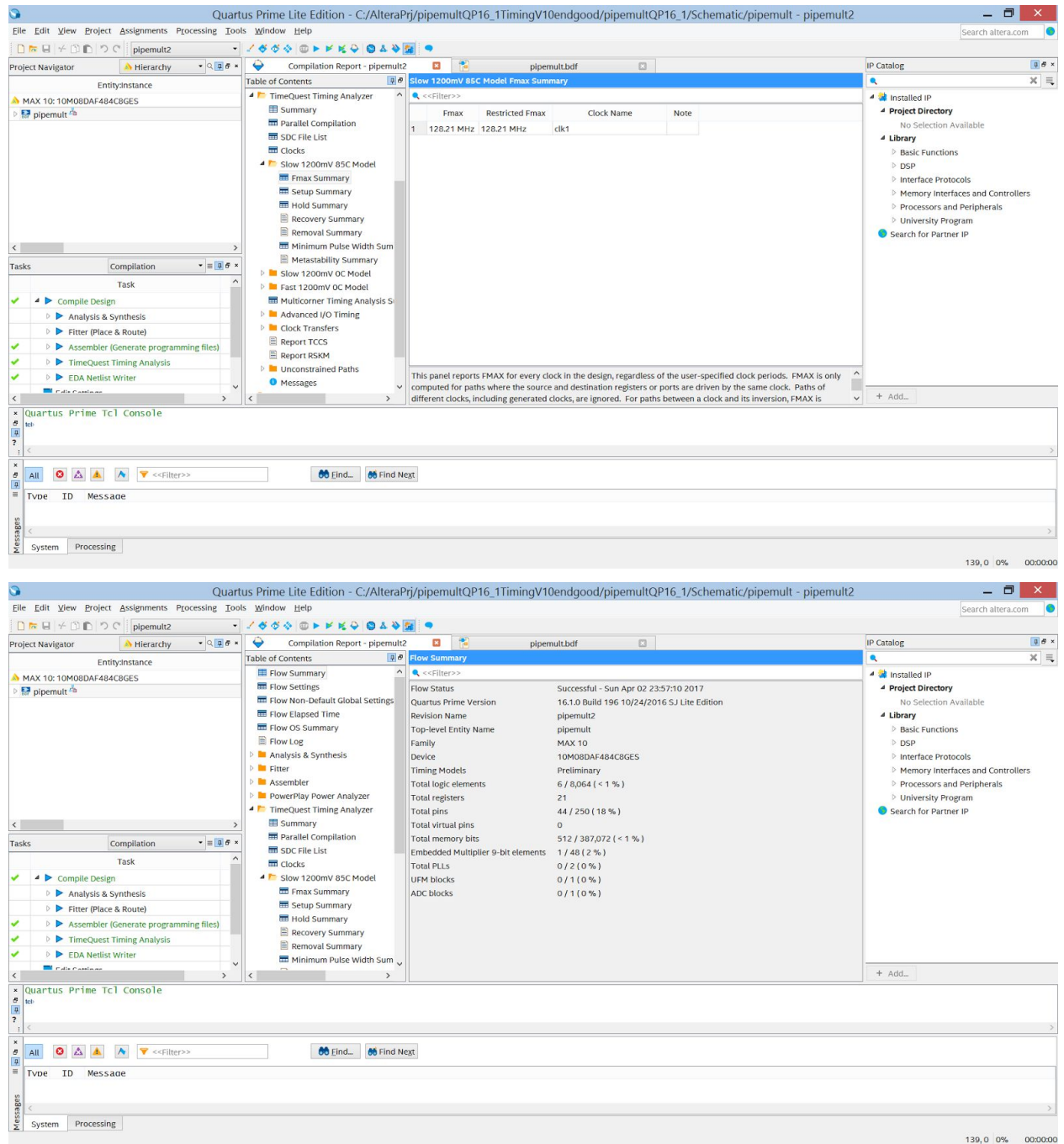


Revision2 Fmax

3) A high level RTL view after Video #8



4) The Compilation Report at the end of Video #10 showing Fmax and % utilization



5) The ModelSim Simulation waveform window at the end of Video #11

