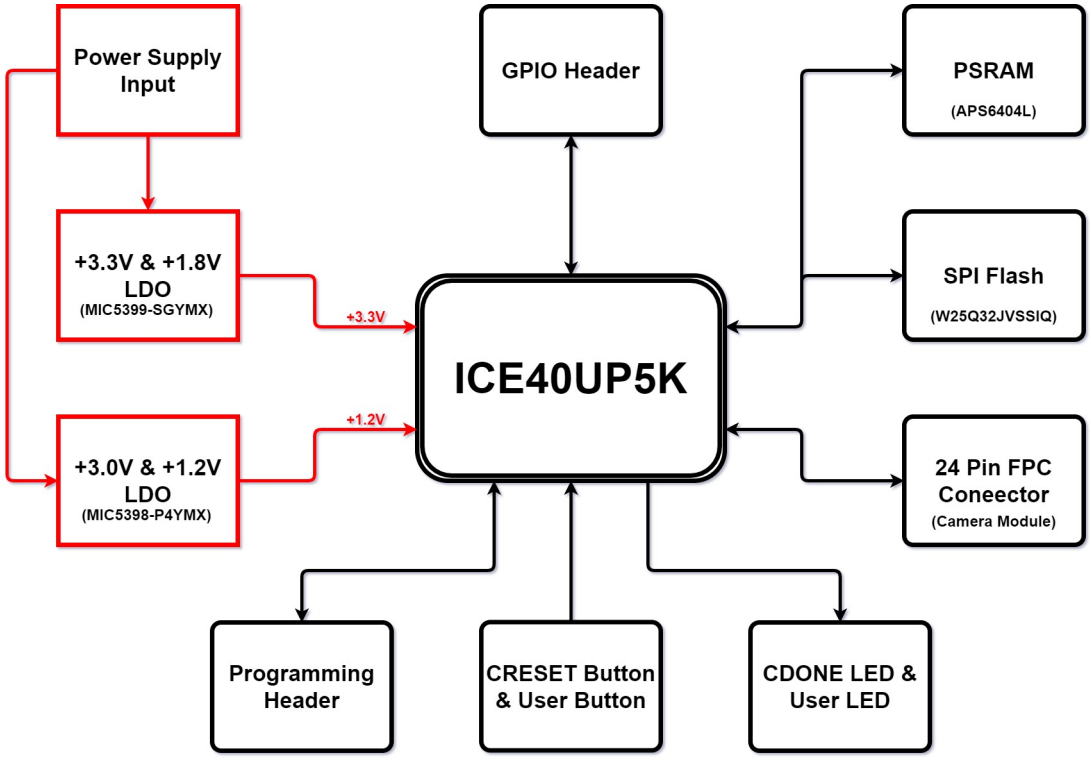
Block Diagram



Sheet: power_supply
File: power_supply.sch

Sheet: iCE40UP5K
File: iCE40UP5K_SG48ITR.sch

Sheet: io_headers
File: io_headers.sch

Sheet: OV7670_spi-flash_SRAM
File: OV7670_spi-flash_SRAM.sch

H1 H2 FID1 FID2 FID3 FID4

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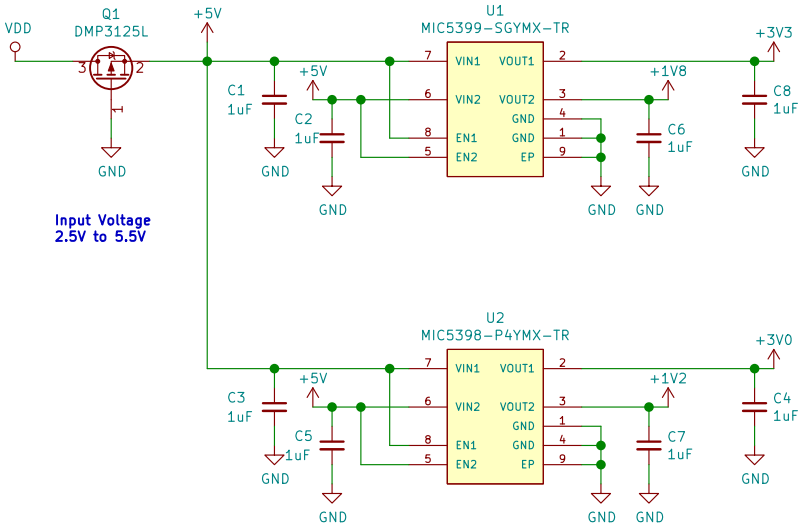
Sheet: /
File: fpga-play.sch

Title: fpga.play

Size: A4	Date: 2020-06-19	**Rev: 0.1**
KiCad E.D.A. kicad (5.1.5)-3		Id: 1/5

Power Supply



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Sheet: /power_supply/
File: power_supply.sch

Title: fpga.play

Size: A4	Date: 2020-06-19	**Rev: 0.1**
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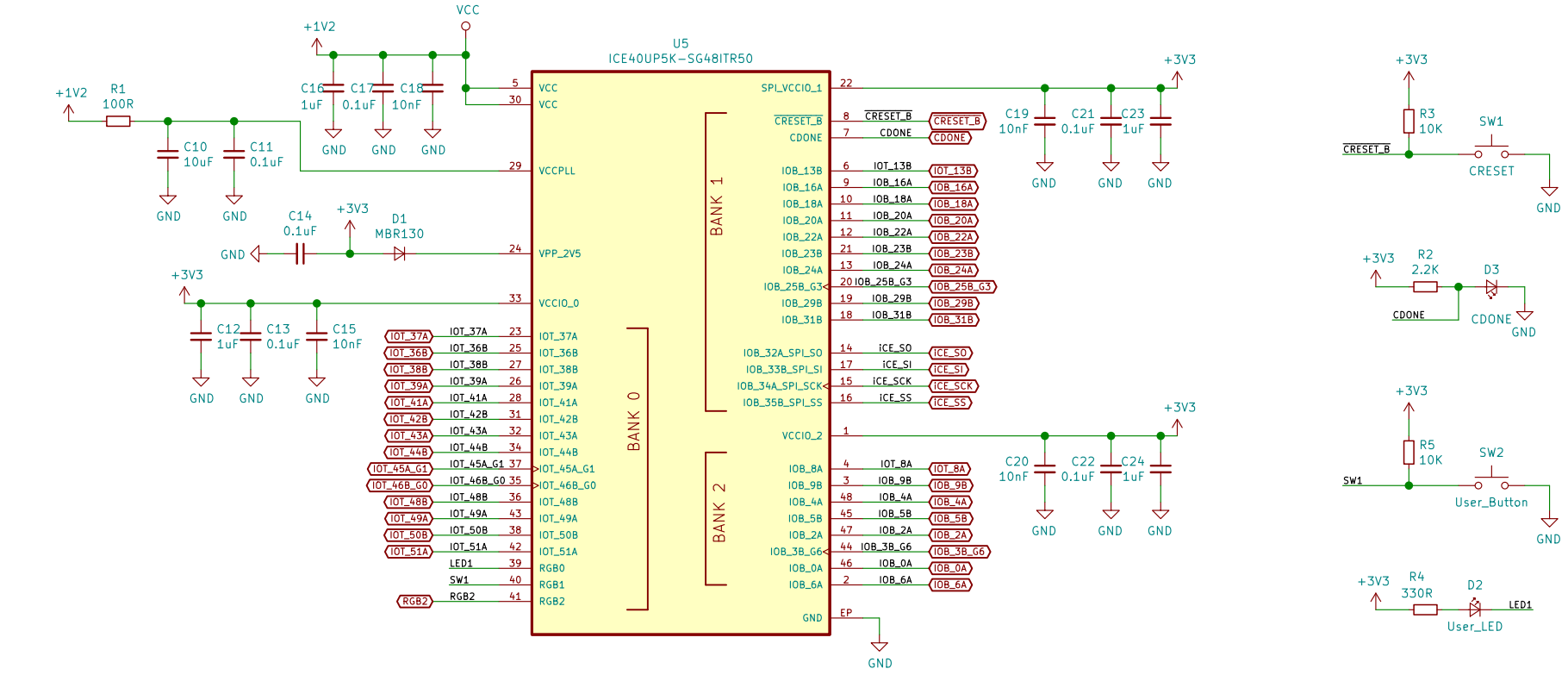
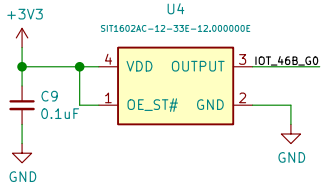
ICE40UP5K





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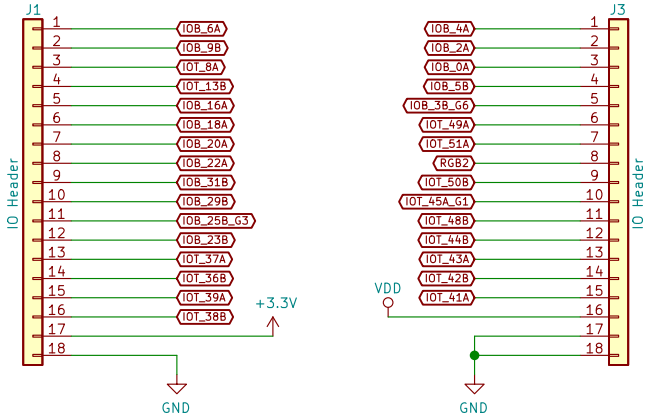
Sheet: /iCE40UP5K/
File: iCE40UP5K_SG48ITR.sch

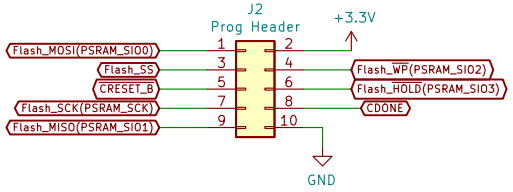
Title: fpga.play

Size: A4	Date: 2020-06-19	**Rev: 0.1**
KiCad E.D.A. kicad (5.1.5)-3		Id: 3/5

GPIO Header



Programming Header



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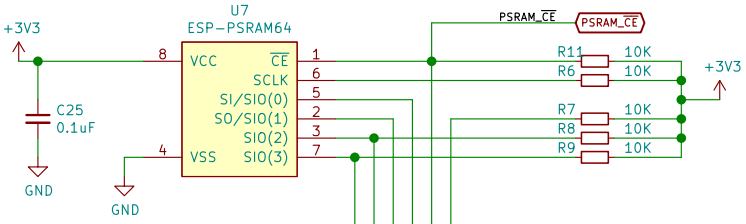
Sheet: /io_headers/
File: io_headers.sch

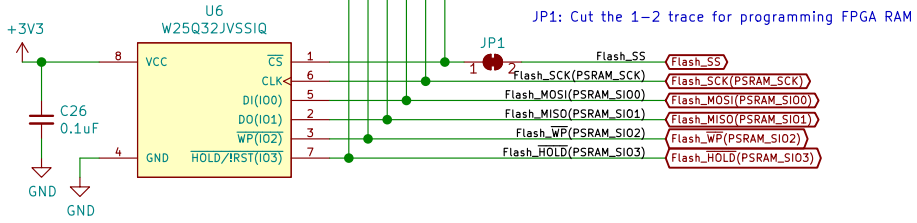
Title: fpga.play

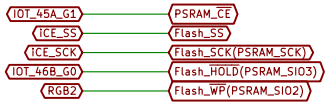
Size: A4	Date: 2020-06-19	**Rev: 0.1**
KiCad E.D.A. kicad (5.1.5)-3		Id: 4/5

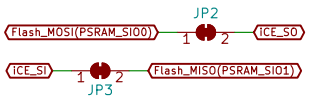
PSRAM



Flash Memory





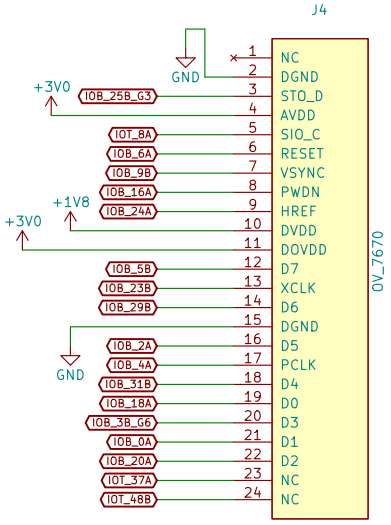


= For programming Flash

|| For programming FPGA RAM

For programming FPGA RAM directly cut the 1-2 traces from JP2 and JP3 and connect them as 1-1 and 2-2.

24 Pin FPC Connector



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Sheet: /OV7670_spi-flash_SRAM/
File: OV7670_spi-flash_SRAM.sch

Title: fpga.play

Size: A4	Date: 2020-06-19	**Rev: 0.1**
KiCad E.D.A. kicad (5.1.5)-3		Id: 5/5