Nikhil Kunjoor

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Education

Arizona State University — Tempe, US
Master of Science in Computer Engineering (Electrical Engineering) — *May 2026*
- Related Coursework: Hardware and Systems for Machine Learning, Machine Vision and Pattern Recognition, Advanced Analog Integrated Circuit Design, Semiconductor Heterogeneous Integration, VLSI Design and Computer Architecture

PES University — Bangalore, India
Bachelor of Technology in Electronics and Communication Engineering — *Aug 2023*
- Related Coursework: Microcontroller Programming, Circuit Design and Testing, Electronic Design Automation

Experience

Software Associate — Jul. 2023 – Jul. 2024
PricewaterhouseCoopers — *Kolkata, India*
- Executed comprehensive system validation test plans for datacenter server prototypes (HGX baseboards, DGX Servers), ensuring that new cloud software features met performance and quality objectives.
- Collaborated closely with Cloud Architecture, DevOps, and Software teams to debug infrastructure-level issues and optimize deployment configurations, reducing production defects by 30%.
- Built test scripts using Python, TCL, and Linux-based tools to streamline continuous integration and system validation in cloud environments.
- Supported integration testing in Linux environments to verify system performance, scalability, and reliability of cloud server products.

Software Intern — Jan. 2023 – Jul. 2023
PricewaterhouseCoopers — *Kolkata, India*
- Automated EBS Volume resizing via CloudFormation, cutting manual intervention by 50% while ensuring client control.
- Designed an ETL pipeline for gathering data via AppFlow, processing in AWS Glue and visualizing data in QuickSight.
- Created comprehensive documentation on set up of AWS Control Tower and several custom Automation procedures.

Projects

Hybrid Adaptive Compression Algorithms for Energy-Efficient AI Inference — Fall 2024
- Leveraged hardware profiling for edge devices, implemented a recommendation system for hardware-specific compression.
- Explored quantization and pruning and crafted a custom algorithm to vary the extent to which the algorithm's were applied.
- Crafted a custom RL agent to suggest alternative combinations of compression techniques based on hardware architecture.

Design and Simulation of a 4×4 Systolic Array — Fall 2024
- Architected and implemented a 4×4 systolic array for efficient matrix multiplication using SystemVerilog, emphasizing parallel data processing and pipelined execution.
- Simulated the systolic array under diverse workloads with ModelSim to verify functional correctness and timing closure.
- Performed power estimation and using Synopsys Design Compiler showing 12% higher power efficiency.
- Leveraged additional verification in QuestaSim for comprehensive debugging and coverage analysis.

CPU Microarchitecture Verification Framework — Spring 2023
- Implemented a UVM-based verification environment to simulate and validate CPU microarchitecture features.
- Developed testbenches in SystemVerilog to assess branch prediction, pipeline hazards, and clock domain crossing.
- Collaborated with cross-functional teams to correlate simulation results with schematic design improvements.

Cache Memory Subsystem Design with Stream Buffer Prefetching — Fall 2022
- Implemented a cache simulator in C++ to model a multi-level cache hierarchy for CPU performance analysis.
- Developed stream buffer prefetching algorithms that reduced cache miss rates by 20%.

2x2 SRAM Cell & 6T DRAM Cells (Memory Design Project) — Spring 2021
- Designed and layout-implemented 2x2 SRAM and 6T DRAM cells in Cadence Virtuoso from gate level to full layout.
- Integrated memory blocks into digital CPU schematics and verified performance through simulation.

Technical Skills

Languages: SystemVerilog, Verilog, VHDL, C/C++, Python, MATLAB, TCL, Perl, Assembly
Tools: Cadence Virtuoso, Xilinx Vivado, Mentor Questa Sim, ModelSim, Synopsys Design Compiler, Quartus Prime, Solidworks
Concepts: RTL Design, CPU Microarchitecture, Schematic Capture, Board-Level Design, Timing Closure, Clock Domain Crossing, Digital Verification, FPGA Prototyping, Hardware Testing & Debugging
Other: Linux, Static Timing Analysis, Hardware Debugging, MOSFET Analysis, Digital Circuit Analysis