

Design of a Class AB Hi-Fi Amplifier

The Boom Boom Box

Johan Askjær, Frederik Sofus
Hansen, Valdemar Jensen,
Niclas Pedersen, Markus Toribio



Electronics and System Design

Aalborg University

<http://www.aau.dk>

AALBORG UNIVERSITY

STUDENT REPORT

Title:

Design of a class AB Hi-Fi amplifier,
The Boom Boom Box

Abstract:

This is an abstract

Project:

P4 Project

Project Period:

Spring semester 2024

Project Group:

ESD4-410

Participants:

Johan Askjær

Frederik Sofus Hansen

Valdemar Jensen

Niclas Pedersen

Markus Heinrich Toribio

Supervisor:

Jens Frederik Dalsgaard Nielsen

Page Numbers: 118

Date of Completion:

May 20, 2024

Contents

Preface	vi
1 Introduction	1
2 Problem Analysis	2
2.1 Case	2
2.1.1 Initial Problem	2
3 Technical analysis	4
3.1 System Introduction	4
3.1.1 Phono- and Line-inputs	4
3.1.2 Preamplifier and RIAA	5
3.1.3 Equalizer and Volume Control	5
3.1.4 Power Amplifier	5
3.1.5 Speakers	5
3.2 Electrical Sound Signals	5
3.3 Equalizer	6
3.3.1 Phase Considerations	10
3.4 Transistors	10
3.4.1 The basic transistor	10
3.4.2 Bipolar Junction Transistor(BJT)	11
3.4.3 Field effect Transistor(FET)	14
3.5 Classes of amplifiers	15
3.5.1 Class A	16
3.5.2 Class B	17
3.5.3 Class AB	18
3.5.4 Class D	18
3.6 Record players	18
3.7 Powersupply	20
3.7.1 Unregulated power supply	21
3.7.2 Linear regulated power supplies	21
3.7.3 Switch-mode power supply	22
3.8 Speakers	22
3.8.1 The Basic Function of Speakers	23
3.8.2 Types of Speakers	23
3.8.3 Components of a Speaker	23
3.8.4 Speaker Performance and Specifications	23

3.8.5	Role in Audio Systems	24
3.9	Harmonic Distortion	24
4	Specification	26
4.1	General Concept of The Project	26
4.2	Functional Requirements	26
4.3	System Technical Requirements	26
4.4	Subsystem technical requirements	26
4.4.1	AUX-amp	26
4.4.2	RIAA	27
4.4.3	Equalizer and Volume Control	27
4.4.4	Power Amplifier	27
5	System design	28
5.1	AUX-amp	28
5.1.1	Specifications	28
5.1.2	Topology Choices	28
5.1.3	Theoretical Design	29
5.1.4	Simulation	32
5.1.5	Conclusion	33
5.2	RIAA	33
5.2.1	Specifications	33
5.2.2	Topology Choices	33
5.2.3	Theoretical Design	34
5.2.4	Simulation	37
5.2.5	Conclusion	38
5.3	Equalizer	38
5.3.1	Specifications	38
5.3.2	Topology Choices	38
5.3.3	Theoretical Design	39
5.3.4	Simulation	42
5.3.5	Conclusion	44
5.4	Volume Control	44
5.4.1	Specification	44
5.4.2	Topology Choices	44
5.4.3	Theoretical Design	44
5.4.4	Simulation	44
5.4.5	Conclusion	45
5.5	Filtering	45
5.5.1	Specifications	45
5.5.2	Topology Choices	46
5.5.3	Theoretical Design	46
5.5.4	Simulation	48
5.5.5	Conclusion	48
5.6	Power Amplifier	48
5.6.1	Specifications	49
5.6.2	Topology Choices	49
5.6.3	Theoretical Design	52

5.6.4	Simulation	68
5.6.5	Conclusion	73
5.7	Power Supply	73
5.7.1	Specifications	73
5.7.2	Topology choices	73
5.7.3	Theoretical design	73
5.7.4	Simulation	76
5.7.5	Conclusion	77
6	Integration	78
6.1	Integration on PCB	78
6.1.1	Pre-amp / RIAA	79
6.1.2	Equalizer / Volume control	80
6.2	System integration	82
6.2.1	Power amplifier	82
6.3	Power Supply	84
6.3.1	Case	85
6.4	PCB Revisions	88
7	Testing	90
7.1	System Technical Requirements	90
7.2	Subsystem technical requirements	90
7.2.1	AUX-amp	90
7.2.2	RIAA	91
7.2.3	Equalizer and Volume Control	91
7.2.4	Power Amplifier	91
8	Discussion	92
8.1	Preamp Consolidation	92
8.2	Overshoot Protection	92
8.3	Power Amplifier Input Filter	92
8.4	Input Level Detection	92
9	Conclusion	93
A	Attachments	98
B	Attached files	99
C	Simulation Schematics	100
C.1	Open Loop Gain	100
D	Test Journals	101
D.1	THD and Frequency Response	101
D.1.1	Purpose	101
D.1.2	Equipment	101
D.1.3	Procedure	101
D.1.4	Results	103
D.2	Input Impedance	108

D.2.1	Purpose	108
D.2.2	Equipment	109
D.2.3	Procedure	109
D.2.4	Results	110
D.3	Output Impedance	114
D.3.1	Purpose	114
D.3.2	Equipment	114
D.3.3	Procedure	114
D.3.4	Results	116
D.4	Signal-to-Noise Ratio	117
D.4.1	Purpose	117
D.4.2	Equipment	117
D.4.3	Procedure	117
D.4.4	Results	118

Preface

This is a preface

Aalborg University, 19-12-2023

Frederik Sofus Hansen
fha22@student.aau.dk

Johan Askjær
@student.aau.dk

Markus Heinrich Toribio
mtorib22@student.aau.dk

Nicklas Pedersen
@student.aau.dk

Valdemar Jensen
@student.aau.dk

1 | Introduction

High-fidelity audio reproduction has been a focus in the world of electronics for over a hundred years. Audio reproduction takes many forms, from movies, concerts, video games, music, and more, however, the main focus of this project will be on recorded music. At its dawn audio reproduction was made possible by expensive vacuum tubes, today the same systems can be designed with inexpensive transistors.

Recorded music comes in many forms, from vinyl to online services, if an amplifier system is to fulfill current consumer needs, it should allow inputs from a vast amount of different sources. This might seem like a vast task, however, most of the inputs have been standardized, which makes this task much easier.

High fidelity has a varying definition, depending on who you ask, and some Hi-fi enthusiasts will proclaim that they can hear even the subtlest of noise, in a system. This strife to get as close as possible to perfection, even though the human ear has its limits, sets the ground for never-ending challenges. This is the ground from which this project will start, to build a shameless amplifier, with multiple inputs, to satisfy the consumer.

2 | Problem Analysis

2.1 Case

This project will use a case as takeoff and motivation for further work. This case will serve as a setting and as an insight into the user's needs and requirements.

The study group found a pair of old speakers in the electronics laboratory. These speakers are the Dali 2a's which are old, high-quality, Danish-built speakers. Despite their age, these speakers are in great condition and the group therefore agrees that they deserve a Hi-Fi amplifier specifically built for this set of speakers. To match the speaker's age the group therefore decides to build an old-school analog transistor-based amplifier.

Although the speakers and the amplifier are old-school the group still wants new equipment to be able to play audio through the system. So a 3.5mm jack(aux cable) is chosen as the main way to play music throughout the system. Staying with the old-school theme the group also wants to be able to play vinyl records from the system. Additionally, the group also wants to control the volume and have tone control to for example boost bass and treble.

From the case some functional requirements have been made for the system:

- Audio interface 3.5mm Jack for newer devices such as phones and Phono for the vinyl record player.
- The system should feature an equalizer and a volume control.
- A power supply that plugs into wall power.
- The system should amplify the input signal such that it can drive the Dali speakers with a consumer line level.
- The system should be able to play in stereo.
- The system should reproduce audio at the DIN45500 Hi-Fi standard described in chapter 4.

2.1.1 Initial Problem

The report will use the initial problem statement as motivation for the technical analysis. It will help guide the technical analysis by correcting the focus on the necessary technical topics.

How to design and implement a transistor-based analog Hi-Fi amplifier capable of replaying high-quality audio signals from modern and vintage input sources to a Dali 2a

speaker output.

3 | Technical analysis

3.1 System Introduction

To get an overview of the possible system solving the initial problem fig 3.1 has been created. The figure outlines the different blocks necessary for the Hi-Fi system. Additionally, the Hi-Fi system will be designed for stereo, therefore all system blocks are effectively doubled from the drawing except the input lines of RIAA and line level. Furthermore, a switch is implemented so the user can alternate between phono or line levels depending on the use case.

To get an overview of the possible system solving the initial problem, this section will explain in short, each part of the system, and how the different parts will interact with each other.

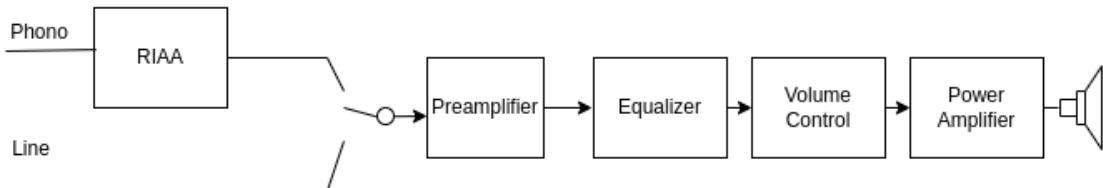


Figure 3.1: Overview of a generic Hi-Fi amplifier system

3.1.1 Phono- and Line-inputs

Depending on the use case of the Hi-Fi amplifier the system could be able to accommodate a multitude of inputs, as Hi-Fi enthusiast might have anything from CD's (Compact Disks), Vinyl or AUX directly from a smartphone or PC. For most of these inputs, it is easy to acquire a device outputting consumer line level which is 0.316 V RMS. The only direct exception to this is Vinyl, as most Record Players follow a RIAA characteristic. Some PC's and smartphones don't adhere to the consumer line level input, but it is chosen to continue with a consumer line level input, as this is the most common for both CD's, Smartphones, etc. Apart from the consumer line level input, a RIAA input should be accessible as well, so that the consumer can play Vinyl discs, through the amplifier.

Then the only real exception of inputs will be pro line level, which is 1.228 V RMS, inputs, and mic level inputs. However this project will focus on playing pre-recorded audio, so live signals are not of interest.

The inputs will not need to be powered, but only to transfer the signal to the pre-amplifiers. Apart from that, they should together with the rest of the system, have a high impedance, to not affect the device outputting the audio signal.

3.1.2 Preamplifier and RIAA

The pre-amplifier stage is connected to the inputs. There should be one solution for the RIAA input, which is an amplifier and a RIAA filter. Also, an opamp-based pre-amplifier as well as a Class A pre-amplifier will be designed.

The output signal from all the channels should be amplified to pro-line level. This ensures, that no matter if the input is AUX or RIAA, it will be able to go through the rest of the system, all the same.

3.1.3 Equalizer and Volume Control

Both of the subsystems should have line-level pro in and out. The Equalizer should allow customization of the output signal from the user's perspective. The Volume Control should allow the user to adjust the volume of the sound.

3.1.4 Power Amplifier

The power amplifier must amplify the signal to the level of the speakers. This includes some sort of input stage, as well as a voltage amplification stage and an output stage. Apart from that the system might also contain negative feedback, to ensure a high-quality signal.

3.1.5 Speakers

When designing a Hi-Fi system the speakers of which the system should always be considered first. This is highlighted later on in section 3.8.

3.2 Electrical Sound Signals

Electrical signals have many capabilities, among them is the transportation of information. This report will focus on audio transportation.

Electrical audio signals are a transformation of the physical air pressure waves or a transformation from the physical world to the electrical. This is very useful as it allows for recording, saving, and reproducing certain sound waves on demand. The most common example of this is music where an artist records a song typically in a studio from where it gets saved and distributed to the world to listen to. These audio signals are a representation of air pressure waves which means the electrical signals will look like a wave. The simplest form of this is a constant tone in which case the audio signal can be described as a simple sine wave with a certain frequency.

A constant tone can be used for many different purposes such as testing but music consists of many different frequencies mixed into one signal. As seen in the figure below one such combination of tones can be seen as an example.

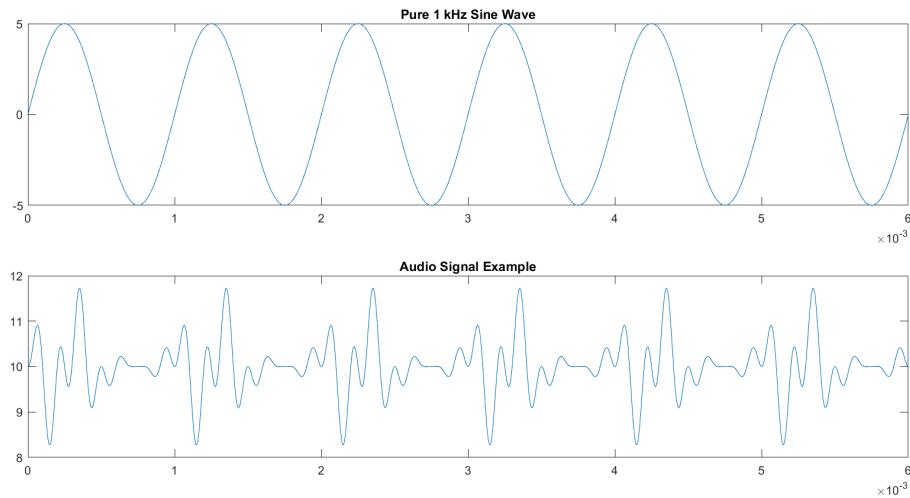


Figure 3.2: A sine wave and an example of an audio signal

This representation of sound is however still a single source generating multiple frequencies but in music, there are lots of different instruments, beats, pauses, and maybe singers producing signals at the same time

3.3 Equalizer

An equalizer changes the volume of an input signal at different frequency bands of an audio signal. Such frequency bands could be bass, mid, and treble where a user can increase the volume of one band and decrease another by adjusting the equalizer. Another use of equalization can be found in balancing out any discrepancies found in the initial output signal by the loud speaker or the room in which the system is placed.

A HP filter functions by attenuating the lower frequencies more than the higher frequencies whereas the LP filter operates in reverse. The frequency response of such filters can be seen in fig 3.3.

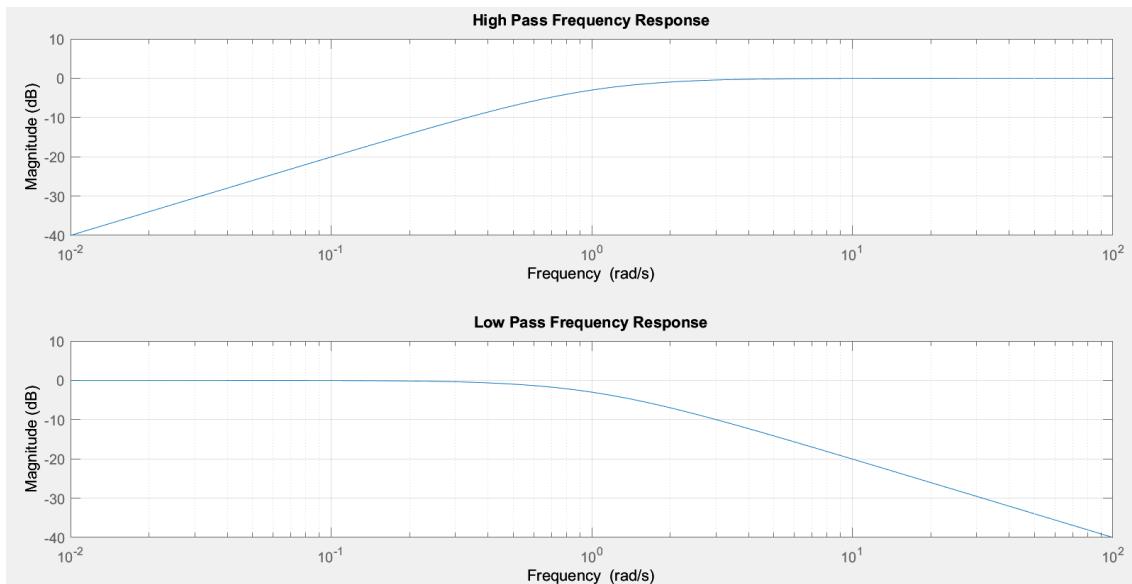


Figure 3.3: Frequency response with rad/s for HP and LP filter

This frequency response shown in fig 3.3 is of first-order since the filter attenuates frequencies after the cutoff at 3dB with 20dB per decade. By increasing the order of the filter the attenuation increases so e.g. a second-order filter has 40dB per decade attenuation instead of 20 dB. The transfer functions for specifically a first order HP filter and a LP filter are shown in eq 3.1. Here "s" is the complex frequency from the Laplace domain with unit rad/s [1].

$$\frac{s}{s + \omega_0} \quad \frac{\omega_0}{s + \omega_0} \quad (3.1)$$

$$s = \sigma + j\omega \quad \omega = 2\pi f$$

With second-order filters, resonance can be achieved around a given frequency as seen in fig 3.4 with e.g. a series RLC filter. The resonance frequency is at 1 rad/s. The resonance frequency is attained at the point where the impedance of the circuit is purely real and no imaginary component is present from either the capacitor or inductor [1]. The transfer function is shown in eq 3.2 [2]. ζ is described as the damping factor.

$$H(s) = 2\zeta\omega_0 \frac{s}{s^2 + 2\zeta\omega_0 s + \omega_0^2} \quad \zeta = \frac{R}{2} \sqrt{\frac{C}{L}} \quad \omega_0 = \frac{1}{\sqrt{LC}} \quad (3.2)$$

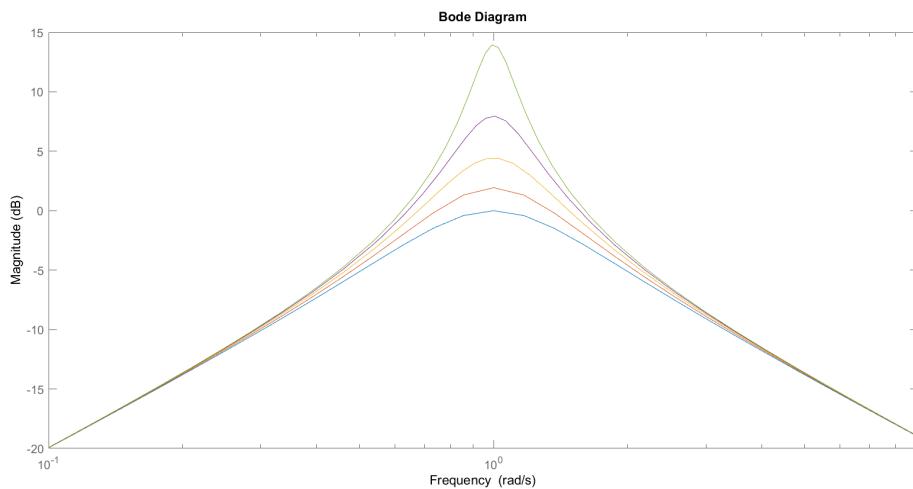


Figure 3.4: 2nd order bandpass filter with varying degrees of Q factors

Here the response is not only governed by the chosen frequency but also its Q-factor. The formula for Q is given in eq 3.3

$$Q = \frac{\omega_0 \cdot L}{R} = \frac{1}{\omega_0 \cdot C \cdot R} = \frac{1}{R} \sqrt{\frac{L}{C}} \quad (3.3)$$

The Q-factor is the amount of peak energy stored divided by the dispersed energy in the circuit. Therefore, a large Q-factor yields a frequency response with a small bandwidth and high amplitude whereas a low Q-factor gives low amplitude but a broader bandwidth. Bandwidth is given by the span between the -3dB points from the center of the resonant frequency [1]. This is illustrated in fig 3.5 and associated formulas shown in eq 3.4.

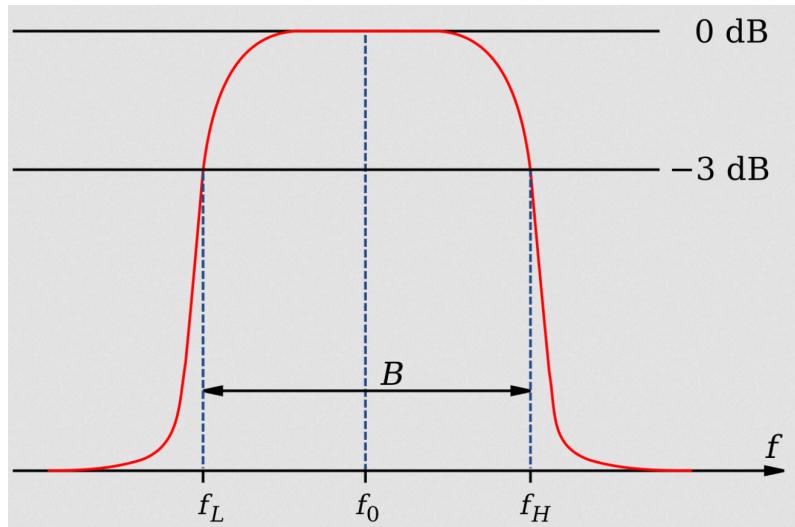


Figure 3.5: Visualaztion of bandwidth for a transfer function

$$BW = f_H - f_L = \frac{f_0}{Q} \quad (3.4)$$

With these basic building blocks, more nuanced frequency manipulation can be achieved by combining or chaining multiple filters together which is done by the various forms of equalizers such as graphic equalizers, shelving equalizers, and parametric equalizers.

Graphic equalizers

feature a set of vertical sliders, each representing a specific frequency band, allowing users to visually shape the frequency response curve.

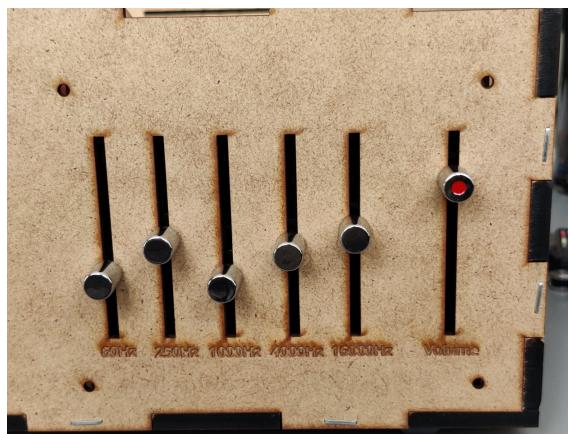


Figure 3.6: Graphic Eq face plate

Parametric equalizers

offer more precise control, allowing adjustment of parameters such as center frequency, bandwidth, and gain for each band.



Figure 3.7: Parametric Eq face plate[3]

Shelving equalizers

are specialized for boosting or cutting frequencies above or below a certain threshold, and useful for adjusting bass or treble levels.

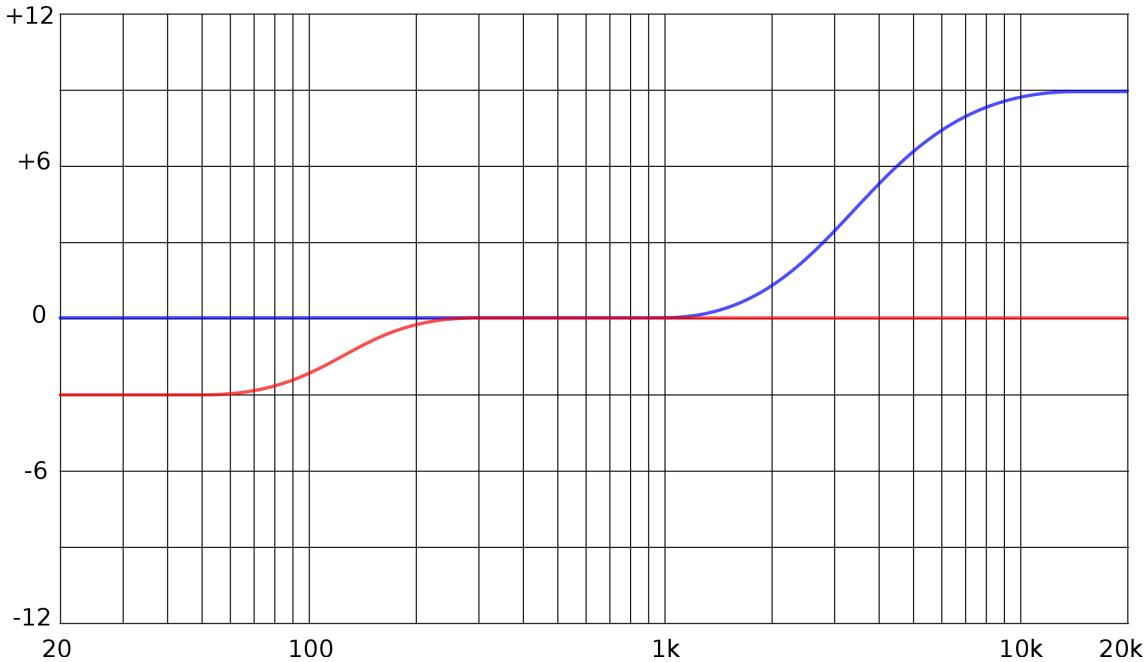


Figure 3.8: amplitude plot of a Shelving Eq[4]

3.3.1 Phase Considerations

as seen on this simulation of a graphic Eq most Eq's has a big phase shift especially at higher frequencies. This is due to the many filters the signal has to pass through. This is something to be aware of as it can create audible issues with the sound in the most extreme cases.

3.4 Transistors

In the realm of electronics, the transistor stands as a fundamental building block, pivotal in the evolution of modern technology. This section delves into the technical aspects of transistors, exploring their operation principles, types, and role in analog amplifiers. This section will start by examining the basic structure and function of a transistor, then move on to the BJT a current controlled device Lastly, swiftly cover the FET a voltage controlled device as this transistor type is not often used in audio amplifiers.

3.4.1 The basic transistor

A Transistor at its core, is a semiconductor device used to amplify or switch electronic signals and electrical power. The basic structure of a transistor is as follows:

- Input Terminal(Base for BJT and Gate for MOSFET)
- Output Terminal(Collector for BJT and Drain for MOSFET)
- Common Terminal(Emitter for BJT and Source for MOSFET)

Transistors are made from semiconductor materials, commonly silicon or germanium. These materials are chosen due to their ability to conduct current under certain conditions but not others, making them ideal for switching applications. These materials are doped with impurities to create regions with excess electrons(N-type) or holes(P-type). The arrangement of these doped regions defines the transistor's type and characteristics.

Basic function

Transistors are mainly used for 3 different purposes.

- Amplification: Transistors amplify weak input signals into stronger output signals. They achieve this by using a small signal at the input terminal to control a larger current flow between the other two terminals.
- Switching: A transistor can act as a switch, turning current flow on or off in response to its input signal. This function is critical in digital circuits, like those in computers and smartphones.
- Control Element: The input terminal controls the flow of current between the output and common terminals, effectively functioning as a valve that modulates the signals passing through the device.

3.4.2 Bipolar Junction Transistor(BJT)

The bipolar junction transistor is a fundamental type of transistor, that both plays a crucial role in amplification and switching signals across a wide range of applications. Unlike MOSFET's which are controlled by voltage, BJT's are current-controlled devices that use both electrons and holes in their operation, making them unique among semiconductor devices.

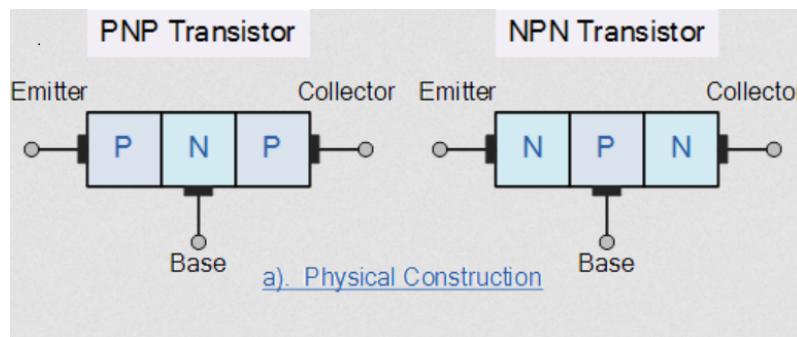


Figure 3.9: Construction of physical layers of a BJT [5]

A BJT is composed of three layers of doped semiconductor material, forming two PN junctions. This configuration as seen in the figure 3.9 is classified into two types: NPN and PNP, each with differing charge carrier predominance and polarity. The central layer as seen in the figure is very thin and lightly doped, positioned between the more heavily doped emitter and collector layers. The operation of a BJT depends significantly on the voltage applied to its junctions, which modulates the current flow from the emitter to the collector through the base.

A transistor as described before a 3-terminal device where the schematic can be seen in fig 3.10. This device has the following properties for NPN devices and polarities are just

reversed for PNP devices.

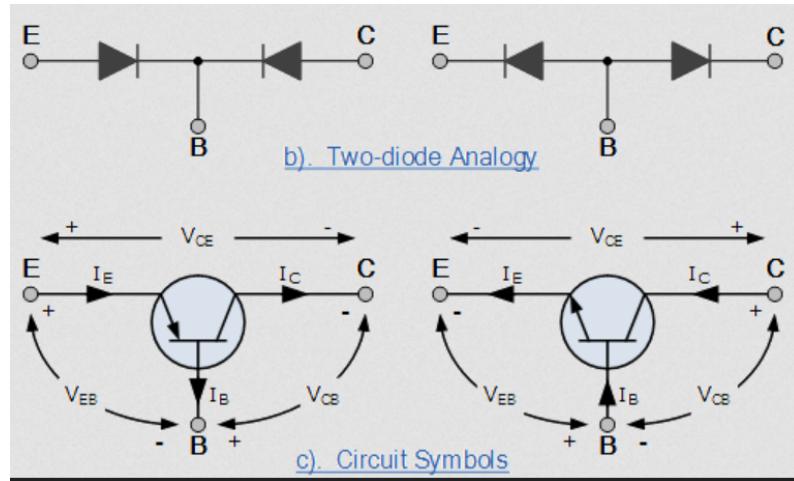


Figure 3.10: Schematic symbol of a PNP and a NPN BJT [5]

1. The collector must be more positive than the emitter.
2. The base-emitter and base-collector circuits behave like diodes. Normally the base-emitter diode is conducting and the base-collector diode is reverse biased, i.e. the applied voltage is in the opposite direction to easy current flow.
3. Any given transistor has maximum values of I_C , I_B , and V_{CE} that cannot be exceeded without costing the exceeding the price of a new transistor. There are also other limits, such as power dissipation ($I_C V_{CE}$), temperature, V_{BE} , etc, that must be kept in mind.
4. When rules 1-3 are obeyed, I_C is roughly proportional to I_B and can be written as: $I_C = h_{FE} I_B = \beta I_B$

Where h_{FE} is the current gain(also called beta). Property 4 here gives the transistor its usefulness, a small current flowing into the base controls a much larger current flowing into the collector. It should be said that h_{FE} is not a "good" parameter for the transistor as this value can vary a lot depending on the individual transistor as can be seen in figure 3.11.

h_{FE}	DC current gain BC546A BC546B; BC547B BC547C	$V_{CE} = 5 \text{ V}; I_C = 10 \mu\text{A};$ see Figs 2, 3 and 4	-	90	-	
			-	150	-	
			-	270	-	
	DC current gain BC546A BC546B; BC547B BC547C BC547	$V_{CE} = 5 \text{ V}; I_C = 2 \text{ mA};$ see Figs 2, 3 and 4	110	180	220	
			200	290	450	
			420	520	800	
			110	-	800	

Figure 3.11: Table from bc547 datasheet showing the inconsistency in the H_{FE} parameter [6]

Operating regions of a BJT

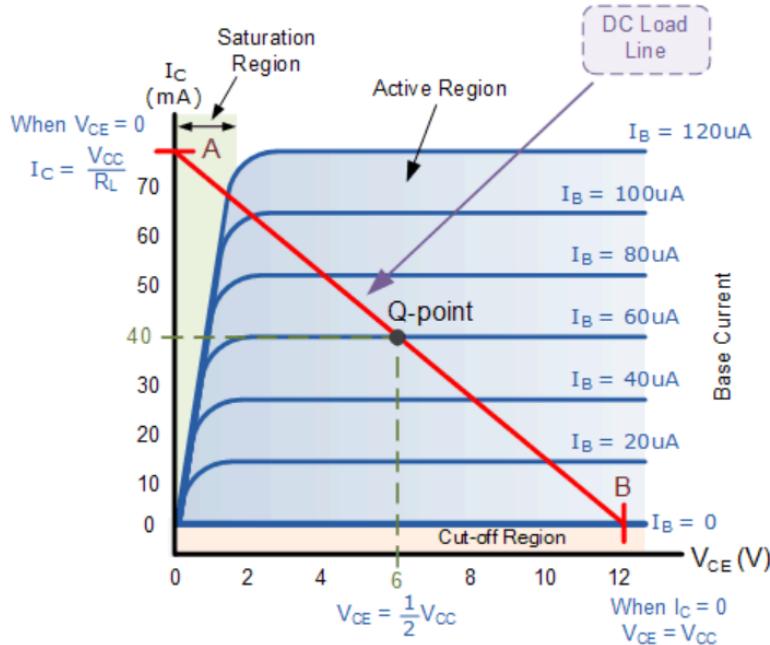


Figure 3.12: Ideal operating regions of an NPN transistor [7]

A BJT operates in three main regions as seen in fig 3.12 that determine how it functions within a circuit.

- **Cut-off Region:** In the cut-off region, the transistor acts almost like an open switch. This region is characterized by having insufficient base-emitter voltage (V_{BE}) to turn the transistor on. For an NPN transistor, this means that the base-emitter junction is not forward-biased, for silicon devices this is less than 0.6 or 0.7 Volts. This results in no significant current flowing from the collector to the emitter.
- **Active Region:** The active region is where the BJT acts as an amplifier. In this region, the base-emitter junction is forward-biased and the base-collector junction is reverse-biased. This setup allows a small base current to control a much larger collector current. In flowing into the base (I_B), modulated by the transistor's current gain (β). This property is why BJT's are so useful in amplifier circuits where small input signals need to be amplified.
- **Saturation Region:** In the saturation region, the transistor behaves like a closed switch. This occurs when both the base-emitter and base-collector junctions are forward-biased. For an NPN transistor, this means applying enough positive voltage to the base relative to the emitter and also ensuring the collector voltage is sufficiently low relative to the base. In saturation, the transistor allows maximum current to flow from the collector to the emitter, limited only by the external circuitry. The transistor cannot amplify in this state because any increase in base current does not significantly increase the collector current; it's essentially at its maximum value.

This however is an ideal transistor operating region model that strays away from the reality that the transistors used in real circuits aren't ideal and therefore their regions

look a bit different as seen in figure 3.13.

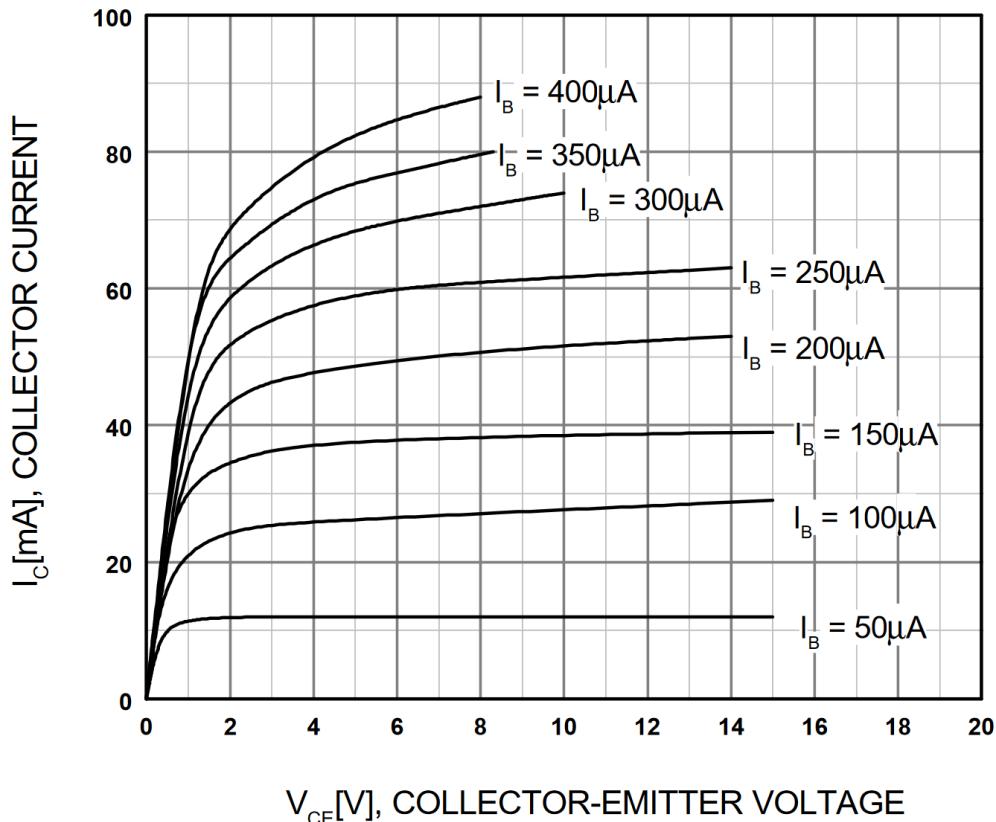


Figure 3.13: Graph for bc547 non ideal operating regions

3.4.3 Field effect Transistor(FET)

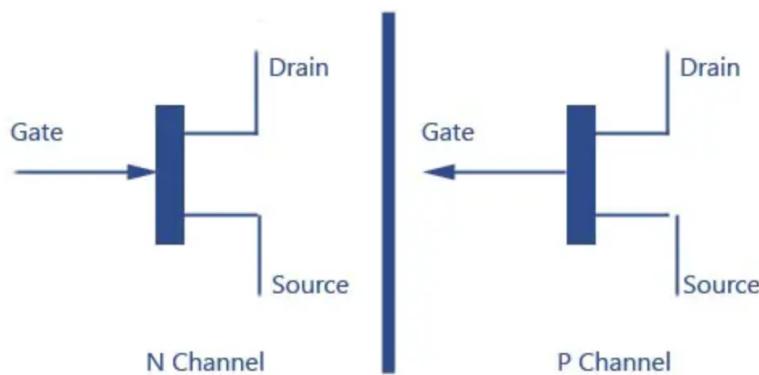


Figure 3.14: Schematic symbol of a FET[8]

Field effect transistors are different from BJT transistors. The main difference is in the way they are controlled as we know from the previous chapter the BJT is current-controlled. This is different in a FET as it is voltage-controlled because as the name

suggests conduction in a channel is controlled by an electric field. There are no forward-biased junctions, so the gate draws no current, this is one of the biggest advantages of the FET. Like with BJT's there are two polarities for FET's n-channel and p-channel. These are comparable with the npn and pnp types of the BJT transistor. FET's can be made with two different types of gates(MOSFET and JFET).

Metal Oxide Semiconductor Field Effect Transistor(MOSFET)

Let's first take a look at the n-channel MOSFET. Normal operation requires the drain(collector) to be more positive than the source(emitter). No current flows from the drain to the source unless the gate(base) is brought positive concerning the source. Once the gate is then "forward-biased" there will be a drain current which all flows to the source. The physical construction of a MOSFET can be seen below

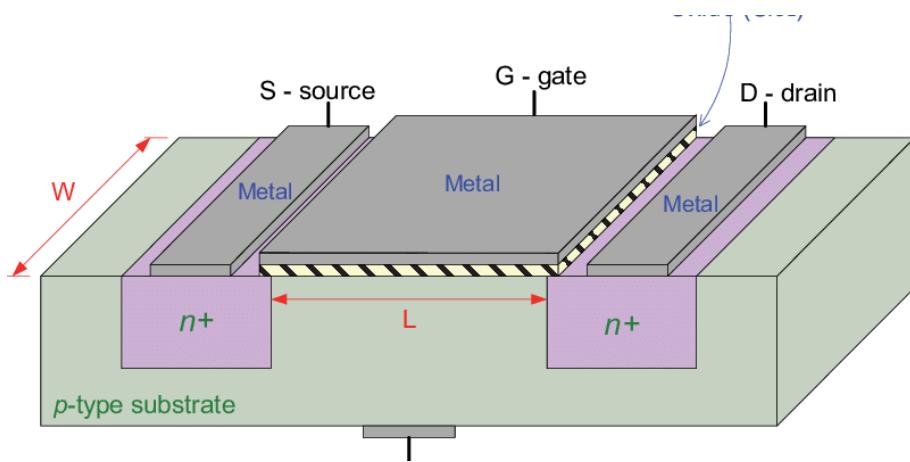


Figure 3.15: Figure showing the physical structure of a n-channel Mosfet

3.5 Classes of amplifiers

This section is based on Douglas self's "Audio Power Amplifier Design Handbook". and "Understanding Amplifier Operating 'classes'" by Don Tuite[9, 10]. The following classes of amplifiers will be covered in this section:

- Class A
- Class B
- Class AB
- Class D

These classes are defined by the amount of a cycle that the output stage devices conduct as can be seen in both the table and the figure 3.16.

Class A	Conducts for 100% of the cycle
Class AB	Conducts less than 100% but more than 50% of the cycle
Class B	Conducts for nearly 50% of the cycle
Class D	Either on or off, conduction period is not specified

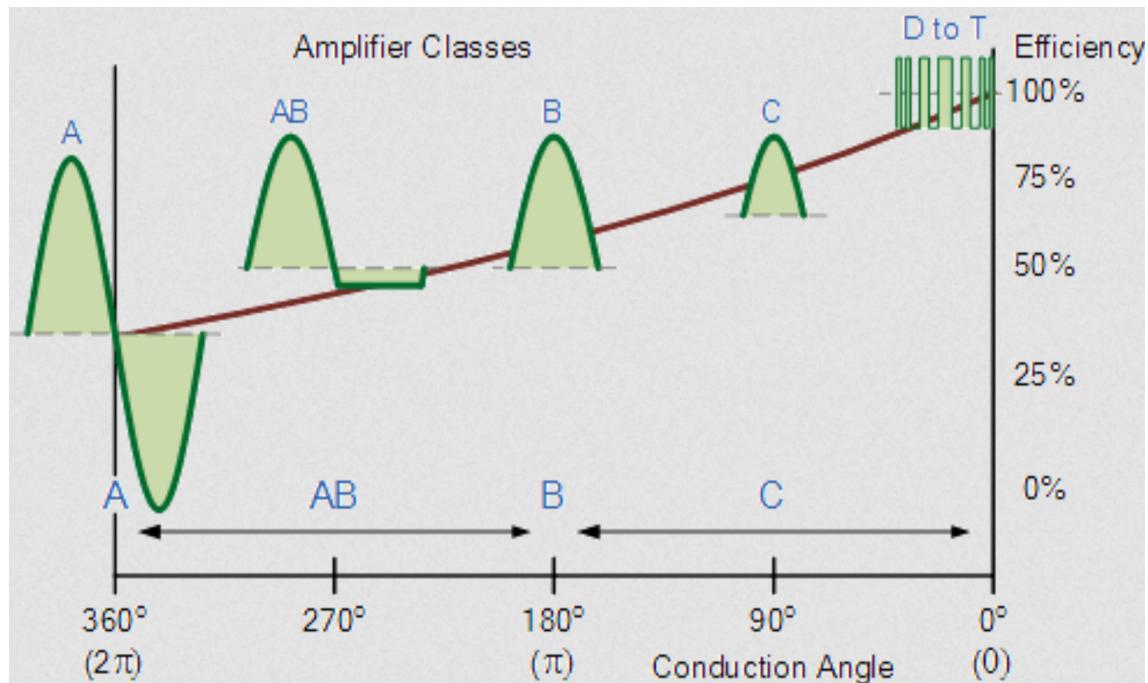


Figure 3.16: amplifier output stage conduction and efficiency

There are many more types of amplifier classes than those above but they are usually a combination or a slight modification of those above.

3.5.1 Class A

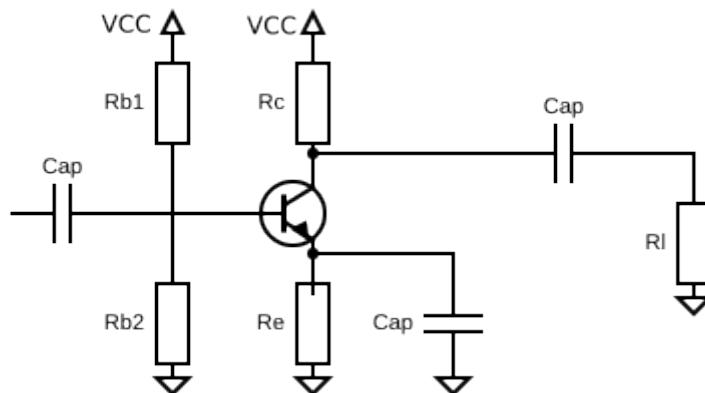


Figure 3.17: Generic Class a circuit

A Class A amplifier is a type of power amplifier where the output transistor is always biased “ON”, meaning it conducts during one complete cycle of the input signal waveform. This configuration ensures minimum distortion and maximum amplitude of the output signal. The Class A amplifier is the simplest form of power amplifier, it's often used as a “small signal amplifier”, but can also drive large resistive loads such as a loudspeaker or a motor in a robot. One of the main disadvantages of Class A amplifiers is their low efficiency, typically around 25-30%.

fiers is their low overall conversion efficiency. Large currents mean that a considerable amount of power is lost in the form of heat. Despite this, Class A operation ensures that the transistor is working in its most linear operating region, so sound distortion levels are minimal. In summary, Class A amplifiers are known for their high fidelity and immunity to crossover distortion, but they also have practical issues such as large power consumption and heat generation.

3.5.2 Class B

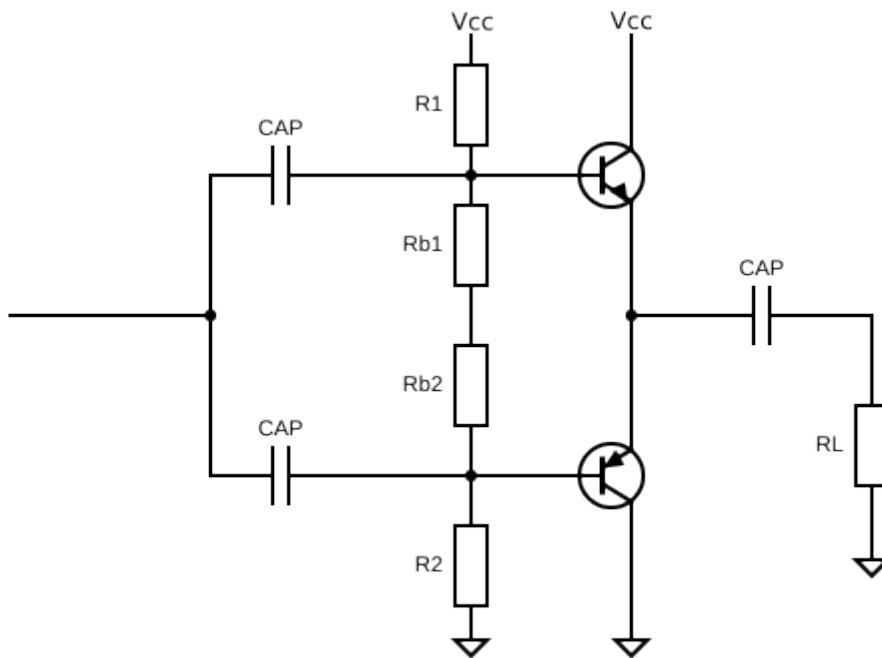


Figure 3.18: Generic class b circuit

A class B amplifier functions much like a class A, however, the output transistors conduct only during the one-half cycle (180 degrees) of the input signal waveform. This is achieved by using two transistors that are biased in such a way that each transistor only conducts during one-half cycle of the input waveform. The most common class B amplifier is a push-pull amplifier. This uses two complementary transistors, one being an NPN-type and the other being a PNP-type. Both power transistors receive the same input signal that is equal in magnitude but in opposite phases to each other. This results in one transistor amplifying one half of the input waveform cycle while the other transistor amplifies the other half. The advantage of Class B amplifiers over Class A amplifiers is that no current flows through the transistors when they are in their quiescent state (i.e., with no input signal), therefore no power is dissipated in the output transistors or transformer when there is no signal present. The switching of the two complementary transistors can cause crossover distortion in the output signal. Despite this, Class B amplifiers are commonly used in battery-operated devices due to their low heat generation and high efficiency.

3.5.3 Class AB

This class some wouldn't call it a class of its own because it's merely a combination of classes A and B. However, in this context, class AB will be seen as its class because it combines the advantages of class B and class A operating modes. It utilizes class A operating mode for small signals where distortion would be most noticeable and class B mode for larger signals where efficiency is more critical. This is done by biasing both transistors in the standard push-pull configuration of a class B output stage so they are slightly turned on at idle state. This reduces the crossover distortion commonly seen in class B operation and increases idle power consumption and efficiency. Due to this class, AB amplifiers are the most common output stage in HiFi audio systems. A Class A amplifier is a type of power amplifier where the output transistor is always

3.5.4 Class D

Class D output devices also called digital amplifiers utilize a PWM. This class of amplifiers, in theory, has the highest efficiency, therefore great effort has been devoted to this approach. There are however a lot of practical difficulties regarding this approach as a sharp cut-off low-pass filter is required between the amplifier and the speaker to remove the high frequency used to amplify the signal. This usually includes inductors which are not only heavy and large but also cost quite a lot. The digital nature of this class of amplifiers also counteracts the study curriculum for this semester and therefore it will not be discussed further. The working principle of Class D can be seen in figure 3.19.

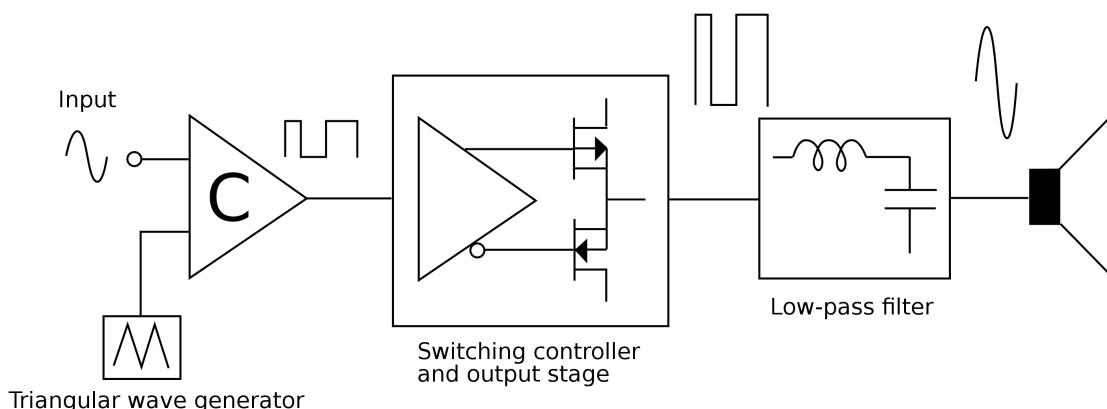


Figure 3.19: Class D amplifier working principle

3.6 Record players

Vinyl records have been used by audiophiles for over a hundred years. Vinyl records are flat discs made from polyvinyl chloride (PVC) that contain analog audio recordings. The sound is encoded onto the surface of the record in the form of V-shaped grooves, which spiral from the outer edge to the center. Each side of the V-shaped groove carries one of the two stereo recordings. The side outwards from the center carries the right channel, while the side inwards to the center carries the left channel. When a stylus, or needle, traces these grooves, it vibrates according to the recorded waveform, and reproduces the original sound.

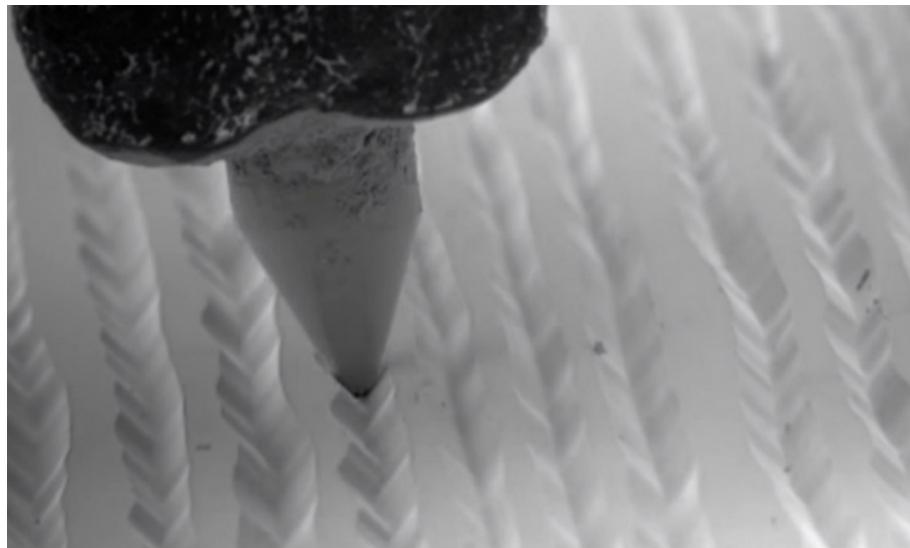


Figure 3.20: Close up of a vinyl groove

A record player consists of a couple of components to extract sound from vinyl records. The stylus, typically made from diamond or sapphire, is mounted on a cartridge, which houses an electromechanical transducer. The electromechanical part can either be a moving magnet and a stationary coil or a moving coil and a stationary magnet. As the record spins at a constant speed (33.33, 45 or 78 RPM), the stylus tracks the grooves, generating electrical signals proportional to the vibrations. These signals are then amplified and fed to speakers, where they are converted back into audible sound. When the record player reads the sound on the vinyl record, it amplifies the high frequencies and dampens the low. This is done to preserve the vinyl record and keeps the grooves small. It is referred to as the RIAA equalization curve. This became the effective standard in 1954,[11].

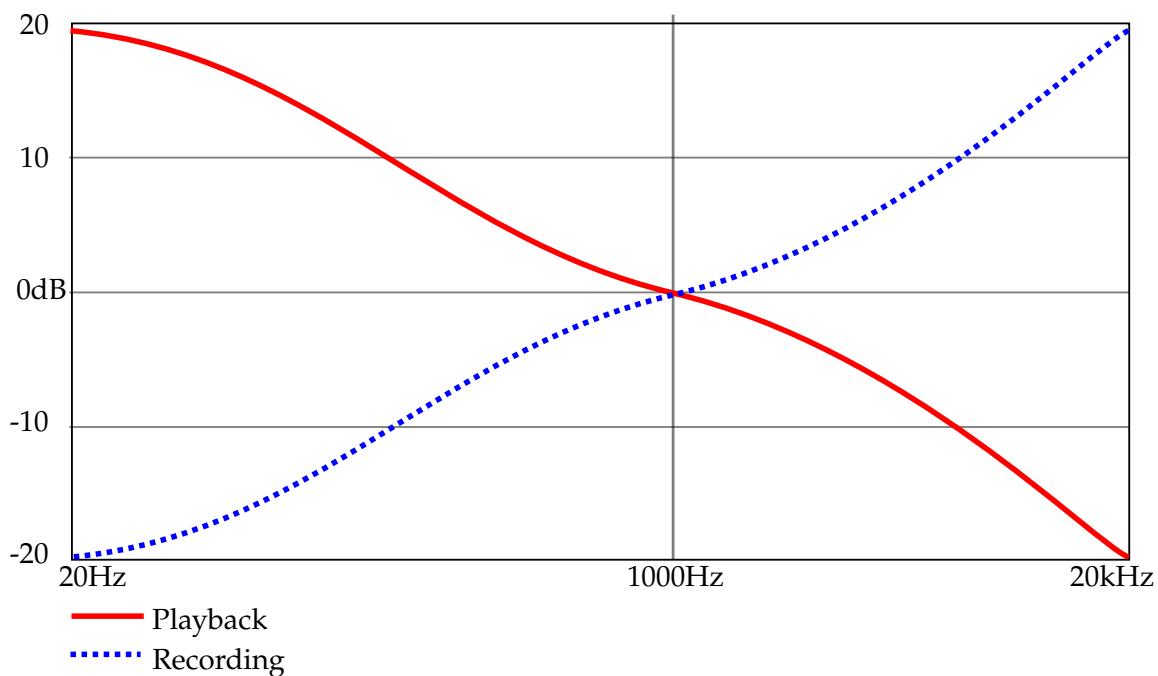


Figure 3.21: RIAA equalization curve (Playback and recording[12])

The RIAA curve is characterized by three time constants $T_3 = 3180\mu s$, $T_4 = 318\mu s$ and $T_5 = 75\mu s$. This is close to 50 Hz, 500 Hz and 2122 Hz. Some may add a roll-off time constant $T_2 = 7950\mu s$. This roll-off is called the IEC amendment and it came to be in IEC 98 1976. The reason behind this extra roll-off was to reduce subsonic frequencies from the preamplifier[13]. Apart from that, T_1 and T_6 is on each side of the audio band respectively, and therefore often ignored, they are depend on each other, and they follow the equation $T_1 \cdot T_4 \cdot T_6 \geq T_2 \cdot T_3 \cdot T_5$. If solved as $T_1 \cdot T_4 \cdot T_6 = T_2 \cdot T_3 \cdot T_5$, it simplifies the RIAA-Filter circuit a bit, and makes the calculations a bit easier as well. The gain function of the RIAA filter should follow: $G(s) = \frac{(1+T_1s) \cdot (1+T_4s) \cdot (1+T_6s)}{(1+T_2s) \cdot (1+T_3s) \cdot (1+T_5s)}$ [14]

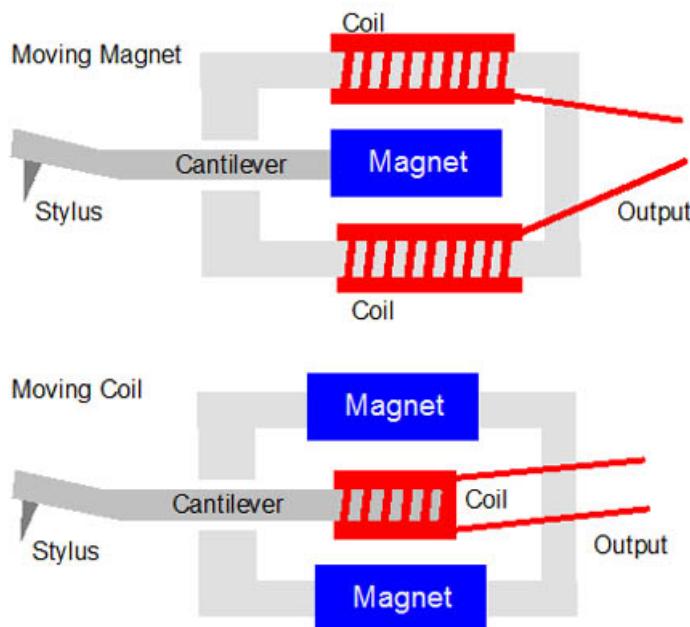


Figure 3.22: Figure showing cartridges with a moving magnet and a moving coil[15]

The difference between a moving coil cartridge and a moving magnet cartridge, is quite clear by the name. The most affordable is the moving magnet cartridge. However moving coil cartridges are often used in equipment where a clearer audio is desired, as the coil weighs less, making it easier to move by the grooves in the vinyl record. The reason the moving magnet approach is most often used, is that it is both more affordable and it produces a higher output, which leaves less work for the pre-amp.[16]

3.7 Powersupply

Power supplies come in varying different shapes and sizes, these supplies come in three principal different ways. These pros and cons are all seen from supplying the power amplifier in the circuit.

- An unregulated power supply, that consists of a transformer, rectifier, and capacitors.
- A linear regulated power supply.
- A switch-mode power supply.

In this section, only the mains supply powering the amplifier will be discussed, usually a microcontroller is deployed to handle the other rails and functionalities in the amplifier.

3.7.1 Unregulated power supply

Advantages:

- Simple, reliable, and cheap. Relatively speaking the transformer will probably be the most expensive component in the amplifier.
- No interference of instability issues from switch-mode frequencies.
- The amplifier can deliver high power on peaks.

Disadvantages:

- If a 4Ω load is connected instead of a 8Ω load the power will not be doubled since the supply voltage will fall with increased current demand. The power amplifier will on the other hand always deliver maximum power possible. (This is a simplified explanation, since the speakers impedance is frequency dependent)
- This causes significant DC ripple on the voltage rail's and therefore the amplifier needs to have significant PSRR to use such a power supply optimally.
- The main transformer will be heavy and costly.

3.7.2 Linear regulated power supplies

Advantages:

- A regulated supply-rail means that the amplifier could deliver twice the power in 4Ω that it gives into 8Ω .
- It gives absolute consistent audio power output in the face of mains voltage variation.
- The supply can be designed so it has no DC clipping on the rails.

Disadvantages:

- Linear power supplies are ineffective unless they are made very complex with the use of transistors.
- They also include a heavy and costly transformer like the unregulated supply.
- The complex linear supplies often fail, if the power amplifier fails therefore costing more transistors to repair.
- IC voltage regulators are often not powerful enough to deliver the amount of current and voltage that a power amplifier requires, therefore defaulting to the discrete transistor design.
- The power amplifier can not deliver higher power on peaks compared to the unregulated supply.

3.7.3 Switch-mode power supply

Advantages:

- Has most of the advantages of linear regulated supplies, as listed above.
- Ripple is considerably better than for unregulated power supplies but not quite as good as linear power supplies.
- There is no heavy mains transformer as in the unregulated and linear power supply, saving in overall weight.
- Can be bought as an OEM item.
- Can be specified to operate with a wide range of mains voltage.

Disadvantages:

- Switch-mode supplies are a prolific source of high-frequency interference. This can be difficult to eliminate from the audio output.
- The DC ripple such as in unregulated supplies needs to be handled as in the unregulated power supply.
- Much more complex to design and build than an unregulated power supply and therefore less reliable.
- Their design is very much a matter for specialists.

3.8 Speakers

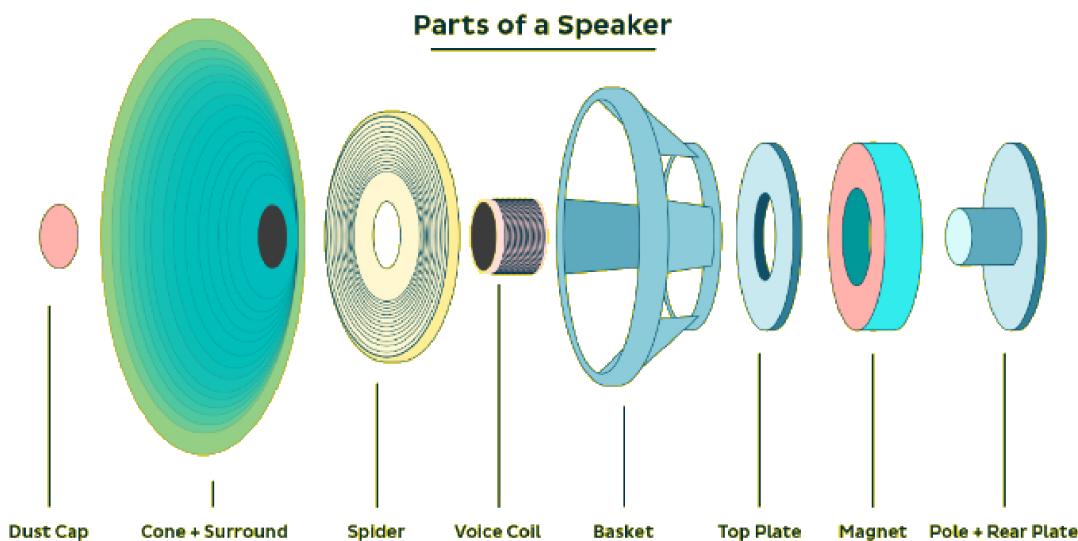


Figure 3.23: Build of a electrodynamic speaker

Speakers are transducers that convert electrical energy into acoustic energy, effectively bringing sounds to life by allowing us to hear music, voices, and other audio content from various media devices. They are ubiquitous in the modern world, featured in everything from tiny earbuds and smartphones to massive concert hall sound systems.

3.8.1 The Basic Function of Speakers

At its core, a speaker functions by using an electrical signal to move a diaphragm back and forth. This movement creates sound waves through the vibration of the diaphragm, which moves the air, thereby producing sound. The nature of this sound can vary widely in fidelity, loudness, and quality, depending on the speaker's design and the materials used.

3.8.2 Types of Speakers

Speakers come in various shapes and sizes, each designed for specific applications and acoustic environments:

- **Dynamic Speakers:** The most common type, using a magnetic field to move a cone-shaped diaphragm.
- **Electrostatic Speakers:** Known for their crisp, detailed sound, these use a high-voltage electric field to vibrate a thin, lightweight membrane.
- **Planar Magnetic Speakers:** Blend characteristics of dynamic and electrostatic speakers, using a thin membrane and magnetic fields to produce sound.
- **Horn Speakers:** Often used for their efficiency and ability to project sound over long distances, ideal for live sound applications.

3.8.3 Components of a Speaker

A typical speaker consists of several key components:

- **Driver:** The element that converts the electrical audio signal into mechanical motion.
- **Cone/Diaphragm:** Moves in response to the driver, pushing against the air to create sound waves.
- **Voice Coil:** A coil of wire that moves in the magnetic field of the permanent magnet.
- **Magnet:** Creates a stable magnetic field through which the voice coil moves.
- **Enclosure or Cabinet:** A housing that protects the internal components and can significantly influence the sound quality.

3.8.4 Speaker Performance and Specifications

Speaker performance can be evaluated based on several key specifications:

- **Frequency Response:** The range of frequencies the speaker can reproduce, typically measured in Hertz (Hz).
- **Impedance:** Measured in ohms, indicating how much resistance the speaker offers to the flow of current.
- **Sensitivity:** How efficiently a speaker converts power into sound, measured in decibels (dB).

- **Power Handling:** The amount of power, measured in watts, that a speaker can handle without damage.
- **THD:** Speakers usually have a quite high THD the speakers chosen in this project have a THD of 0.6% [17].

3.8.5 Role in Audio Systems

Speakers are integral to any audio system, serving the final and critical role in the sound chain. They can be optimized for various environments, from intimate home settings to expansive outdoor venues, each configuration bringing unique challenges and requirements. Understanding the types of speakers and their respective characteristics helps in choosing the right speaker for any audio need, ensuring the best possible listening experience.

3.9 Harmonic Distortion

Harmonic distortion is a critical concept in the realm of audio engineering and signal processing. It describes a form of signal distortion characterized by the appearance of additional frequencies in the output signal that are integer multiples of the original frequencies present in the input signal. This alteration occurs due to non-linearities in the amplification or reproduction process.

Origin of Harmonic Distortion

Harmonic distortion arises when an audio or electronic system (such as amplifiers, speakers, or other signal-processing devices) reacts non-linearly to the input signal. These non-linearities cause the output to include not only the original frequencies but also their harmonics, which can significantly alter the sound's quality.

Types of Harmonic Distortion

- **Even Harmonic Distortion:** This occurs when the distortions produce frequencies that are even multiples of the fundamental frequency (e.g., $2f, 4f, 6f, \dots$). These tend to add a certain warmth to the sound, often perceived as musically pleasing.
- **Odd Harmonic Distortion:** This involves frequencies that are odd multiples of the fundamental frequency (e.g., $3f, 5f, 7f, \dots$). Odd harmonics tend to be more harsh and dissonant and are generally less desirable in audio output.

Measuring Harmonic Distortion

Harmonic distortion is quantified by the Total Harmonic Distortion (THD)[18], which is a measure of the cumulative sum of all harmonic frequencies generated by the system relative to the fundamental frequency. THD is calculated using the following formula 3.5, where V_n is the voltage amplitude of the nth harmonic and V_1 is the voltage amplitude of the fundamental frequency:

$$\text{THD} = \frac{\sqrt{\sum_{n=2}^{\infty} V_n^2}}{V_1} \quad (3.5)$$

THD is typically expressed as a percentage, with a lower percentage indicating a cleaner reproduction of the original signal. In high-fidelity audio systems, a THD of less than 1% is usually desirable.

Minimizing Harmonic Distortion

Reducing harmonic distortion involves several techniques, including:

- **Linearity Improvement:** Designing equipment to operate more linearly over the desired range of signal amplitudes.
- **Negative Feedback:** Implementing negative feedback in amplifiers to reduce gains and thus decrease the distortion.
- **Component Quality:** Using high-quality components that inherently exhibit lower distortion characteristics.

Impact of Harmonic Distortion

The presence of harmonic distortion can have a significant impact on audio quality, affecting the clarity, color, and texture of the sound. While a certain level of harmonic distortion might be subjectively pleasing in some musical contexts, generally, high-fidelity systems aim to minimize distortion to ensure accurate reproduction of the original sound.

Understanding harmonic distortion is essential for anyone involved in the design, production, and critical listening of audio products. Managing this form of distortion is key to achieving high-quality audio performance.

4 | Specification

4.1 General Concept of The Project

4.2 Functional Requirements

4.3 System Technical Requirements

ID	Requirement	Tolerance	Traceability
T1.1	The system must have a THD < 0.9 % at 40 Hz to 12.5 kHz	0.1 %	DIN 45 500 Clause 2.3.1
T1.2	The system must have a SNR > 55 dB	1 dB	DIN 45 500 Clause 2.5
T1.3	Output power must be at least 6 W per channel	±1%	DIN 45 500 Clause 2.6
T1.4	Operating frequency range must be at least 20 Hz to 20 kHz	±1%	-

Table 4.1: Technical requirements for the Hi-Fi amplifier.

4.4 Subsystem technical requirements

4.4.1 AUX-amp

ID	Requirement	Tolerance	Traceability
T2.1	Input RMS voltage must be 316 mV (line level consumer)	-	DIN 45 500 Clause 3.1
T2.2	Output RMS voltage must be less than 1.228 V (line level pro)	±10%	DIN 45 500 Clause 3.2
T2.3	Input impedance at least 470kΩ	-	DIN 45 500 Clause 3.1
T2.4	Output impedance of maximum 47kΩ	-	DIN 45 500 Clause 3.2

Table 4.2: Technical requirements for the AUX-amp.

4.4.2 RIAA

ID	Requirement	Tolerance	Traceability
T3.1	Input impedance $47\text{k}\Omega$ parallel with 220pF	5%	IEC DS-61938-1 Section 10 Table 8
T3.2	Nominal input voltage: 5mVrms	-	IEC DS-61938-1 Section 10 Table 8
T3.3	Input voltage range: 2mVrms to 35mVrms	-	IEC DS-61938-1 Section 10 Table 8
T3.4	Output RMS voltage must be less than 1.228 V (line level pro)	$\pm 10\%$	T2.2

Table 4.3: Technical requirements for the RIAA.

4.4.3 Equalizer and Volume Control

ID	Requirement	Tolerance	Traceability
T4.1	Input RMS voltage must be less than 1.228 V (line level pro)	$\pm 10\%$	T2.2, T3.4
T4.2	Must be a 5-band graphic equaliser	-	-
T4.3	Output RMS voltage must be less than 1.228 V (line level pro)	$\pm 10\%$	T5.4

Table 4.4: Technical requirements for the equalizer and volume control.

4.4.4 Power Amplifier

ID	Requirement	Tolerance	Traceability
T5.1	Output power must be at least 6 W	-	T1.3
T5.2	Gain must be constant in the 20 Hz to 20 kHz effective frequency range	$\pm 2\text{dB}$	IEC 581-6 Clause 4
T5.3	The power amplifier must be able to operate at maximum output power for at least 10 minutes at an ambient temperature between 15°C and 35°C	-	IEC 581-6 Clause 7
T5.4	Input RMS voltage must be less than 1.228 V (line level pro)	$\pm 10\%$	-
T5.5	Input impedance at least $470\text{k}\Omega$	-	DIN 45 500 Clause 3.1
T5.6	The power amplifier must have a $\text{THD} < 0.6\%$ at 40 Hz to 12.5 kHz	0.1 %	DIN 45 500 Clause 2.3.1

Table 4.5: Technical requirements for the power amplifier.

5 | System design

This chapter outlines the details of the system design process. An overview of the system is previously illustrated by fig 3.1 where the different system blocks are shown which all will be expanded upon within the chapter.

5.1 AUX-amp

The following section explains the considerations involved in designing the AUX-preamp circuit. The main objectives here are to achieve sufficient amplification to ensure the final output matches line level pro and to get a high input and low output impedance.

5.1.1 Specifications

The specifications for the AUX-amp is outlined in table 4.2 and will be used as the key principles in the design process.

- $470\text{k}\Omega$ or higher input impedance
- $47\text{k}\Omega$ or lower output impedance
- 0.316Vrms max input
- 1.228Vrms max output

5.1.2 Topology Choices

As the preamp is a part of the small-signal chain power efficiency of this amplifier is of relatively low concern, since the current draw will be relatively small. Thus, a class A topology was chosen as it has fewer components and therefore is cheaper to produce. A class A amplifier also usually has a lower THD leading to a lower overall system THD. Noise is also a larger factor at the input as the passive noise would be larger at the input and any noise would be amplified along with the signal. The chosen topology can be seen in figure 5.1. Apart from the class A design, a simple non-inverting opamp was designed. Such a design is quite simple, and an opamp is both cheap and have a low THD, thus is an excellent candidate to a pre-amplifier which can be found in fig 5.2.

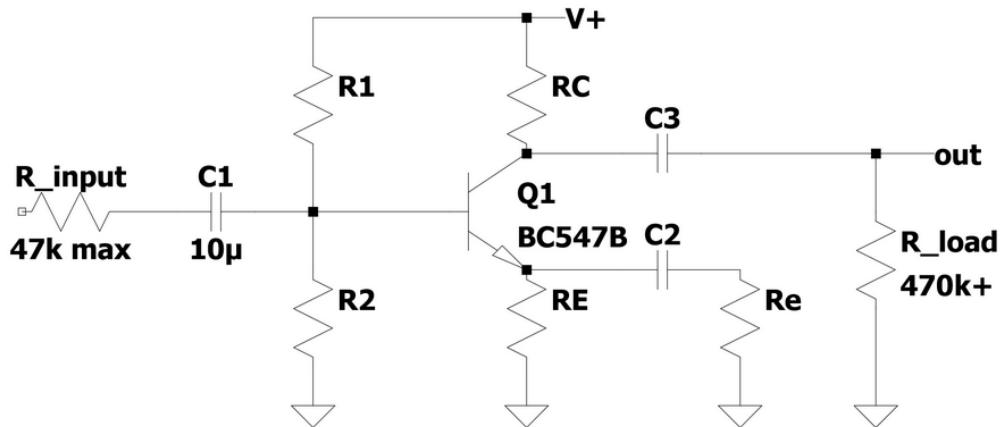


Figure 5.1: Pre-amp class A topology design

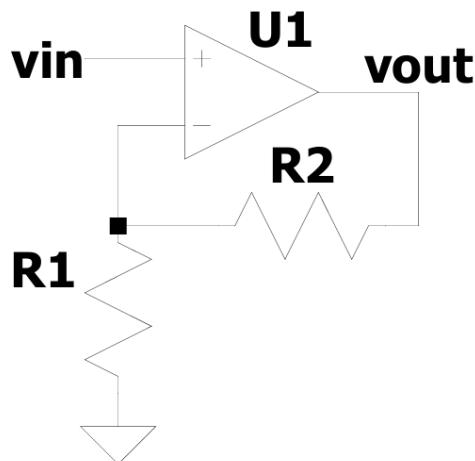


Figure 5.2: Pre-amp non inverting topology design

5.1.3 Theoretical Design

The following section will contain the theoretical design of both the opamp pre-amp and the class A amplifier.

Opamp pre-amp

The gain can be calculated by the following equation $A_v = 1 + \left(\frac{R_2}{R_1}\right)$. To go from consumer line level to pro line level a gain of 3.89 is required. R_1 is chosen to be $1k\Omega$ and then the remaining resistor is found to be $R_2 = 2.88k\Omega$ (as this is the value closest to 2.89 in the E96 series). Apart from this, a large resistor of $499k\Omega$ is placed between the positive input and ground, to ensure a sufficient input impedance and eliminate a floating input.

Class A

The first thing to consider when designing the class A amplifier is the input and output impedance along with the desired gain. The gain should be 3.89, and the input impedance should at least be $470k\Omega$. The first step in designing a class A amplifier with a BJT, is to find V_C , it must be below V_{CC} which is 30V, it must also be above $V_{R_E} + V_{CE,sat}$. $V_{CE,sat}$ can be found from the transistors data-sheet, here the BC547 was chosen, as this was readily available, the value is at max 600 mV at $I_C = 100mA$ and $I_B = 5mA$ [6]. The maximum will be used, since there is lots of room for V_C , and it is better to choose a point a bit too high, to minimize the risk of clipping. V_{R_E} is chosen as 6 V, because this gives more than enough of space for the amplifier to operate in. This results in $V_C = 6.6V$, from this large resistor values were calculated for R1 and R2, the values were chosen with the help of V_C with a chosen current of $10\mu A$. $10\mu A$ was chosen since this will draw little power, and lead to large bias resistors, the only negative impact, is that a considerable amount of current goes into the resistor.

$$R1 = \frac{30V - 6.6V}{10\mu A} = 2.34M\Omega$$

$$R2 = \frac{6.6V}{10\mu A} = 660k\Omega$$

To calculate the approximate gain the equation $-A_v = \frac{R_C}{R_E}$ As a rule of thumb the emitter resistor should be within the following: $\frac{1}{2}$

$$R_E \gg \frac{R_{bias}}{\beta} \approx 1.6k\Omega$$

Here R_{bias} is the resistance of the biasing resistors in parallel. β is a transistor parameter for common-emitter current gain[19] and can also be found in the datasheet where the average value of 325 was chosen. R_E should be a lot larger than $1.6k\Omega$ so $6k\Omega$ was chosen. It was then chosen as $R_E = 6k\Omega$ and then R_C is calculated to be $23.3k\Omega$.

R_e was chosen as $100k\Omega$ and was to be later adjusted by simulation if necessary. This is adjusted until the right gain is obtained.

The input impedance is then calculated. The input impedance should be equal to the following equation (Here the resistors on the emitter of the transistor is multiplied by its β):

$$R_{input} = R1 || R2 || (\beta \cdot (R_E || R_e)) = 400k\Omega \quad (5.1)$$

This means that the bias resistors should be increased, to adhere to the input resistance requirement of $470k\Omega$.

Class A small signal model

It is desirable to draw the small signal model of the circuit, to gain insight into the design. For this the first thing that is done is drawing the small signal equivalent circuit.

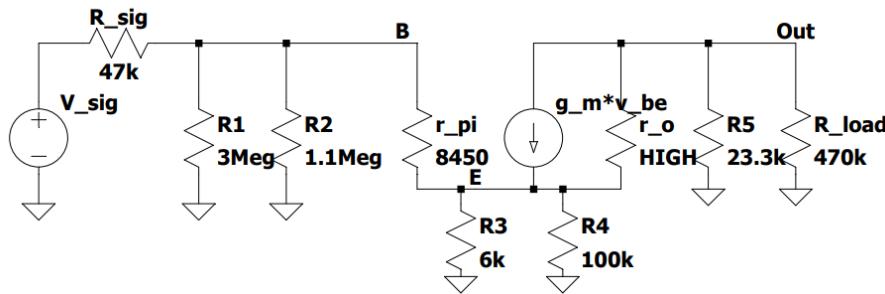


Figure 5.3: Pre-amp small signal equivalent[19]

To find r_π the following equation is used $r_\pi = \frac{V_{be}}{I_B}$ where V_{be} is 600mV. The current from the emitter is $I_E = 1mA$, the input must then be $I_B = \frac{I_E}{\beta}$.

$$I_B = \frac{1mA}{325} = 3\mu A$$

$$r_\pi = \frac{V_{be}}{I_B} = 200k\Omega$$

To calculate the current of the current source g_m must be found where $I_E \approx I_C \approx 1mA$.

$$g_m = \frac{I_C}{V_T}$$

$$V_T = 26 \cdot 10^{-3}V$$

$$g_m = 0.038S$$

The current source is dependent on V_{be} , it is known that the voltage at the base is $V_b = 6.6V$, while the voltage at the emitter is $V_e = V_{RE} \approx 6V$. This means the current source is equal to $0.6V \cdot 0.038S = 22.8mA$.

$$r_o = \frac{1}{\frac{h_{oe} - (1 + \beta)}{\frac{r_\pi}{h_{re}}}}$$

Since the only h-parameter that is available in the data-sheet is h_{fe} , r_o is simply assumed to be high.

The input resistance is calculated with the small signal model. This is calculated as:

$$R_{input} = R2 || R1 || (r_\pi + \frac{1}{\beta \cdot R_E} + \frac{1}{\beta \cdot R_e})$$

$$R_{input} \approx 410k\Omega$$

5.1.4 Simulation

During simulation it was clear that the Class A was biased wrong. This was solved by increased R_1 to $3M\Omega$ and R_2 to $1.1M\Omega$. The reason that this change was necessary is that a considerable amount of the current goes into the transistor, and then R_2 has to be larger to maintain the right voltage at the base of the transistor.

For the simulation a 1 kHz consumer line signal was simulated as the input. The output was then expected to be a pro-line level 1 kHz signal. The program which was used for the simulation was LTspice. Simulation for the class A can be seen in fig 5.4 and for the non-inverting opamp in fig 5.5.

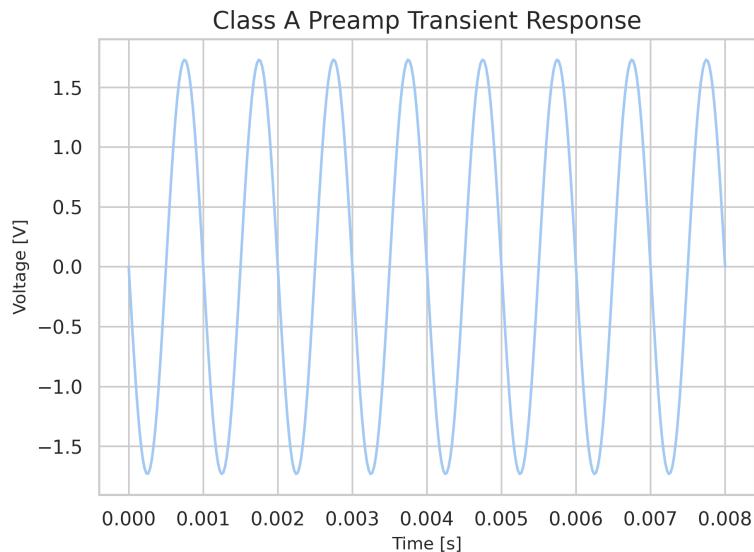


Figure 5.4: Simulated output of class A pre-amp

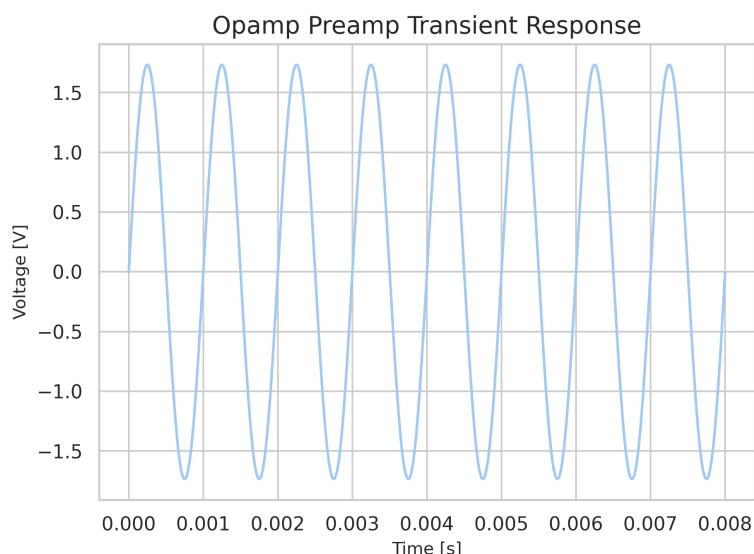


Figure 5.5: Simulated output of a non-inverting opamp

It is clear from the figures that the output is 1 kHz pro-line level.

Along with this, the THD was simulated, $THD = 0.0037\%$ for class A and $THD = 0.000091\%$ for the non-inverting opamp. The THD was simulated with the following LTspice directive:

```
.four 1000 5 8 V(out)
```

5.1.5 Conclusion

It is possible to conclude that a class A and non inverting opamp preamplifier has been designed and that the simulation is nearly identical to the expectations from the design.

5.2 RIAA

The following section delves into the considerations made to achieve the design of the RIAA circuit. The central elements here are achieving the RIAA equalization curve and sufficient gain so that the final output is line level pro as the rest of the preamplifiers.

5.2.1 Specifications

The specifications outlined in table 4.3 from section 4 are the guiding principles for the system design. The maximum input voltage has been chosen to be 5mVrms since its within the range given by the table and in Small Signal Audio Design by Douglas Self the input voltage range on average is between 3.5mVrms to 6mVrms [13]. Lastly, the IEC amendment time constant will be included along side a filter for high frequency roll off(T_6) for completeness and reducing ultrasonic signals.

5.2.2 Topology Choices

For the choice of topology, the deciding factor is the time constants. The 4 filter configurations shown in fig 5.6 and their corresponding impedances in eq 5.2 are all capable of RIAA equalization as described by the Lipshitz paper [14].

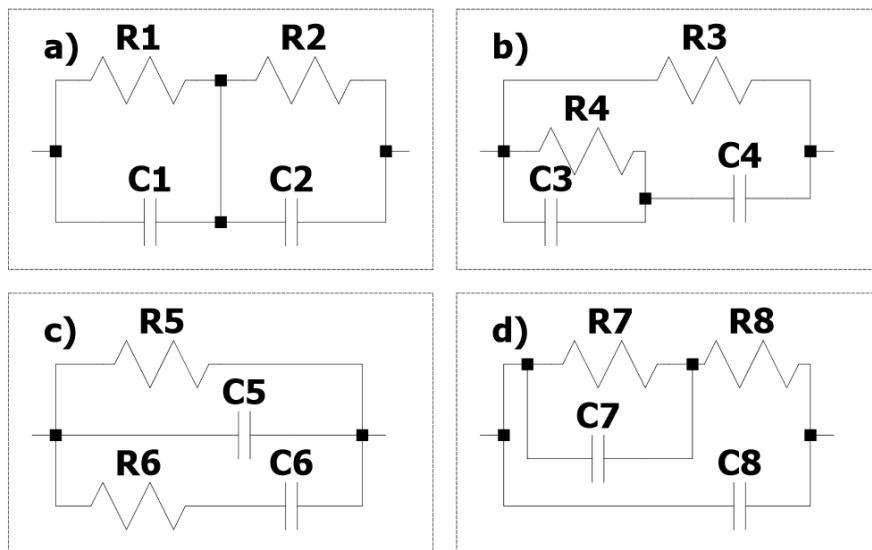


Figure 5.6: Filter configurations for RIAA equalization.

$$\begin{aligned}
 \text{a)} \quad Z(s) &= \frac{(R_1 + R_2)[1 + \frac{R_1 R_2}{R_1 + R_2} (C_1 + C_2)s]}{(1 + R_1 C_1 s)(1 + R_2 C_2 s)} \\
 \text{b)} \quad Z(s) &= \frac{R_1 [1 + R_2(C_1 + C_2)s]}{1 + [R_1 C_1 + R_2(C_1 + C_2)]s + R_1 C_1 R_2 C_2 s^2} \\
 \text{c)} \quad Z(s) &= \frac{R_1(1 + R_2 C_1 s)}{1 + [R_1(C_1 + C_2) + R_2 C_1]s + R_1 C_1 R_2 C_2 s^2} \\
 \text{d)} \quad Z(s) &= \frac{(R_1 + R_2)[1 + \frac{R_1 R_2}{R_1 + R_2} C_1 s]}{1 + [R_1(C_1 + C_2) + R_2 C_2]s + R_1 C_1 R_2 C_2 s^2}
 \end{aligned} \tag{5.2}$$

Among these circuits "a)" is chosen since its mathematical computations are simpler due to the impedance calculations consisting of the sum of the series connection of the resistors and capacitors. This configuration consists of two low pass filters and a high pass filter covering the time constants from T_3 until T_5 . Two additional filters are required to necessitate T_2 (IEC amendment) and T_6 the high frequency roll which both are chosen to be LP filters. Since the requirements state an output voltage of 1.228Vrms an active component such as an OPAMP is required inorder to have the necessary gain to achieve such output levels. As such an OPAMP will be used in the filter section and an inverting OPAMP configuration will be placed in series afterwards to achieve line level pro out. Lastly, an input impedance of 47kOhm and a matching capacitor is required with a value of 220pF. The final topology is seen in fig 5.7.

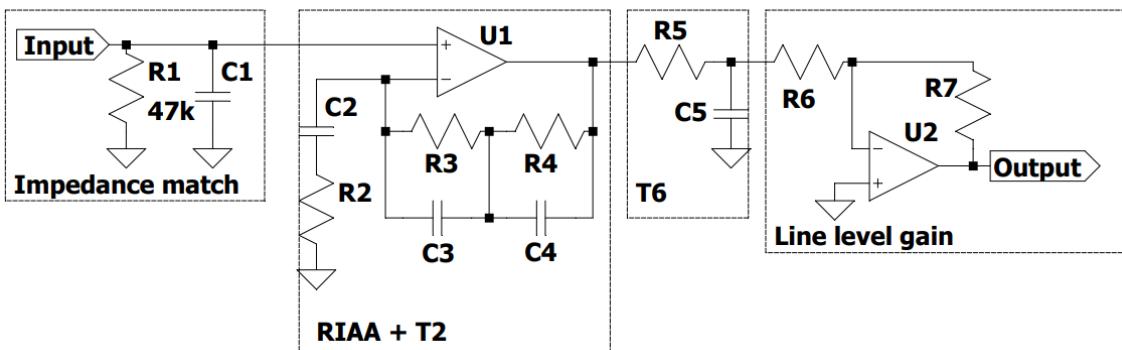


Figure 5.7: RIAA system.

The two low pass filters for T_2 and T_6 are comprised of R_2 , C_2 , R_5 , and C_5 respectively.

5.2.3 Theoretical Design

The known time constants and their frequencies alongside a desired output gain from the RIAA circuit are all variables that will dictate the design process. The goal is firstly to determine f_1 and f_6 and then work backwards calculating the component values for the different filters. The following equations used for calculating the component values are all derived from the Lipshitz paper and the same design procedure is applied here [14].

The circuit shown in fig 5.8 is taken from the Lipshitz paper where the difference from the topology fig 5.7 is R_8 . However to simplify calculations R_8 can be chosen to equal 0 therefore is not shown in the previous section.

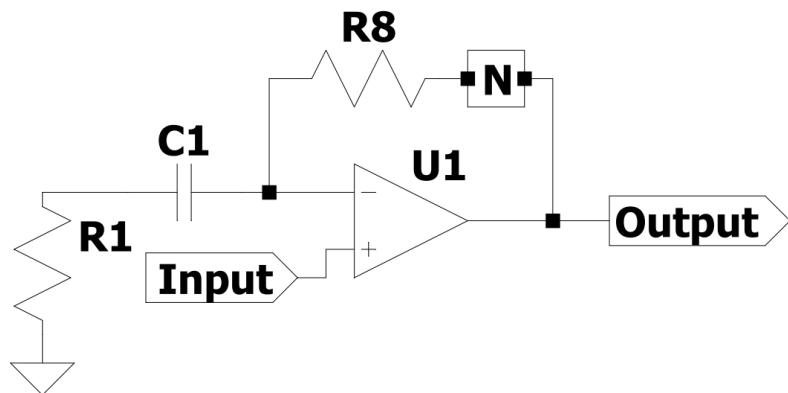


Figure 5.8: RIAA de-emphasis circuit as per Lipshitz.

N is equivalent to the filter configuration chosen in subsection 5.2.2. With this configuration the frequency response will take shape as shown in fig 5.9.

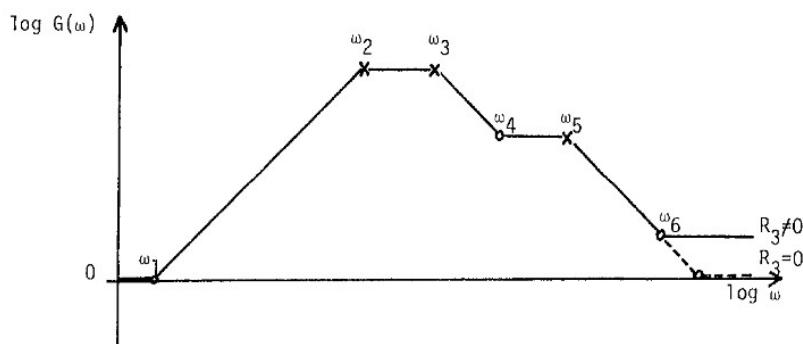


Figure 5.9: Transfer function of the RIAA curve and system[14].

The given frequencies from the figure are listed here:

$$\omega_2 = 2\pi f_2$$

$$\omega_3 = 2\pi f_3$$

$$\omega_4 = 2\pi f_4$$

$$\omega_5 = 2\pi f_5$$

$$f_2 = 20.02 \text{Hz}$$

$$f_3 = 50.05 \text{Hz}$$

$$f_4 = 500.5 \text{Hz}$$

$$f_5 = 2122.1 \text{Hz}$$

$$T_2 = \frac{1}{2\pi f_2} = 7.95 \cdot 10^{-3} \text{s}$$

$$T_3 = \frac{1}{2\pi f_3} = 3.18 \cdot 10^{-3} \text{s}$$

$$T_4 = \frac{1}{2\pi f_4} = 317.99 \cdot 10^{-6} \text{s}$$

$$T_5 = \frac{1}{2\pi f_5} = 75.00 \cdot 10^{-6} \text{s}$$

Seeing that the total gain is split into two parts the gain at the RIAA filter is chosen to be 30dB at 1kHz then the theoretical gain at 20.02Hz should be 49.9dB which is visualized from fig 5.9. Moving forward the frequency of f_1 can be determined by figuring out the gain difference between f_1 and f_2 since f_1 has 0dB gain. Which leads to equation 5.3 that calculates the output level for f_2

$$49.9 = 20 \cdot \log_{10}\left(\frac{x}{1}\right) \Leftrightarrow x = 312.607 \quad (5.3)$$

Thus, f_1 can be expressed by dividing f_2 with the obtained output level

$$f_1 = \frac{f_2}{312.607} = 0.064\text{Hz}$$

From this point f_6 can be found now that f_1 has been obtained which is done in equation 5.4

$$f_6 = \frac{f_2 f_3 f_5}{f_1 f_2} = 66.338\text{kHz} \quad (5.4)$$

With all the frequencies known the component values can be calculated. R_2 is a free variable and is chosen to be $5\text{k}\Omega$. Then R_3 and R_4 can be calculated in the following way:

$$R_3 = R_2 \frac{T_5(T_1 - T_3) \cdot (T_3 - T_4) \cdot (T_3 - T_6)}{T_1 T_4 T_6 (T_3 - T_5)} = 1.44\text{M}\Omega$$

$$R_4 = R_2 \frac{T_3(T_1 - T_5) \cdot (T_4 - T_5) \cdot (T_5 - T_6)}{T_1 T_4 T_6 (T_3 - T_5)} = 118.41\text{k}\Omega$$

For the capacitors the following equations are used:

$$C_3 = \frac{T_2}{R_2} = 1.59\mu\text{F} \quad C_4 = \frac{T_5}{R_3} = 2.21\text{nF}$$

Then for the high frequency roll off (f_6) either R_5 or C_5 can be freely chosen. Here the value of the capacitor C_5 is picked to be 1.6nF since the physical selection of resistor values are more plentiful than capacitors. Thus calculating R_5 is given by

$$R_5 = \frac{T_6}{C_5} = 2\text{k}\Omega$$

With this, the component values for the RIAA de-emphasis filter are finalized. Proceeding from here the values of the second stage of gain must be calculated. The known value of the output from the RIAA circuit is 158.1mVrms and the final output voltage is required to be 1.228Vrms to achieve line level. Hence, the gain value may be computed utilizing the subsequent formula for an inverting operational amplifier

$$\text{Gain(Av)} = -\frac{V_{out}}{V_{in}} = -\frac{R_7}{R_6} \quad \frac{1.228\text{Vrms}}{158.1\text{mVrms}} = -7.76 [.]$$

$$20 \cdot \log(-7.76) = 17.79\text{dB}$$

Hereafter acquiring Av finding one of the resistor values is easily solvable by choosing an appropriate resistor size for either R_6 or R_7 .

Considering impedance matching between the second gain stage and the RIAA equalization circuit alongside the low pass filter responsible for T_6 , the resistor R_6 is chosen to be $154\text{k}\Omega$ since a larger value minimize its influence on the RIAA equalization. However, as R_5 is in series with R_6 the final resistance is $156\text{k}\Omega$. From here R_7 can be found by substituting the now-chosen value for R_6 into this equation

$$A_v = -\frac{R_7}{R_6} \quad 7.76 = -\frac{R_7}{154\text{k}\Omega + 2\text{k}\Omega} \Leftrightarrow R_7 = 1.21\text{M}\Omega$$

Thus all component values have been found hereafter an OPAMP must be chosen to suit the different stages. Among the choices from "Komponenten" TLC274 is the most readily available component and was therefore decided upon.

5.2.4 Simulation

The fig 5.8 shown in section 5.2.2 yields the following frequency response seen in fig 5.10 which has been simulated using LTspice.

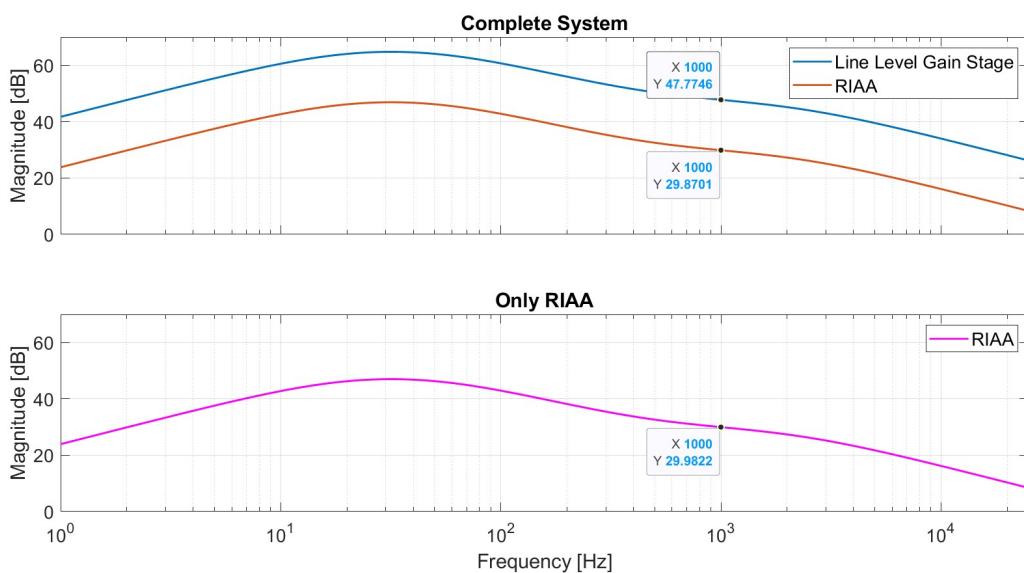


Figure 5.10: Frequency response of the complete system where the blue graph depicts the final output, orange the output after R_5 , purple with the inverting stage disconnected.

Illustrated by the figure the difference between the RIAA filter with and without the inverting OPAMP connected results in 0.1121dB which can be attributed to impedance matching. This can further be mitigated by increasing R_6 and subsequent R_7 for better impedance matching, however as the final output gain results in an output voltage of

$$47.7746\text{dB} = 20\log_{10} \frac{V_{out}}{5\text{mVrms}} \Leftrightarrow V_{out} = 1.223\text{Vrms} \quad (5.5)$$

and is deemed sufficient since it is within $\pm 10\%$ tolerance given by the specification table 4.3.

The THD is simulated for the RIAA filter with preamp. The simulation is done with the following LTSpice directive.

```
.four 1000 5 8 V(Out)
```

The THD is simulated to 0.047493% which is deemed adequate for the RIAA filter to not affect the sound quality.

5.2.5 Conclusion

In summary, the RIAA equalization curve has been achieved, and a sufficient final output signal voltage. However, the simulated differs slightly from the calculated values due to impedance matching between the subcircuits.

5.3 Equalizer

This section will go into detail, with the design choices of the equalizer. The equalizers task is to attenuate chosen frequencies, while boosting others, such that when listening to music, it is possible to adjust the audio as to ones desires. As described in the technical analysis 3.3.

The first thing to decide is which kind of equalizer is chosen to design. Here the main contenders are a parametric equalizer and a graphic equalizer, the graphic equalizer is chosen as this fills the specifications of the amplifier system,4.4.3.

The second thing to decide is, how many bands the equalizer should contain. In this case, 5 bands were chosen. The midpoints for the different bands were chosen as 60 Hz, 250 Hz, 1 kHz, 4 kHz and 16 kHz. This results in the different frequencies being 4 times of each other, this is called a two-octave equalizer. This is only approximately true for 60 Hz to 250 Hz, but the use of capacitors will emit some error due to the tolerance of the components, so in this case there is not much of a difference between 60 Hz and 62.5 Hz.

5.3.1 Specifications

- 1.228 Vrms Max Input
- 1.228 Vrms Max Output
- Input impedance Minimum 47 kohm
- 5-Bands (60 Hz, 250 Hz, 1 kHz, 4kHz and 16 kHz)

5.3.2 Topology Choices

The Equalizer will need 5 band pass filters, which is adjusted with a potentiometer each. The first important decision to make, is if the filters should be passive or active. The main advantage of passive filters, is that they are always stable. One of the other main advantages is that they do not require any power supply. However, it has already been established, that power supply to opamps is required by other modules, so it is not an issue.

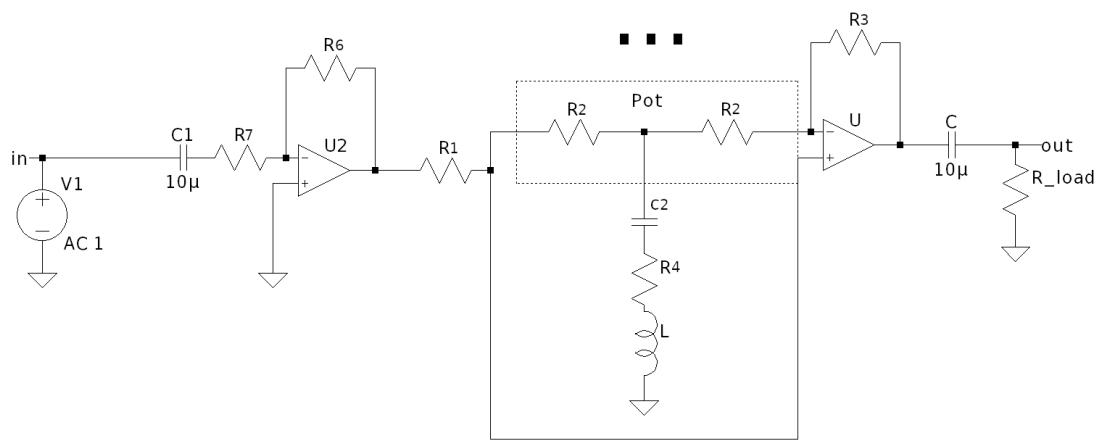


Figure 5.11: The Chosen Equalizer Topology[20]

5.3.3 Theoretical Design

Simulated Inductors

It is decided to go with active filters, this is done by replacing the inductor with a simulated inductor. The primary reason for this is that there are many disadvantages of inductors (availability, size, crosstalk, price).

A simulated inductor can be created with an opamp, 2 resistors and a capacitor, as seen in figure 5.12

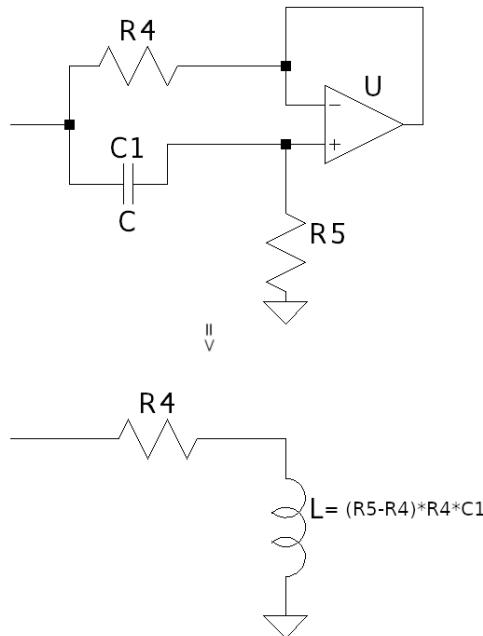


Figure 5.12: Circuit and formula for inductor simulated with opamp

This circuit can be used to replace the coil in the topology in figure 5.11. Please notice that R4 is the same resistor as in figure 5.11

Component Values of Single Band

For the design of the equalizer, one must first consider which Q-factor should be used for the filter. For a two-octave equalizer, the desired Q-factor is 0.85, [20]. The first step to designing a band of the equalizer, is to find the desired inductive reactance X_L .

$$X_L = 2 \cdot \pi \cdot f_0 \cdot L \quad (5.6)$$

From the inductive reactance and the R4 resistor in figure 5.11 and 5.12, the Q-factor can be found.

$$Q = \frac{X_L}{R4} \quad (5.7)$$

The simulated inductors value is found with the following equation.

$$L = (R5 - R4) \cdot R4 \cdot C1 \quad (5.8)$$

And the resonant frequency can be found by using the inductance of the simulated inductor and the capacitance of C2, [20].

$$f_0 = \frac{1}{2 \cdot \pi \sqrt{L \cdot C2}} \quad (5.9)$$

the equation for X_L and the equation for Q can be used to solve for L . From this we can derive the relation between L and R4.

$$\frac{Q}{2 \cdot \pi \cdot f_0} = \frac{L}{R4} \quad (5.10)$$

Then a value for R4 is picked, $R4 = 470\Omega$ and a frequency of $f_0 = 60Hz$ can be chosen, L is calculated from that.

$$L = \frac{R4 \cdot Q}{2\pi \cdot f_0} = \frac{470 \cdot 0.85}{2 \cdot \pi \cdot 60} \quad (5.11)$$

$$L = 1.06H \quad (5.12)$$

This would be a quite large inductor luckily that is not a problem as the inductor will be simulated with the circuit seen in figure 5.12. The electromagnetic field of such a large inductor would also have needed to be taken into account, since it could be noisy to surrounding electronics.

The next step would be to choose some of the values which make up the simulated inductor. Here R5 is chosen as $100k\Omega$, The reasons for this, is that in this design it kept simple, by only varying in the size of the capacitors. Some might argue, that is smarter to pick a specific capacitor value, as the supply of differently valued resistors is better than the supply of differently valued capacitors. The reason this is not the case here, is that R1 and R3 in figure 5.11 is dependent on the desired gain, and the resistors R4 and R5. The values for the resistors R1 and R3 can be solved as

$$R1 = R3 = \frac{R4}{Av} \quad (5.13)$$

as long as R4 is much smaller than R5.

Then we can calculate C1 from the equation for the simulated inductor.

$$C1 = \frac{L}{(R5 - R4) \cdot R4} \quad (5.14)$$

$$C1 = 23nF \quad (5.15)$$

Now to design the 60Hz band $f_0 = 60Hz$, the Q-factor should be 0.85. From this we can start by solving for $L \cdot C2$.

$$L \cdot C2 = \frac{1}{2 \cdot \pi \cdot f_0}^2 \quad (5.16)$$

$$L \cdot C2 = 7.04 \cdot 10^{-6} \quad (5.17)$$

C2 can be found from the relation between L and C2.

$$C2 = \frac{7 \cdot 10^{-6}}{1.06} \quad (5.18)$$

$$C2 = 6.6\mu F \quad (5.19)$$

The same procedure is used to calculate the rest of the band-pass filter value.

The only remaining thing to do, is to make the equalizer have unity gain. At first this was done by using an opamp at the end of the equalizer, thus attenuating the overall signal. However, in practice, there were problems with the opamps clipping in the equalizer part. Which lead to attenuating the signal before, instead of after.

Since this solved both problems. The attenuation is simply made by varying R6 and R7, according to the equation for inverting OPAMPS.

$$Av = -\frac{R6}{R7} \quad (5.20)$$

This attenuation should be equal to half the equalizers dynamic range, since the standard design had an unnecessarily large dynamic range, this was changed to $\pm 7dB$ which is equal to 2.24 gain/attenuation.

To calculate the value of R1 and R3 the value of R4 is needed, along with the desired gain/attenuation.

$$R1 = R3 = R4 \cdot (Av - 1) \quad (5.21)$$

$$R1 = R3 = 470 \cdot (2.24 - 1) \approx 604\Omega \quad (5.22)$$

The R6 and R7 relationship should attenuate $Av = 2.24 \cdot 1.41^5 = 12.5$. It was later discovered that this would still cause clipping in the opamps, to solve this 15 db extra attenuation was added before, and then an inverting opamp with a gain of 15 dB is

placed after the equalizer. Thus the values of the inverting opamp became $R1 = 232\Omega$ and $R2 = 1.21k\Omega$, and the values of R6 and R7 became $R7 = 500k\Omega$ and $R6 = 41.2k\Omega$.

The final Eq circuit can be seen in figure 5.13

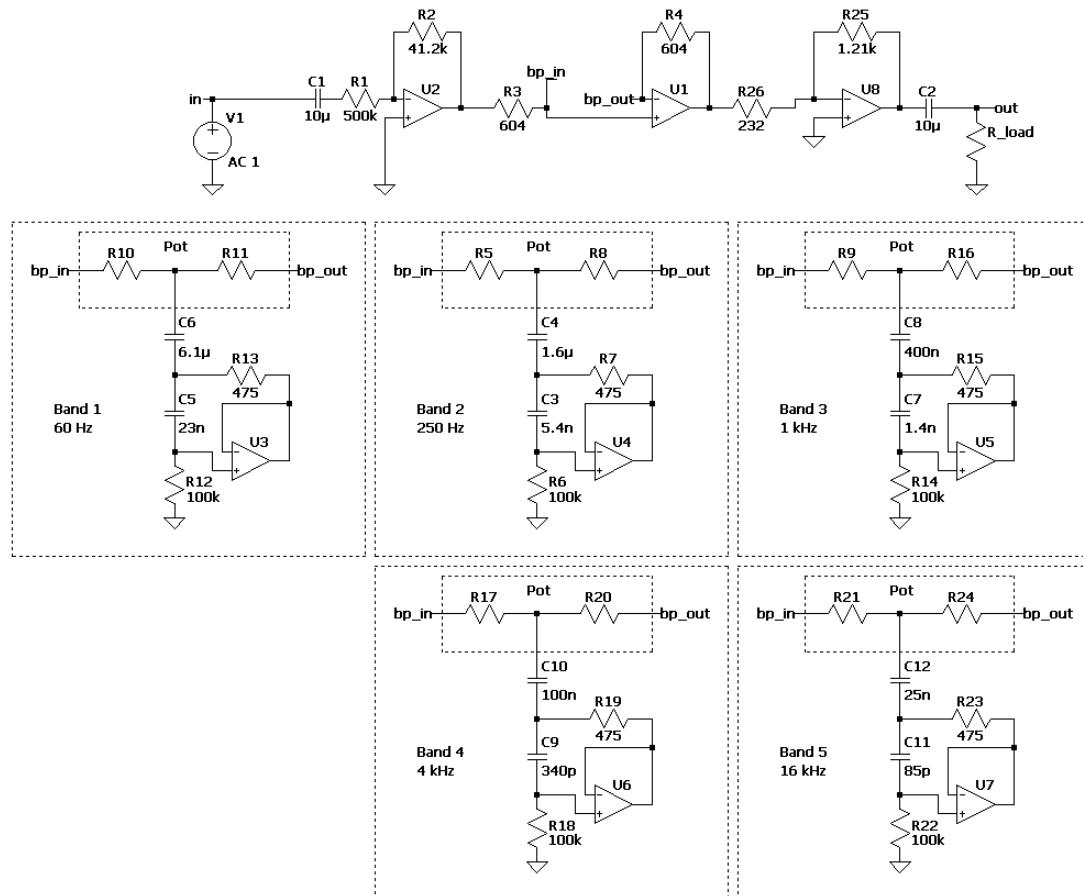


Figure 5.13: The final Eq circuit

5.3.4 Simulation

Since $10k\Omega$ potentiometers was what was readily available, they were used. This meant that $10k\Omega$ potentiometers were used for the simulation, when changing the size of the potentiometers, A larger potentiometer equates to a smaller dynamic range for the equalizer. This is not a huge issue, as there are no exact demands to the dynamic range of the equalizer, hence it is only needed to scale the aforementioned attenuation so that the equalizer would take Pro-Line level in, and output the same level when turned up to max.

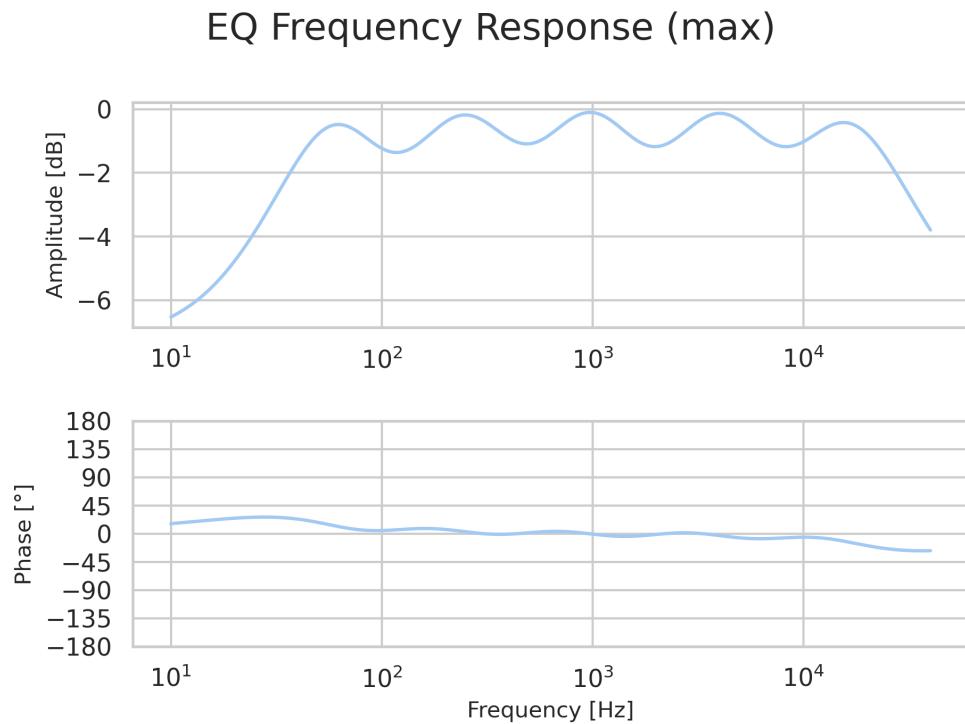


Figure 5.14: Frequency response of 5-band Eq with all bands high

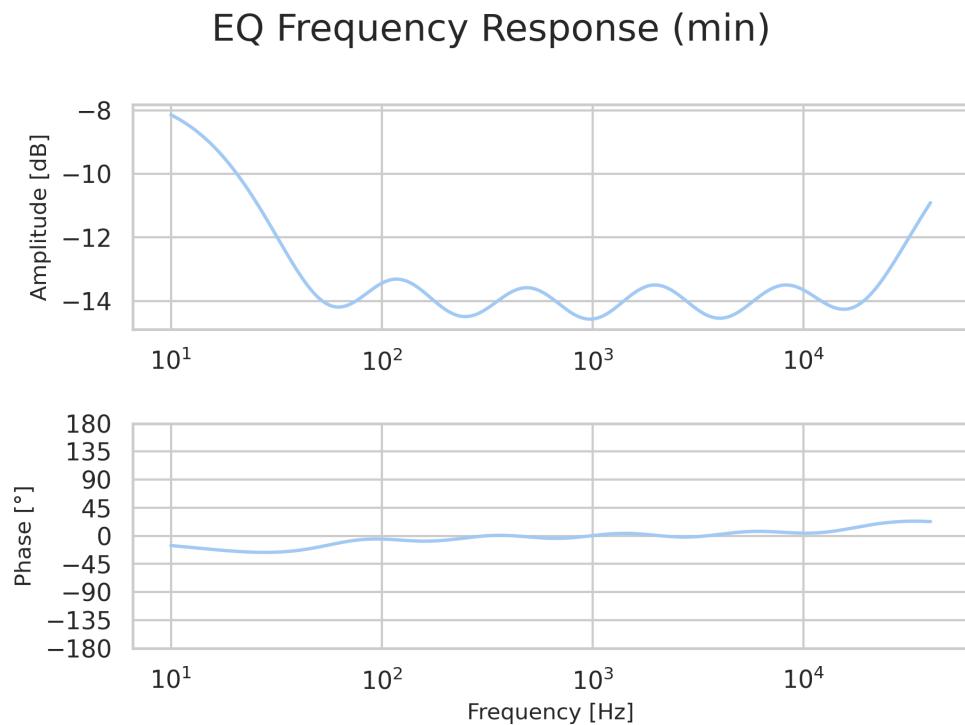


Figure 5.15: Frequency response of 5-band Eq with all bands low

5.3.5 Conclusion

As the LTspice simulations of the theoretical design shows a characteristic graphical equalizer curve, as well as the right gain for both maximum and minimum. It is concluded that the equalizer design is complete.

5.4 Volume Control

The volume control allows the user to adjust the amplitude of the signal in turn adjusting how loud the speakers will play.

5.4.1 Specification

The volume control should not output more than 1.228V RMS (pro line level). The input of the volume control should also never exceed 1.228VRMS. These specifications can be seen in section 4.4.3

5.4.2 Topology Choices

The Baxendall volume control topology was chosen, as it is the most common. This topology can be seen in figure 5.16

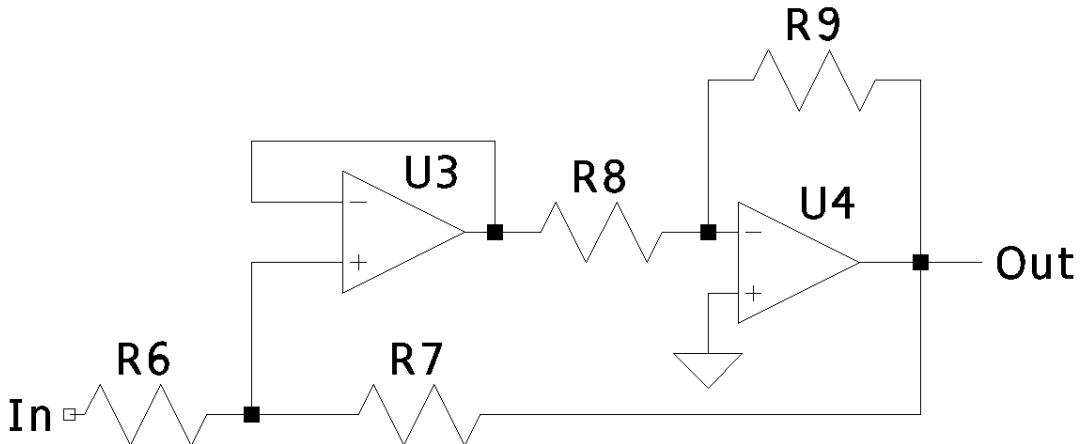


Figure 5.16: A general Baxendall volume control circuit. R6 and R7 would normally be a potentiometer

5.4.3 Theoretical Design

as the input max and the output max are the same, the max volume of the volume controller should be unity gain. To do this R9 and R8 on figure 5.16 should be equal. R6 and R7 are controlled with a potentiometer to get volume control with unity gain.

the chosen R9 and R8 values were 1kΩ and a 4.7kΩ potentiometer was used.

5.4.4 Simulation

This circuit was simulated with many different potentiometer positions, this can be seen in figure 5.17

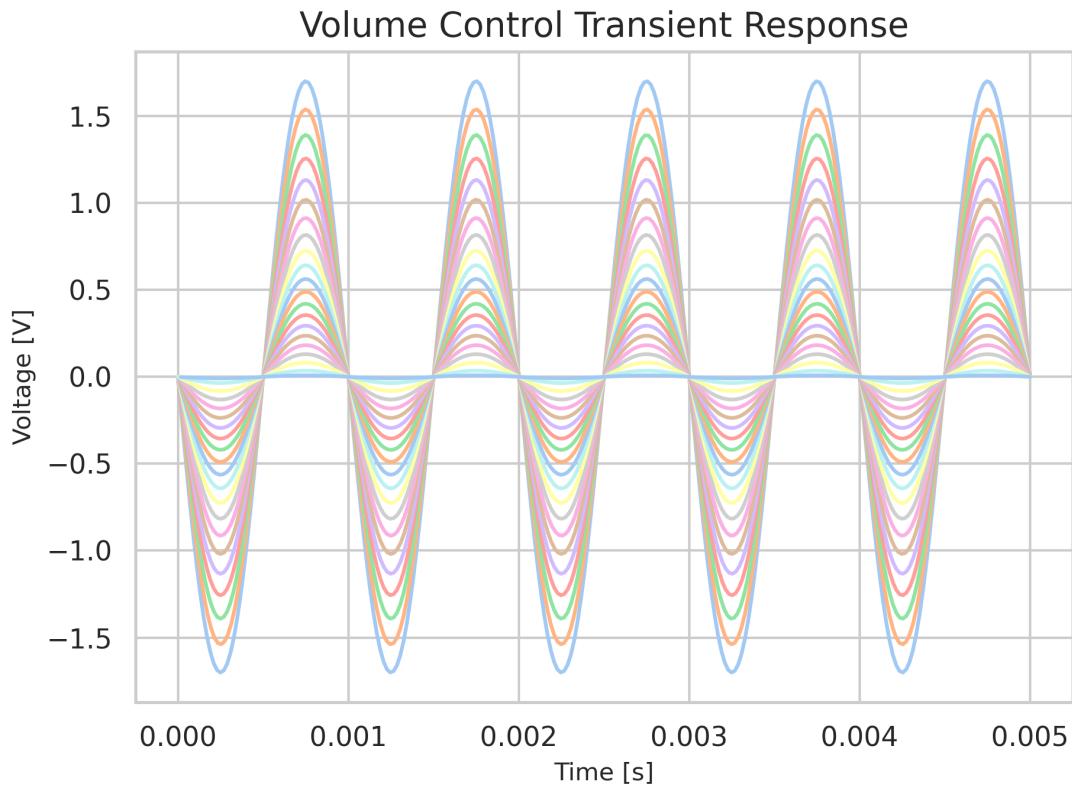


Figure 5.17: A monte-carlo simulation of the Baxendall volume controller

5.4.5 Conclusion

in the end, a Baxendall volume control with unity gain was designed constructed and tested successfully

5.5 Filtering

The last block before a power amplifier is usually a sub-sonic and ultra-sonic filtering block. This section will cover the design and simulation of such filters to dim unwanted frequencies reaching the power amplifier.

5.5.1 Specifications

The specifications for the filter are chosen as follows:

- Pass-band from 20Hz to 20kHz as per T1.4 in chapter 4.
- Maximally flat pass-band to not distort the signal.
- 0dB gain in pass-band.
- Quality factor Q of 0.707 to not distort the signal unnecessarily while keeping sharp corners.
- 40dB attenuation per decade to adequately filter out unwanted frequencies.

5.5.2 Topology Choices

To fulfill the above requirements a Butterworth filter response is chosen to provide the maximally flat pass-band response with no ripple. This filter response can also fulfill the Q factor requirement as the response has a Q factor of 0.707. The filter topology used to realize the filter is the sallen-key topology which means that by cascading a low pass filter and a high pass filter the band-pass filter can be achieved. The filter topology can be seen in figure 5.18.

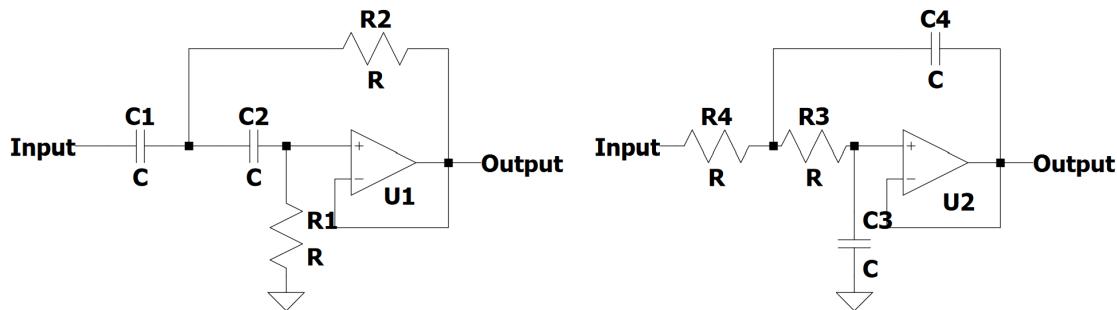


Figure 5.18: Sallen-key topology first a High pass then a Low pass

5.5.3 Theoretical Design

By cascading the high-pass and low-pass filter seen above a 4th-order band-pass filter is achieved. The standard transfer function for such a filter can be seen in the equation below [2].

$$H(s) = \frac{Ks^2}{(s^2 + \frac{\omega_{01}}{Q_1}s + \omega_{01}^2)(s^2 + \frac{\omega_{02}}{Q_2}s + \omega_{02}^2)} \quad (5.23)$$

High pass

The cutoff frequency of the high pass filter is given by [2]:

$$\omega_{02} = \frac{1}{\sqrt{R_1 \cdot C_2 \cdot R_2 \cdot C_1}} \quad (5.24)$$

The quality factor, when the gain is 1 is given by the following equation[2]:

$$Q_2 = \frac{\omega_{02}}{\frac{1}{R_1 \cdot C_2} + \frac{1}{R_1 \cdot C_1}} \quad (5.25)$$

The method of designing the filter is chosen as setting the components as ratios this means that the components have the following ratios:

$$R_1 = mR \quad (5.26)$$

$$R_2 = R \quad (5.27)$$

$$C_1 = nC \quad (5.28)$$

$$C_2 = C \quad (5.29)$$

When gain is set to 1 Q factor can be calculated with the following equation with this method[2]:

$$Q_2 = \frac{\sqrt{m \cdot n}}{n + 1} \quad (5.30)$$

Since a Q factor of 0.707 is desired, m is set to 2, and n is set to 1. This means that the capacitors will be identical while R_1 will be 2 times R_2 . The capacitors are chosen to be 470nF which means the resistors can be calculated as follows:

$$R_1 = \frac{1}{\sqrt{2} \cdot C \cdot \pi \cdot f_c} = \frac{1}{\sqrt{2} \cdot 22\text{nF} \cdot \pi \cdot 20\text{Hz}} \approx 511\text{k}\Omega \quad (5.31)$$

$$R_2 = \frac{R_1}{2} = \frac{511\text{k}\Omega}{2} \approx 255\text{k}\Omega \quad (5.32)$$

The component values are then:

$$R_1 = 511\text{k}\Omega \quad (5.33)$$

$$R_2 = 255\text{k}\Omega \quad (5.34)$$

$$C_1 = 22\text{nF} \quad (5.35)$$

$$C_2 = 22\text{nF} \quad (5.36)$$

Low pass

To determine the values for the low pass filter the same method is used as for the high pass filter. The values of m and n are switched and the values are as well. The capacitors now have to be double the size of each other they are chosen to $C_4 = 100\text{nF}$ and $C_3 = 200\text{nF}$ these values will be used to calculate the resistors:

$$R_3, R_4 = \frac{1}{\sqrt{2} \cdot \pi \cdot f_c \cdot C_3} = \frac{1}{\sqrt{2} \cdot \pi \cdot 20\text{kHz} \cdot 200\text{nF}} = 56.269\Omega \approx 56.2\Omega \quad (5.37)$$

The component values for the low pass filter are then.

$$R_3 = 56.2\Omega \quad (5.38)$$

$$R_4 = 56.2\Omega \quad (5.39)$$

$$C_3 = 200\text{nF} \quad (5.40)$$

$$C_4 = 100\text{nF} \quad (5.41)$$

Transfer function of the bandpass filter

The final transfer function of the filter then becomes:

$$H(s) = \frac{1.5831 \cdot 10^{10} \cdot s^2}{(s^2 + s(177935.9431) + 1.5831 \cdot 10^{10})(s^2 + s(\frac{2000000}{11421}) + 15396)} \quad (5.42)$$

The transfer function plotted in a bode plot can be seen below:

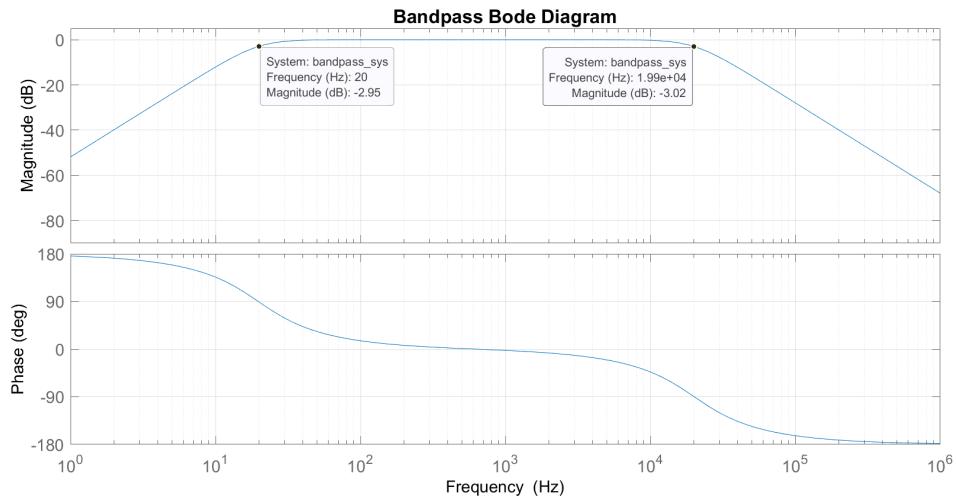


Figure 5.19: Matlab simulated transfer function bode plot

5.5.4 Simulation

The bandpass filter will now be implemented and simulated in LTspice to see if the response is correct. The simulation frequency response can be seen in the figure 5.20 below simulated from 20Hz to 20kHz

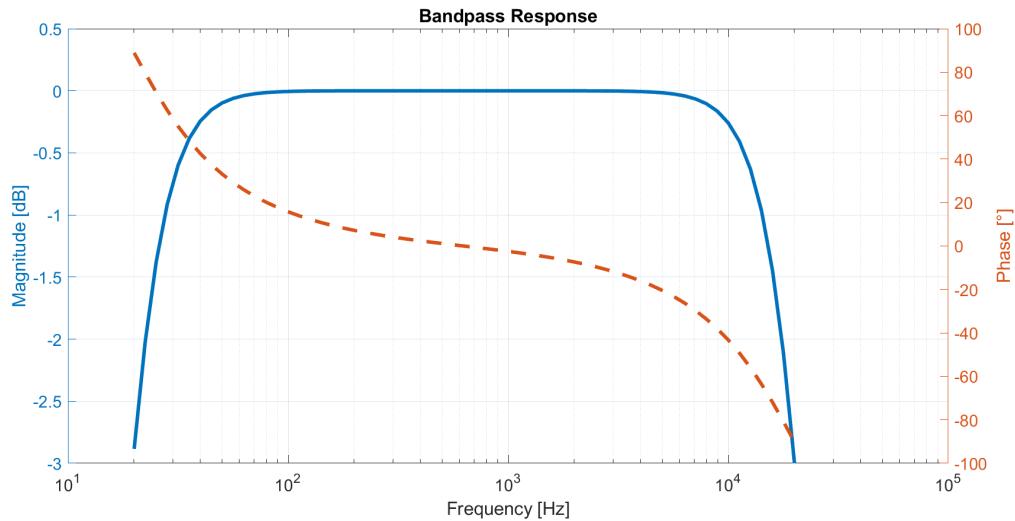


Figure 5.20: The bandpass filter simulated in LTspice

5.5.5 Conclusion

It is concluded that both from the simulation from LTspice and the plot of the transfer function the filter fulfills all requirements set for it.

5.6 Power Amplifier

This chapter goes through the design choices of the Power Amplifier. The section starts by defining the necessary specifications, followed by the selection of an appropriate

topology. The subsequent sections cover theoretical design, simulation testing, and a conclusion.

5.6.1 Specifications

- THD < 0.7%
- Class AB
- 1.228Vrms max input
- 35 Watt RMS into 8 ohms
- Efficiency above 50 at max output power%
- Input impedance of at least $470\text{k}\Omega$
- Constant gain within 20Hz to 20kHz within $2 \pm \text{dB}$

5.6.2 Topology Choices

This section will go through the topology choices made for the power amplifier. The vast majority of power amplifiers use the conventional three-stage architecture shown in figure 5.21. There are three stages in total in this configuration, the first being a transconductance stage (differential voltage in, current out). The second stage is a trans-impedance stage (current in, voltage out), and the third is a unity-voltage-gain output stage. The second stage has to provide all the voltage gain and therefore it is commonly called the Voltage Amplification Stage or VAS.

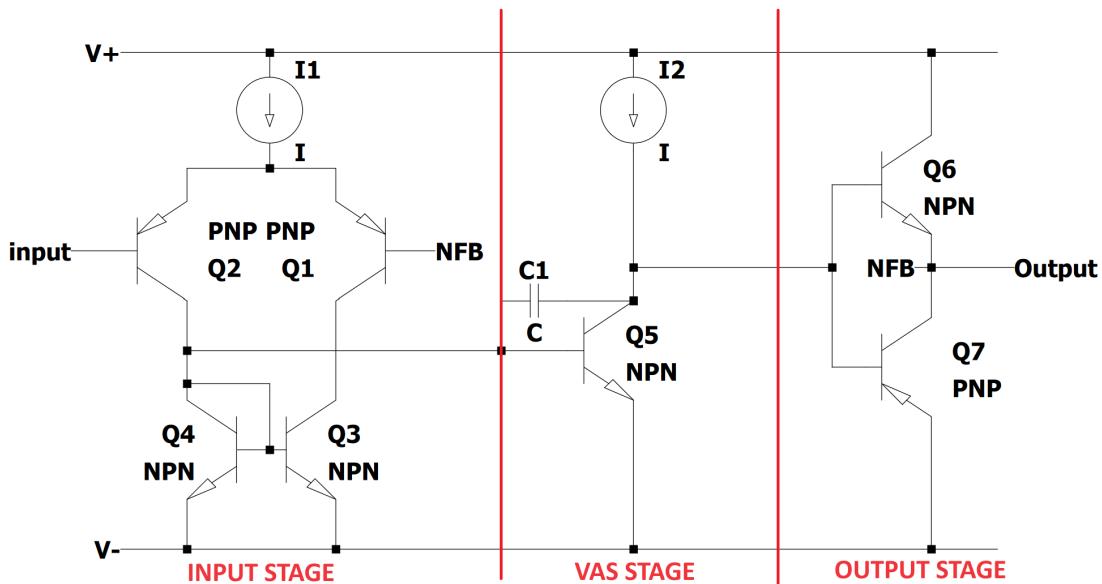


Figure 5.21: Standard three-stage Power amplifier with Input stage, VAS, and Class B output stage

This three-stage architecture has several advantages, the most important of these is that it is easy to arrange things so that there is little to no interaction between stages. This makes it easy to design the individual stages one at a time, to satisfy the overall goal of the amplifier which is to fulfill the requirements set in the specifications section.

Output stage choices

As learned from section 3.5 there are 3 main classes used in power amplifier output stages, A, B, and AB. As this project focuses on creating an amplifier with a THD under the specification of 0.7% and an efficiency of around 50%, therefore, a Class AB output stage is chosen. The class AB output stage has to be biased to make it class AB and this bias can be made in many different ways among them being diodes and a VBE multiplier. In this project, the VBE multiplier is chosen as it is both efficient and consistent. The entire output stage topology can be seen in the figure 5.22.

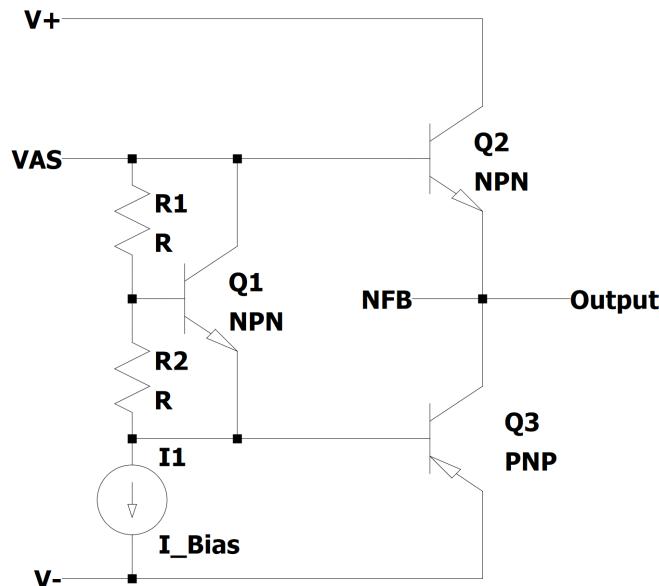


Figure 5.22: Class AB output stage with VBE multiplier biasing of output transistors

VAS stage choices

There are three common transistor couplings, common-emitter, common-base, and common-collector (emitter-follower). Since the purpose of this stage is voltage amplification the common-collector is ruled out. The common-base configurations are awkward to work with as the input voltage has to be lower than the base. The simplest VAS therefore is the common emitter with a single transistor and a resistor to limit the load on the collector as seen in figure 5.21 in the VAS stage. To linearize this conventional type of VAS the Cdom(C1) capacitor is used to create a local feedback network, this is used as simply increasing the resistor on the collector to increase voltage gain will simply decrease I_C in the transistor and reducing the gm which just gets you back to square one [9]. Therefore an active load is used as seen in figure 5.21 to enhance local loop gain, this also ensures that the VAS can source enough current to drive the upper stage of the output stage. This simple VAS stage however has one problem and that is that it creates too much distortion. This can be improved by adding a simple emitter-follower transistor to increase local feedback as seen in [9] book about audio amplifiers. Therefore the Emitter-follower VAS topology is chosen and can be seen in figure 5.23

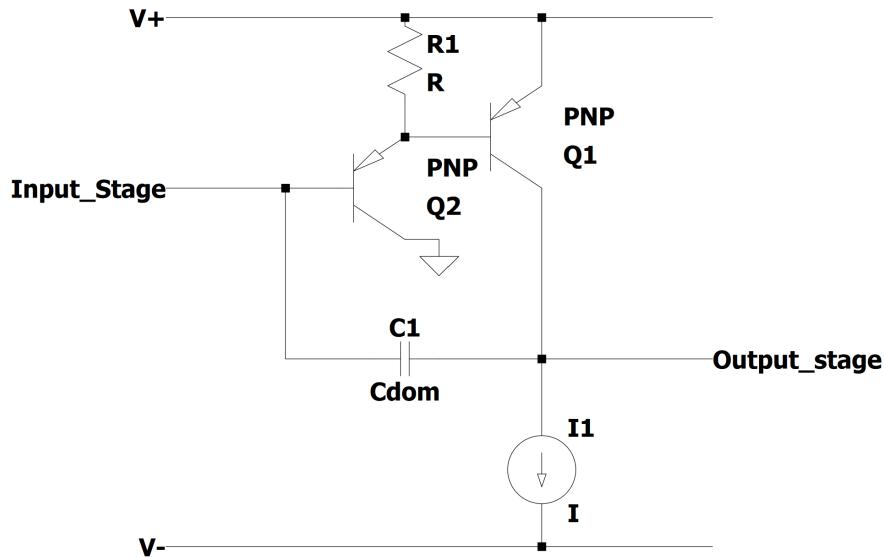


Figure 5.23: Emitter follower VAS with active load current source

Input stage choices

The standard input stage[9] is chosen for the input stage topology because it can be made very linear, by utilizing a current mirror, which provides the tail current for the mirror. It also provides easy implementation of Negative Feedback which is crucial in power amplifiers and will be touched on later in this section.

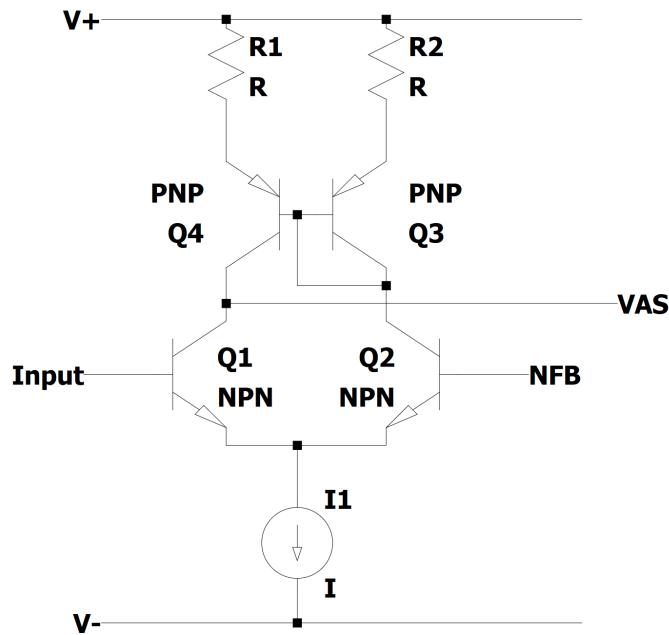


Figure 5.24: Standard input stage with a tail current source

Final power amplifier topology

This all leads to the final topology for the power amplifier based on the standard three-stage design with negative feedback and the previously discussed individual stages. The

rest of the design will be based on this topology. The topology can be seen in figure 5.25. Note that it is upside down compared to the standard model presented in figure 5.21, this is just the way the group designed the power amplifier when it was first designed because the inspiration at the time, was this example of a power amplifier.

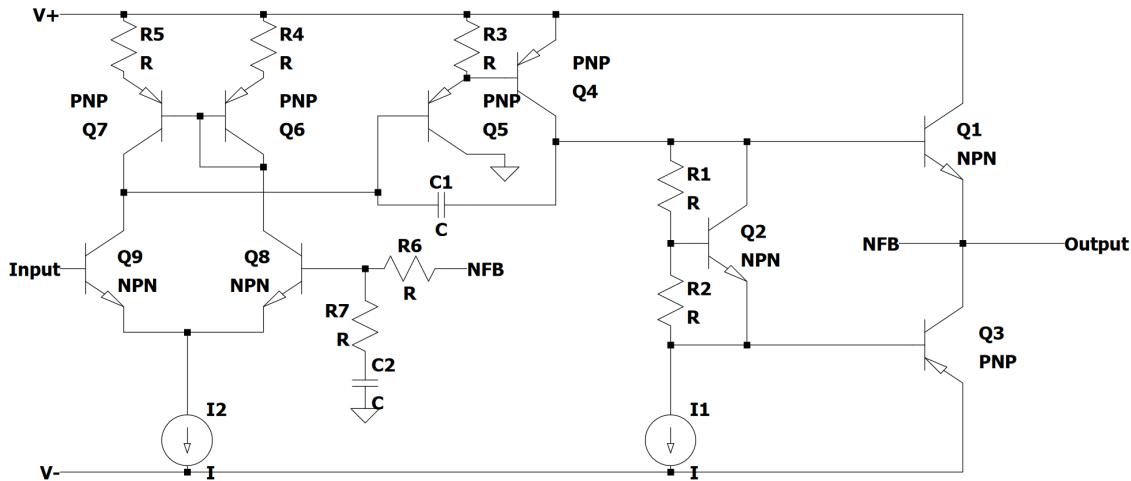


Figure 5.25: Final topology for the Power amplifier

5.6.3 Theoretical Design

The design begins at the output stage of the power amplifier, where requirements for the transistors used in the output stage will be determined concerning large signals. The thermal relations are taken into account in the choice of output transistors as they will have to handle some heat. When the output transistors are chosen the bias can be designed. After this, the VAS stage can be designed to deliver the necessary signal to the output stage to deliver the required power of 35W. Then the input stage can be designed along with the feedback system to reduce distortion so it meets the requirements for distortion.

Output stage

The basis of these calculations is based on the topology chosen for the output stage as seen in figure 5.22. The following calculations are done without taking cross-distortion commonly known problem in class B output stages. This is done because the output stage chosen is AB and this should therefore eliminate this problem. All the calculations used are for class B output as with large signals the class AB stage will have little to no say in efficiency. Given that the load impedance is set to 8Ω and that the power dissipated through the load is 35W the voltage required for this can be calculated as follows[19] :

$$P_L = \frac{\hat{V}_0^2}{2 \cdot R_L} \quad (5.43)$$

where:

- P_L = Power dissipated by the load [W]

- \hat{V}_0 = Peak signal amplitude [V]
- R_L = The resistance of speaker [Ω]

the peak signal amplitude can be isolated and calculated as follows [19]:

$$\hat{V}_0 = \sqrt{2 \cdot P_L \cdot R_L} = \sqrt{2 \cdot 35W \cdot 8\Omega} = 23.664V \approx 24V \quad (5.44)$$

This means that the maximum peak voltage necessary to generate 35W across the load resistance.

The maximum current through the load resistance can be calculated using the following formula [19]:

$$\hat{I}_0 = \frac{\hat{V}_0}{R_L} = \frac{24V}{8\Omega} = 3A \quad (5.45)$$

To determine the supply voltage a series of considerations must be made. These considerations are dependent on the choice of components and design and will therefore be discussed later on. Until then the supply voltage is set at 30V as this should be more than enough supply voltage. To ensure that the transistors chosen for the output stage can withstand the power dissipated in them a worst-case scenario is calculated. The power of the power supply is calculated [19]:

$$P_{cc} = \frac{2 \cdot \hat{V}_0}{\pi \cdot R_L} \cdot V_{cc} = \frac{2 \cdot 24V}{\pi \cdot 8\Omega} \cdot 30V = 57.296W \approx 58W \quad (5.46)$$

The average power dissipated in the output stage must then be [19]:

$$P_D = P_{cc} - P_L \quad (5.47)$$

where P_L is the power dissipated in the load. This means that we can substitute equation 5.43 and 5.46 into equation 5.47 get the following equation:

$$P_D = \frac{2 \cdot \hat{V}_0}{\pi \cdot R_L} \cdot V_{cc} - \frac{\hat{V}_0^2}{2 \cdot R_L} \quad (5.48)$$

Partial Differentiating this expression with regards to \hat{V}_0 and equating to zero gives the value of \hat{V}_0 for which the output voltage creating the worst-case average power dissipation in the output stage will be [19]:

$$\frac{\partial P_D}{\partial \hat{V}_0} = \frac{\partial}{\partial \hat{V}_0} \left(\frac{2 \cdot \hat{V}_0}{\pi \cdot R_L} \cdot V_{cc} - \frac{\hat{V}_0^2}{2 \cdot R_L} \right) = 0 \Rightarrow \hat{V}_0 = \frac{2}{\pi} \cdot V_{cc} \quad (5.49)$$

This equation substituted into equation 5.48 gives the following:

$$P_{Dmax} = \frac{2 \cdot \frac{2}{\pi} \cdot V_{cc}}{\pi \cdot R_L} \cdot V_{cc} - \frac{\left(\frac{2}{\pi} \cdot V_{cc}\right)^2}{2 \cdot R_L} = \frac{2 \cdot V_{cc}^2}{\pi^2 \cdot R_L} \quad (5.50)$$

This means we now have an equation that can calculate the worst-case scenario for power dissipation in the output transistors which will be:

$$P_{Dmax} = \frac{2 \cdot 30V^2}{\pi^2 \cdot 8\Omega} = 22.797W \approx 23W \quad (5.51)$$

However, in the Class AB output stage, this power dissipation will be evenly distributed in the two output transistors due to symmetry. When such a high power dissipation is required it is necessary to choose the so-called power transistors, which are transistors capable of extremely high currents and power dissipation. These transistors usually suffer from low current gain values, which will therefore require a higher base current as can be seen in the following equation:

$$I_B = \frac{I_C}{\beta} \quad (5.52)$$

Where:

- I_C is the collector current.
- I_B is the base current.
- β is the current gain.

So if the β value is low high base currents are required to reach the required power output of the amplifier. This creates bias difficulties as the rest of the system has to create this high bias current and by extension thermal issues and gain issues. This issue can be solved in many ways this is a complimentary coupling of the output stage using multiple transistors. This method allows for the reduction of the base current necessary for driving the output stage as a driver transistor and a power transistor is used. One of the ways of doing this is called a Darlington transistor coupling and this solution is chosen in this project as it's simple and can be found in many single-housing transistor packages. The coupling can be seen in the figure below 5.26.

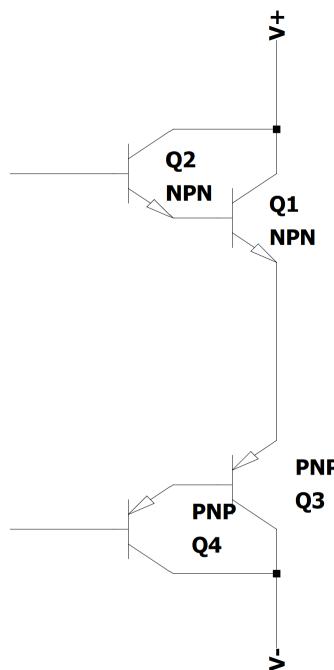


Figure 5.26: Two complimentary npn and pnp darlington couplings in a class B output stage

Using this transistor coupling will greatly increase the current gain as the current gain can be expressed as [19]:

$$\beta_{Total} = \beta_{Driver} \cdot \beta_{Power} \quad (5.53)$$

The obvious drawback of the coupling is that the base-emitter voltage increases and can be expressed as [19]:

$$V_{BETotal} = V_{BEDriver} + V_{BEPower} \quad (5.54)$$

This however just means that the bias voltage will have to be increased in the class AB design. So to summarise the transistors have to be capable of delivering a peak output current of 3A, delivering a peak voltage of 24V, and being able to handle a power dissipation of 23W. With these requirements in mind the MJ11016(npn) and MJ11015(pnp)[21] Darlington transistors are chosen as the output transistors. The schematic for these transistors can be seen in the figure 5.27 below.

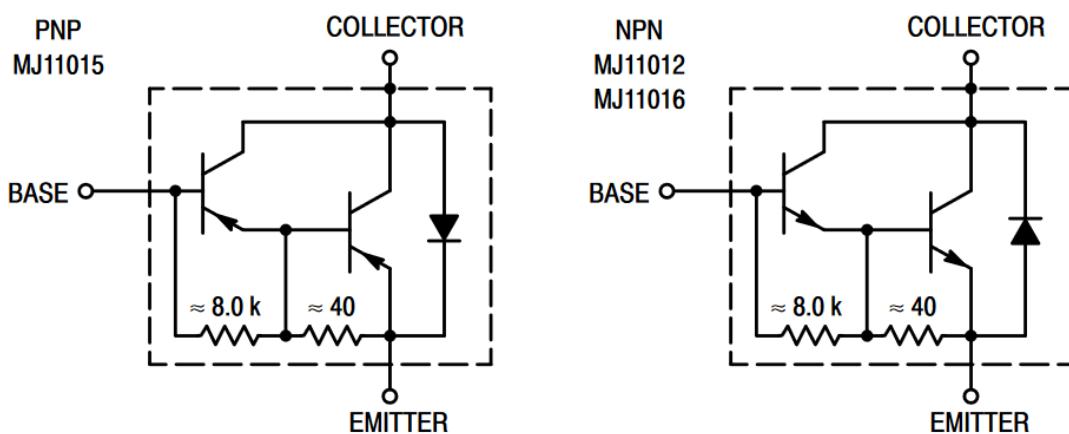


Figure 5.27: MJ11016 and MJ11015 schematic[21]

From the datasheet, a couple of worst-case scenarios are found for the transistors that are going to be used later in the calculations. Specifically, the h_{fe} differs by about 2000 between the two transistors however 6000 is chosen as it is the worst-case scenario. The transistor's small signal current gain begins to fall off at around 30kHz which is also within specification for the frequency range[21].

- $V_{BESat} \approx 2\text{V}$ Base emitter saturation voltage.
- $V_{CESat} \approx 1.2\text{V}$ Collector emitter saturation Voltage
- $B_{DC} = h_{fe} \approx 6000$ DC current gain

From this information, the bias current can be calculated as follows [19]:

$$I_B = \frac{I_C}{\beta_{DC}} = \frac{3\text{A}}{6000} = 0.5\text{mA} \quad (5.55)$$

Bias Design

As mentioned in topology choices the choice for bias design is the Vbe multiplier method where a transistor is used to create the adequate voltage to bias the transistors. The schematic for the Vbe multiplier can be seen in the figure 5.28 below.

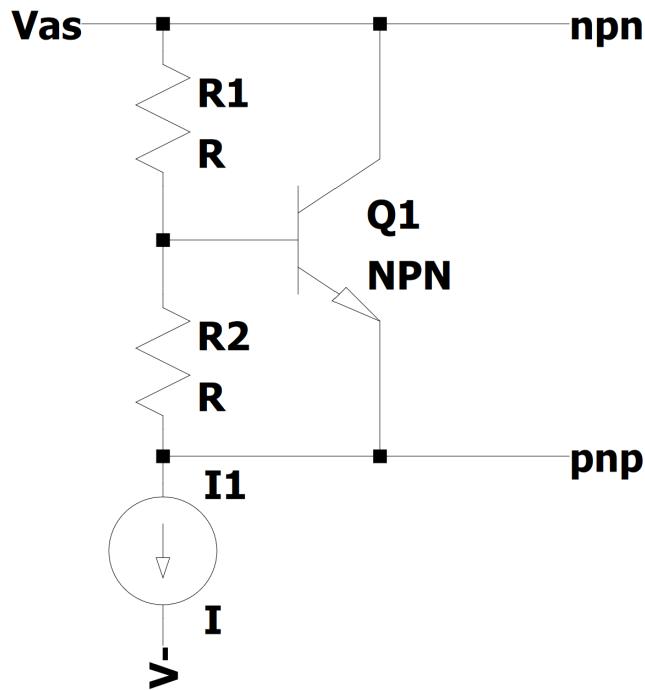


Figure 5.28: Vbe Multiplier schematic

This design makes use of a constant current source, a resistor connected between the collector and base of the transistor, and a resistor connected between the base and the emitter of the transistor. If the base current is neglected the current through the two resistors can be approximated as [19]:

$$I_R = \frac{V_{BE}}{R_2} \quad (5.56)$$

Where:

- I_R is the current through both resistors
- V_{BE} is the Base emitter voltage in the transistor
- R_2 is the resistor value

Using the same approximation the voltage across the two resistors can be estimated to [19]:

$$V_{BB} = I_R \cdot (R_1 + R_2) \quad (5.57)$$

Substituting equation 5.56 into equation 5.57 the following relationship can be obtained:

$$V_{BB} = \frac{V_{BE}}{R_2} \cdot (R_1 + R_2) = V_{BE} \cdot \left(\frac{R_1}{R_2} + 1 \right) \quad (5.58)$$

With this relation, it becomes clear that the design amplifies the V_{BE} by a factor decided by the resistors. By altering the values of these resistors it is possible to obtain a suitable value for V_{BB} to bias the output transistors properly.

The Darlington transistors require a base-emitter voltage of 2V each which means the total voltage is $2 \cdot 2V = 4V$ to activate. It's a good idea however to design with a little more than this to accommodate for non-ideal components and other components in the circuit therefore it is chosen to make it adjustable by placing one of the resistors in series with a potentiometer. The R_1 resistors are chosen to be $1k\Omega$ and R_2 is as said before chosen to be a resistor in series with a potentiometer to make sure you can't overbias the circuit. Using equation 5.58 and estimating a V_{BE} saturation for the transistor of 0.7V the resistor value of R_2 can be calculated as follows [19]:

$$V_{BB} = 4V = 0.7V \cdot \left(\frac{1k\Omega}{R_2} + 1 \right) \Leftrightarrow \frac{1k\Omega}{R_2} = \frac{4V}{0.7V} - 1 = 4.71 \quad (5.59)$$

The value of R_2 can now be calculated with this ratio:

$$R_2 = \frac{R_1}{4.71} = \frac{1k\Omega}{4.71} = 212.31\Omega \quad (5.60)$$

Since this resistance is a worst-case scenario for both transistors a 220Ω resistor is chosen in series with a $1k\Omega$ potentiometer so the variance in transistors can be accounted for.

Output stage Current source

The constant current source in the output stage can be made in various ways in this design a current mirror is chosen for its stability and ease of design. Further, the Wilson mirror is less thermally unstable, as most of the power in this mirror is dissipated in the first transistor[19] Q_1 see figure 5.29.

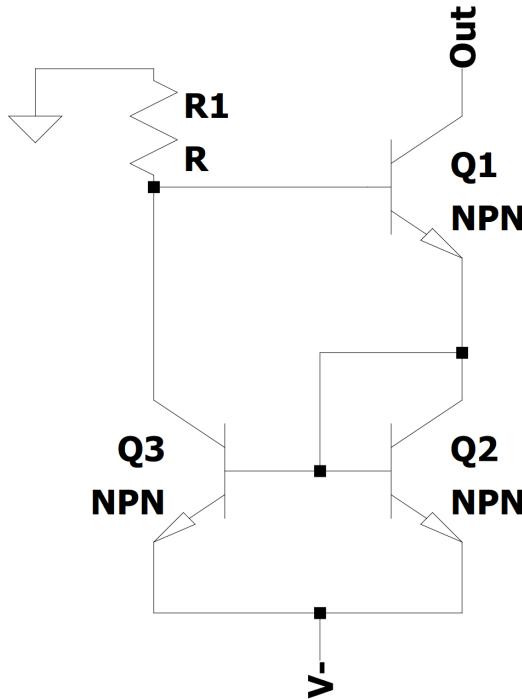


Figure 5.29: Wilson current mirror

The Wilson mirror is also favorable in the way that its output impedance is very high

thus making the resistances it is connected to less impactful, due to the current flowing in the mirror.

In the Wilson mirror the current flowing the resistor R_1 can be calculated as[19]:

$$I_{R_1} = \frac{V_{cc} - V_{BE2} - V_{BE1}}{R_1} \quad (5.61)$$

Where:

- V_{BE2} is the shared base-emitter voltage drop of Q_2 and Q_3 .
- V_{BE1} is the base-emitter voltage drop of Q_1 .
- R_1 is the resistance.
- V_{cc} is the supply voltage.

The relationship between the input and output can then be described as[19]:

$$\frac{I_{Out}}{I_{R_1}} \approx \frac{1}{1 + \frac{2}{\beta^2}} \quad (5.62)$$

Where:

- I_{Out} is the current drawn from "Out" in the figure 5.29.
- β is the DC current gain of the transistors Q_2 and Q_3

For transistors with a high β value, the ratio is approximately unity which means that $I_{Out} \approx I_{R_1}$.

To prevent thermal runaway in the current mirror, emitter resistors can be added. This will however cause a voltage drop of V_{R_e} resulting in a reduced current in the mirror, which means equation 5.61 must be revised:

$$V_{cc} = V_{BE1} + V_{BE3} + I(R_1 + R_e) \quad (5.63)$$

Which results in an expression for the output current as follows [19]:

$$I_{Out} \approx \frac{V_{cc} - V_{BE1} - V_{BE3}}{R_1 + R_e} \quad (5.64)$$

To ensure that enough current always can be drawn from the output stage, while still maintaining a constant voltage across the V_{BE} -multiplier. The following component values are chosen $R_{e1} = R_{e2} = 200\Omega$ and $R_1 = 3k\Omega$. This gives the following output current:

$$I_{Out} \approx \frac{30V - 2 \cdot 0.7V}{3k\Omega + 200\Omega} \approx 8.94mA \quad (5.65)$$

Implementing the current mirror as the current source for the output stage yields the following circuit seen in figure 5.30

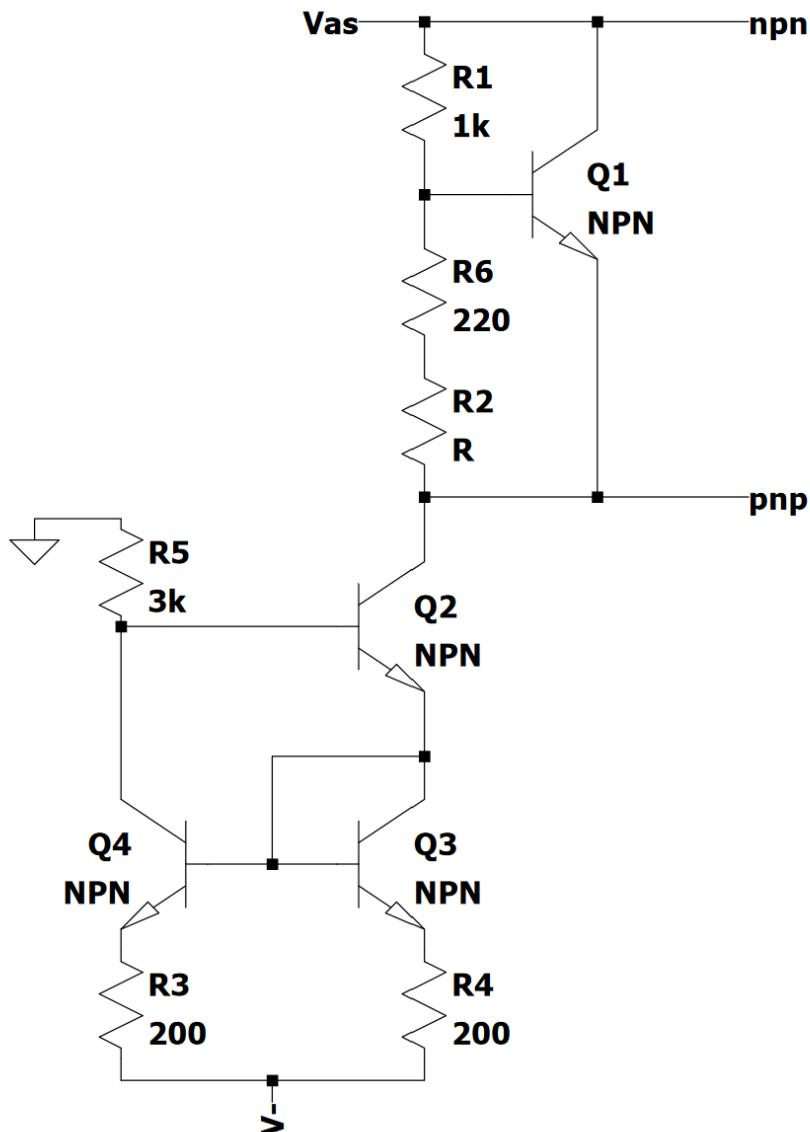


Figure 5.30: Final bias design with VBE multiplier and Wilson current mirror. R_2 is the potentiometer and therefore has no value

This configuration ensures a bias current and a constant voltage so that the output stage may function as a class AB push-pull stage.

Thermal Examination

The efficiency of the transistors used in the Darlington coupling is not ideal, resulting in power dissipation in the transistors. When the transistors are heated, the base-emitter saturation is decreased, making thermal runaway a possibility. For that reason, it is necessary to take precautions for this problem.

To prevent this two methods are commonly used one is attaching and dimensioning a heatsink to the output transistors and the other is adding emitter resistors to the output transistors[9]. Emitter resistors have a smaller effect as the amplification increases, and then they do not have good enough thermal protection for large amplifiers, unless very

large. In this output stage, both methods will be used to ensure thermal stability.

From equation 5.51 it is known what the maximum amount of power dissipated in the output transistors and is approximately 23W in both Darlingtons. If the provided power P_Q is larger than P_{Dmax} , it will induce thermal runaway in the transistors [19]. Therefore the provided power must be lower or equal to P_{Dmax} ($P_Q \geq P_{Dmax}$)

This can be expressed by the following formula[19]:

$$\Theta_{JA} = \frac{T_{Jmax} - T_A}{P_{Dmax}} = \frac{200^\circ\text{C} - 35^\circ\text{C}}{\frac{23\text{W}}{2}} = 14.35 \frac{^\circ\text{C}}{\text{W}} \quad (5.66)$$

Where:

- Θ_{JA} is the total thermal resistance from the circuit in the transistor to the ambient air.
- T_{Jmax} is the maximum temperature, the transistor can handle, which is taken from the datasheet [21].
- T_A is the surrounding temperature(Worst case).

The components of Θ_{JA} are Θ_{JC} , Θ_{CS} and Θ_{SA} Where:

- Θ_{JC} is the thermal resistance from the inner circuit to the case. This value is given by the datasheet [21] and is $0.875 \frac{^\circ\text{C}}{\text{W}}$
- Θ_{CS} is the thermal resistance of the isolation between the case and the heat sink. This value is given by the datasheet [22] and is $0.35 \frac{^\circ\text{C}}{\text{W}}$
- Θ_{SA} is the thermal resistance from the heat sink to the ambient air.

Therefore Θ_{SA} is the only unknown and of interest as it relates directly to the dimensioning of the heatsink and can be calculated the following way[19]:

$$\Theta_{JA} = \Theta_{JC} + \Theta_{CS} + \Theta_{SA} \Leftrightarrow \Theta_{SA} = \Theta_{JA} - \Theta_{JC} - \Theta_{CS} = 14.35 \frac{^\circ\text{C}}{\text{W}} - 1 \frac{^\circ\text{C}}{\text{W}} - 0.35 \frac{^\circ\text{C}}{\text{W}} = 13 \frac{^\circ\text{C}}{\text{W}} \quad (5.67)$$

Since there are two transistors, the maximum value for Θ_{SA} must be $\frac{13}{2} = 6.5 \frac{^\circ\text{C}}{\text{W}}$. This means the heatsink must have a thermal resistance value below $6.5 \frac{^\circ\text{C}}{\text{W}}$ to make sure P_Q doesn't exceed P_{Dmax} .

It is decided that the heatsink should not increase in temperature of more than 60°C compared to the surrounding environment. The new value for Θ_{SA} is calculated below:

$$\Theta_{SA} = \frac{60^\circ\text{C}}{\frac{23\text{W}}{2}} = 5.22 \frac{^\circ\text{C}}{\text{W}} \quad (5.68)$$

This should effectively be half the size as a stereo amplifier is built and the same heatsink will be used for both channels. Therefore the thermal resistance should be:

$$\Theta_{SA} = \frac{5.22 \frac{^\circ\text{C}}{\text{W}}}{2} = 2.61 \frac{^\circ\text{C}}{\text{W}} \quad (5.69)$$

The chosen heat sink is of the type WA 202, which if made long enough has a max thermal resistance of approximately $1\frac{^{\circ}\text{C}}{\text{W}}$ which happens at a heatsink length of around 15cm according to the datasheet [23].

Emitter resistors

Another method of keeping the circuit thermally stable is adding emitter resistors which can be done by using the following equation [19]:

$$R_e \geq 4 \frac{\text{mV}}{^{\circ}\text{C}} \cdot V_{cc} \cdot \Theta_{JA} - \frac{V_T}{I_C} \quad (5.70)$$

Where I_C is the maximum current defined as [19]:

$$I_C \leq \frac{V_T}{-K \cdot V_{cc} \cdot \Theta_{JA}} = \frac{26\text{mV}}{4 \frac{\text{mV}}{^{\circ}\text{C}} \cdot 30\text{V} \cdot 7.175 \frac{^{\circ}\text{C}}{\text{W}}} = 30.20\text{mA} \quad (5.71)$$

Where Θ_{JA} is half the value found in equation 5.66, as the power is shared between the two output transistors because of symmetry. Thereby the emitter resistors are found:

$$R_e \geq 4 \frac{\text{mV}}{^{\circ}\text{C}} \cdot 30\text{V} \cdot 7.175 \frac{^{\circ}\text{C}}{\text{W}} - \frac{26\text{mV}}{30.2\text{mA}} \approx 0 \quad (5.72)$$

The value for the resistors is low because of the large heatsink used and the oversized transistors compared to the output power in the amplifier. Two emitter resistors are still used at 0.4Ω to keep it completely thermally stable.

Voltage Amplification Stage(VAS)

The VAS stage usually consists of just one transistor trading current for voltage therefore the name of the voltage amplification stage. However, one transistor distorts the signal in higher frequencies because of β breakdown the higher the frequency [9]. Therefore an emitter follower VAS setup with two transistors is chosen as seen in figure 5.31.

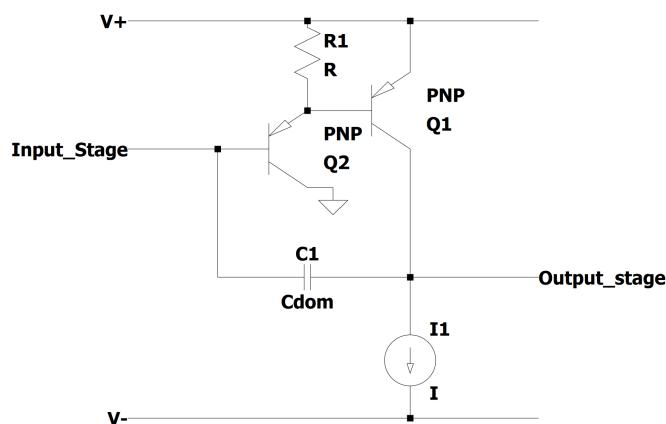


Figure 5.31: Voltage amplification stage

The resistor is chosen to be a low value because of THD gets lower the less restriction on the ability of the transistor to draw current however a resistor is necessary to not burn out the transistor. Therefore a value of 50Ω is chosen as R_1 [9]. The capacitor C_{dom} is chosen in the simulation chapter when looking at the stability of the amplifier.

Input stage

As described earlier in the topology choices section the input stage consists of a differential amplifier. The differential amplifier is required to operate as a small signal amplifier, which means that the signal to be amplified is limited to a low voltage. This is done so the amplifier operates in the linear region.

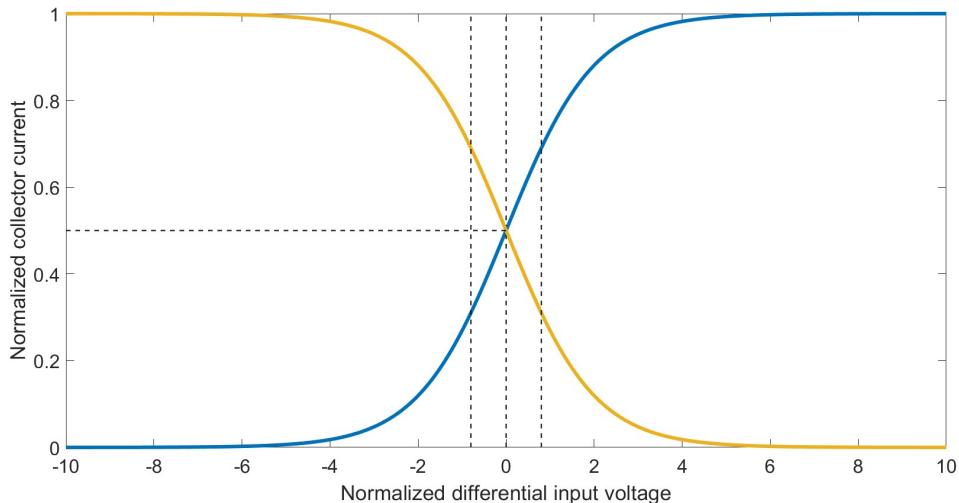


Figure 5.32: Transfer characteristic of a BJT differential pair. Dotted lines represent the linear region of the transistors

The two input signals will in this case be the signal into the power amplifier and the signal from the feedback from the output stage.

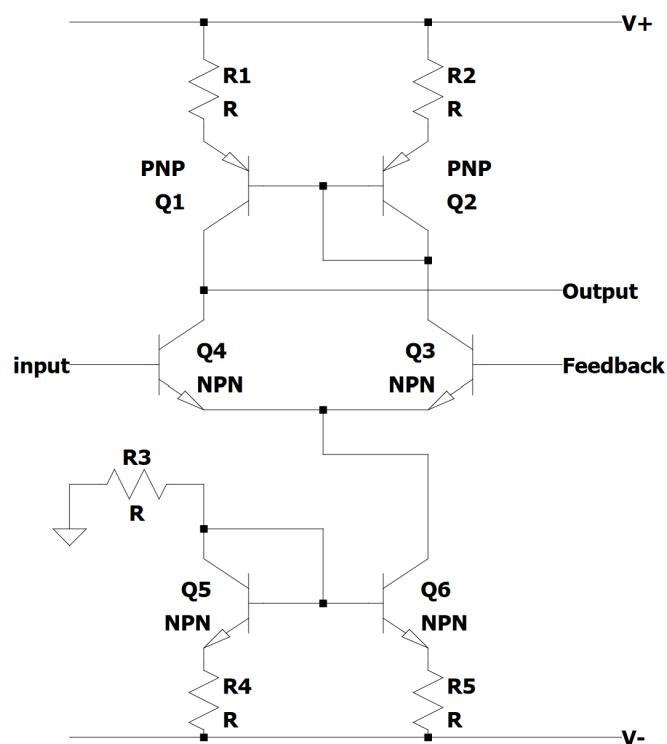


Figure 5.33: Input stage with current mirror as the current source

Exact DC balance of the input differential pair is essential for minimum distortion [9]. Therefore a current mirror is chosen to both drive collector current and emitter current of the differential pair. At the bottom of the circuit transistors Q_5 and Q_6 compose the current source in the shape of a basic current mirror. The Wilson mirror is not used here as thermal stability will not be an issue when only driving small signal transistors. At the top of the circuit, another current mirror is composed of Q_1 and Q_2 which are used as an active load, these are balanced by the resistors R_1 and R_2 to keep them balanced. The current biasing of the differential pair can be chosen to be many different values but in general the bigger the current the less THD at the cost of efficiency [9]. Therefore a current of 2mA is chosen to bias the input stage this can be calculated with the following equation.

$$I_{Out} \approx I_{Ref} = \frac{V_{cc} - V_{BE}}{R_5 + R_3} = \frac{30V - 0.7V}{10k\Omega + 5k\Omega} = 1.95mA \quad (5.73)$$

This is a rough estimation of the current generated by the mirror as it is more dependent on the DC current gain of the transistors but it is deemed adequate for the application.

Negative Feedback

The power amplifier generates a peak value into the load of 24V which means the feedback signal must be scaled accordingly as the amplifier is made to receive a 1.7366V peak voltage.

The amplifier can be depicted using a simple signal model with one module as the amplifier with a feedback network, this model is seen in figure 5.34:

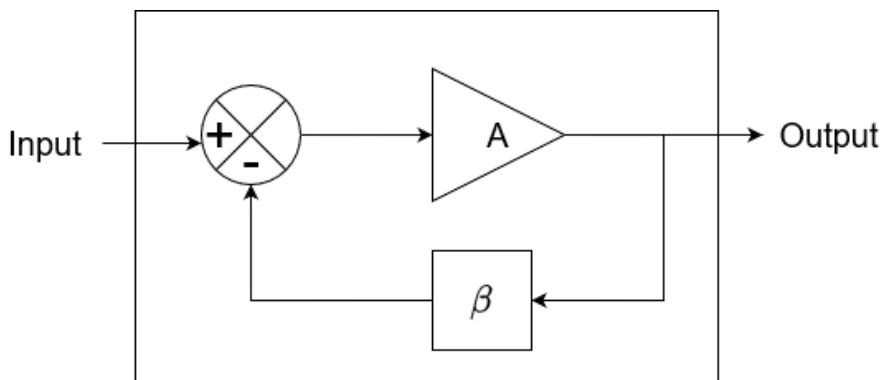


Figure 5.34: Negative feedback depiction

It is pretty clear by this figure that the one input to the subtractor is V_{In} and the other is $V_{Out} \cdot \beta$ so simply subtracting these two and multiplying by A then the output signal is:

$$V_{Out} = A(V_{In} - \beta \cdot V_{Out}) \quad (5.74)$$

Collect the V_{Out} s and the equation becomes:

$$V_{Out}(1 + A\beta) = A \cdot V_{In} \quad (5.75)$$

So the closed loop gain is:

$$\frac{V_{Out}}{V_{In}} = \frac{A}{1 + A \cdot \beta} \quad (5.76)$$

If the amplifier gain is large this expression can be simplified to:

$$\frac{V_{Out}}{V_{In}} \approx \frac{1}{\beta} \quad (5.77)$$

With this expression, the feedback system can now be designed for $V_{In} = 1.7366V$ and $V_{Out} = 24V$

$$\frac{24V}{1.7366V} = 13.82 \Rightarrow \beta \leq \frac{1}{13.82} \approx 0.07 \quad (5.78)$$

Using a voltage divider such feedback can be obtained:

$$\frac{1k\Omega}{1k\Omega + 13.82k\Omega} = \frac{1}{13.82} \quad (5.79)$$

The feedback system implemented in circuitry can be seen in figure 5.35. The capacitor seen in the figure is placed in the feedback network so that all DC-offset is accounted for in the differential amplifier, by only grounding the AC signal in the voltage divider of the feedback system.

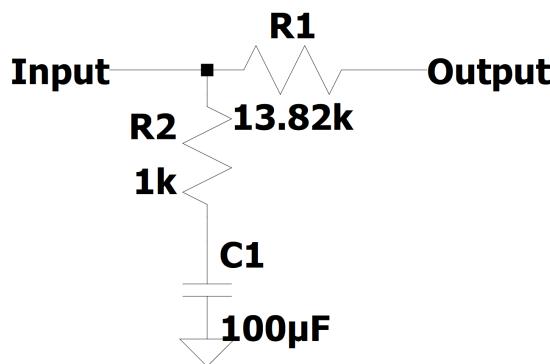


Figure 5.35: The feedback system implemented in circuit

Input filter

To eliminate any DC getting to the input of the amplifier a simple CR high pass filter is put in place to make sure it does not oscillate out of control when no input is applied to the amplifier. This filter has to have no interference on input frequencies which starts at 20Hz which means the cutoff frequency is set one decade before this at 2Hz so no interference occurs. The filter can be calculated with the following formula where the capacitor value has been isolated as the resistor value of 10kΩ has been chosen:

$$C = \frac{1}{2 \cdot \pi \cdot R \cdot F_c} = \frac{1}{2 \cdot \pi \cdot 10k\Omega \cdot 2Hz} = 7.95\mu F \quad (5.80)$$

Since that capacitor value is an odd value and not likely to be found in a physical capacitor. The value is rounded up to $10\mu\text{F}$ as this can be found physically and will only lower the cutoff frequency to:

$$\frac{1}{2 \cdot \pi \cdot 10\text{k}\Omega \cdot 10\mu\text{F}} = 1.59\text{Hz} \quad (5.81)$$

The recalculated frequency is deemed adequate.

Input impedance

The input filter is necessary for stability and to make sure the input on the amplifier doesn't oscillate the output out of control. This however affects the input impedance of the amplifier so it doesn't fulfill the specification. The current input impedance is dominated by the $10\text{k}\Omega$ resistor in the input filter and is therefore approximated to this value. This is well out of specification which requires it to be above $470\text{k}\Omega$. Therefore an op-amp is used as a voltage follower to utilize the extremely high input impedance of the op-amp and the extremely low output impedance. The voltage follower can be seen in figure 5.36.

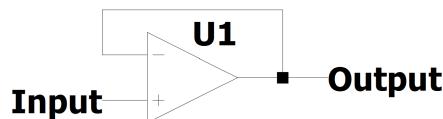


Figure 5.36: Voltage follower schematic

The input impedance is now approximately the input impedance of the chosen op-amp.

Compensation

All power amplifiers except the most rudimentary kinds include some kind of output compensation [9]. The first one covered here is the simple Zobel network which is included to reduce HF instability. This network is comprised of a simple resistor and a capacitor in series connected to the output to the ground. This network prevents the inductive reactance presented to the amplifier by the voice coil in the loudspeaker thereby preventing feedback from the loudspeaker from entering the NFB loop in the amplifier. The standard value for this network is a resistor of 10Ω and a capacitor of 100nF which seem to be just the right values to prevent HF instability. The other compensation technique is an output inductor in parallel with a dampening resistor right after the Zobel network on the output of the amplifier. The output inductor much like the Zobel network is used as a preventative strategy against capacitive loads connected to the amplifier preventing their feedback from entering the NFB loop on the amplifier[9]. The value of this inductor is usually in the range of $1 - 7\mu\text{H}$ as this prevents the inevitable high pass filter created from having a too-aggressive cut-off frequency. As this inductor has to be air-cored due to minimizing distortion from magnetic materials often used to increase inductor value, it is designed by the group as the correct inductor value

could not be found. Wheeler's formula is used as a good approximation when the coil diameter/length ratio is less than 3[9]:

$$L = 1000 \cdot \frac{r^2 N^2}{228 \cdot r + 254 \cdot l} \quad (5.82)$$

Where:

- L is the inductance in μH .
- N is the number of turns.
- r is coil radius in meters.
- l is the coil length in meters.

Coil length l is typically not an independent value but dependent on the number of turns N and the diameter of the inductor. The number of turns has to be an integer as the lead-out wires have to be soldered into the PCB this will be rounded up to ensure the value is higher than the chosen rather than lower. This yields the following equation:

$$N = \frac{w}{2 \cdot \pi \cdot r} \quad (5.83)$$

Where:

- r is the coil radius in meters.
- w is the wire length in meters.
- N is the number of turns.

The inductor designed here uses a coil diameter of 0.8mm. Number of turns is calculated by guessing the wire length in meters:

$$N = \frac{1.1}{2 \cdot \pi \cdot 9\text{mm}} = 19.45 \quad (5.84)$$

Which is rounded up to 20 turns as described earlier. The coil length is then calculated with the following formula:

$$l = b \cdot N = 0.8\text{mm} \cdot 20 = 16\text{mm} \quad (5.85)$$

The inductance of the inductor is then calculated:

$$L = 1000 \cdot \frac{(10\text{mm})^2 \cdot 20^2}{228 \cdot 10\text{mm} + 254 \cdot 16\text{mm}} = 5.96\mu\text{H} \quad (5.86)$$

Lastly, the ratio of diameter and length of the coil is checked to make sure that Wheeler's approximation can be used:

$$\frac{18}{16} = 1.12 \quad (5.87)$$

This ratio is acceptable as it's adequately under the requirement of 3 for the approximation. The resistance of the inductor will now be calculated by first calculating the cross-sectional area of the wire and then calculating the resistance with this value. The cross-section is calculated as follows:

$$a = \pi \cdot \left(\frac{b}{2}\right)^2 = \pi \cdot \left(\frac{0.8\text{mm}}{2}\right)^2 = 502.65 \cdot 10^{-3}\text{mm}^2 \quad (5.88)$$

5mm of wire will be added to each side for the lead-out wires so they can be soldered to the PCB. The resistance is calculated as:

$$R = \frac{\rho \cdot w}{a} = \frac{1.72 \cdot 10^{-8} \cdot 1.11\text{m}}{502.65 \cdot 10^{-3}\text{mm}^2} = 0.038\Omega \quad (5.89)$$

Where:

- ρ is the resistivity of the metal used here it is copper.

The resistance though high is due to the relatively small radius of the coil used which was the only coil available so this is deemed adequate. The final output compensation can be seen in figure 5.37.

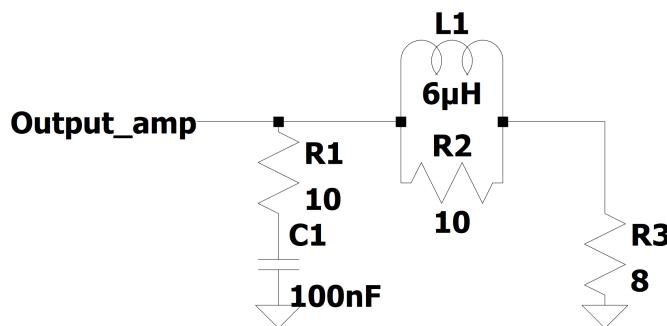


Figure 5.37: Final schematic of output compensation with both Zobel network and inductor compensation

Small signal analysis

The small signal analysis will aid in determining the transfer function of the differential stage of the power amplifier. Here the hybrid pi model will be used and the working area is in medium frequency where the capacitors are considered shorted for the analysis.

The circuit in question is seen in fig 5.33 where the current mirror in the top can be simplified to two resistors R_C and the current mirror at the bottom can be omitted since the junction between is "virtual ground". Thus, the equivalent small signal model can be seen in fig ??

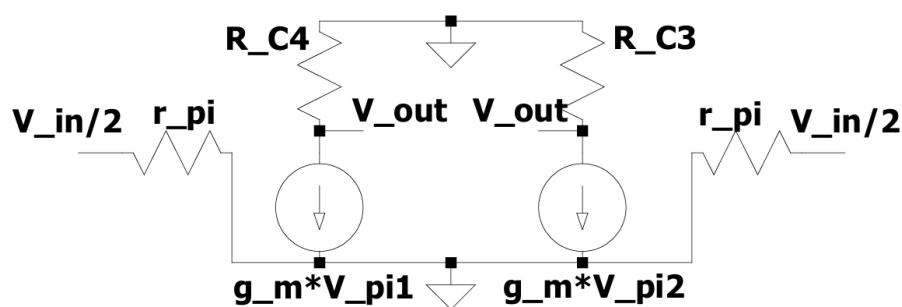


Figure 5.38: Small signal model of differential input stage

The output from differential amplifier is the single endend and not the differential. Hence the differentiel gain can be expressed from the figure with the following equations

$$V_{o1} = \frac{g_m R_C}{2} \quad V_{o2} = \frac{g_m R_C}{2}$$

$$A_v = V_o / V_{in} = \frac{g_m R_C}{2} \quad (5.90)$$

g_m can be expressed by the following equation $g_m = \frac{I_C}{V_T} = 0.038S$

Efficiency

The efficiency of the Class AB power amplifier should be above 50% as per the specification. From the already calculated values in the system design of the power amplifier, the efficiency can be calculated:

$$\eta = \frac{P_L}{P_{cc}} \cdot 100\% = \frac{35W}{58W} \cdot 100\% = 60.34\% \quad (5.91)$$

An efficiency of 60% is well within specification and is therefore deemed adequate.

PSRR(Power supply rejection ratio)

To make sure the power amplifier can source enough current from the rails even on peaks capacitors are used on each rail close to the different stages of the amplifier to provide the current for the amplifier. These capacitors are chosen in 3 different sizes for each stage in a size that's deemed adequate for the individual stage. In this amplifier, the 3 sizes are chosen as follows $2200\mu F$, $220\mu F$ and $22nF$. These are put on each rail yielding the following current amplifier design can be seen in figure 5.39

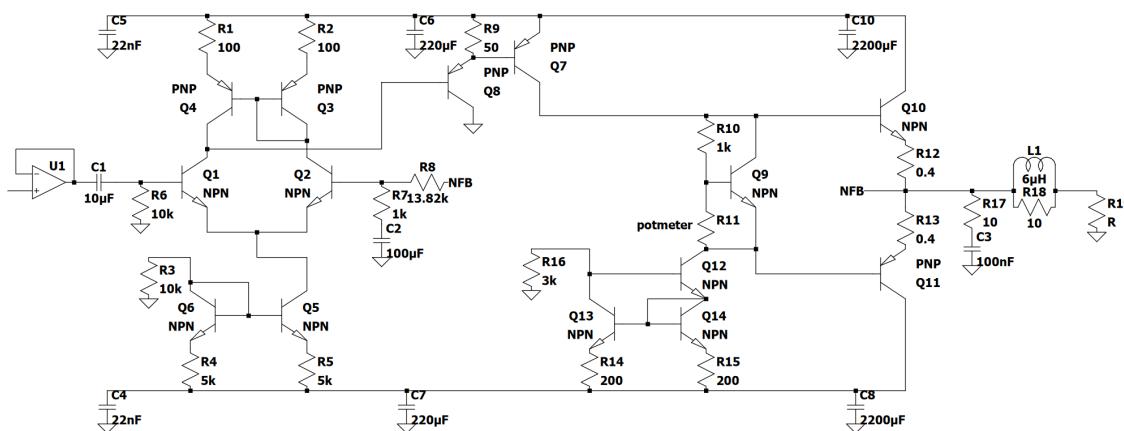


Figure 5.39: The current power amplifier after theoretical design process

5.6.4 Simulation

This section will cover all the design choices that used simulation to determine the values and choices for the power amplifier.

Gain

The different stages will now be simulated to determine their gain. The gain is calculated as follows:

$$\frac{V_{Out}}{V_{In}} = Gain \quad (5.92)$$

The differential input stage gain is tested from the input of the power amplifier to the input of the VAS. The gain in the differential stage is $-10m$ which is quite low but it's important to note that the feedback is ideal in the sense that it's the same as the input which is why the gain is so low.

The VAS stage is tested where the input signal on the base of the first transistor is compared to the output of the VAS stage. The gain in the VAS stage is determined to be $4.7k$ which is quite high.

The Output stage is tested where the input signal on the base of the transistors is compared to the output signal of the amplifier. The gain of the output stage is very close to the unity gain at a gain of $1m$ which is deemed adequate.

Stability

To determine whether the system is stable or not, it is brought into open loop mode specific simulation can be seen in appendix C.1 in figure C.1. which means that the input is grounded and there is no AC feedback. A negative input signal is then applied to the feedback system so that the open loop gain is positive(purely done to make it easier to determine whether or not the system is stable). The phase shift at 0dB should not exceed $\pm 180^\circ$, else the system will be unstable. Ideally, it should not exceed $\pm 135^\circ$ because when building the circuit component tolerances might shift the value.

Open loop test

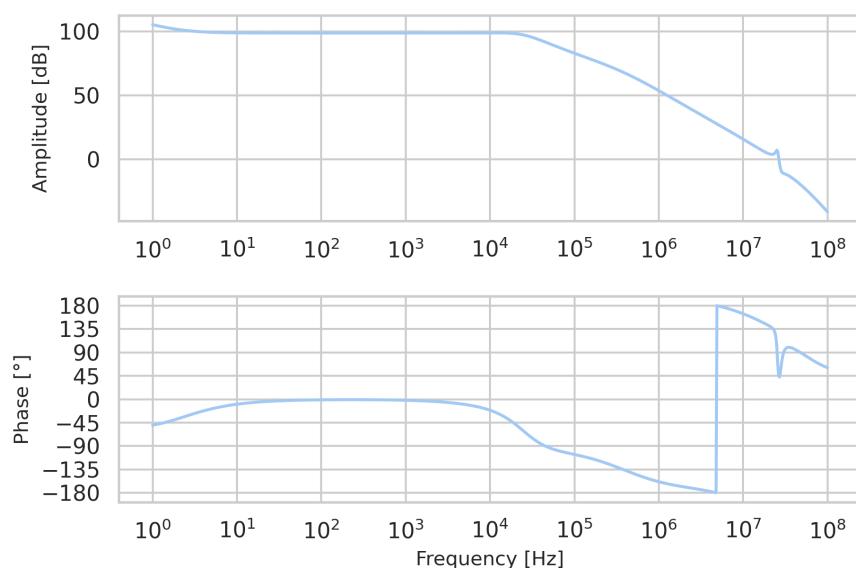


Figure 5.40: Simulated bode plot of the power amplifier as developed until now in open loop mode showing the gain and phase

As can be seen in the figure the phase at 0dB is around -180° . This means it will be unstable one compensation technique is creating local feedback in the VAS stage with a capacitor as drawn into the VAS stage in topology choices. The choice of this capacitor is done by simulation and a value of 470pF is found to be sufficient. The stability of the amplifier in an open loop can now be seen in figure 5.41.

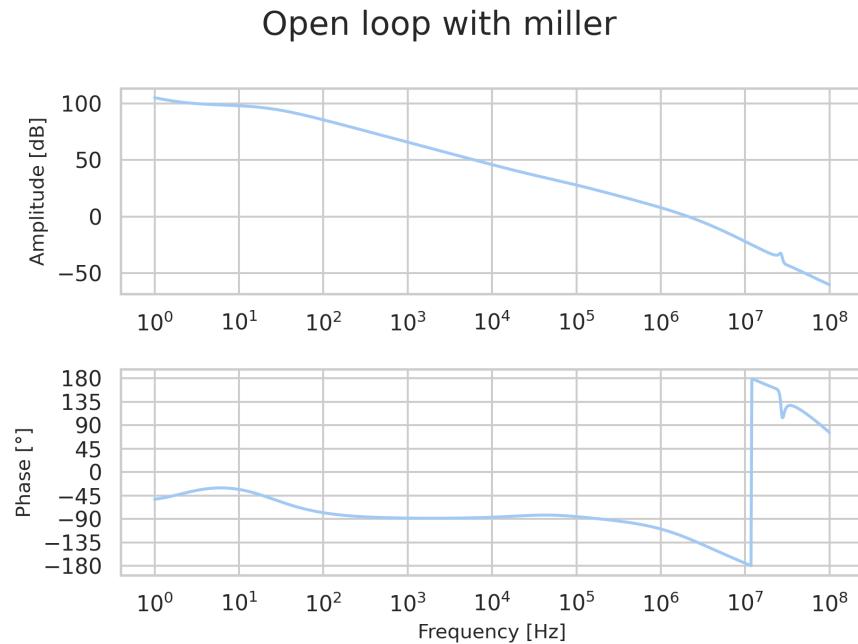


Figure 5.41: Open loop test with Miller capacitor compensation

The new open loop test now shows only a phase shift of -45° at 0dB amplification. This means the system should be stable. The capacitor can result in problems with slew rate [9] if it can't source enough current from the current source. However, the Wilson mirror designed previously delivers more than enough current for both the output transistors and the VAS so this new current draw from the capacitor is seen as negligible. For further analysis of stability, the amplifier is brought into a closed-loop mode with the new Miller compensation capacitor can be seen in figure 5.42.

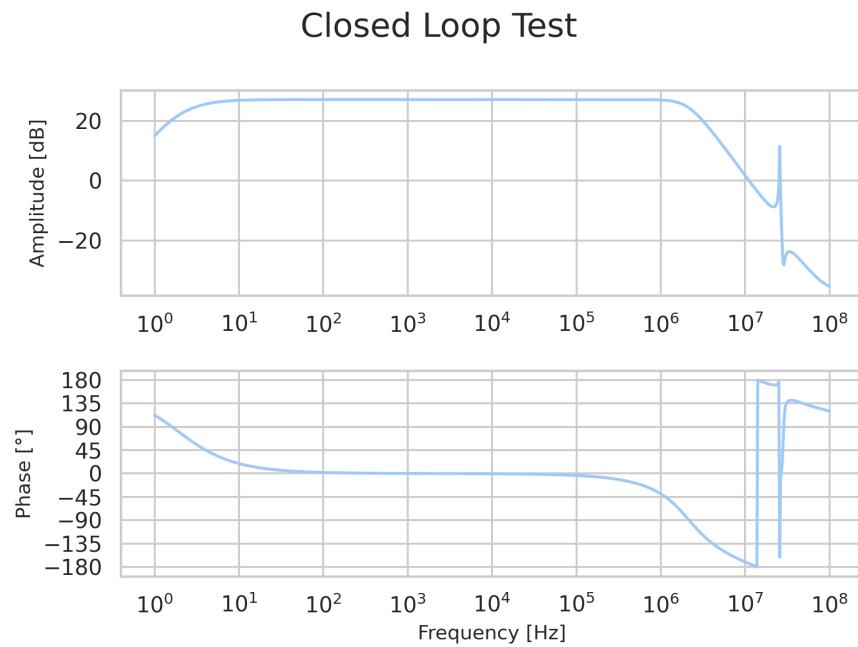


Figure 5.42: Simulated closed loop bode plot of the power amplifier with Miller compensation

The closed-loop test shows some gain and phase problems at around 10MHz which can be solved by adding an HF compensation capacitor across the VBE multiplier. the capacitor value is found with simulation and is found to be 470nF as this gives stability and a low THD. A closed loop test I performed again on the system is shown in figure 5.43.

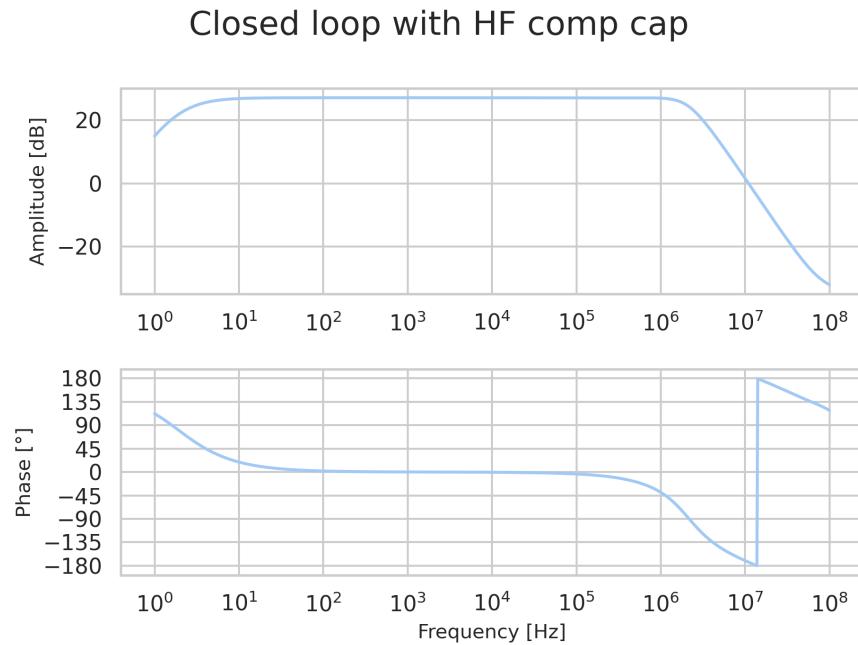


Figure 5.43: Simulated closed loop bode plot of the power amplifier with HF compensation capacitor across VBE multiplier

The now-implemented system is seen as having good stability and is therefore tested

in a transient analysis to test THD and to see the amplification in simulation. This can be seen from the phase being stable at around 0° in the frequency range and the amplification being flat in the range as well. The transient analysis can be seen in figure 5.44.

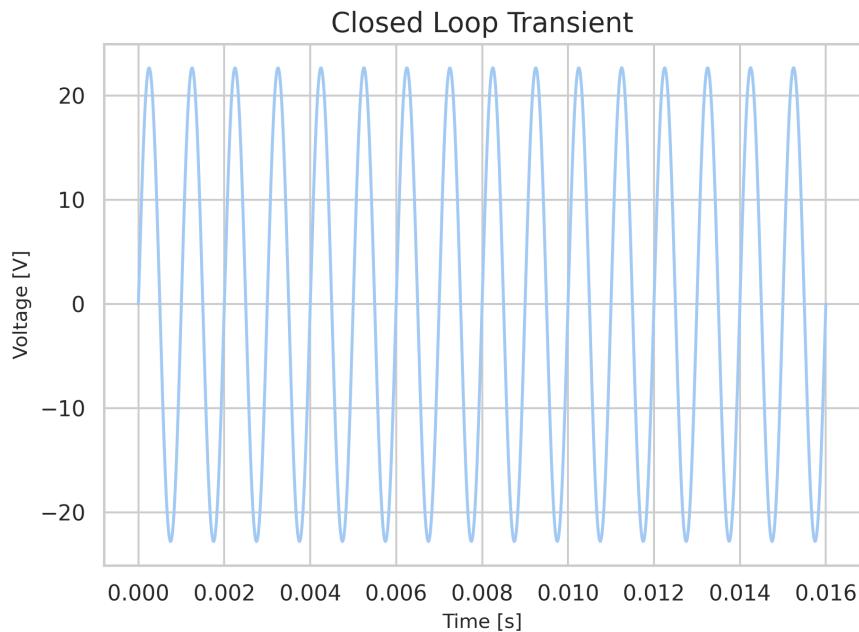


Figure 5.44: Closed loop transient analysis of the amplifier tested at 1kHz

The final power amplifier design after simulations can be seen in the figure below:

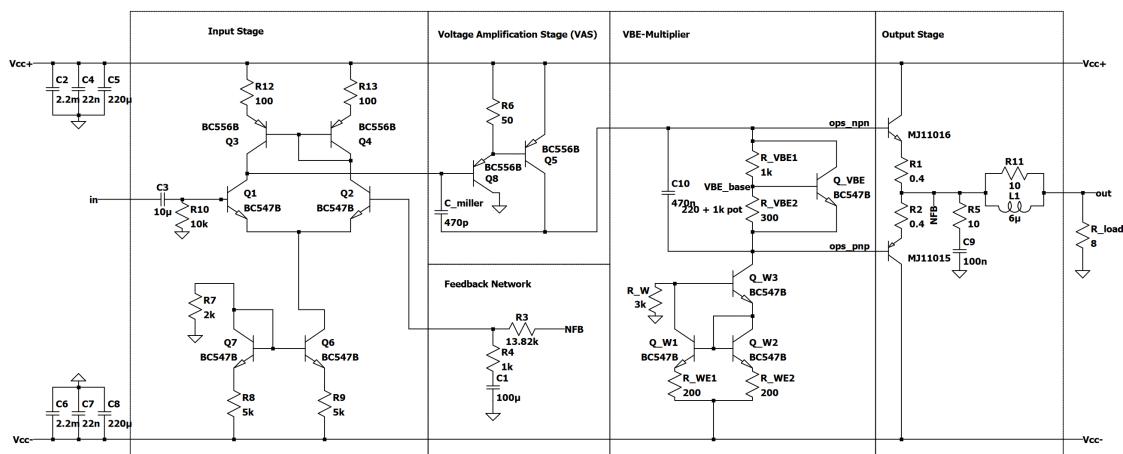


Figure 5.45: Final Power Amplifier after simulations

The following spice directive is used to simulate the THD of the amplifier:

```
.four 1000 5 8 V(out)
```

This spice directive yields the THD by performing a Fourier analysis on the amplifier from 1kHz it then includes the next 5 harmonics and waits 8 periods for the signal to stabilize. The test is performed at an input voltage of 1.18V as described in D.1 the

largest power resistor available for testing requires this input. This simulation yields a THD of 0.001%.

5.6.5 Conclusion

5.7 Power Supply

This section will cover the specifications topology choices and design choices for the power supply built for the entire system

5.7.1 Specifications

- 8V regulated rail for small signal circuitry.
- 30V unregulated rail for power amplifier.
- Adequate power delivery
- 230VAC input.

5.7.2 Topology choices

A power supply can be made in three principally different ways mentioned in 3.7 in this project the simplest and yet most used of these methods the unregulated power supply is chosen because of its simplicity and ease of design. For the regulated rails a switch mode power supply IC is chosen as it's efficiency is high and noise low, the specific chip chosen is the lm2575. This was chosen as it was readily available and its 1A current output was more than enough for this application [24]. The unregulated power supply will include a transformer, a full bridge rectifier, and capacitors.

5.7.3 Theoretical design

The power supply design starts by designing the transformer used for the supply. The primary side of the transformer is known as its 230VAC50Hz single-phase signal coming out of the power socket. A full bridge rectifier will be put after the transformer so to determine the secondary voltage of the transformer the voltage drop over the rectifier has to be accounted for. The diode used for the rectifier is the BY214 [25] which has a maximum forward voltage of 1.2V so with this in mind the constant voltage drop model is used to calculate the overhead in voltage on the secondary side. As each rail will go through two diodes in a full bridge rectifier the following equation is derived:

$$V_{Out} = V_{In} - 2 \cdot 1.2V \quad (5.93)$$

This means that in the worst-case scenario 2.4V of overhead room in the secondary winding has to be accounted for. As the peak voltage required is 30V the transformer will have a secondary voltage of 32.4V to account for the diode voltage drop. As the rest of the calculations will be in the RMS value this is calculated:

$$V_{SecondaryRms} = \frac{32.4V}{\sqrt{2}} = 22.910 \approx 23V \quad (5.94)$$

it is known from the power amplifier that the power supply for each power amplifier is 58W therefore the transformer needs to at least deliver $2 \cdot 58W = 116W$. The power

supply also needs to power all the small circuitry and have quite a bit of headroom therefore a 150W power rating is set for the transformer. So the specs for the transformer needs to have the following specifications:

- Primary side: 230VAC
- Secondary side: 23VAC
- Power rating: 150W
- Frequency: 50Hz

Now that the transformer specifications are known the rest of the supply can be designed. The diodes used are already predetermined as they were needed for the transformer therefore they will not be touched but they are over-dimensioned as they were chosen first. The capacitor size can be calculated as a product of the amount of ripple the supply can have. This is set at 5% for this supply as too much ripple would bypass the PSRR precautions taken in the power amplifier design. The capacitor for the rails can be calculated as:

$$V_c \cdot C = I \cdot t \quad (5.95)$$

Where:

- V_c Voltage change allowed on output(ripple).
- I maximum current draw.
- t period between 2 peaks.
- C value of the capacitor

I can be calculated by ohms law:

$$I = \frac{P}{V} = \frac{150W}{30V} = 5A \quad (5.96)$$

The ripple in volts is now calculated:

$$V_c = \frac{5}{100} \cdot 30V = 1.5V \quad (5.97)$$

The time in seconds can now be calculated as well:

$$t = \frac{1}{2 \cdot 50Hz} = 0.01s \quad (5.98)$$

Now the capacitor value can be calculated:

$$C = \frac{(5 \cdot 0.01)}{1.5} = 33mF \quad (5.99)$$

This capacitor is generally a good idea to split it into 3 smaller capacitors as specific capacities like that will be hard to get a hold of. So the capacitance will be split into the following capacitors:

- 20mF

- 10mF
- 3000μF

The last part of an unregulated power supply is the fuse which will be placed on the primary side typically and therefore will be chosen at a value a bit above what is the maximum power rating. So the fuse will be a 6A fuse on the secondary side to protect for over current. The final power supply can be seen in figure 5.46.

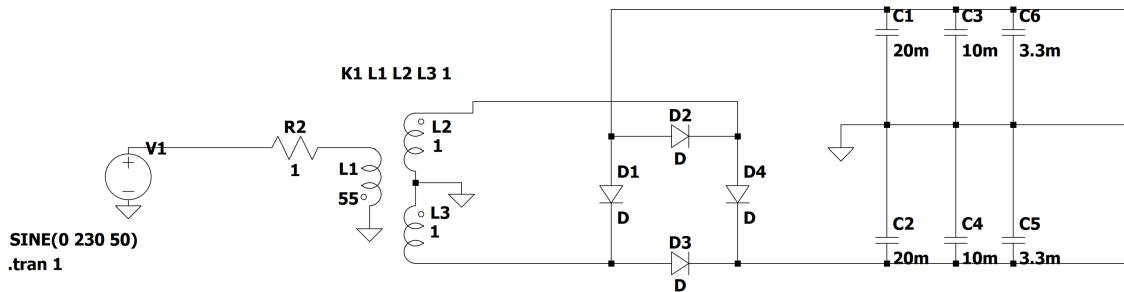


Figure 5.46: The final unregulated power supply with a simulated transformer

SMPS(Switch mode Power supply) regulated 8 V rails

As mentioned before the lm2575 chip is chosen and therefore setup for the regulated rail follows the typical application in the datasheet. This can be seen in the figure below 5.47.

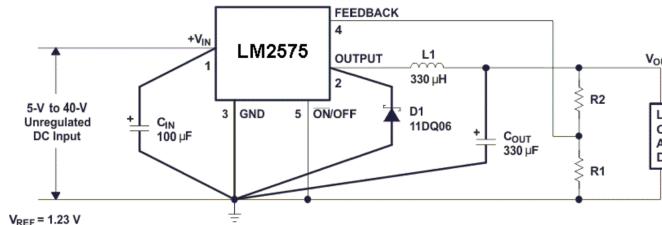


Figure 5.47: LM2575 typical application circuit[24]

To calculate the feedback resistors R_1 and R_2 the following formula from the datasheet is used:

$$V_{Out} = V_{ref} \cdot \left(1 + \frac{R_2}{R_1} \right) \quad (5.100)$$

The datasheet R_1 is recommending being between $1\text{k}\Omega$ and $5\text{k}\Omega$, therefore, a value in between these in the e96 is chosen at $3.01\text{k}\Omega$ which is used to calculate R_2 . The datasheet also tells us that $V_{ref} = 1.23\text{V}$ The one supply has to bring the voltage up from -30V to -8V , therefore, V_{Out} is set at 22V for the other rail it has to bring the voltage from 30V down to 8V , therefore, V_{Out} is set at 8V .

Negative rail is calculated:

$$R_2 = \left(\frac{22\text{V}}{1.23\text{V}} - 1 \right) \cdot 3.01\text{k}\Omega = 50827\Omega \approx 50.8\text{k}\Omega \quad (5.101)$$

Positive Rail is calculated:

$$R_2 = \left(\frac{8V}{1.23V} - 1 \right) \cdot 3.01k\Omega = 16567\Omega \approx 16.5k\Omega \quad (5.102)$$

The datasheet specifies that the diode should have a max current of 1.2 times the max output current, and a reverse breakdown voltage of 1.25 times the input voltage, [24]. The diode should also be a fast switching schotky diode.

the 1N5408 was chosen as it is easily available at Aalborg University, and has a max current of 3A and a reverse breakdown voltage of 1000V, [26]. Putting it well within spec.

The chip can now be implemented in the power supply to provide regulated rails for all the small signal circuitry in the amplifier. and a final circuit can be seen on figure

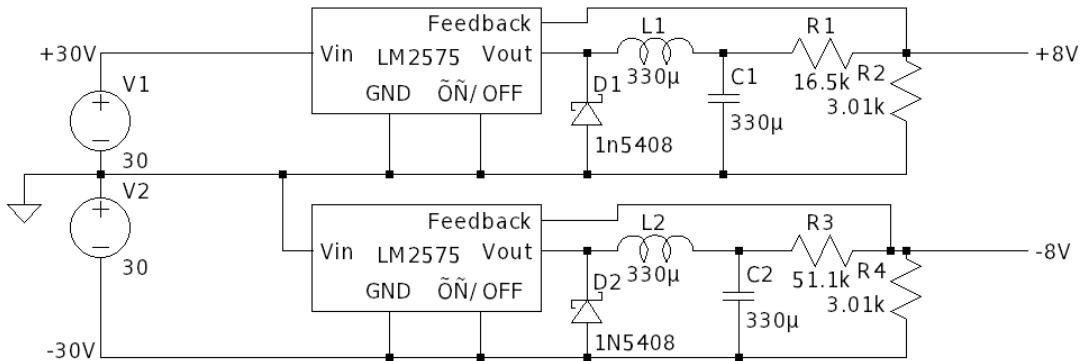


Figure 5.48: Final circuit for the small signal SMPS

5.7.4 Simulation

The unregulated power supply as designed will now be simulated and can be seen in figure 5.49.

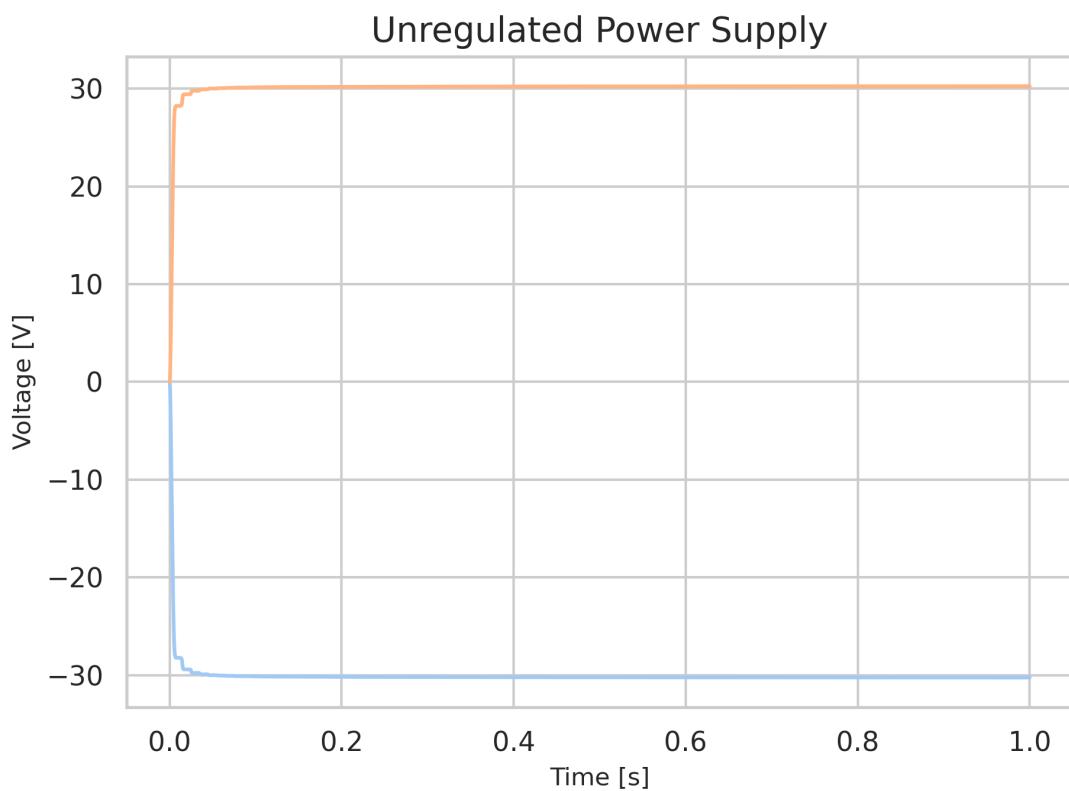


Figure 5.49: The unregulated power supply rails simulated in LTspice with the specified transformer

The small circuit supply could not be simulated as a LM2575 model was not available.

5.7.5 Conclusion

From the simulation of the unregulated power supply it is seen that it works as per the specification and has little to no ripple on the rails and if the correct transformer is used fulfills the requirements for the voltage rails so the power amplifier works.

6 | Integration

In this chapter, the integration details for the project will be covered.

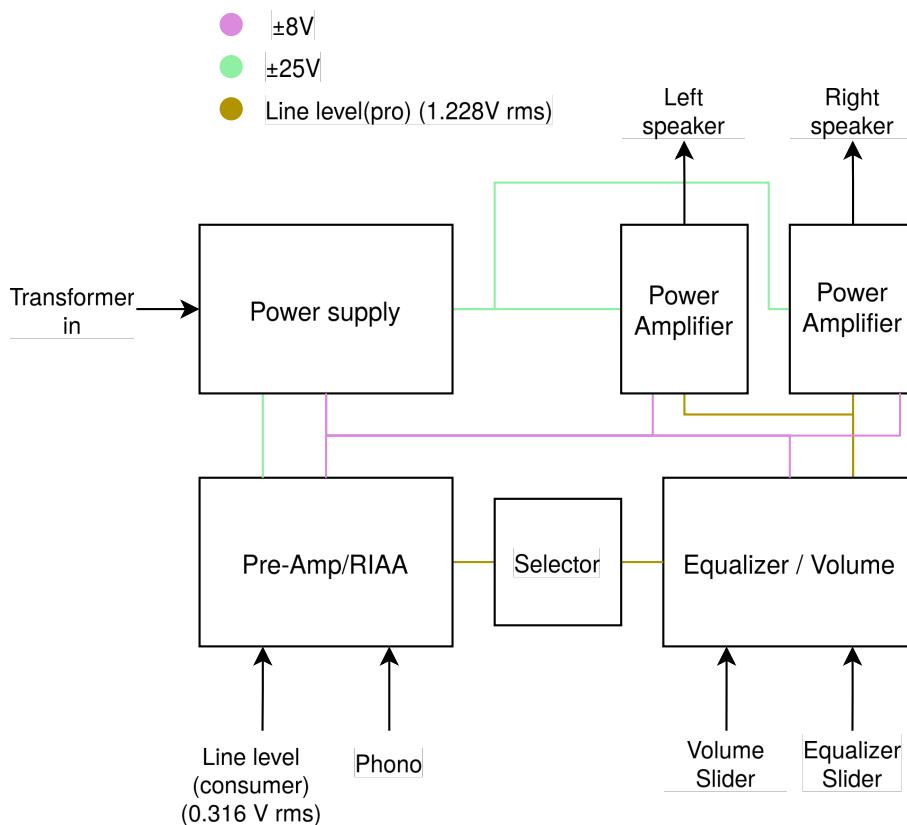


Figure 6.1: Block diagram of the system, each box represent a PCB

6.1 Integration on PCB

Some systems have been put on the same PCB for size and convenience, these systems have been integrated before the final system integration. By specifying the input and output impedance of each module as well as the output and input voltage level, it does not make much of a difference in which order the modules are placed in, except for the pre-amps and power amplifier itself. It was unanimous for all the PCBs that for quick testing, there were placed banana plugs for the power supply, and screw terminals for the signals as well as the power supply.

6.1.1 Pre-amp / RIAA

All three pre-amps are placed on the same PCB, since they will all be connected to a Selector. The only disadvantage with this, is that the Class A pre-amp requires a 30 V power supply, and for the other pre-amplifiers and the RIAA filter is unnecessary to have 30 V on the PCB. In reality 25 V was connected instead of 30 V, since that was the largest voltage which was possible to create with the transformer available.

The PCB was designed in Altium designer.

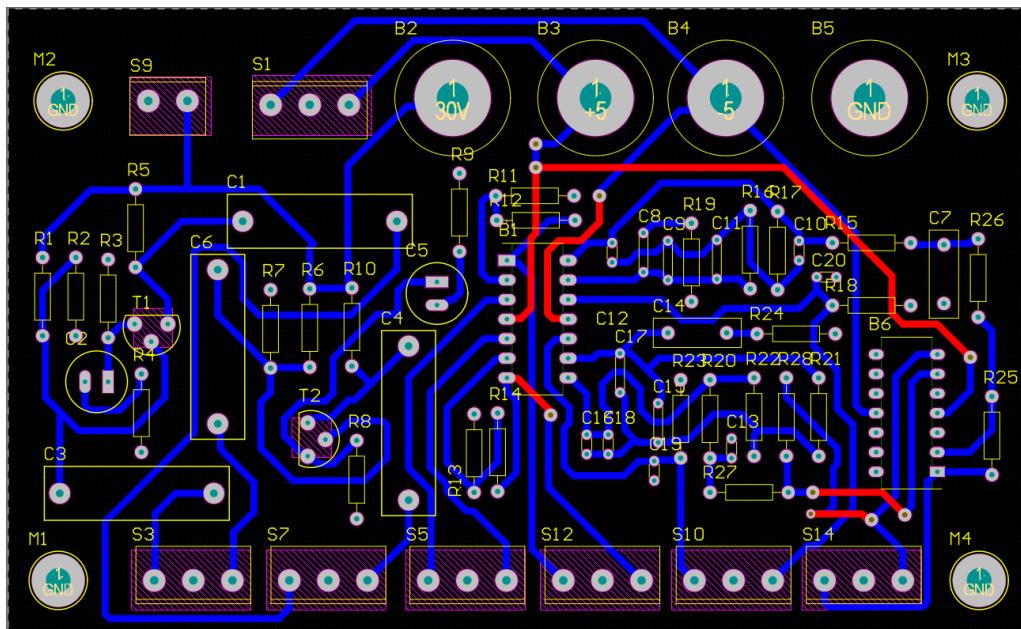


Figure 6.2: Pre-amplifier and RIAA figure from Altium Designer

Inputs (Pre-amplifier and RIAA):

1. Ground (From Power Supply)
2. +25 V (From Power Supply)
3. +8 V (From Power Supply)
4. -8 V (From Power Supply)
5. Left Signal (From AUX)
6. Right Signal (From AUX)
7. Left RIAA Signal (From Record Player)
8. Right RIAA Signal (From Record Player)

Outputs (Pre-amplifier and RIAA):

1. Ground (To Selector)
2. Left Class A signal (To Selector)
3. Right Class A signal (To Selector)
4. Left opamp pre-amp signal (To Selector)

5. Right opamp pre-amp signal (To Selector)
6. Left RIAA pre-amp signal (To Selector)
7. Right RIAA pre-amp signal (To Selector)

Then the PCB was produced.

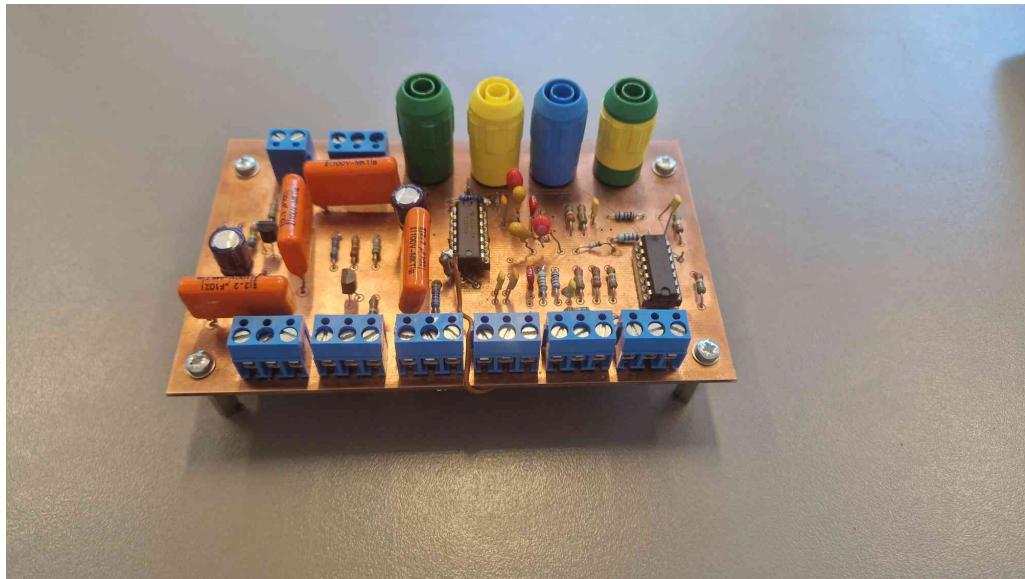


Figure 6.3: Picture of the finished RIAA and Pre-Amplifier PCB.

6.1.2 Equalizer / Volume control

The equalizer and volume control were placed on the same PCB. This was done to cut down on the amount of PCBs, and the amount of connections for power from the power supply, since both the Volume control and the Equalizer require $\pm 8V$. The input comes from the Selector, which can switch between all the different pre-amplifiers.

The PCB was designed in Altium designer.

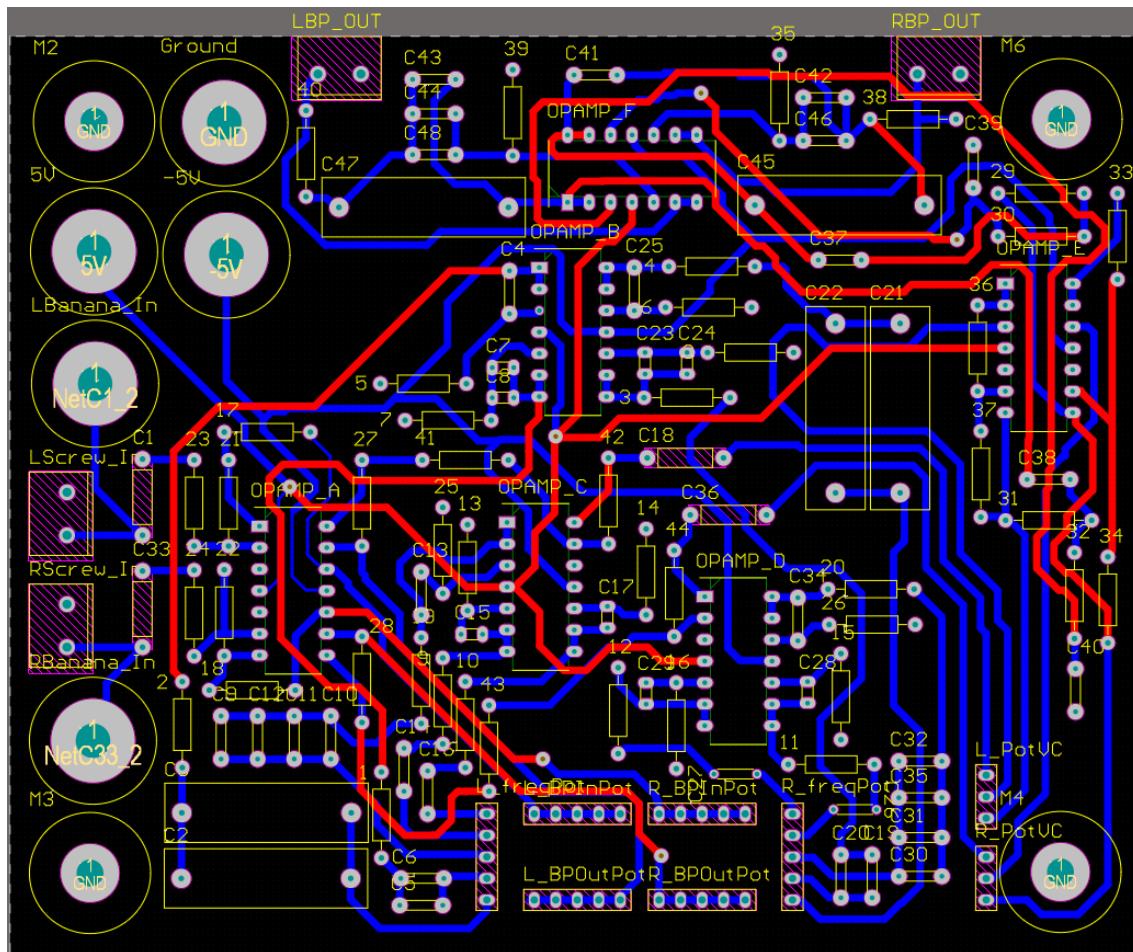


Figure 6.4: Equalizer and Volume Control figure from Altium Designer

Inputs:

1. Right Signal (From Selector)
2. Left Signal (From Selector)
3. +8 V (From Power Supply)
4. -8 V (From Power Supply)
5. Ground (From Power Supply)
6. Ground (From Selector)

Outputs:

1. Right Signal (To Right Power Amplifier)
2. Left Signal (To Left Power Amplifier)
3. Ground (To Right Power Amplifier)
4. Ground (To Left Power Amplifier)

Bandpass filter

Then the PCB was produced.

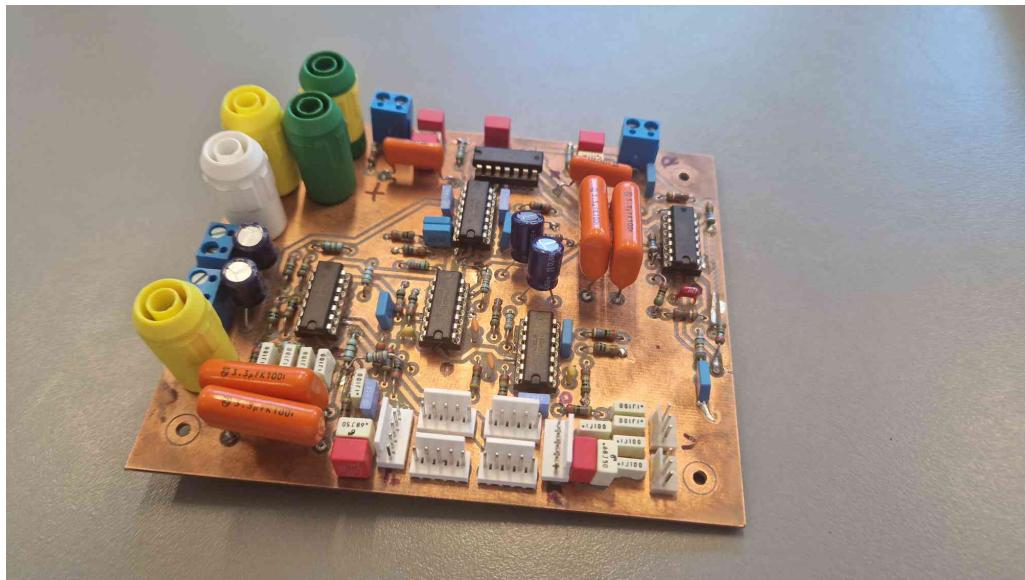


Figure 6.5: Picture of the produced equalizer and volume control.

6.2 System integration

After integrating some systems on PCB the rest of the system was integrated by working backwards from the power amplifier

6.2.1 Power amplifier

The important implementation details of the power amplifier are the inductor's position compared to each so their magnet fields don't interfere with each other. That's why two separate PCBs were chosen as the solution so the position of these wouldn't have to be worried about when laying the PCB. The other important factor is keeping the supply rails close to each other before entering the power transistors so transistor noise doesn't enter the small signal supply rail. Another implementation detail is the type of grounding used for the whole system, but this is covered in the power supply. The PCB along with a list of inputs and outputs on the amplifiers can be seen below.

The PCB was designed in Altium Designer.

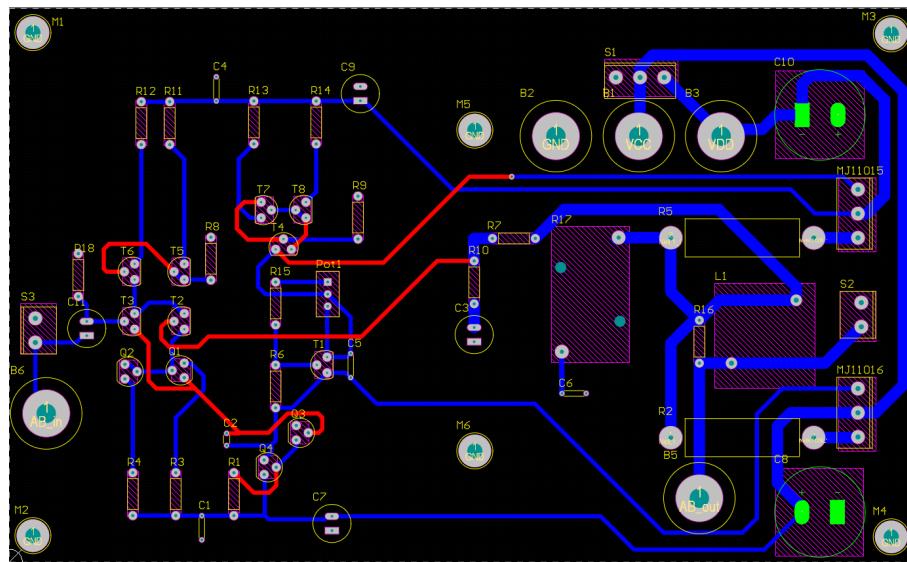


Figure 6.6: PA figure from Altium Designer

The inputs and outputs of the power amplifier are as follows:

Inputs (Left Power Amplifier):

1. Left Signal (From Equalizer and Volume Control)
2. Ground (From Equalizer and Volume Control)
3. +25 V (From Power Supply)
4. -25 V (From Power Supply)
5. Ground (From Power Supply)

Outputs (Left Power Amplifier):

1. Left Signal (To Left speaker)
2. Ground (To Left Speaker)

Inputs (Right Power Amplifier):

1. Right Signal (From Equalizer and Volume Control)
2. Ground (From Equalizer and Volume Control)
3. +25 V (From Power Supply)
4. -25 V (From Power Supply)
5. Ground (From Power Supply)

Outputs (Right Power Amplifier):

1. Left Signal (To Right speaker)
2. Ground (To Right Speaker)

Then the PCBs were produced along with the heat sink.

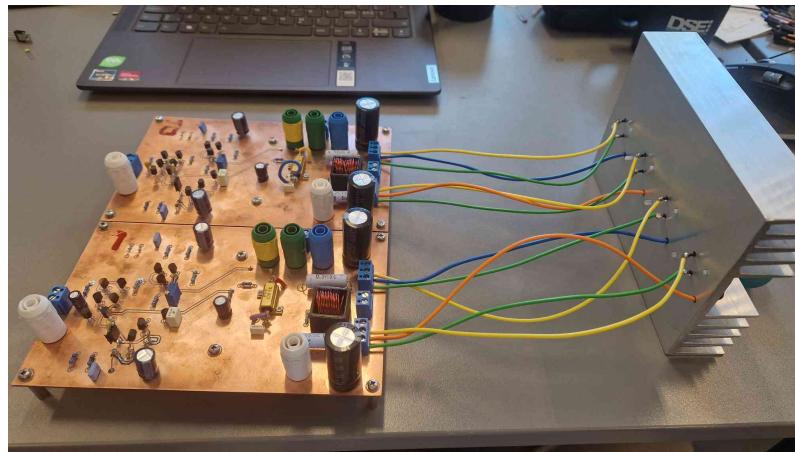


Figure 6.7: Picture of the finished power amplifier.



Figure 6.8: Picture of the power amplifier heat-sink.

6.3 Power Supply

The main power supply implementation detail was that the available transformer only has a fuse of 250mA on the main side which totals to around 50W. The transformer also has secondary winding of 18VAC which means the rails after rectification is $\pm 25V$. This was a problem since the huge capacitors chosen to keep the voltage as steady as possible when turned on draw a lot of current so two NTC thermistors on each rail were implemented seen as R_5 and R_6 so the capacitors don't blow the fuse in the transformer. The rails were drawn with a width of 100mil to ensure that enough current could be drawn without heating the trace too much. The SMPS chips were drawn as recommended by the datasheet [27]. The drawn PCB can be seen in figure 6.9.

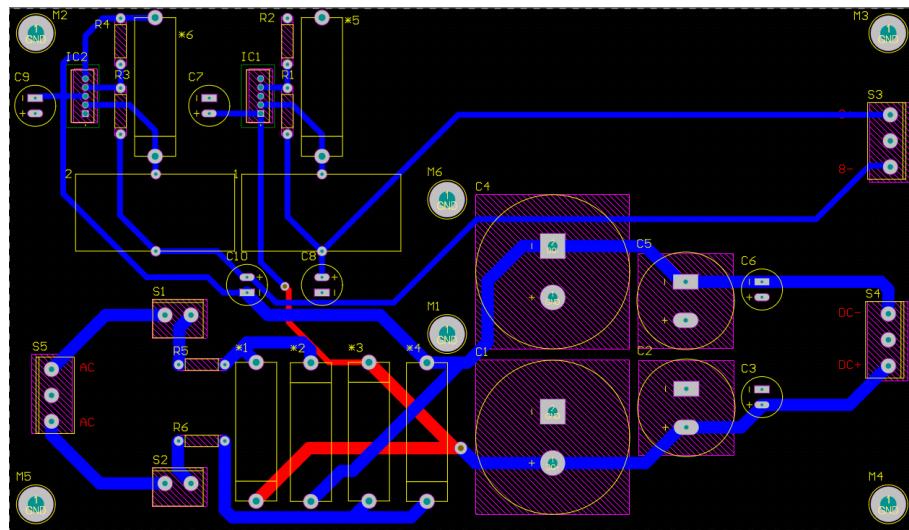


Figure 6.9: Power Supply figure from Altium Designer

The inputs and outputs on the power supply print are as follows: Inputs:

- AC
- GND
- AC

Outputs:

- +25 V
- GND
- -25 V
- +8 V
- GND
- -8 V

The final power supply can be seen in the picture below

6.3.1 Case

In order to protect the circuit from accidental touches, dust and other external factors, and to make sure eventual users don't accidentally touch rails with up to 60v across them.

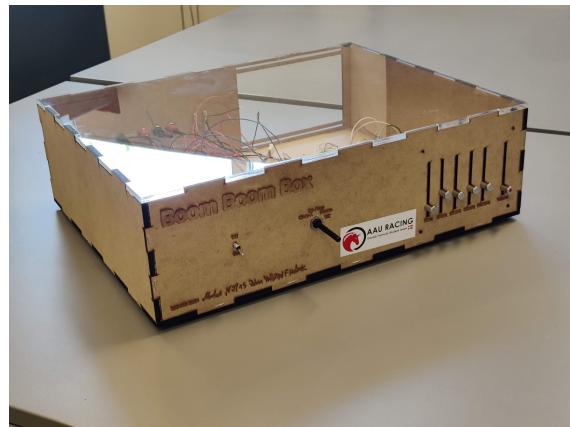


Figure 6.10: Picture of the empty amplifier case

Cad drawing

The box was first designed in CAD software and then later laser cut out of MDF and Plexiglas. The chosen design software used was OnShape.

Front Panel

On the front panel there are cutouts for the:

- Power Switch
 - Volume Control
 - Equalizer Slides
 - Selector Switch

The cad drawing for the front panel can be seen on figure 6.11.

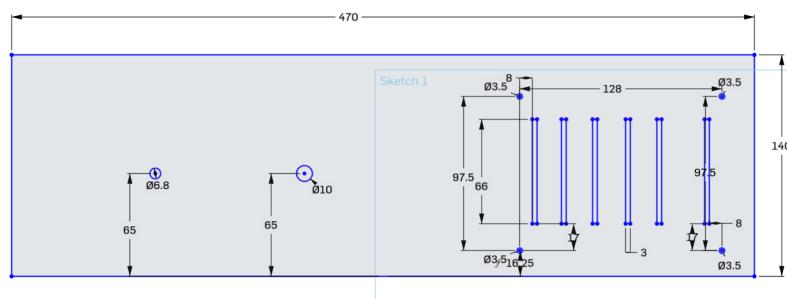


Figure 6.11: Front pane CAD drawing

The front panel will be cut out of 3mm MDF.

Back Panel

on the back pane there are cutouts for the:

- Transformer input
 - 3.5mm AUX
 - Phono left and right

- Speaker screw terminals
- Heatsink

The cad drawing for the back panel can be seen on figure 6.12.

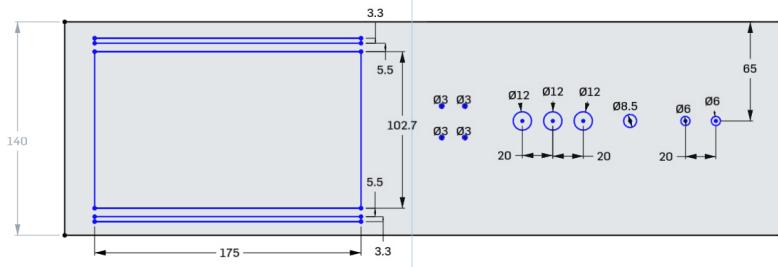


Figure 6.12: Back pane CAD drawing

The back panel will be cut out of 3mm MDF.

Bottom panel

On the bottom panel there are only screw holes for mounting all the circuit boards, the CAD drawing of the bottom panel can be seen on figure 6.13.

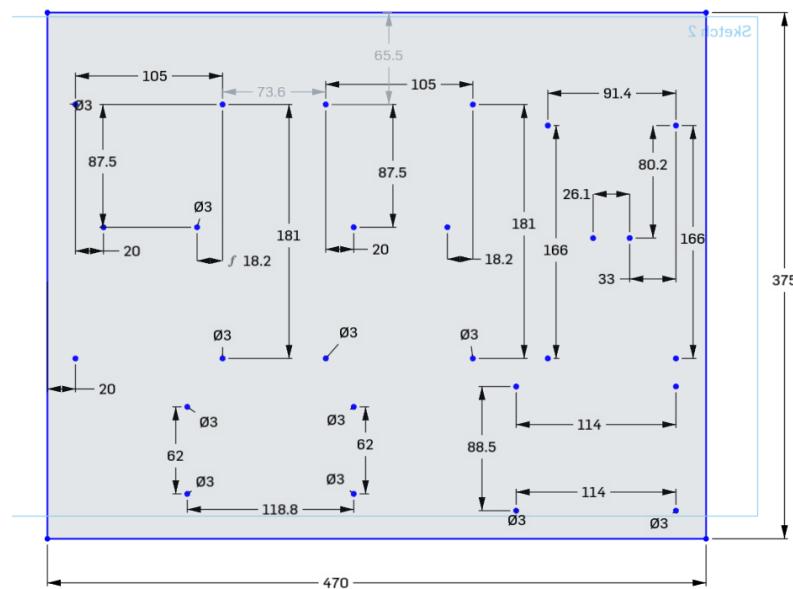


Figure 6.13: Bottom pane CAD drawing

The bottom pane will be cut out of 6mm MDF.

Side and Top

The top of the box is cut out of 5mm plexiglass so the components can be visible to the user. The side of the box will also be cut out of 6mm MDF like the bottom.

After drawing all the panel in 2D the CAD software was used to extrude these drawings

into 3D and generate the joints for assembly. A few niceties like Labels and Names where also added. The 3D model can be seen in figure 6.14

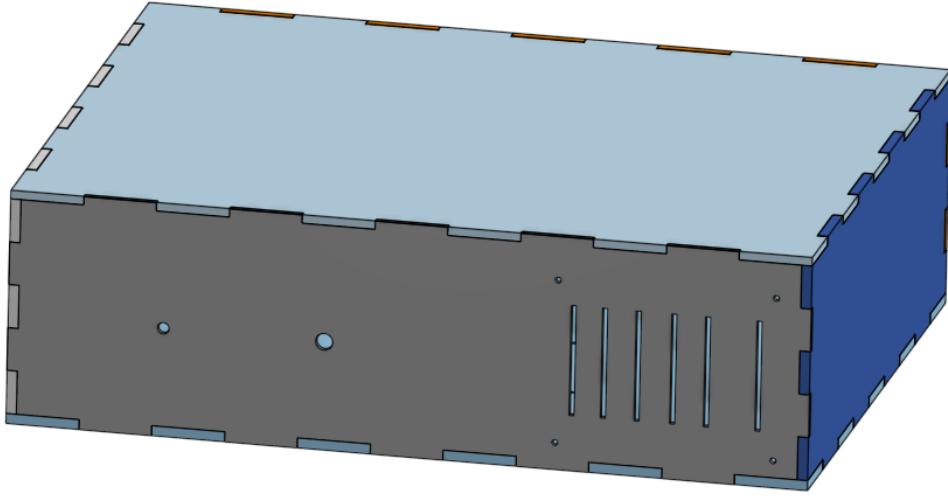


Figure 6.14: 3D CAD view of the box

6.4 PCB Revisions

During the project many iterations of printed circuit boards where made. on figure 6.15 these can be seen.

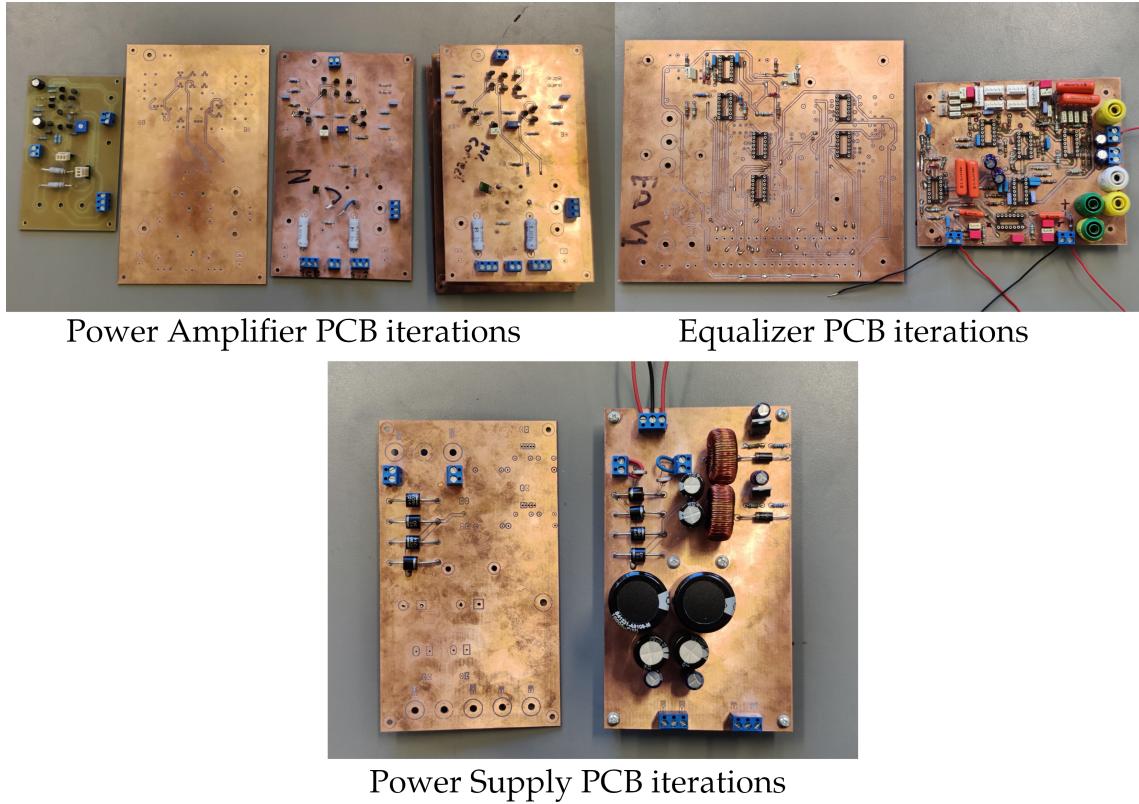


Figure 6.15: shows PCB iterations for multiple systems. Left most PCB is the oldest

7 | Testing

All test journals (setup, procedure, results, etc.) can be found in appendix D. The purpose of these tests are to determine whether the system design and integration lives up to the requirements set in section 4.

7.1 System Technical Requirements

ID	Requirement	Tolerance	Compliance
T1.1	The system must have a THD < 0.9 % at 40 Hz to 12.5 kHz	0.1 %	Not Tested
T1.2	The system must have a SNR > 55 dB	1 dB	Yes
T1.3	Output power must be at least 6 W per channel	$\pm 1\%$	Yes
T1.4	Operating frequency range must be at least 20 Hz to 20 kHz	$\pm 1\%$	Yes

Table 7.1: Technical requirements for the Hi-Fi amplifier.

7.2 Subsystem technical requirements

7.2.1 AUX-amp

ID	Requirement	Tolerance	Compliance
T2.1	Input RMS voltage must be 316 mV (line level consumer)	-	Design Choice
T2.2	Output RMS voltage must be less than 1.228 V (line level pro)	$\pm 10\%$	Yes
T2.3	Input impedance at least $470\text{k}\Omega$	-	No ¹
T2.4	Output impedance of maximum $47\text{k}\Omega$	-	Yes

¹ Passed until approx. 8 kHz.

Table 7.2: Technical requirements for the AUX-amp.

7.2.2 RIAA

ID	Requirement	Tolerance	Compliance
T3.1	Input impedance $47\text{k}\Omega$ parallel with 220pF	5%	Yes
T3.2	Nominal input voltage: 5mVrms	-	Design Choice
T3.3	Input voltage range: 2mVrms to 35mVrms	-	Design Choice
T3.4	Output RMS voltage must be less than 1.228 V (line level pro)	$\pm 10\%$	Yes

Table 7.3: Technical requirements for the RIAA.

7.2.3 Equalizer and Volume Control

ID	Requirement	Tolerance	Compliance
T4.1	Input RMS voltage must be less than 1.228 V (line level pro)	$\pm 10\%$	Yes
T4.2	Must be a 5-band graphic equaliser	-	Yes
T4.3	Output RMS voltage must be less than 1.228 V (line level pro)	$\pm 10\%$	Yes

Table 7.4: Technical requirements for the equalizer and volume control.

7.2.4 Power Amplifier

ID	Requirement	Tolerance	Compliance
T5.1	Output power must be at least 6 W	-	Yes
T5.2	Gain must be constant in the 20 Hz to 20 kHz effective frequency range	$\pm 2\text{dB}$	Yes
T5.3	The power amplifier must be able to operate at maximum output power for at least 10 minutes at an ambient temperature between 15°C and 35°C	-	Not Tested
T5.4	Input RMS voltage must be less than 1.228 V (line level pro)	$\pm 10\%$	Design Choice
T5.5	Input impedance at least $470\text{k}\Omega$	-	Yes
T5.6	The power amplifier must have a $\text{THD} < 0.6\%$ at 40 Hz to 12.5 kHz	0.1 %	Yes

Table 7.5: Technical requirements for the power amplifier.

8 | Discussion

Due to time constraints, the project will include no further design work, however, this section will cover lessons learned in terms of improving the design in further iterations.

8.1 Preamp Consolidation

The current design includes 2 (3) different preamps: aux preamp (class A and opamp) and RIAA preamp. Since the RIAA module contains two amplification stages, the second being similar to the aux preamp gain (consumer line level input), the preamps could be consolidated into a single preamp with an input selector switching between aux input and RIAA input. This would reduce both cost and complexity of the system.

8.2 Overvoltage Protection

The amplifier lacks overvoltage protection, rendering it vulnerable to damage or failure when subjected to excessively large input signals. Overvoltage clamping diodes could be implemented on the aux and RIAA inputs to mitigate damage to the amplifier.

8.3 Power Amplifier Input Filter

The bandpass input filter between the volume control and power amplifier is integrated on the same PCB as the equalizer and volume control. By integrating it as part of the power amplifier, the input impedance of this module would be sufficient such that the input voltage follower would not be required, thereby saving an opamp.

8.4 Input Level Detection

Many amplifier designs implement some form of input level detection. This allows the amplifier to turn off the power output when no music signal is connected, decreasing audible noise.

9 | Conclusion

Bibliography

- [1] J. David Irwin and R. Mark Nelms. *Engineering Circuit Analysis*. 12th ed. John Wiley and Sons Singapore Pte. Ltd, 2021.
- [2] Kendall L. Su. *Analog Filters*. Second. Springer, 2002. ISBN: 978-0792376566.
- [3] Ianf. "Equaliser-section.jpg". In: Wikimedia (2006). URL: <https://commons.wikimedia.org/wiki/File:Equaliser-section.jpg>.
- [4] Ianf. "Shelving-eq.svg". In: Wikimedia (2006). URL: <https://en.m.wikipedia.org/wiki/File:Shelving-eq.svg>.
- [5] Electronics Tutorials. *Bipolar Transistor*. 17-04-2024. 2024. URL: https://www.electronics-tutorials.ws/transistor/tran_1.html.
- [6] BC546/BC547/BC548/BC549/BC550 NPN Epitaxial Silicon Transistor. Accessed 23/04/2024. SparkFun Electronics. Niwot, Colorado, USA, 2008. URL: <https://www.sparkfun.com/datasheets/Components/BC546.pdf>.
- [7] Electronics Tutorials. *NPN Transistor*. 17-04-2024.
- [8] Circuits Today. *FET - Field Effect Transistors Introduction*. Accessed on April 23, 2024. 2024. URL: <https://www.circuitstoday.com/fet-field-effect-transistors-introduction>.
- [9] Douglas Self. *Audio Power Amplifier Design Handbook*. eng. focal press, 2009. ISBN: 978-0-240-52162-6.
- [10] Don Tuite. "Understanding Amplifier Operatin "Classes"". In: *Electronic Design* (2012). URL: <https://www.electronicdesign.com/technologies/analog/article/21801654/understanding-amplifier-operating-classes>.
- [11] Rich Tozzoli. *How Does a Vinyl Record Make Sound?* Accessed: April 17, 2024. 2021. URL: <https://hub.yamaha.com/audio/vinyl/how-does-a-vinyl-record-make-sound/>.
- [12] Wikipedia contributors. *RIAA equalization*. Online; accessed 17-April-2024. 2024. URL: <http://en.wikipedia.org/w/index.php?title=RIAA\%20equalization&oldid=1218177104>.
- [13] Douglas Self. *Small Signal Audio Design*. eng. Focal Press, 2020.
- [14] S. P. Lipshitz. *On RIAA Equalisation Networks*. eng. Journal of Audio Engineering Society, 1979.
- [15] The Free Dictionary. *Moving Coil*. Online; accessed 17-April-2024. URL: <https://encyclopedia2.thefreedictionary.com/Moving+Coil>.

- [16] Craig Walker. *Moving Coil vs Moving Magnet Cartridges: What's The Difference?* Online; accessed 17-April-2024. 2024. URL: https://www.kbaudio.co.uk/blogs/reco_rd-players/moving-coil-vs-moving-magnet-cartridges-what-s-the-difference.
- [17] DALI Danish American LTD. Inc. *You can afford to listen to DALI.* <https://www.dali-speakers.com/media/3262/dali-2-brochure.pdf>. 1982.
- [18] Wikipedia contributors. *Total Harmonic Distortion.* Accessed: April 17, 2024. 2024. URL: https://en.wikipedia.org/wiki/Total_harmonic_distortion.
- [19] Adel S. Sedra and Kenneth C. Smith. *Microelectronic Circuits.* 7th ed. Oxford University Press, 2014.
- [20] Bruce Carter. *An audio circuit collection, Part 3.* 2005. URL: https://www.ti.com/lit/an/slyt134/slyt134.pdf?ts=1714587756560&ref_url=https%3A%2F%2Fwww.google.com%2F.
- [21] *MJ11016/5 Power Transistor.* NPN Silicon Power Darlington Transistor. ON Semiconductor. 2022. URL: <https://www.onsemi.com/pdf/datasheet/mj11012-d.pdf>.
- [22] *TO-3 Isolation Pad.* <https://www.tme.eu/en/details/mica-to3/heatsinks-equiment/ninigi/>. Accessed on: May 6, 2024.
- [23] *WA202 Heatsink Datasheet.* https://www.komponenten.es.aau.dk/fileadmin/komponenten/Data_Sheet/Applikation/Wa202.pdf. Accessed on: May 6, 2024.
- [24] Texas Instruments. *lm2575 datasheet.* May 2015. URL: <https://www.ti.com/lit/ds/symlink/lm2575-n.pdf>.
- [25] *BY214-1000 datasheet.* 2005. URL: <https://datasheetspdf.com/datasheet-pdf/118618/BY214-1000.html>.
- [26] *1n5408 datasheet.* 2001. URL: https://www.komponenten.es.aau.dk/fileadmin/komponenten/Data_Sheet/Diode_og_Brokobling/1N5407.pdf.
- [27] Brigitte Hauke. *Basic Calculation of a Buck Converter's Power Stage.* 2015. URL: <https://www.ti.com/lit/an/slva477b/slva477b.pdf?ts=1711517988809>.

Glossary

AC Alternating Current. 64

BJT Bipolar Junction Transistor. 10–15

CD Compact disk. 4

DC Direct Current. 21, 22, 63, 64

DUT Device Under Test. 101, 102, 109, 110, 114, 115, 117

Eq Equalizer. 9, 10

FET Field Effect Transistor. 10, 14, 15

Hi-Fi High Fidelity. 2, 4, 26, 90

HP High Pass. 6, 7

IC Integrated Circuit. 21, 73

JFET Junction Field Effect Transistor. 15

LP Low Pass. 6, 7, 34

MOSFET Metal Oxide Semiconductor Field Effect Transistor. 10, 11, 15

NC Not Connected. 102, 110, 115

PC Personal Computer. 4

PCB Printed Circuit Board. 92

PSRR Power Supply Rejection Ratio. 21

PWM Pulse Width Modulation. 18

RIAA Recording Industry Association of America. 4, 5, 19, 27, 91, 92

RMS Root mean square. 4, 44

RPM Revolutions Per Minute. 19

SMPS Switch Mode Power Supply. 76

SNR Signal-to-Noise ratio. 26, 90, 117, 118

THD Total Harmonic Distortion. 26–28, 90, 91, 101–106, 108

A | Attachments

B | Attached files

The files from the project repository https://github.com/niclasapdk/esd4_project/ are also attached in a zip archive. The attached files have the following paths relative to the zip archive root.

1. *integration_test/audio_analyser_plot.py*
2. *integration_test/input_impedance_analogdiscovery.py*
3. *integration_test/output_impedance_analogdiscovery.py*

C | Simulation Schematics

C.1 Open Loop Gain

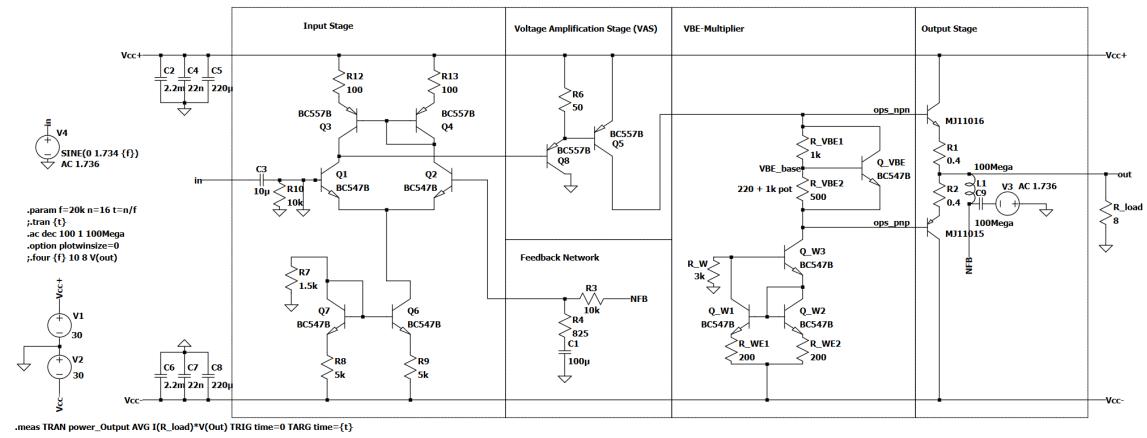


Figure C.1: Schematic of the open loop test as performed in LTspice

D | Test Journals

D.1 THD and Frequency Response

D.1.1 Purpose

Measure the THD and frequency response of all subsystems to determine whether they comply with the requirements.

D.1.2 Equipment

- NI-PCI-4461 audio analyzer
- Hameg HM7042 power supply
- DUT

D.1.3 Procedure

1. Connect the equipment as shown in figure D.1. Specific test parameters are shown in table D.1.
2. Set the audio analyzer to the following settings:
 - 204.8 kHz sampling rate.
 - 20 Hz to 20 kHz frequency sweep in 300 steps.
 - Input amplitude for the respective DUT is shown in table D.1.
 - 5th harmonic as maximum THD harmonic.
3. Turn on power supply.
4. Start frequency sweep.
5. Save results as a tsv file.
6. Use the python script provided as attachment 1 to process results.

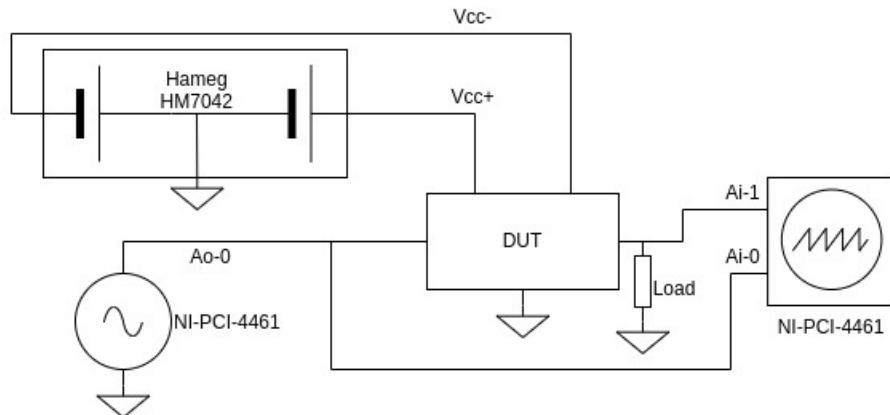


Figure D.1: Test setup for THD and frequency response measurements.

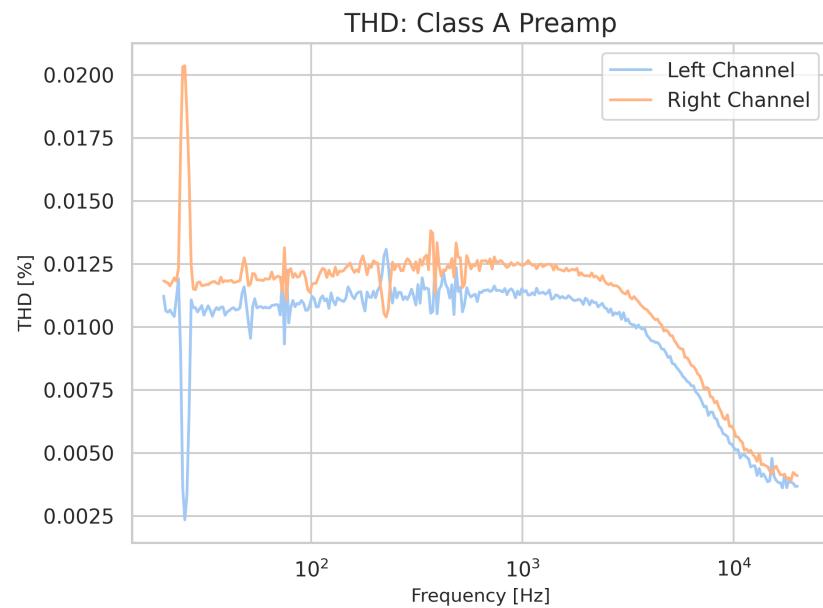
DUT	Input amplitude [V]	Load [Ohm]	Vcc+ [V]	Vcc- [V]
Class A preamp	0.447	470k	30	NC
Opamp preamp	0.447	470k	8	-8
RIAA	0.007	470k	8	-8
RIAA with opamp	0.007	470k	8	-8
EQ and Volume Control	1.736	470k	8	-8
Power Amplifier	1.18 ^a	8.2	30	-30

^a The power resistor which was available as a load was 18W, so the input amplitude of the power amplifier is lower than line level pro in order to not exceed the power rating of the resistor.

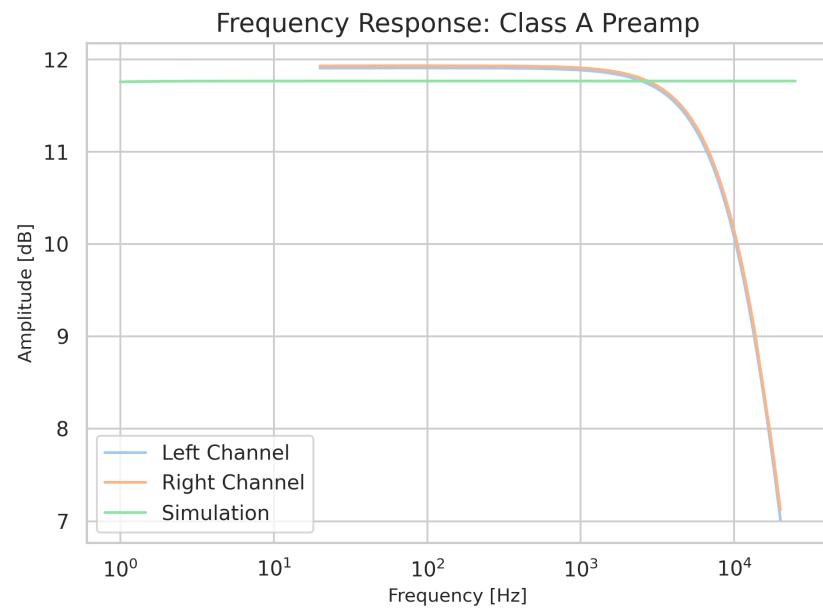
Table D.1: Test parameter overview.

D.1.4 Results

Class A

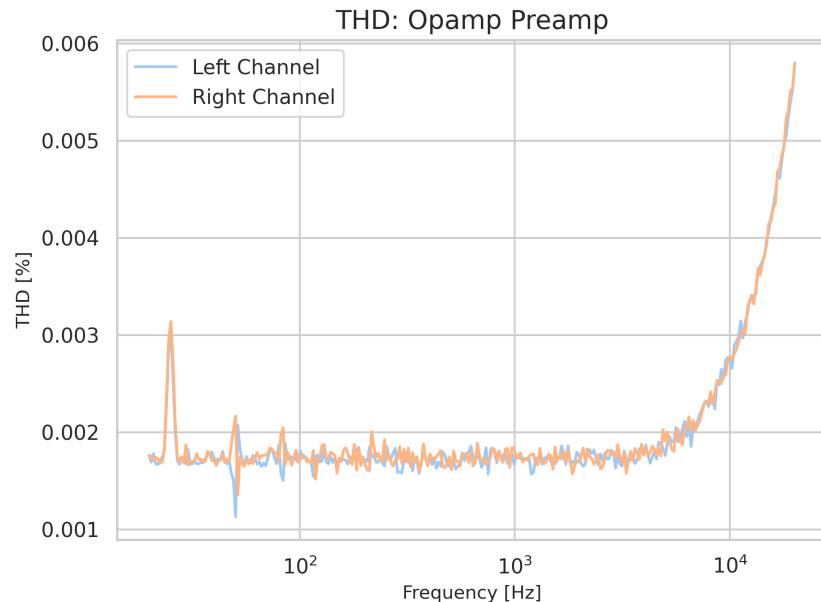


(a) THD for class A preamp.

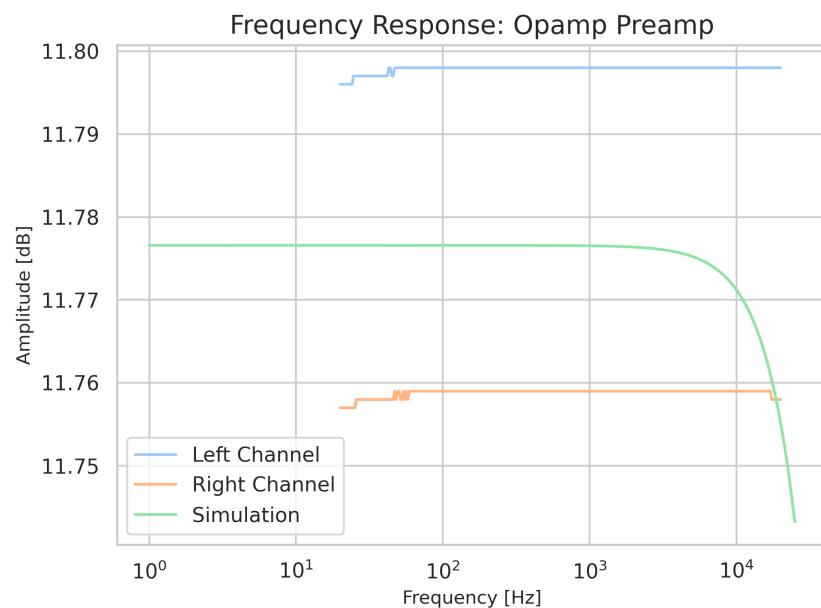


(b) Frequency response for class A preamp.

Figure D.2: Test results for class A preamp.

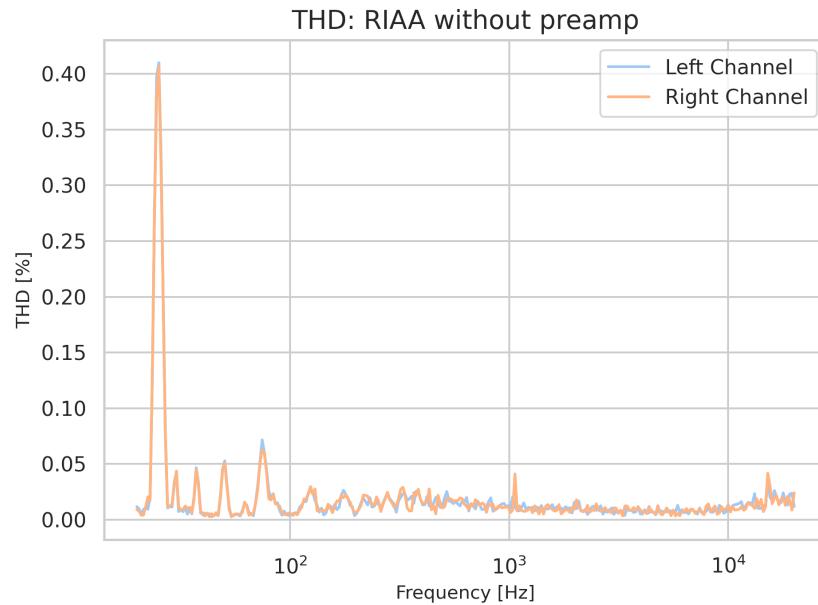
Opamp preamp

(a) THD for opamp preamp.

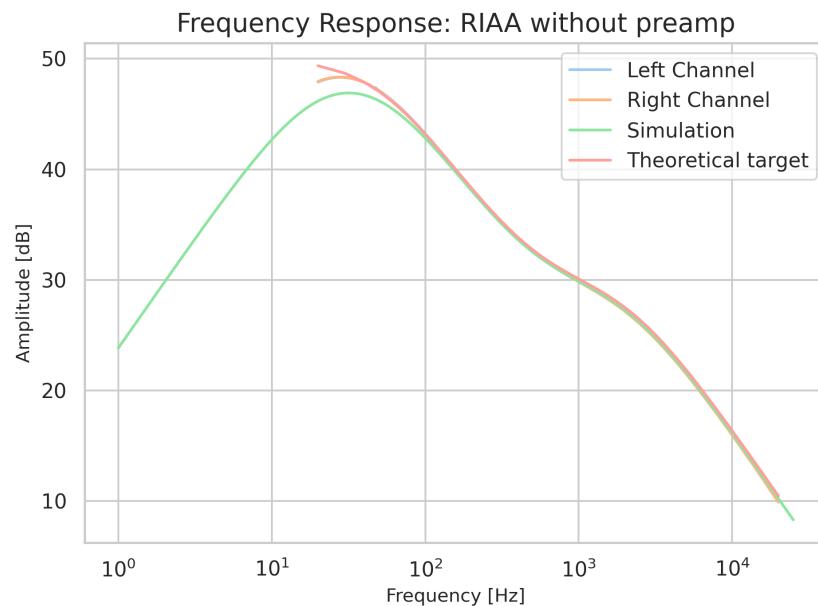


(b) Frequency response for opamp preamp.

Figure D.3: Test results for opamp preamp.

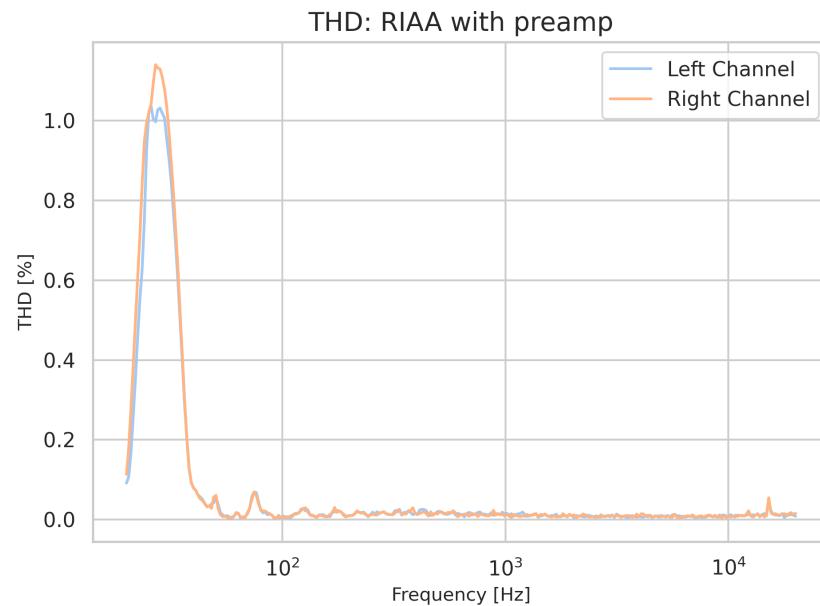
RIAA

(a) THD for RIAA.

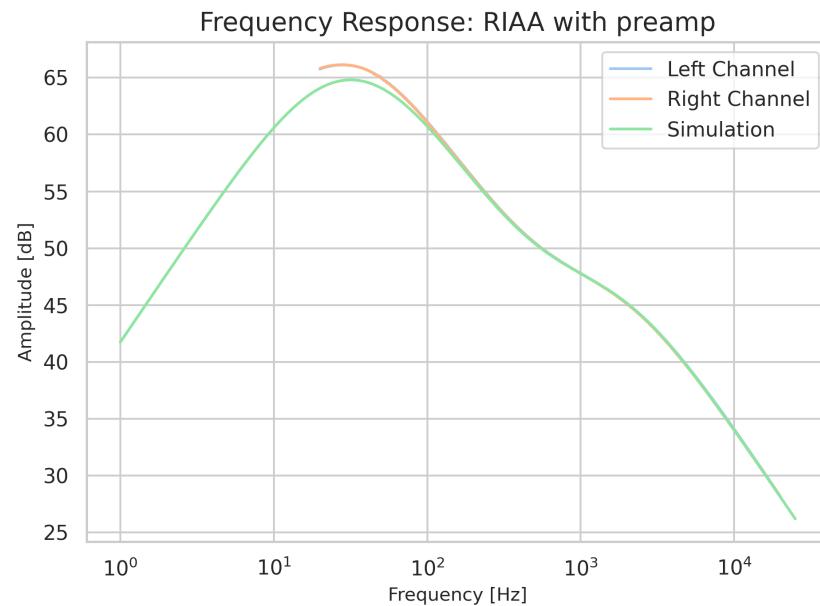


(b) Frequency response for RIAA.

Figure D.4: Test results for RIAA.



(a) THD for RIAA with opamp.

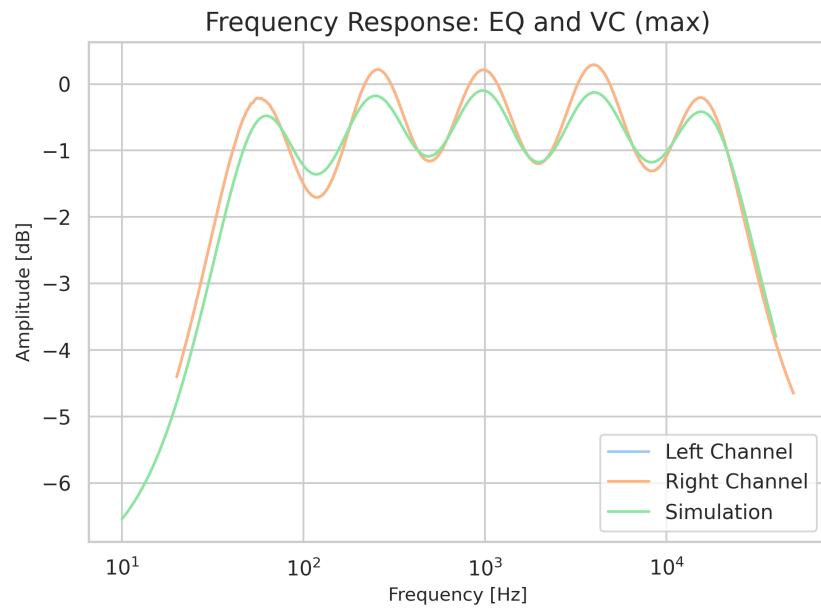


(b) Frequency response for RIAA with opamp.

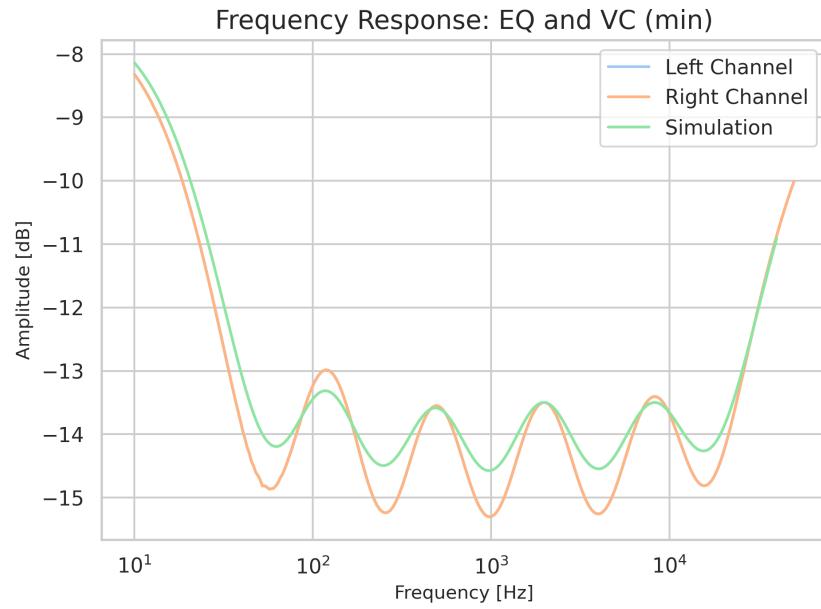
Figure D.5: Test results for RIAA with opamp.

Equalizer and Volume Control

Note that data for left and right channels are identical and are the exact same data file.



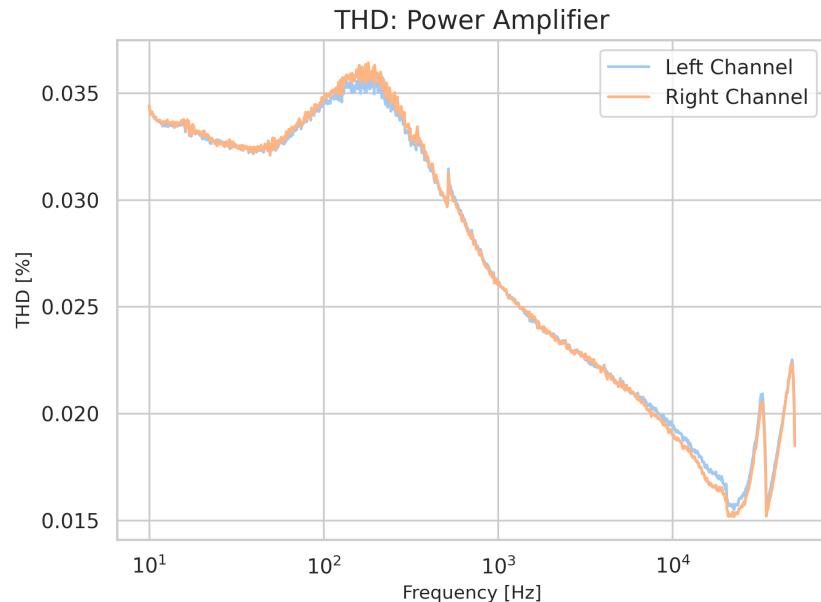
(a) Frequency response for EQ and Volume Control at maximum setting.



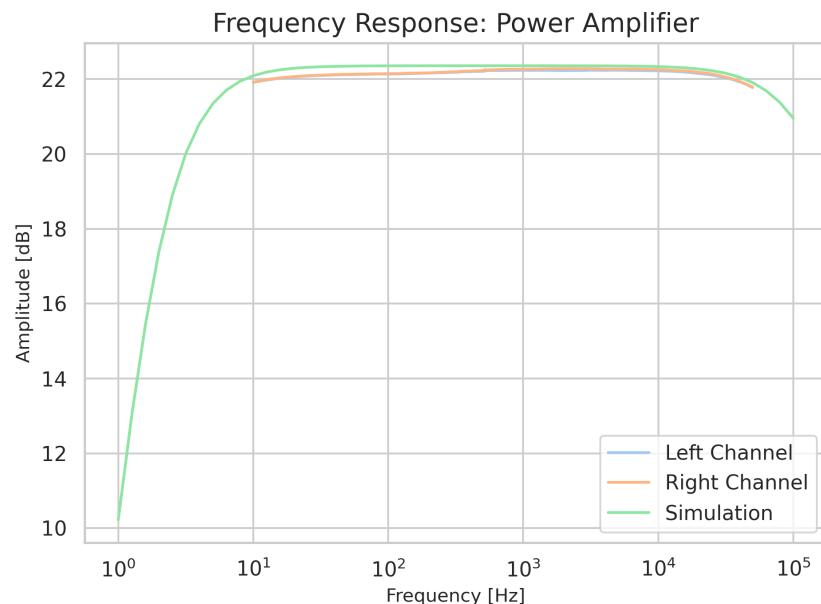
(b) Frequency response for EQ and Volume Control at minimum setting.

Figure D.6: Test results for EQ and Volume Control.

Power Amplifier



(a) THD for Power Amplifier.



(b) Frequency response for Power Amplifier.

Figure D.7: Test results for Power Amplifier.

D.2 Input Impedance

D.2.1 Purpose

Measure the input impedance of all subsystems to determine whether they comply with the requirements.

D.2.2 Equipment

- Analog Discovery 2 and Analog Discovery Impedance Analyzer
- Hameg HM7042 power supply
- DUT

D.2.3 Procedure

1. Connect the equipment as shown in figure D.8. Specific test parameters are shown in table D.2.
2. Set the Analog Discovery 2 to impedance measurement.
3. Turn on power supply.
4. Start frequency sweep.
5. Save results as a csv file.
6. Use the python script provided as attachment 2 to process results.

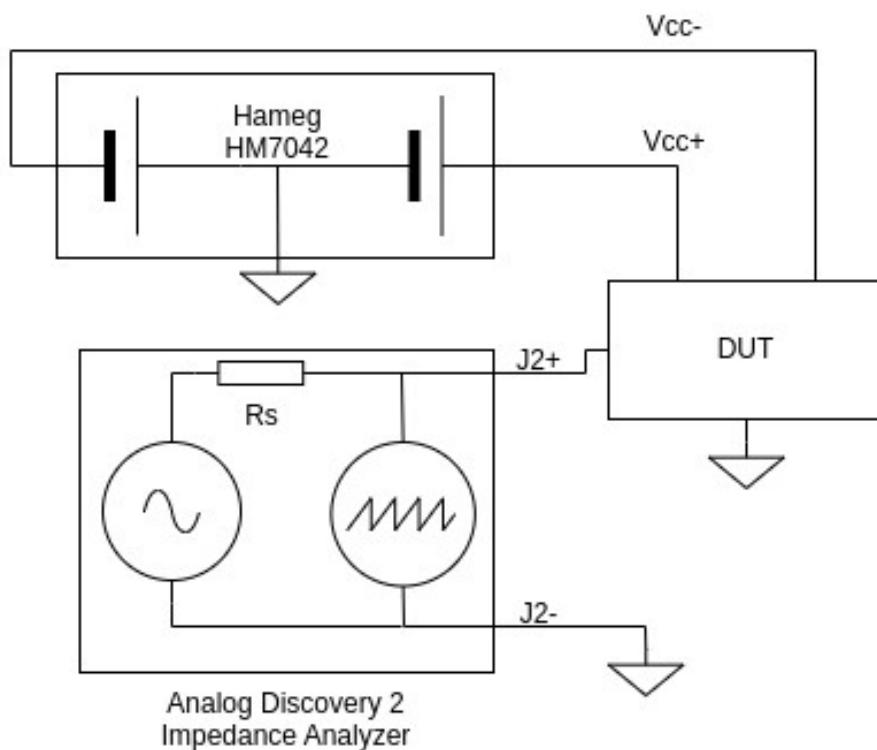


Figure D.8: Test setup for input impedance measurement.

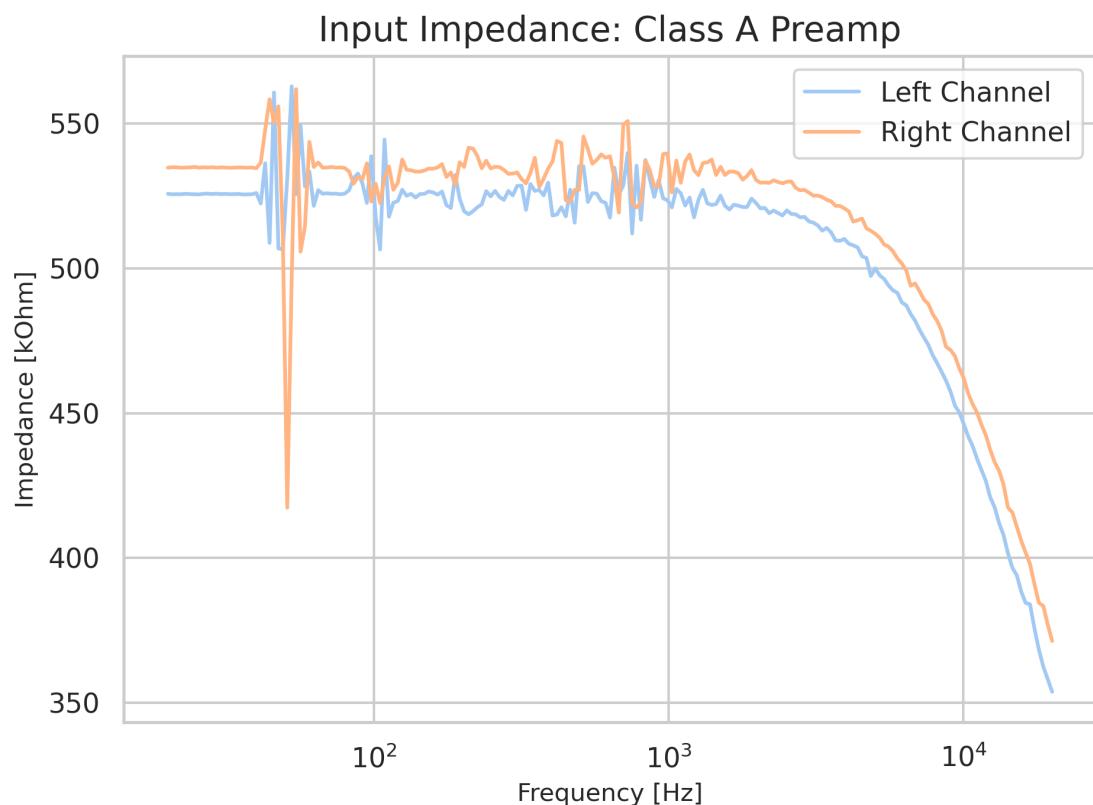
DUT	Input amplitude [V]	Resistor [kOhm]	Vcc+ [V]	Vcc- [V]
Class A preamp	0.447	100	30	NC
Opamp preamp	0.447	100	8	-8
RIAA	0.007	1000	8	-8
EQ and Volume Control	1.736	1000	8	-8
Power Amplifier	1.18 ^a	1	30	-30

Table D.2: Test parameter overview.

^a The power resistor which was available as a load was 18W, so the input amplitude of the power amplifier is lower than line level pro in order to not exceed the power rating of the resistor.

D.2.4 Results

Class A

**Figure D.9:** Input Impedance for class A preamp.

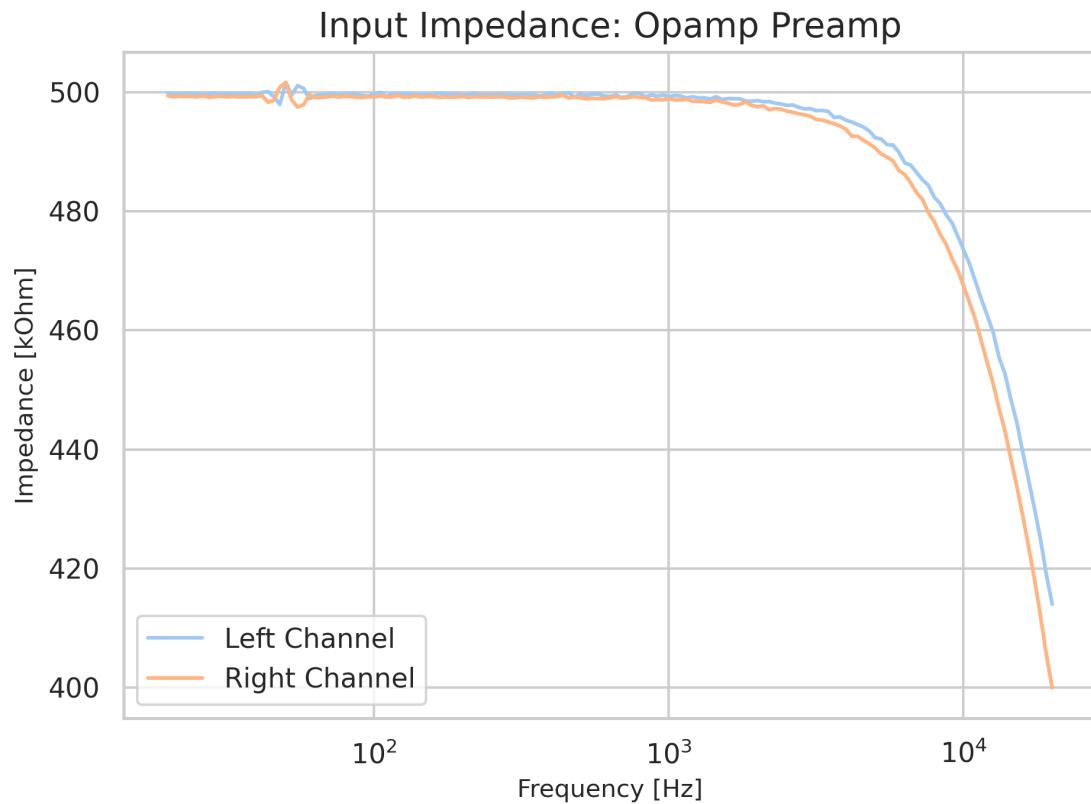
Opamp preamp

Figure D.10: Input Impedance for opamp preamp.

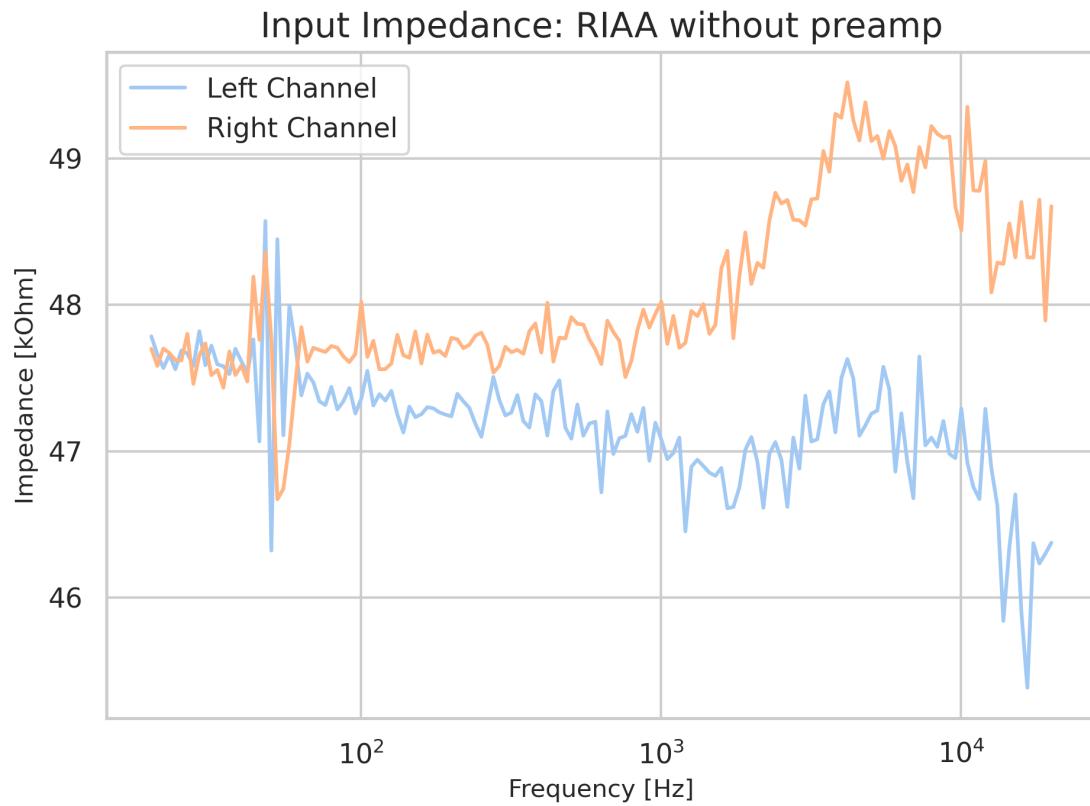
RIAA

Figure D.11: Input Impedance for RIAA.

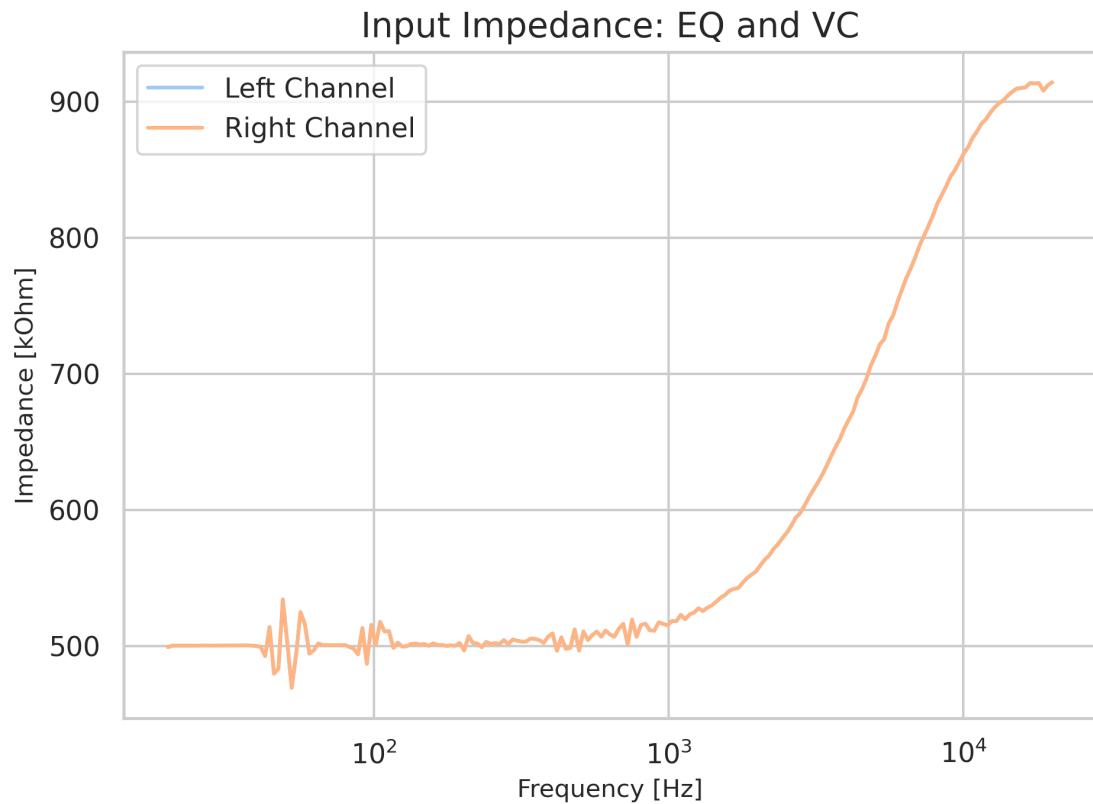
Equalizer and Volume Control

Figure D.12: Frequency response for EQ and Volume Control.

Power Amplifier

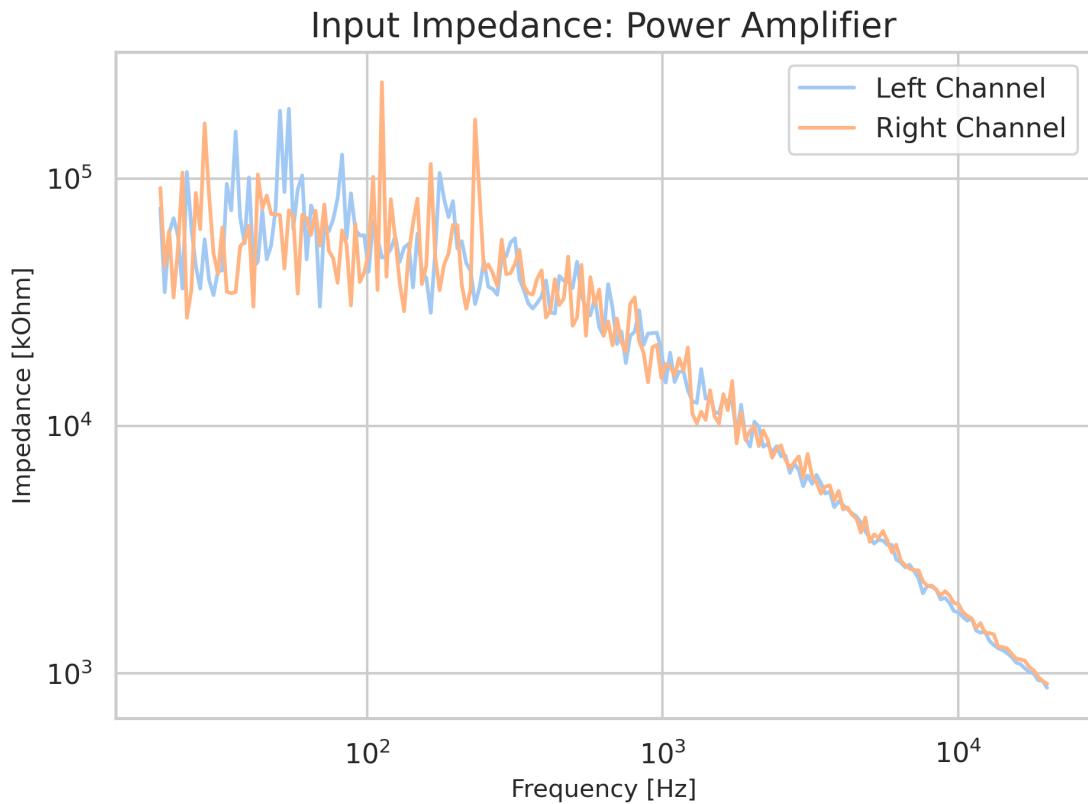


Figure D.13: Input Impedance for Power Amplifier.

D.3 Output Impedance

D.3.1 Purpose

Measure the output impedance of pre-amps to determine whether they comply with the requirements.

D.3.2 Equipment

- Analog Discovery 2
- Hameg HM7042 power supply
- DUT
- Series resistors

D.3.3 Procedure

1. Connect the equipment as shown in figure D.14. Specific test parameters are shown in table D.3.
2. Set the Analog Discovery 2 to frequency sweep.
3. Turn on power supply

4. Start frequency sweep
5. Save results as a csv file
6. Use the python script provided as attachment 3 to process results

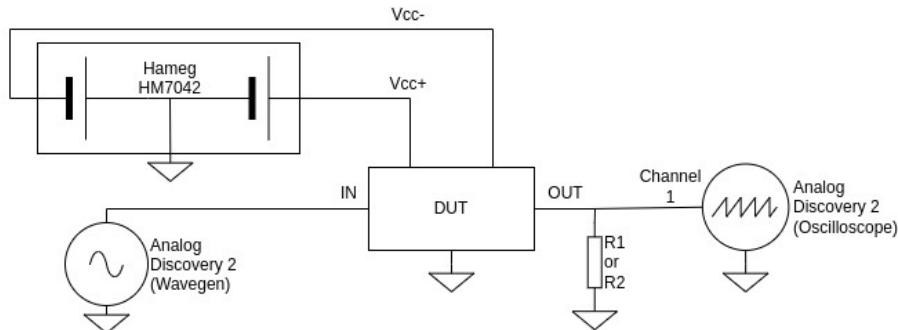


Figure D.14: Test setup for output impedance measurement.

DUT	Input amplitude [V]	Resistor [kOhm]	Vcc+ [V]	Vcc- [V]
Class A pre-amp	0.447	100 and 200	30	NC
Opamp pre-amp	0.447	1 and 2	8	-8

Table D.3: Test parameter overview.

Measurement Principle

Figure D.15 shows the model for an equivalent circuit for the output impedance measurement test setup. The goal is to measure the value Z_{out} . Complex voltage division means V_{div} can be expressed as

$$V_{div} = V_{in} \frac{R_i}{R_i + Z_{out}} \quad (D.1)$$

Isolating Z_{out} yields

$$R_i = \frac{R_i}{V_{div}} V_{in} - Z_{out} \quad (D.2)$$

Measuring frequency sweep with two different resistors gives a system of linear equations with two unknowns, $[V_{in}, Z_{out}]$.

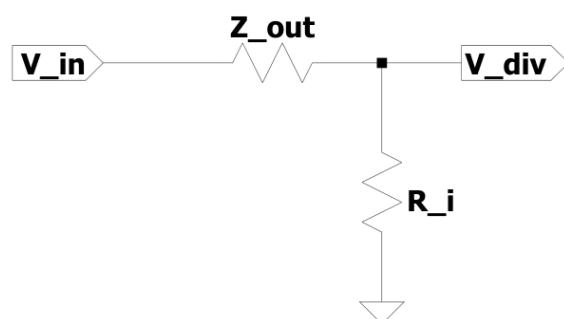


Figure D.15: Equivalent circuit for output impedance measurement.

D.3.4 Results

Class A

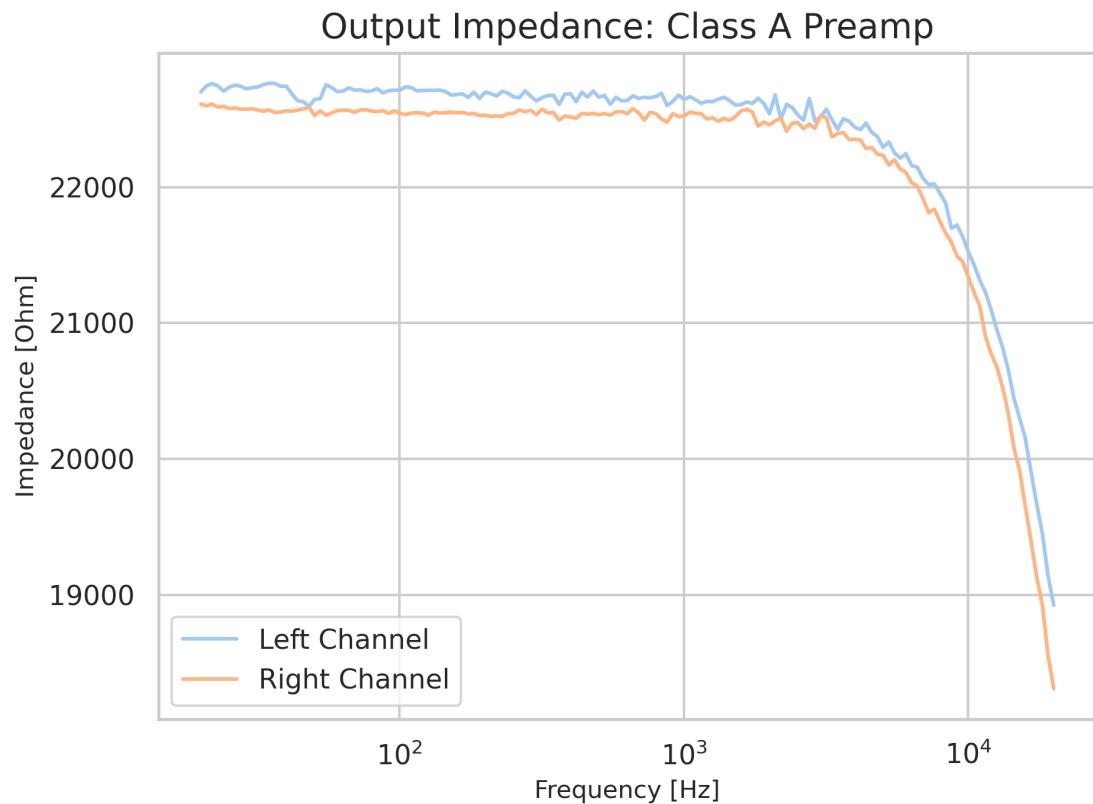


Figure D.16: Output Impedance for class A pre-amp.

Opamp pre-amp

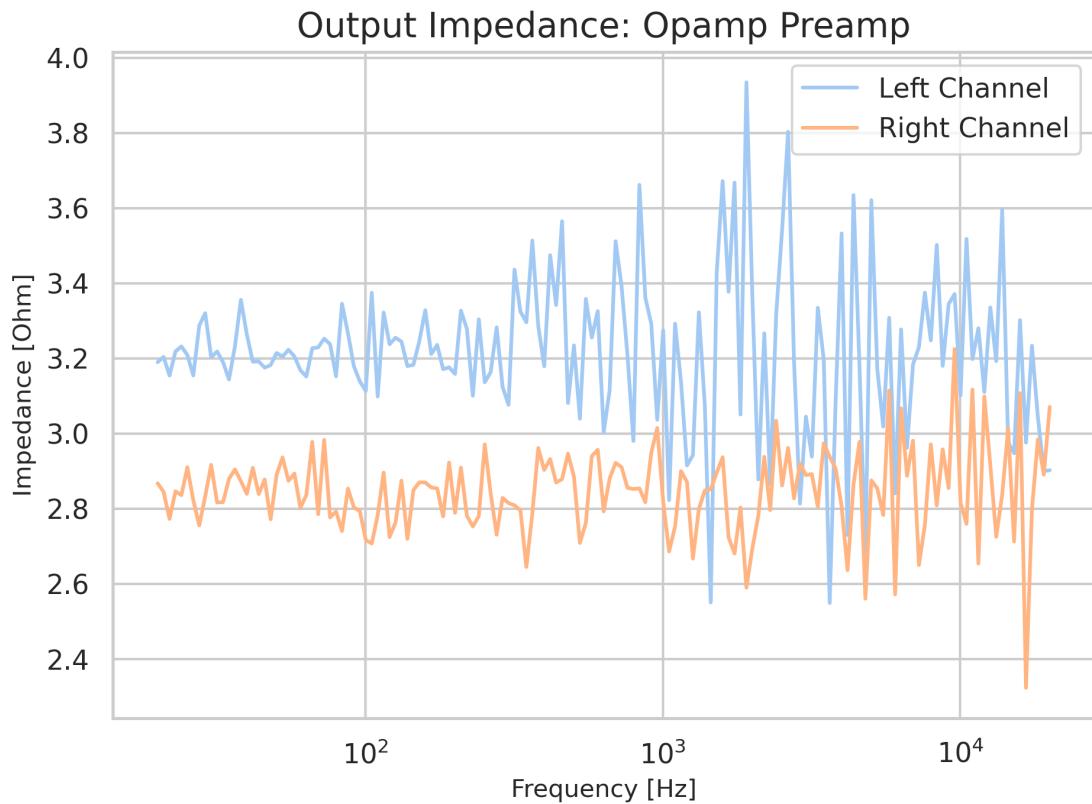


Figure D.17: Output Impedance for opamp pre-amp.

D.4 Signal-to-Noise Ratio

D.4.1 Purpose

Measure the SNR of the whole system to determine whether it complies with the requirements.

D.4.2 Equipment

- Oscilloscope: Keysight DSOX1102G
- Hameg HM7042 power supply (2)
- DUT

D.4.3 Procedure

1. Connect the equipment as shown in figure D.18.
2. Turn on power supply ($\pm 30V$ and $\pm 8V$).
3. Measure peak-peak output level, $v_{nosignal}$.
4. Save results as a csv file.

5. Turn on signal generator at 1 kHz, 0.447mV amplitude sine-wave.
6. Measure peak-peak output level, v_{signal} .
7. Save results as a csv file.
8. Calculate

$$\text{SNR} = 20 \cdot \log_{10}\left(\frac{v_{\text{signal}}}{v_{\text{nosignal}}}\right) \quad [\text{dB}] \quad (\text{D.3})$$

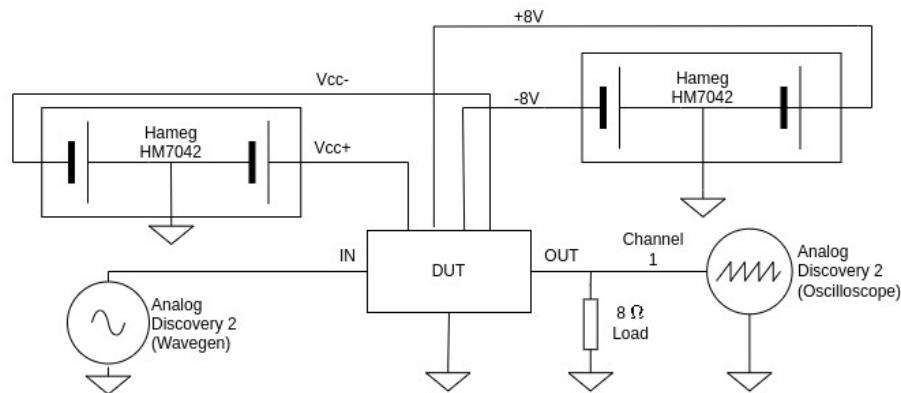


Figure D.18: Test setup for SNR measurement.

D.4.4 Results

Measurement results yielded

$$v_{\text{nosignal}} = 12.9 \text{ mV}$$

$$v_{\text{signal}} = 18.5 \text{ V}$$

$$\text{SNR} = 63.1 \text{ dB}$$