

Operational Transconductance Oscilloscope Driver Amplifier

Columbia University ELEN 4312 Analog Electronic Circuits

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Abstract—In this design project, we designed an on-chip CMOS feedback amplifier that can drive an oscilloscope input, where its input impedance is a $1\text{M}\Omega$ resistor in parallel with a 20pF capacitor. The amplifier was to buffer on-chip signals with a gain of $10\frac{V}{V}$ and a maximum current draw of $700\mu\text{A}$, meeting target specifications of being able to measure DC voltages to within 0.1% accuracy, as fast as possible a step response with an overshoot of less than 1%, as large a dynamic range as possible, and an integrated noise power of under $30\mu\text{V}$. The amplifier made use of the tsmc025.scs model library for 0.25um CMOS technology with a $+1.25\text{V}/-1.25\text{V}$ power supply and central ground. An ideal $10\mu\text{A}$ current reference was available to derive amplifier biasing and all devices were biased in strong inversion with an overdrive voltage of at least 200mV .

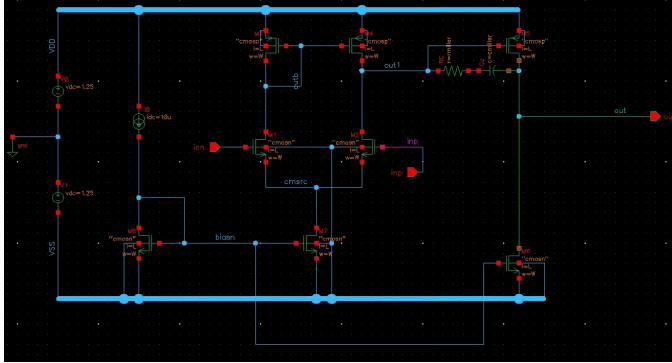


Fig. 1. 2-Stage Operational Transconductance Amplifier

I. INTRODUCTION

The design of this 2-stage Operational Transconductance Amplifier (OTA) began by understanding how to extract the DC operating point of each node from the Cadence schematic, as well as understanding how to adjust the sizing of each transistor in order to ensure that each one was in saturation and in strong inversion. From there, a small signal equivalent could be trivially derived from the circuit, and then simplified, allowing for a quick estimation of whether the model would meet the specifications required. After being derived manually, these checks were implemented in a spreadsheet, facilitating iterative design.

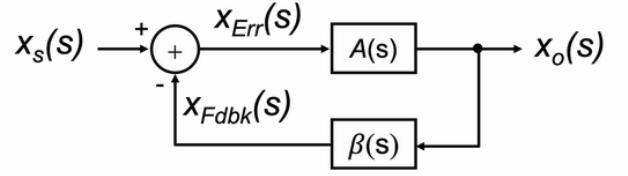


Fig. 2. Generalized Feedback System

II. SMALL SIGNAL EQUIVALENT

A. Derived Design Requirements

The closed loop gain of a feedback system (as seen in figure 1) can be determined

$$G = \frac{1}{\beta} \frac{A_{OL}}{1 + \beta A_{OL}} \quad (1)$$

where A_{OL} is the open loop gain of the system. For a closed loop gain of $10\frac{V}{V}$, the feedback factor (β) must be 0.1 in the ideal case where Open Loop DC Gain $A_{OL} \rightarrow \infty$. Solving for a 0.1% DC Accuracy, it was determined that the minimum A_{OL} was $9990\frac{V}{V}$.

Our other constraint was that the maximum current draw from the power supply had to be less than $700\mu\text{A}$. Accounting for a $10\mu\text{A}$ input bias current we were provided, the first and second stages of our OTA would have to split a maximum of $690\mu\text{A}$. As the unity gain frequency (to have a given phase margin) is limited by the location of the second pole, approximately

$$f_{p2} \approx \frac{g_{m2}}{2\pi C_{load}}, \quad (2)$$

devoting more current to the second stage generally results in a better loop gain as

$$g_{m2} = \frac{g_{m2}}{I_{ds}} * I_{ds} \approx \frac{2}{V_{ov}} * I_{ds} = 10I_{ds}. \quad (3)$$

While this is an approximation, this provides a framework for guiding design decisions in the correct direction. In addition, V_{ov} was targeted to be 0.2V , as this would maximize transconductance efficiency $\frac{g_{m2}}{I_{ds}}$ while keeping the transistors in saturation.

In addition, the gain of each stage was targeted to be equal, with an overall $A_{OL} = 10,000\frac{V}{V}$, each stage would have a

target gain of $100\frac{V}{V}$ to meet the DC accuracy requirement.

Finally, to have an acceptable transient response, a phase margin (PM) of 70° was attempted. With a feedback factor of 0.1, this resulted in an approximate ratio of the unity gain frequency and second pole of .36 from (4).

$$\frac{f_u}{f_{p2}} = \tan(90^\circ - PM) \quad (4)$$

B. Resulting Specifications

While a $300\mu A$ and $390\mu A$ division was targeted for the first and seconds stages respectively, the A_{OL} was too small to meet the required DC accuracy requirement without heavily increasing the minimum lengths and widths of the transistors. Instead, a $150\mu A$ and $540\mu A$ was used as the target currents, resulting in a better transient response and lower required output resistances of the small signal equivalent.

The approximated required transconductance of M2 and M5 can be found from (3), and the required output resistance to have the needed gain is

$$r_{ox} = \frac{g_{ox}}{g_{mx}}. \quad (5)$$

The second pole can then be found from (2) resulting in a unity gain frequency of

$$f_u = f_{p2} * \frac{f_u}{f_{p2}} \approx f_{p2} * 0.36 \quad (6)$$

and a first pole from

$$f_{p1} = \frac{1}{2\pi R_{o1} R_{o2} g_{m1} g_{m2}}. \quad (7)$$

The miller capacitance C_c can then be found

$$C_c = \frac{\beta^* g_{m1}}{2\pi f_u} \quad (8)$$

from the Gain-Bandwidth Product $\frac{f_u}{\beta}$.

Using a $R_C = 740\Omega$, the zero introduced by the miller right-hand zero compensation is

$$f_z = \frac{g_{m2}}{2\pi C_c (g_{m2} R_C - 1)}. \quad (9)$$

PM can thus be better estimated from

$$PM = 90^\circ + \arctan\left(\frac{f_u}{f_z}\right) - \arctan\left(\frac{f_u}{f_{p2}}\right) \quad (10)$$

for a $f_u \gtrsim 10 * f_{p1}$.

After simulating with the below values, the specifications were within the required ranges, allowing for a starting point for current division and miller capacitance.

TABLE I
SMALL SIGNAL ESTIMATES FOR (A) COMPONENT VALUES AND (B)
FREQUENCY RESPONSE

Frequency Response		Component Values	
fp1	11.3kHz	Cc	4.23pF
fp2	31MHz	Ro1	33.3kOhms
fz	77.9MHz	Ro2	25.6kOhms
fu	11.3MHz	gm1	3mS
Phase Margin	78.3 deg	gm2	3.9mS

II. TRANSISTOR SIZING

For the same overdrive voltage and sizing, a PMOS will not pull the same magnitude of drain current as an NMOS transistor. This is due to differences in the electron and hole mobility. To determine the ratio of sizing that would produce the same current magnitude for the same given V_{ov} , we ran a DC simulation of each transistor in diode-connected configuration with the same V_{ov} resulting in a ratio of

$$\frac{I_{ds,p}}{I_{ds,n}} = 3.4 = \left(\frac{W}{L}\right)_p / \left(\frac{W}{L}\right)_n \quad (11)$$

corresponding to the expected ratio of respective carrier mobilities. Setting $\frac{W}{L} = 1$ and increasing the number of fingers m to increase effective width results in a sizing as seen in (II). Due to imprecise current mirroring and rounding, the current division was not exactly the target. This could be improved by using a more complex current mirror and refining the $\frac{W}{L}$ ratio; however, for the purposes of this project increasing the effective width of the mirror accounted for inaccuracies. If any transistors were found to be in the linear region, decreasing their effective width while having the same current running through it increases the overdrive voltage, pushing it into the saturation region.

After measuring the DC operating point of the amplifier with each transistor in saturation, a small signal equivalent model in figure 3 could be made to estimate whether the design would theoretically meet specifications.

TABLE II
SIZING CALCULATIONS

Column1	Type	uCox [A/V^2]	Vov	Id (uV)	m*(W/L) ideal	m*(W/L) actual	W	L	W/L	m	m (new)
M1	nmos	2.49E-04	2.00E-01	75.00	15.060241	15	2.10E-06	2.10E-06	1.00	15	15
M2	nmos	2.49E-04	2.00E-01	75.00	15.060241	15	2.10E-06	2.10E-06	1.00	15	15
M3	pmos	7.32E-05	2.00E-01	75.00	51.204819	51	2.10E-06	2.10E-06	1.00	51	51
M4	pmos	7.32E-05	2.00E-01	75.00	51.204819	51	2.10E-06	2.10E-06	1.00	51	51
M5	pmos	7.32E-05	2.00E-01	550.00	375.50201	376	2.10E-06	2.10E-06	1.00	376	365
M6	nmos	2.49E-04	2.00E-01	550.00	110.44177	110	2.10E-06	2.10E-06	1.00	110	106
M7	nmos	2.49E-04	2.00E-01	150.00	30.120482	30	2.10E-06	2.10E-06	1.00	30	30
M8	nmos	2.49E-04	2.00E-01	10.00	2.0080321	2	2.10E-06	2.10E-06	1.00	2	2

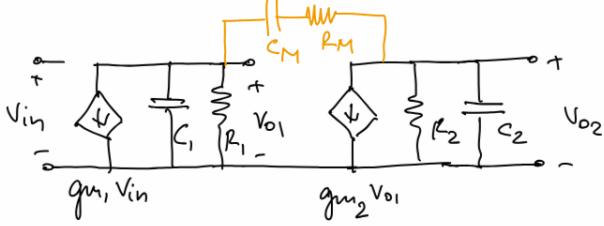


Fig. 3. Miller Compensated 2-Stage OTA Equivalent Model

The equivalent component values can be calculated through the following relationships:

$$g_{m2} = g_{m,M5} \quad g_{m1} = g_{m,M1} \quad (12)$$

$$R_1 = \frac{1}{g_{ds,M2} + g_{ds,M4}} \quad (13)$$

$$C_1 = C_{dB,M2} + C_{dB,M4} + C_{dg,M2} + C_{dg,M4} + C_{gs,M5} \quad (14)$$

$$R_2 = \frac{1}{g_{ds,M5} + g_{ds,M6} + g_{Load}} \quad (15)$$

$$C_2 = C_{Load} \quad (16)$$

resulting in the component values below.

TABLE III
SMALL SIGNAL EQUIVALENT COMPONENT VALUES

Small Signal Equivalent Estimates	
Ro1	217391.3043
Co1	8.093E-12
Rc	4000
Cc	4.56E-12
gm1	0.0006324
gm2	0.0035
Co2	2.00E-11
Ro2	33333.33222
beta	0.1
G1	137.4782609
G2	116.6666628

Using these component values, the following expected poles, unity gain frequency, open-loop gain, and zero can be calculated, where

$$f_u = \beta A_{OL} f_{p1}. \quad (17)$$

TABLE IV
SMALL SIGNAL EQUIVALENT FREQUENCY RESPONSE ESTIMATES

Frequency Response	
fp1 (Hz)	1.35E+03
fp2 (Hz)	2.79E+07
fu (Hz)	2.16E+06
fzero (Hz)	9.41E+06
Adc (V/V)	1.60E+04

The PM can be calculated as in (10), and DC accuracy

$$\varepsilon_{rel} = \frac{G_{actual} - G_{expected}}{G_{expected}} * 100\% \quad (18)$$

and total integrated noise power

$$Noise = \sqrt{\frac{8\pi kT}{3g_{m1}}} BW_{closed\ loop} \quad (19)$$

where k is the Boltzmann constant, T is the absolute temperature, and $BW_{closed\ loop}$ is the closed loop bandwidth of the amplifier, measured by the unity gain frequency of the loop gain, resulting in the estimates in table V.

TABLE V
SMALL SIGNAL EQUIVALENT SPECIFICATION CHECKS

Specification Checks	
Phase Margin	98.5 deg
DC Accuracy	0.06%
Total DC Current	689.3uA
Noise Estimate Calculation	10.9uV

III. SIMULATIONS

A. DC Open Loop Simulation

Measuring the open-loop response of the OTA as in figure 4 resulted in an open loop response as in figure 5.

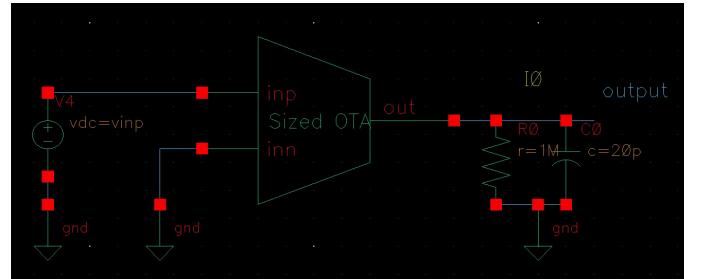


Fig. 4. Open Loop Response Testbench

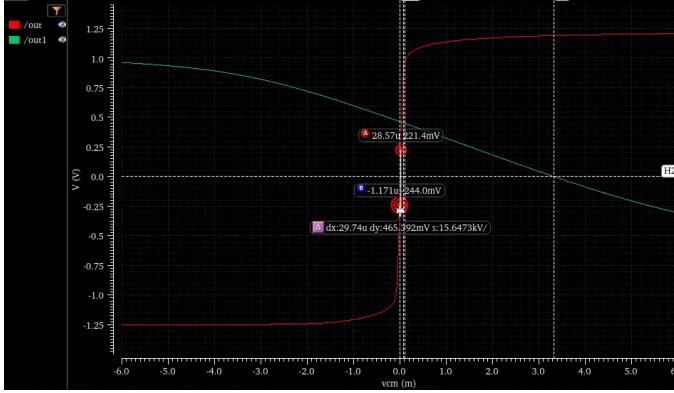


Fig. 5. DC Open Loop Response: First Stage Gain (green)
Overall OTA Gain (red)

From the above figure, the overall OTA gain G was measured to be $15647 \frac{V}{V}$ and the first stage gain was approximately $-132.4 \frac{V}{V}$. As a result, the second stage gain was determined to be $-118.2 \frac{V}{V}$. Relative to the estimated gains in table III, there is an error of 3.7% and 1.05%, respectively.

B. DC Closed Loop Simulation

To measure the dynamic range and DC transfer characteristics of the OTA, the circuit was tested in the configuration below.

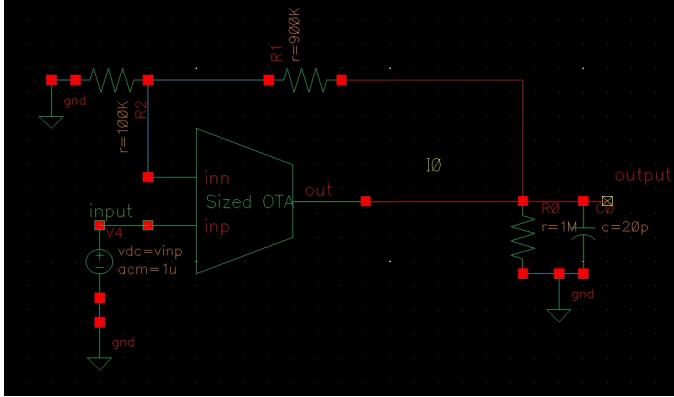


Fig. 6. Closed Loop Response Testbench

This resulted in the transfer characteristic below, marking the input and output referred offsets, as well as the dynamic range at 0.1% relative DC error measured as

$$\varepsilon_{rel} = 100\% * \frac{V_{out} - V_{out,o} - 10V_{in}}{10V_{in}} \quad (20)$$

where $V_{out,o}$ is the DC output offset ($144.3\mu\text{V}$), marking the input range from -102.607mV to 97.5621mV , and the output range to -1.025V to 974.5mV .

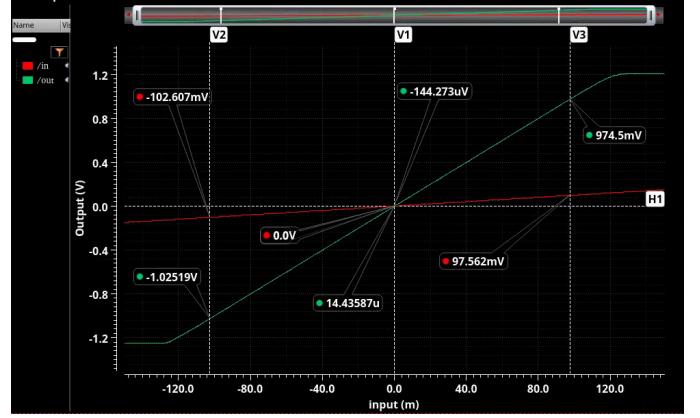


Fig. 6. DC Closed Loop Transfer Characteristic

Plotting the relative error of V_{in} vs V_{out} allowed for measurements of DC accuracy at $\pm 1\text{mV}$, which was symmetric at 0.0595% relative error, and for measurements of the dynamic range where DC Accuracy is within 0.1%.

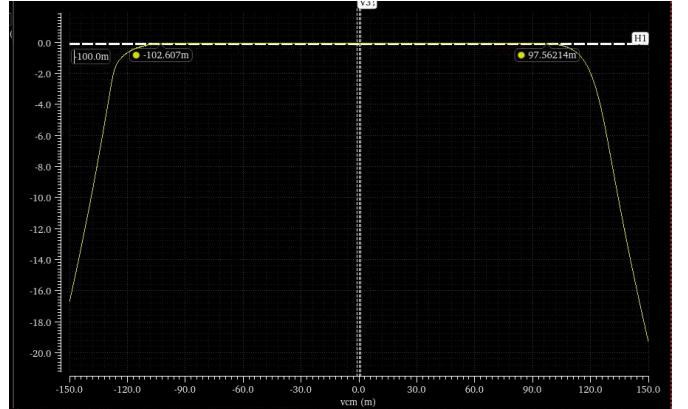


Fig. 7. DC Accuracy in Closed Loop (%) vs. V_{in}

C. AC Loop Gain

In order to measure the loop gain of the system, the system must be in AC Open Loop but still have DC feedback, so that the operating point can be calculated by Cadence and the AC analysis can occur around those linearized values.

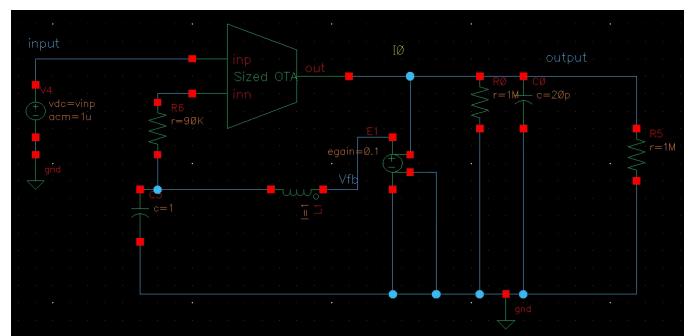


Fig. 8. Loop Gain Response Testbench

Plotting the frequency response of $V_{out}/V_{feedback}$ allows for a calculation of the Loop Gain Bode Plot plot in Figure 15 if the L and C values are large (1H and 1F), where the loop gain can be measured after ~ 10 Hz. After this value, the low frequency Loop Gain is 63.6dB (close to our estimate of 64.1dB), with a unity gain frequency of 1.93MHz and a Phase Margin of 72.52° .

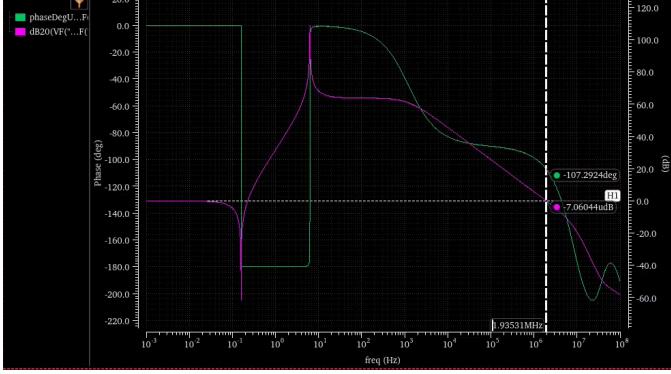


Fig. 9. AC Loop Gain Response

D. AC Closed Loop Response

We then measured the Closed Loop Frequency Response, confirming DC accuracy with a closed loop gain of 19.9947dB and closed loop 3dB bandwidth of 3.49MHz, which is on the same order of magnitude as our unity gain frequency and small signal estimate. This results in an estimated integrated noise power of $11.4\mu\text{V}$ by (19), meeting specifications.

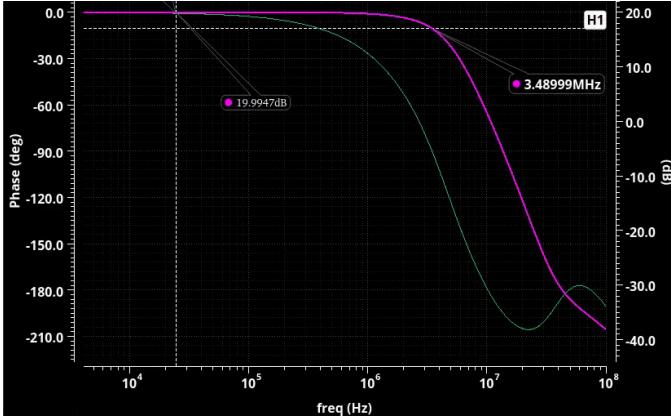


Fig. 10. AC Closed Loop Response

E. Transient Analysis

With the initial miller compensation values, a large overshoot was observed when performing a +1mV step transient analysis. After performing a parametric analysis on the miller resistor, the value was increased to $4\text{k}\Omega$, which brought the LHP zero closer to the unity gain frequency, improving the phase margin. The same parametric sweep was used on the miller capacitor to find the optimal settling time to within 1% of the settling value, changing the capacitance from 4.12pF to 4.556pF .

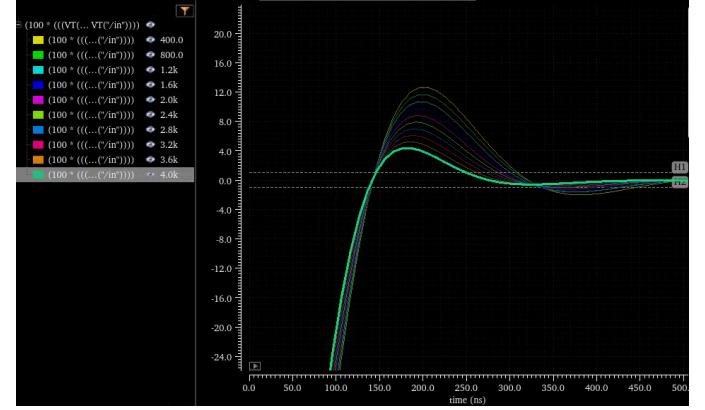


Fig. 11. Transient DC Accuracy R_c Parametric Sweep

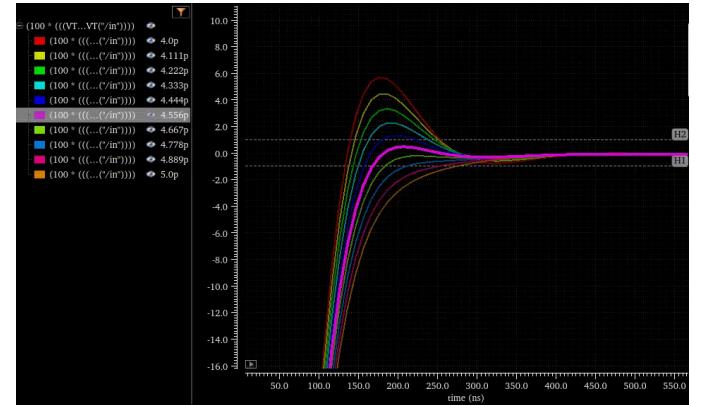


Fig. 12. Transient DC Accuracy C_c Parametric Sweep

Afterwards, transient simulations of $\pm 1\text{mV}$, $\pm 100\text{mV}$, and the minimum and maximum V_{in} step sizes were measured below.

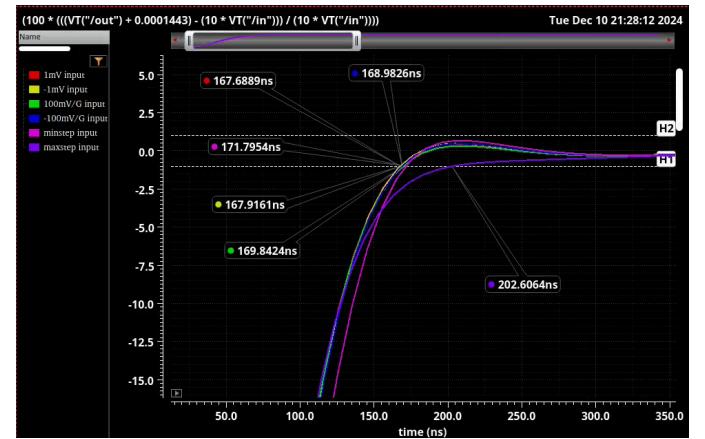


Fig. 13. DC Accuracy Transient Simulations

III. PVT SIMULATIONS

We then analyzed our amplifier across PVT variations, varying voltage across 0.9VDD, VDD, and 1.1VDD, temperature from 0°C, 27°C, and 80°C, and load from direct connection to the scope to a 10x probe. Figure 14 corresponds to the 10x probe load as described in “ISSCC Special Event:

Circuit Design and Testing Mistakes of Beginning Engineers [Conference Reports]" in the project specification. We ran simulations to find Output DC Offset, Input Referred DC Offset, Closed Loop Gain, Closed Loop Bandwidth, and Settling Times to 1% Accuracy for +10mV across all PVT variations as was previously measured.

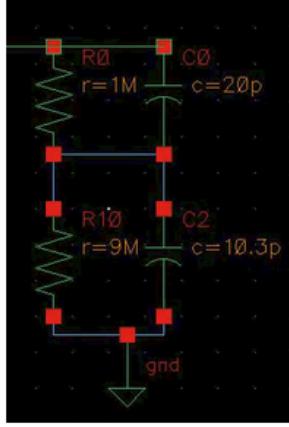


Fig. 14. 10x Probe Load

A. DC Closed Loop Analysis

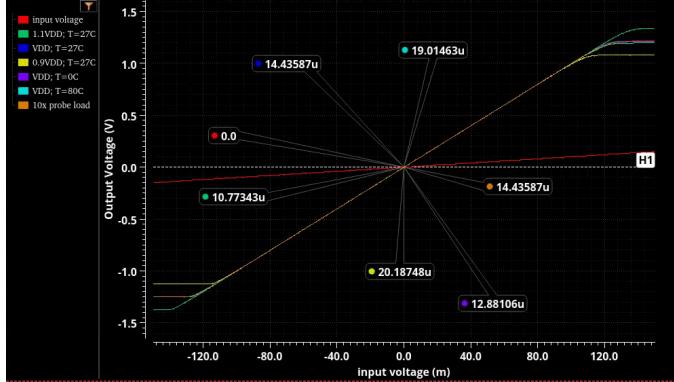


Fig. 15. Input Referred DC Offset Across PVT

A power variation of 1.1VDD seems to correct the offset better with the lowest offset of $10.77\mu V$ while 0.9VDD worsened the offset to $20.187\mu V$. Changing load had no effect on the offset. $0^{\circ}C$ also slightly improved the offset to $12.88\mu V$ while $80^{\circ}C$ worsened the offset to $19.01\mu V$. The output offset magnitude is approximately 10 times the input referred offset for all the PVT variations.

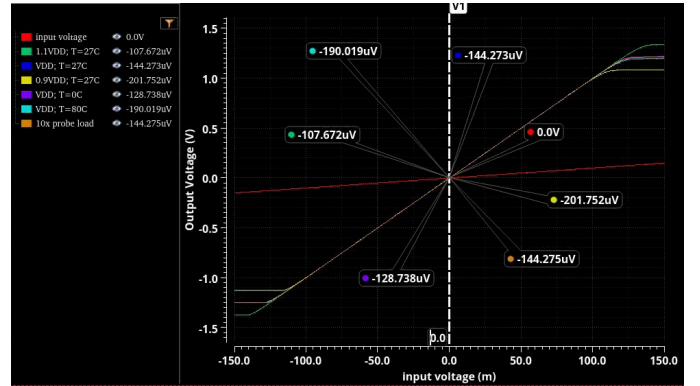


Fig. 16. Output DC Offset Across PVT

B. AC Closed Loop Analysis

Measuring the closed loop bandwidth at -3dB, it appears that voltage variations do not have a large impact on the closed loop bandwidth, but the temperature and load variations do. Using a 10x probe and decreasing temperature increases the bandwidth, and increasing temperature decreases bandwidth. All variations had an effect on the closed loop gain at the frequencies measured.

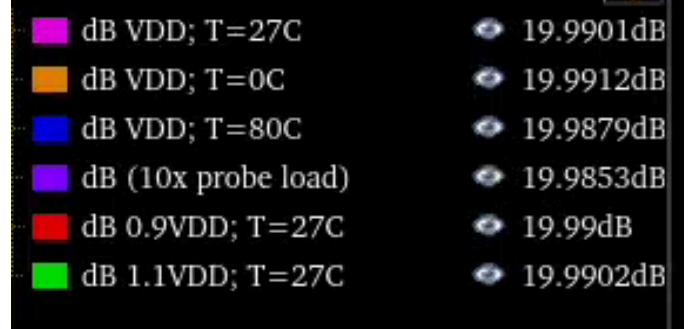


Fig. 17. Closed Loop Low Frequency Gain Across PVT, Corresponding Label and AC Trace Color

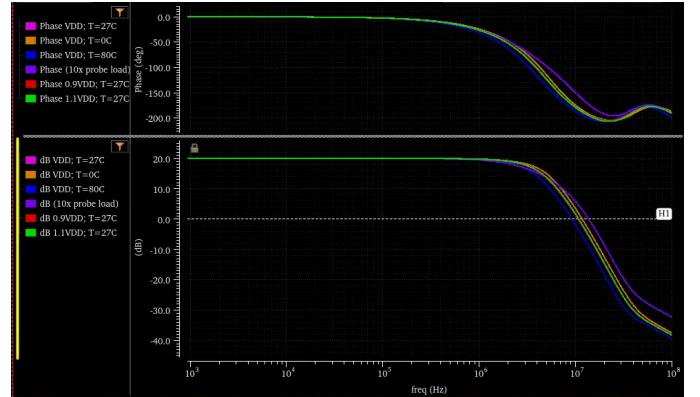


Fig. 18. Closed Loop AC Phase (top) and Closed Loop AC Magnitude (bottom) Across PVT

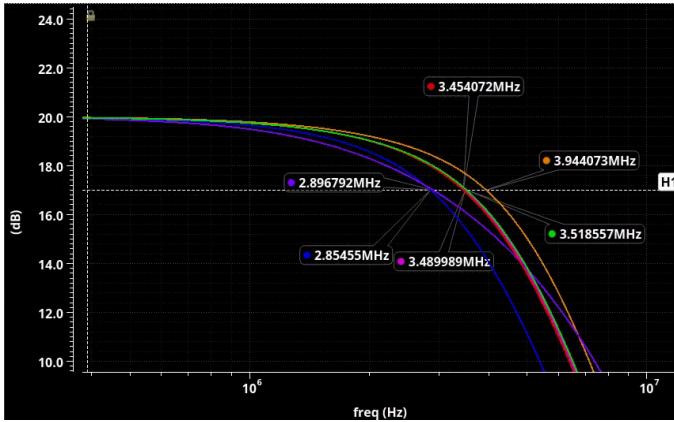


Fig. 19. -3dB Cutoff Frequencies Across PVT

C. Transient Analysis

DC Accuracy was graphed using the measured output offset previously measured; however, this has a negligible effect on the settling time. The gain of all simulations reaches approximately 99.8mV. Variations in VDD had little effect on the settling time. Increasing temperature to 80°C increases settling time by almost 40 ns compared to room temperature and decreasing temperature to 0°C decreases settling time by almost 20ns. The 10x probe load had the largest increase in settling time of 296.34ns with no overshoot.

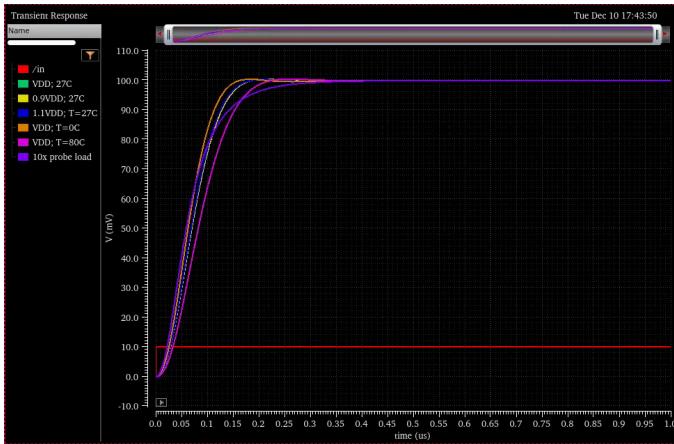


Fig. 20. +10mV Input Step Transient Response Across PVT

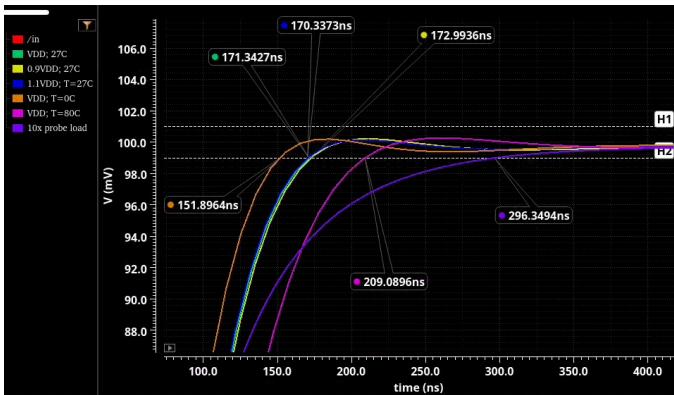


Fig. 21. Settling Times to 1% Accuracy Across PVT

V. CONCLUSION

This oscilloscope driver amplifier successfully made use of a small signal equivalent model, splitting the current draw into two stages, and the Miller compensation technique to achieve an accurate DC, AC, and transient response that met design project specifications. We were then able to observe differences in the above responses when conducting a PVT analysis for our designed amplifier. Future work for this design amplifier may include optimization to minimize differences in the driver's response for the various conditions in the PVT analysis by further optimizing the Miller compensation to a higher degree of accuracy or utilizing different resistor sizes for the feedback network. Exploring other current distributions or opting for a different phase margin goal may also be factors that should be taken into consideration to achieve this future goal.

REFERENCES

- [1] “ISSCC special event: Circuit design and testing mistakes of beginning engineers [conference reports].” IEEE Solid-State Circuits Magazine, vol. 13, no. 2, 2021, pp. 111–118, <https://doi.org/10.1109/mssc.2021.3072270>.
- [2] Roberts, Gordon W. 9.1 the Single-Loop Negative Feedback Structure, www.ece.mcgill.ca/~grober4/SPICE/SPICE_Decks/1st_Edition_LTSPICE/chapter9/Chapter 9 Feedback web version.html. Accessed 1 Jan. 2025.

VII. APPENDIX

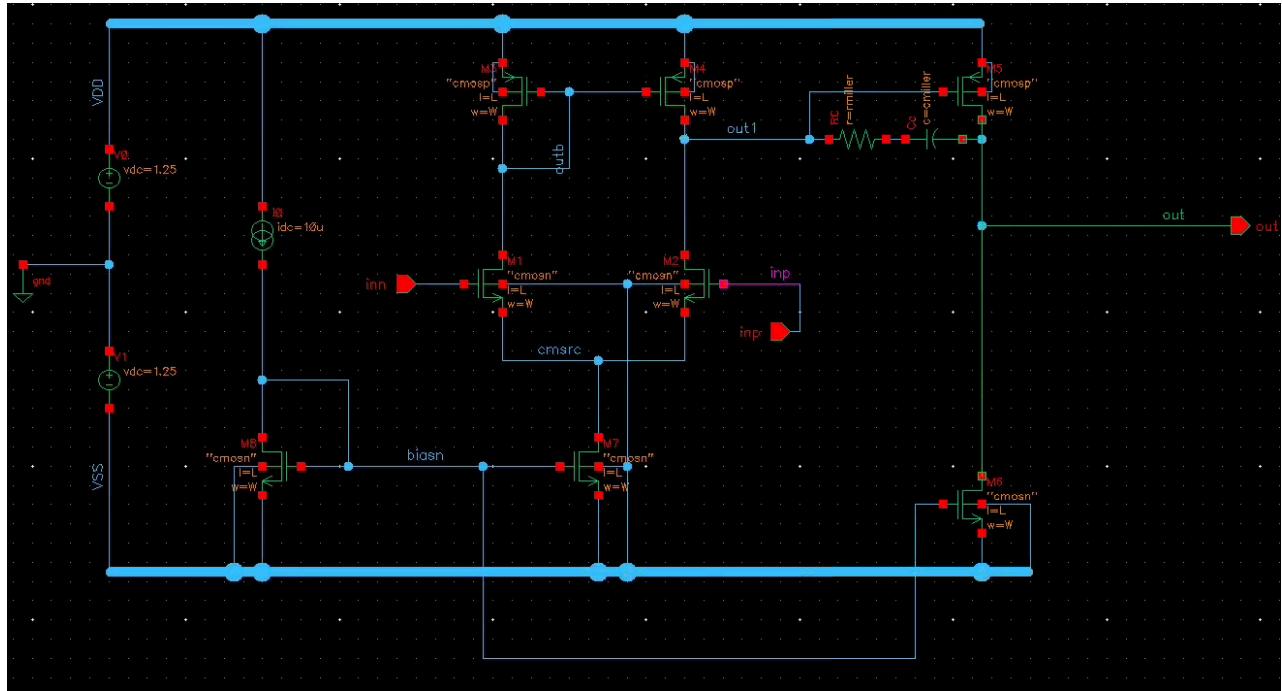


Fig. 1. [Enlarged] 2-Stage Operational Transconductance Amplifier

TABLE VI
SPECIFICATIONS FOR OSCILLOSCOPE DRIVER

Sign Up Info	Max Supply Current IDDmax [uA]	10	uA
	Gain G [V/V]	700	V/V
DC	Current Consumption	689.3	uA
AC	Loop Gain	63.60	dB
	Phase Margin	72.58	deg
	Unity Gain Frequency Loop Gain	1.934	MHz
	Closed-Loop Gain	19.9947	dB
	Closed-Loop 3-dB Bandwidth	3.49	MHz
DC	DC Output Offset Closed Loop	-144.3	uV
	Input-Referred DC Offset	14.43	uV
	Input Operation Range Vin,min	-102.607	mV
	Input Operation Range Vin,max	97.562	mV
	Output @ Vin,min	-1025	mV
	Output @ Vin,max	974.5	mV
	DC Accuracy @ +1mV Input	0.0595	%
	DC Accuracy @ -1mV Input	0.06	%
	DC Accuracy @ Vin, max	0.1	%
	DC Accuracy @ Vin, min	0.1	%
Transient	Settling Time to 1% Accuracy @ 1mV Step	167.6	ns
	Overshoot @ 1mV Step	0.47	%
	Settling Time to 1% Accuracy @ -1mV Step	167.92	ns
	Overshoot @ -1mV Step	0.487	%
	Settling Time to 1% Accuracy @ 100mV/G Step	169.84	ns
	Overshoot @ 100mV/G Step	0.335	%
	Settling Time to 1% Accuracy @ -100mV/G Step	169	ns
	Overshoot @ -100 mV/G Step	0.483	%
	Settling Time to 1% Accuracy @ Max Step	202.6	ns
	Overshoot @ Max Step	0	%
	Settling Time to 1% Accuracy @ Min Step	171.8	ns
	Overshoot @ Min Step	0.685	%
Noise	Estimated Integrated Noise Power [uV]	11.42771	uVRMS

TABLE VII
DC OPERATING POINT OF OPERATIONAL TRANSCONDUCTANCE AMPLIFIER

Parameter	M1b	M2 b	M3 b	M4b	M5 b	M6 b	M7b	M8 b
w	2.1u							
l	2.1u							
m	15	15	51	51	365	106	30	2
as	9.0p							
ad	9.0p							
ps	12.7u							
pd	12.7u							
ids	74.5u	74.5u	-74.5u	-74.5u	-539.1u	539.4u	148.9u	10.0u
vgs	735.8m	735.8m	-785.9m	-785.9m	-785.9m	637.3m	637.3m	637.3m
vds	1.2	1.2	-785.9m	-785.9m	-1.5	1	514.2m	637.3m
vdsat	204.4m	204.4m	-248.7m	-248.7m	-248.7m	201.5m	200.1m	200.4m
region	saturation							
vbs	-514.2m	-514.2m	0	0	0	0	0	0
vth	523.2m	523.2m	-516.5m	-516.5m	-516.5m	412.5m	414.5m	414.0m
vov	212.6m	212.6m	-269.4m	-269.4m	-269.4m	224.8m	222.8m	223.3m
vgsteff	212.1m	212.1m	270.1m	270.1m	270.1m	223.4m	221.4m	221.9m
gm	632.4u	632.4u	481.4u	481.4u	3.5m	4.4m	1.2m	82.7u
gds	3.0u	3.0u	1.6u	1.6u	7.7u	22.3u	9.5u	521.7n
gmb	114.4u	114.4u	153.9u	153.9u	1.1m	979.8u	272.4u	18.3u
gmoverid	8.5	8.5	6.5	6.5	6.5	8.2	8.3	8.3
self_gain	210.2	210.2	307.4	307.4	451.4	199.4	130	158.5
cgs	306.5f	306.5f	981.8f	981.8f	7.0p	2.2p	621.1f	41.4f
cgsolv	15.0f	15.0f	60.5f	60.5f	433.1f	106.2f	30.0f	2.0f
cgb	18.3f	18.3f	108.5f	108.5f	778.0f	148.6f	41.9f	2.8f
cgbowl	30.9a	30.9a	102.7a	102.7a	734.8a	218.6a	61.9a	4.1a
cgd	13.9f	13.9f	61.0f	61.0f	433.5f	97.9f	28.5f	1.9f
cgdowl	15.0f	15.0f	60.5f	60.5f	433.1f	106.2f	30.0f	2.0f
cbd	198.8f	198.8f	820.2f	820.2f	5.1p	1.6p	512.7f	33.0f
cjd	198.7f	198.7f	819.9f	819.9f	5.1p	1.6p	511.9f	33.0f
cbs	280.4f	280.4f	226.3f	226.3f	1.6p	243.6f	69.4f	4.6f
cjs	255.9f	255.9f	0	0	0	0	0	0
csd	484.8a	484.8a	-353.9a	-353.9a	-287.3a	3.4f	360.0a	47.7a
cm	133.1f	133.1f	438.5f	438.5f	3.1p	941.0f	266.4f	17.8f
cmb	25.4f	25.4f	134.9f	134.9f	966.0f	227.7f	64.2f	4.3f
cmx	26.4f	26.4f	43.8f	43.8f	314.6f	213.3f	59.8f	4.0f
fug	297.1M	297.1M	66.6M	66.6M	67.2M	289.4M	283.7M	285.7M

```

// Generated for: spectre
// Generated on: Dec 10 18:34:02 2024
// Design library name: AnalogCircs
// Design cell name: OpenloppDC
// Design view name: schematic
simulator lang=spectre
global 0
parameters rmiller=4k cmiller=4.556p W=2.118u L=2.118u Ldifd=4.236u \
    Ldifs=4.236u muleight=2 mulseven=30 mulsix=106 mulfive=365 mulfour=51 \
    multhree=51 multwo=15 mulone=15
include "/homes/user/stud/fall22/aag2204/Documents/tsmc025.scs"

// Library name: AnalogCircs
// Cell name: OpenloppDC
// View name: schematic
M2 (out1 inp cmsrc VSS) cmosn w=W l=L as=W*Ldifs ad=W*Ldifd ps=2*(W+Ldifs) \
    pd=2*(W+Ldifd) ld=Ldifd ls=Ldifs m=multwo
M1 (outb inn cmsrc VSS) cmosn w=W l=L as=W*Ldifs ad=W*Ldifd ps=2*(W+Ldifs) \
    pd=2*(W+Ldifd) ld=Ldifd ls=Ldifs m=mulone
M8 (biasn biasn VSS VSS) cmosn w=W l=L as=W*Ldifs ad=W*Ldifd ps=2*(W+Ldifs) \
    pd=2*(W+Ldifd) ld=Ldifd ls=Ldifs m=muleight
M7 (cmsrc biasn VSS VSS) cmosn w=W l=L as=W*Ldifs ad=W*Ldifd ps=2*(W+Ldifs) \
    pd=2*(W+Ldifd) ld=Ldifd ls=Ldifs m=mulseven
M6 (out biasn VSS VSS) cmosn w=W l=L as=W*Ldifs ad=W*Ldifd ps=2*(W+Ldifs) \
    pd=2*(W+Ldifd) ld=Ldifd ls=Ldifs m=mulsix
V0 (VDD 0) vsource dc=1.25 type=dc
V1 (0 VSS) vsource dc=1.25 type=dc
I0 (VDD biasn) isource dc=10u type=dc
M3 (outb outb VDD VDD) cmosp w=W l=L as=W*Ldifs ad=W*Ldifd ps=2*(W+Ldifs) \
    pd=2*(W+Ldifd) ld=Ldifd ls=Ldifs m=multhree
M4 (out1 outb VDD VDD) cmosp w=W l=L as=W*Ldifs ad=W*Ldifd ps=2*(W+Ldifs) \
    pd=2*(W+Ldifd) ld=Ldifd ls=Ldifs m=mulfour
M5 (out out1 VDD VDD) cmosp w=W l=L as=W*Ldifs ad=W*Ldifd ps=2*(W+Ldifs) \
    pd=2*(W+Ldifd) ld=Ldifd ls=Ldifs m=mulfive
RC (out1 net2) resistor r=rmiller
Cc (net2 out) capacitor c=cmiller
simulatorOptions options psfversion="1.4.0" reltol=1e-3 vabstol=1e-6 \
    iabstol=1e-12 temp=27.0 tnom=27 scalem=1.0 scale=1.0 gmin=1e-12 \
    rforce=1 maxnotes=5 maxwarns=5 digits=5 cols=80 pivrel=1e-3 \
    sensfile="../psf/sens.output" checklimitdest=psf
modelParameter info what=models where=rawfile
element info what=inst where=rawfile
outputParameter info what=output where=rawfile
designParamVals info what=parameters where=rawfile
primitives info what=primitives where=rawfile
subckts info what=subckts where=rawfile
saveOptions options save=allpub

```

Fig. 22. Spice Netlist