**Freescale Semiconductor**
Application Note

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# Digital Peak Current Mode Control of Buck Converter Using MC56F8257 DSC

**by: Raghavan Sampath**

## 1 Introduction

As the simplest form of DC-DC converter, the buck converter steps down the input voltage without isolation for power levels from less than 1 W to over 100 MW. Buck converter finds its applications ranging from mother boards where voltage needs to be stepped down to 2 V or less to electroplating or polishing with operating voltages in the order of 100 V or more. Control of buck converters is essential to have good voltage regulation and transient responses over a wide load current range. Voltage mode control and current mode control are the major control strategies for buck converter topology. Current mode control has good dynamic performance and inherent properties like short circuit protection. These advantages make current mode control more suitable for mission critical applications.

Current mode control can be classified as average current mode control and peak current mode control. This application note concentrates on the implementation of peak current mode control using MC56F8257 digital signal controller (DSC). Peak current mode control gives a stable output and it is independent of any fluctuations at the input side of the system

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(Feed forward path). Further, the peak current mode control provides the advantages such as cycle-by-cycle current limiting, inherent short circuit protection, good transient response, and less complicated feedback compensation technique. The MC56F8257 DSC from Freescale is a cost-effective low-power controller which meets the requirements of digital peak current mode control. This application note describes the implementation of digital peak current mode control for buck converters using MC56F8257 DSC and provides a reference for customers to implement high-performance DC-DC converters.

This application note includes buck converter control theory, system design concepts, hardware design concepts, and the steps involved in software implementation.

## 2 MC56F8257 DSC advantages and features

The MC56F8257 is a member of the 56800E core-based family of DSCs. It combines the processing power of a DSP and the functionality of a microcontroller with a flexible set of peripherals on a single chip to create a cost-effective solution.

The 56800E core is based on a dual Harvard-style architecture consisting of three execution units operating in parallel, allowing as many as six operations per instruction cycle. The MCU-style programming model and optimized instruction set allow straightforward generation of efficient, compact DSP and control code. The instruction set is also highly efficient for C compilers to enable rapid development of optimized control applications.

The MC56F825x/MC56F824x includes many peripherals that are especially useful for industrial control, motion control, home appliances, general-purpose inverters, smart sensors, fire and security systems, switched-mode power supply, power management, and medical monitoring applications.

The MC56F8257 provides the following peripherals:

- One Enhanced Flexible Pulse Width Modulator (eFlexPWM) with up to 9 output channels, including 6 channels with high (520 ps) resolution, NanoEdge placement and 16-bit resolution for center, edge-aligned, and asymmetrical PWMs
- Two 8-channel, 12-bit Analog-to-Digital Converters (ADCs) with dynamic x2 and x4 programmable gain amplifier, conversion time as short as 600 ns, and input current-injection protection.
- One 12-bit Digital-to-Analog Converter (12-bit DAC) with 12-bit resolution. The output can be routed to internal comparator, or off-chip.
- Two four-channel 16-bit Multipurpose Timer (TMR) modules with cascading capability per module: Up to 120 MHz operating clock
- Up to 54 general-purpose I/O (GPIO) pins; 5 V tolerant I/O; individual control for each pin to be in peripheral or GPIO mode.
- Three High-Speed Comparator modules (HSCMP) with integrated 5-bit DAC references for comparing two analog input voltages. The comparator is designed to operate across the full range of the supply voltage (rail-to-rail operation).

- Intermodule crossbar connection with capability for generic intermodule connections between on-chip control peripherals including ADCs, DAC, comparators, timers, PWM module, and GPIO pins
- Two System Management Bus (SMBus) compatible inter-integrated circuit (I2C) ports; the module supports 10-bit address extension and designed to operate up to 100 kbit/s.
- Two high-speed Queued Serial Communication Interface (QSCI) modules with 13-bit integer and 3-bit fractional baud rate selection; supports full-duplex operation and LIN slave functionality
- Queued Serial Peripheral Interface (QSPI) module supporting full-duplex operation, programmable transmit and receive shift order, programmable length transactions from 2 to 16 bits and 14 master mode frequencies.
- Freescale's Scalable Controller Area Network (MSCAN) module implementing CAN 2.0 A/B protocol
- Computer Operating Properly (COP) Watchdog module to help software recover from runaway code
- Integrated Power-on-Reset (POR) and Low-Voltage Interrupt (LVI) and brown-out reset module
- Cost-effective memory configuration; 64 KB (32K x 16) flash memory; 8 KB (4K x 16) unified data/program RAM
- On-chip relaxation oscillator: 8 MHz (400 kHz at standby mode)
- JTAG/Enhanced On-Chip Emulation (EOnCE) for real-time debugging

The implementation of digital peak current mode control makes use of following peripherals of MC56F8257 DSC to achieve optimum performance:

- Analog-to-Digital Converter
- High-Speed Comparator module
- Digital-to-Analog Converter
- Pulse Width Modulation module
- GPIO

The PWM module offers the following features:

- 16-bit resolution for center, edge-aligned, and asymmetrical PWMs, fractional delay for enhanced resolution of the PWM period and duty cycle
- PWM outputs that can operate as complementary pairs or as independent channels
- Ability to accept signed numbers for PWM generation
- Independent control of both rising and falling edges of each PWM output
- Support for synchronization to external hardware or other PWMs
- Double-buffered PWM registers
    - Integral reload rate 1–16
    - Half-cycle reload capability
- Multiple output trigger events can be generated per PWM cycle via hardware.

- Support for double switching PWM outputs
- Fault inputs can be assigned to control multiple PWM outputs.
- Programmable filters for fault inputs
- Independently programmable PWM output polarity
- Independent top and bottom hardware deadtime insertion
- Each complementary pair can operate with its own PWM frequency and deadtime values.
- Individual software control for each PWM output
- All outputs can be programmed to change status simultaneously via a FORCE_OUT event.
- PWMX pin can optionally output a third PWM signal from each submodule.
- Channels not used for PWM generation can be used for buffered output compare functions.
- Channels not used for PWM generation can be used for input capture functions with enhanced dual-edge capture capability (see the respective chapter of reference manual to see which sub modules include this function).
- Option to supply the source for each complementary PWM signal pair from:
    - Crossbar module outputs
    - External ADC input, taking into account values set in ADC high- and low-limit registers

The analog-to-digital converter (ADC) consists of two separate analog-to-digital converters; each with eight analog inputs and its own sample and hold circuit. The features of the ADC module are as follows.

- Input voltage values that may range from $V_{SSA}$ to $V_{DDA}$
- 12-bit resolution
- Maximum ADC clock frequency of 10 MHz with 100 ns period
- Sampling rate up to 3.33 million samples per second
- Can be synchronized to the PWM
- Sequentially scans and stores up to 16 measurements
- Scans and stores up to eight measurements, each on two ADCs operating simultaneously and in parallel
- Scans and stores up to eight measurements each on two ADCs operating asynchronously to each other in parallel
- Gains the input signal by x1, x2, or x4
- Signed or unsigned result
- Single-ended or differential inputs

The digital peak current mode control system uses two ADC modules set with simultaneous sample mode for reducing the conversion time of the required signals. The trigger of the ADC is synchronized with the PWM for aligning converter analog signals within the required time.

The HSCMP module provides a circuit for comparing two analog signals and has the following features:

- Operates over the entire supply range
- Inputs may range from rail-to-rail.

- Less than 40 mV of input offset
- Less than 15 mV of hysteresis
- Selectable interrupt on rising-edge, falling-edge, or either rising or falling edges of the comparator output
- Selectable inversion of comparator output
- Comparator output may be:
    - Sampled
    - Windowed (ideal for certain PWM zero-crossing-detection applications)
    - Digitally filtered:
        - Filter can be bypassed.
        - May be clocked through the external SAMPLE signal or a scaled peripheral clock
- External hysteresis can be used while the output filter is used for internal functions.
- The plus and minus inputs of the comparator are both driven from 4-to-1 multiplexers, providing additional flexibility in assigning I/O as comparator inputs during PCB design.
- Two software-selectable performance levels:
    - High power, with shorter propagation delay. This mode can be used only when the VDDA rail is above the low voltage interrupt trip point.
    - Low power, with longer propagation delay

The digital peak current mode control uses HSCMP module to compare the actual inductor current and its reference of the combination of voltage regulator output and compensation ramp.

The 12-bit digital-to-analog converter (DAC) provides a reference to on-chip comparators or an output to a package pin. It can also be used as a waveform generator to generate square, triangle, and sawtooth waveforms and has the following features:

- 12-bit resolution
- Power down mode
- Output can be routed to the internal comparator or off the device.
- Choice of asynchronous or synchronous updates (sync input can be connected to internal crossbar)
- Automatic mode to generate square, triangle, and sawtooth output waveforms
- Automatic mode to allow programmable period, update rate, and range
- Support of two digital formats
- Glitch filter to suppress output glitch during data conversion

In digital peak current mode control, the 12-bit DAC is used to generate the compensation ramp. This ramp is useful in damping out sub-harmonic oscillations occurring in the inductor current. (sub-harmonic oscillations details are discussed in Sub Harmonic Oscillations in Peak Current Mode Control.)

# 3 Target control theory

## 3.1 Peak current mode control for buck converter

The current mode control features a dual loop control circuit—a voltage loop and a current loop within a voltage loop. Due to inherent properties like feedforward compensation and short circuit protection, peak current mode control mechanism is most widely-used in the industries. In Figure 1, the power switch SW is turned ON by a constant frequency clock. It is turned OFF when the inductor current reaches a threshold level defined by the outer voltage controller and a compensation ramp (to overcome the problem of sub harmonic oscillations. The details of sub-harmonic oscillations are discussed in Sub Harmonic Oscillations in Peak Current Mode Control).

Peak current mode control technique features some advantages such as simple cycle-by-cycle current limiting, inherent short circuit protection, and a simple feedback compensation network.

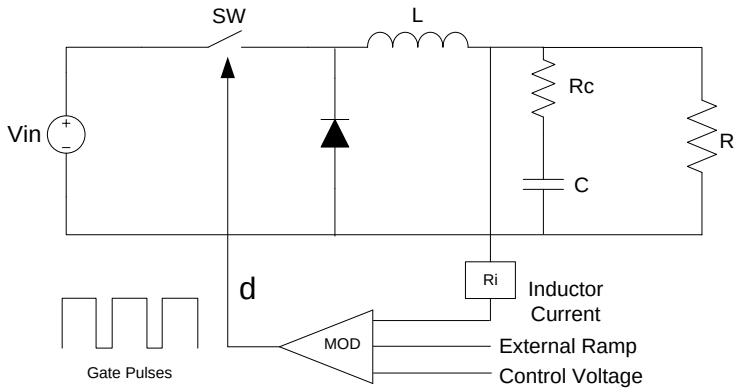


**Figure 1. Buck converter with peak current mode control**

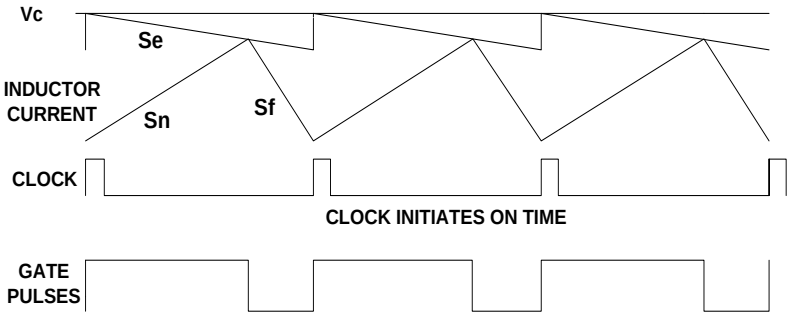


**Figure 2. Peak current mode control technique**

### 3.1.1 Sub-harmonic oscillations in peak current mode control

In a peak current mode controlled converter operating in continuous conduction mode, the inductor current shows a transition to sub-harmonic oscillations depending on the operating conditions. The oscillations are observed when compensation ramp is not added in the control loop. Any perturbations in the inductor current (due to fluctuations in control voltage) either persist or damp out depending upon

the converter operating condition. The perturbation in the inductor current persists for converter operating at duty cycle greater than 50%, as shown in Figure 3. For operation at duty cycle less than 50%, the perturbed inductor current settles down to the steady state value in subsequent cycles which is shown in Figure 4.

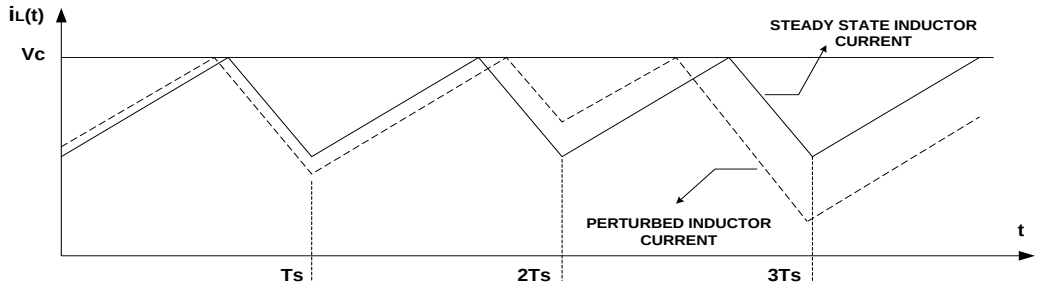


**Figure 3. Perturbed inductor current for D>50%**

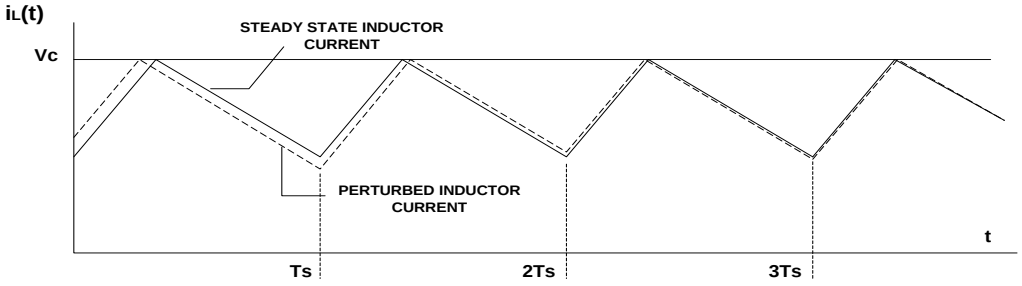


**Figure 4. Perturbed inductor current for D<50%**

## 3.2 Mathematical model of buck converter with peak current mode control

The buck converter model with peak current mode control is shown in Figure 5**.**

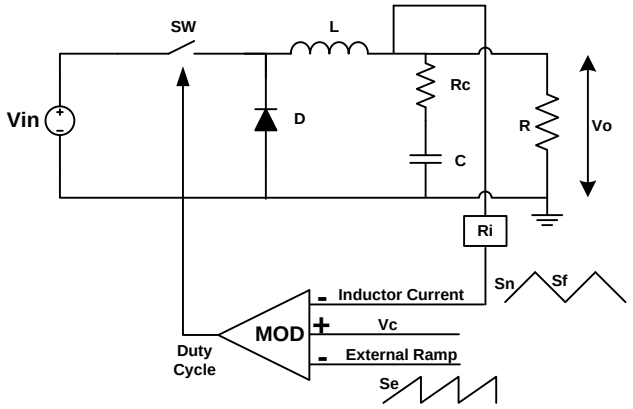


**Figure 5. Modeling methodology for peak current mode control of buck converter**

Where,

- $V_{in}$—input voltage in volts
- $V_O$—output voltage in volts

- L—inductance value in henry
- C—capacitance value in farad
- $R_C$—capacitor ESR (Equivalent Series Resistance) in ohm
- $T_S$—switching period in seconds
- R—load resistance in ohm
- $R_i$—inductor current sense transformer gain in ohm
- $S_e$—slope of compensation ramp
- $S_n$—rising slope of inductor current
- $S_f$ —falling slope of inductor current

The control-to-output transfer function for buck converter with peak current mode control is defined by the product of three terms: a DC gain term $H_{dc}$, a power stage small signal model $F_P(s)$, and a high-frequency transfer function $F_H(s)$ and is given by Equation 1.

$$\frac{V_0(s)}{V_c(s)} = H_{dc}F_p(s)F_h(s)$$

**Equation 1**

$$H_{dc} = \frac{R}{R_i} \quad \frac{1}{1 + \frac{RT_s(m_cD' - 0.5)}{L}}$$

**Equation 2**

$$F_p(s) = \frac{1 + sCR_c}{1 + \frac{s}{\omega_p}}$$

**Equation 3**

$$F_h(s) = \frac{1}{1 + \frac{s}{\omega_n Q_p} + \frac{s^2}{{\omega_n}^2}}$$

**Equation 4**

The pole $\omega_P$ (Equation 3) in the power stage model is formed from the output capacitance and load resistance which is given by Equation 5.

$$\omega_p = \frac{1}{CR} + \frac{T_s(m_cD' - 0.5)}{LC}$$

**Equation 5**

The high-frequency transfer function $F_H(s)$ (Equation 4) is common for all converter topologies with current mode control. In Equation 4, $\omega_n$ denotes the frequency (in rad/s) of oscillation of the double pole. The oscillation due to this double pole is at half the switching frequency (see Equation 6). The damping of this pole pair (denoted by $Q_P$) and the compensation factor (denoted by $m_c$) are given by Equation 7, and Equation 8.

$$\omega n = \frac{\pi}{Ts}$$

**Equation 6**

$$Q_p = \frac{1}{\pi(m_c D' - 0.5)}$$

**Equation 7**

$$m_c = 1 + \frac{S_e}{S_n}$$

**Equation 8**

With no external ramp, the poles at half the switching frequency are all always complex. At D = 0, $Q_P$ has a value of $2/\pi$. As the duty cycle is increased, poles start to move towards the imaginary axis and at D = 0.5, $Q_P$ becomes infinity with the poles becoming purely imaginary. When duty cycle is increased further, the poles move to the right-hand side of the s plane. A high peaking is observed when there is no compensation ramp added and the duty cycle is close to 50%. With the addition of external ramp, the complex poles get damped quickly and the system instability occurring at half the switching frequency is eliminated.

The external ramp must be selected so that the compensation ramp factor corresponds to the damping $Q_P$ = 1 which prevents peaking at half the switching frequency. Then the required external ramp for stable buck converter is given by Equation 9.

$$m_c = \frac{\frac{1}{\pi} + 0.5}{D'}$$

**Equation 9**

Using Equation 8 and Equation 9, the peak-to-peak value of the external compensation ramp can be calculated and is given by Equation 10.

$$V_{PP} = \frac{(D - 0.18)R_i T_S V_{in}}{L}$$

**Equation 10**

## 3.3 Designing the feedback compensator

A type II compensator is used for current mode feedback compensation. The complete buck converter system is obtained after integrating the feedback compensator with the peak current mode model. The poles and zeros of the compensator are placed according to the analysis of the control-to-output transfer function in order to set the desired crossover frequency and phase margin of the closed loop system.

The compensator has one zero and two poles. The compensator transfer function is denoted by $H_C(s)$ and is given by the following equation.

$$H_c(s) = \frac{\frac{\omega_{p1}}{s}\left(1 + \frac{s}{\omega_z}\right)}{1 + \frac{s}{\omega_{p2}}}$$

**Equation 11**

In Equation 11, the zero $\omega_Z$ is set to achieve a suitable phase margin. The frequency of this compensator zero is set to 1/5th of the desired crossover frequency $f_C$. The crossover frequency must be less than about 1/10th of the switching frequency.

$$\omega_Z = \frac{2\pi f_C}{5}$$

**Equation 12**

The compensator pole $\omega_{P2}$ is set to the frequency of the ESR zero of the power stage transfer function (Equation 3). This will cancel out the effect of the ESR zero.

$$\omega_{P2} = 1/(CR_C)$$

**Equation 13**

The compensator pole $\omega_{P1}$is placed at the origin. This pole is set to achieve the desired crossover frequency. $\omega_{P1}$ is the frequency at which the gain due to the pole at origin alone is unity. It can be directly calculated using Equation 14, Equation 15, and Equation 16.

$$\omega_{p1} = \frac{1.23\, f_c R_i R_1 R_2\, (L + 0.32RT_s)}{LR}$$

**Equation 14**

$$R_1 = \sqrt{1 - 4f_c^{\,2}T_s^{\,2} + 16f_c^{\,4}T_s^{\,4}}$$

**Equation 15**

$$R_2 = \sqrt{1 + \frac{39.48C^2 f_c^{\,2} L^2 R^2}{(L + 0.32RT_s)^2}}$$

**Equation 16**

## 3.4 Digital feedback compensator (2p2z compensator)

2p2z feedback compensator is the digital form of type II compensator. It takes sampled error signal (at a sampling time equal to switching period) and filters out any sudden changes in the error. Converting continuous time transfer function of type II compensator to discrete time leads to a 2p2z system. The digital compensator is described by a linear difference equation which can be implemented in the DSC to filter the measured error signal.

A simpler and effective approach to obtain the discrete time transfer function is by applying bilinear transformation or Tustin transformation to the analog transfer function. The compensator in discrete

time domain has two poles and two zeros and hence the name 2 pole 2 zero (or 2p2z) compensator. The discrete time transfer function for the feedback compensator is obtained by replacing the ‘s’ terms in Equation 11 with the approximation given below.

$$s = \left(\frac{2}{T_s}\right)\frac{z-1}{z+1}$$

**Equation 17**

Where $T_S$ is the sampling period and is equal to the switching period of the converter. Applying bilinear transformation to Equation 11 gives

$$(z) = \frac{\frac{\omega_{p1}}{\left(\frac{2}{T_s}\right)\frac{z-1}{z+1}}\left(1+\frac{\left(\frac{2}{T_s}\right)\frac{z-1}{z+1}}{\omega_z}\right)}{1+\frac{\left(\frac{2}{T_s}\right)\frac{z-1}{z+1}}{\omega_{p2}}}$$

**Equation 18**

$$H_C(z) = \frac{Y(z)}{X(z)} = \frac{B_2\, z^{-2} + B_1\, z^{-1} + B_0}{-A_2\, z^{-2} - A_1 z^{-1} + 1}$$

**Equation 19**

The discrete time transfer function in Equation 19 can be rearranged and a linear difference equation describing the compensator can be obtained given by Equation 20.

$$y[n] = B_2\, x[n-2] + B_1\, x[n-1] + B_0\, x[n] + A_2\, y[n-2] + A_1\, y[n-1]$$

**Equation 20**

A compensator of the form in Equation 20 can be easily implemented in a digital controller. For the feedback compensator described in Equation 20:

- x[n] is the error input to the controller in the present sampling period,
- y[n] is the controller output for present sampling period, and
- subscripts [n-1] and [n-2] denote the controller output and error for previous sampling and two sampling periods in the past respectively.

# 4 System design concept

## 4.1 System architecture

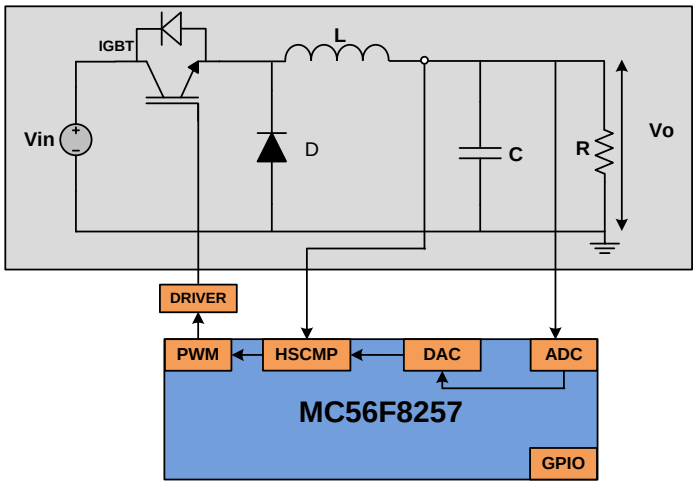


**Figure 6. System block diagram for peak current mode control of buck converter**

The peak current mode control sytem of buck converter incorporates the following stages.

- **Buck converter power stage**: This stage provides a high voltage/current route. The major components utilized for DC-DC conversion include controlled power switch (controlling is done using MC56F8257), power diode, inductor, capacitor, and load.
- **Sensing stage**: It is used to sense the necessary voltage and current information for feedback. Appropriate conditioning is done to match the ADC electrical characteristics of DSC.
- **Driver stage**: This stage modifies the PWM signal of the DSC to make it capable of driving the power switch of the power stage. This stage provides the isolation of the control stage from power stage.
- **Auxiliary power stage**: The desired stable power supply for control, driver, and sensing stages is fed from the auxiliary power supply.
- **MC56F8257-based control stage**: In this stage, the ADC module is used to convert the analog output voltage to accurate digital signals. The DAC module generates the desired ramp to provide slope compensation which helps in damping of sub-harmonic oscillations. The HSCMP module provides the power switch turn off instant to the PWM module. GPIOs are used to receive keypad interface signals and to provide indications through LEDs.

## 4.2 System control process

The peak current mode controlled buck converter yields excellent steady state and dynamic performance. The control scheme features dual loops: an inner inductor current loop and an outer output

voltage loop. Since the control loop is independent of input voltage changes, the performance is unaffected due to input voltage variations.

- The current loop of the buck converter is created by measuring the current through the inductor.
- The outer DC bus voltage feedback is used to control the DC output voltage to quickly follow the change in reference voltage. For better functioning of the outer loop, a type II feedback compensator (digital form of which is called 2 pole 2 zero or 2p2z compensator described in Digital feedback compensator (2p2z compensator) ) is used here.

Figure 7 shows the control scheme of peak current mode control which can be explained in the following steps.

1. The output voltage feedback $V_O$ from the power stage is fed to the ADC pin of the DSC. The digital equivalent $V_f$ of the analog feedback $V_O$ is obtained.
2. A digital reference voltage $V_{ref}$ is subtracted from $V_f$ and the resulting error value is fed to the two pole two zero (2p2z) feedback compensator.
3. The 2p2z output is multiplied by gain K. This gain scales the output of the compensator to a value that is suitable for use with the DAC of the comparator module. It also counteracts the effects of the various gains within the closed loop system.
4. A compensation ramp of peak-to-peak voltage described in Equation 10 is added to the scaled 2p2z output.
5. The resultant is fed to the DAC and an analog current reference $I_{ref}$ is obtained.
6. $I_{ref}$ is compared with the inductor current feedback $I_f$ obtained from a current transformer which has a gain $R_i$. The output of the comparator will cause the power switch to turn OFF when the inductor current reaches the level of the voltage on the DAC output.

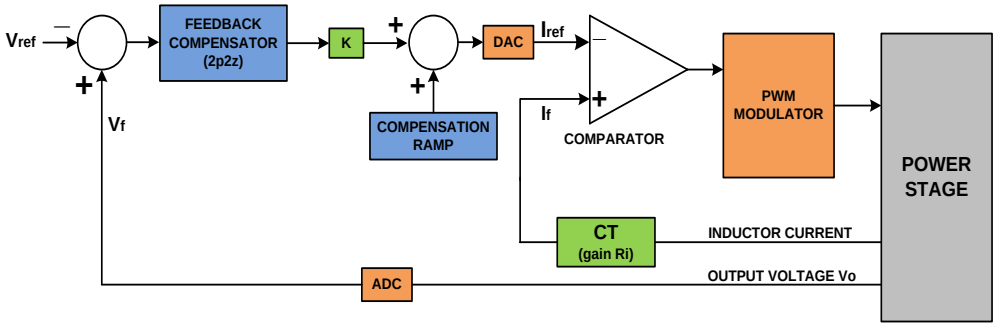


**Figure 7. Control scheme of peak current mode control**

# 5 Hardware design

## 5.1 System hardware structure

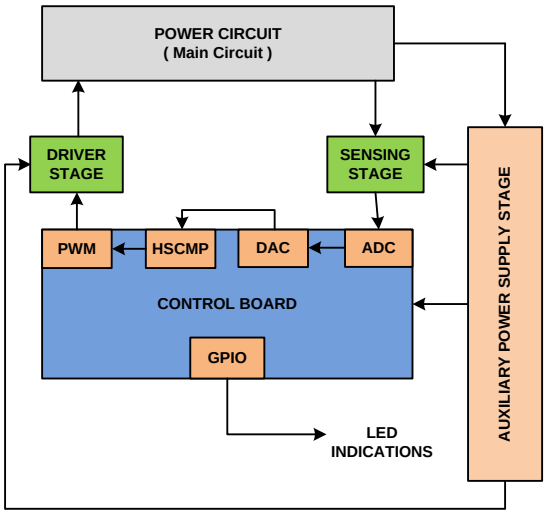


**Figure 8. System hardware structure block diagram**

The hardware structure of the peak current mode controlled buck converter is shown in Figure 8. The hardware system comprises of a MC56F8257-based control stage (control board), power stage (power board), sensing stage, driver stage, and auxiliary power supply stage. See System architecture for brief information on these stages.

## 5.2 MC56F8257 control board

The digital peak current mode control of buck converter described in this document uses the MC56F8257 DSC based system that includes the MC56F8257 DSC, JTAG interface, manual reset circuit, and pin interface.

## 5.3 Power board

### 5.3.1 Main power circuit

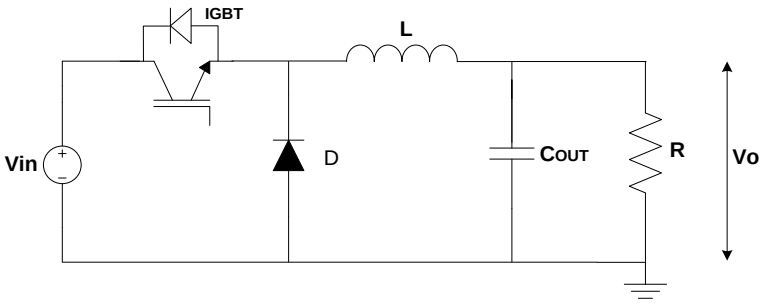


**Figure 9. Main power circuit**

The main power circuit incorporates the buck converter circuit with a power switch (IGBT), freewheeling diode D, inductor L, and capacitor C. R denotes the load resistor.

### 5.3.2 Designing the inductor

The required inductance for continuous conduction mode can be calculated using Equation 21.

$$L = \frac{(V_{in} - V_o)DT_s}{\Delta i\ I_o}$$

**Equation 21**

Vin = 100V
Vo = 10V
Io = 10A
deltaI = 0.01
Ts = 10E3

Where:

- $V_{in}$—input DC voltage to the buck converter in volts
- $V_o$—converter output voltage in volts
- $D = V_o/V_{in}$—converter duty cycle
- $T_S$—switching period in seconds
- $\Delta i$—inductor ripple current as a percentage of load current
- $I_O$—load current in amperes

The minimum inductance that ensures the operation in continuous conduction mode is given by Equation 22.

$$L_{MIN} = \frac{(1 - D)R}{2F_s}$$

**Equation 22**

Where:

- R—load resistance in ohms
- $F_S$—Switching frequency in hertz

Based on the selected magnetic core and inductance, it is possible to determine the number of turns in the windings. At the same time, the cross-sectional area of the winding can be calculated according to the maximum inductance current and suitable current density.

### 5.3.3 Selection of the capacitor

The parameters to be considered when selecting an output capacitor are DC voltage rating, ripple current rating, output ripple voltage requirements, and transient response requirements. An electrolytic capacitor is suitable for this application. The capacitance can be calculated using Equation 23.

$$C = \frac{1 - D}{8{F_s}^2 L V_o\ \Delta V}$$

**Equation 23**

Where:

- $V_O$—converter output voltage in volts

- ΔV—ripple voltage as percentage of output voltage
- $F_S$—switching frequency in hertz
- D—duty cycle
- L—inductor value in Henry as calculated in Equation 21.

### 5.3.4 Selection of the power switch

The maximum switch current is calculated using Equation 24.

$$I_{SWMAX} = \frac{\Delta i}{2} + I_{OMAX}$$

**Equation 24**

Where:

- $I_{SWMAX}$—maximum switch current in amperes
- Δi—inductor ripple current in amperes
- $I_{OMAX}$—maximum output current in amperes

The power switch selected must be capable of handling the current calculated in Equation 24. The reverse voltage handling capability and loss must be considered as well. Power switch with low on-state drop is selected to reduce the conduction loss and improve the whole converter efficiency.

### 5.3.5 Selection of the freewheeling diode

The freewheeling diode selection is based on reverse voltage, forward current, and switching speed. The forward current rating of the diode must be equal to the maximum output current. It is important to use a diode with a fast recovery characteristic.

### 5.3.6 Sensing circuit

The sensing circuits are used to convert the high-voltage and current signals into low-voltage signals. Another function of the sensing circuits is to condition these sensed signals to match the requirements of the ADC input port. High voltages are sensed using potential dividers and high currents are sensed using Hall Effect sensors. A follower circuit and a clamp circuit can be removed because of high equivalent input impedance and internal clamping protection circuit design in every ADC input channel on MC56F8257 DSC.

# 6 Software design

## 6.1 System software organization

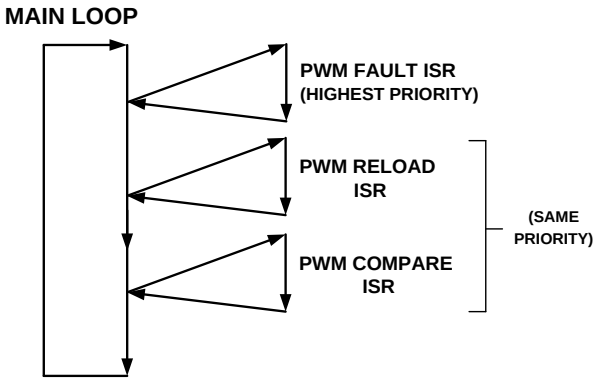


**Figure 10. System software structure**

As shown in Figure 10, the software for peak current mode control has the following threads:

- The Main Loop thread
- The PWM ISR thread
  - PWM Compare ISR thread
  - PWM Reload ISR thread
  - PWM Fault ISR thread

In addition, there are system clock initialization, CPU initialization, peripheral initialization (like ADC, DAC and comparator), PWM module configuration, and variables initialization routines. These ensure that the software runs in the desired manner before the main loop executes.

## 6.2 Main loop description

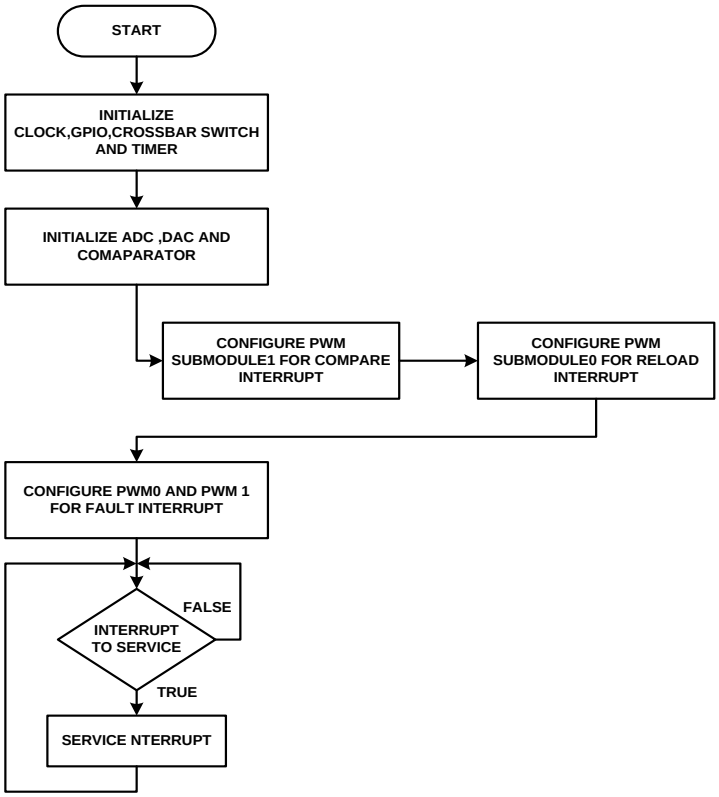


**Figure 11. Main loop flowchart**

After a processor reset, the main loop thread performs the following tasks:

- The system set up consists of the following modules:
  - Clock
  - COP
  - Core
  - ADC
  - HSCMP
  - Timer
  - PWM
  - GPIO
- Initialization of variables
- Interrupt source selection and enabling
- Run/stop control
- LED indication control

## 6.3 PWM ISR description

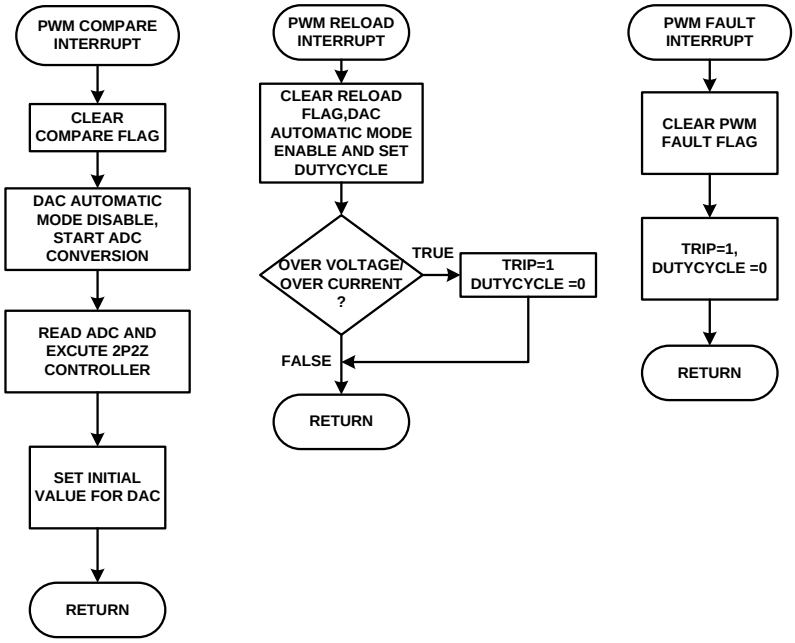


**Figure 12. PWM interrupt subroutines**

The PWM interrupt thread performs the entire peak current mode control algorithm. The implementation has three service routines corresponding to the PWM Compare, PWM Reload, and PWM Fault interrupts as shown in Figure 12.

# 7 Experimental results

A design example is presented for a buck converter with peak current mode control using MC56F8257 DSC. The converter has the following specifications:

- $V_{in}$ = 100 V
- $V_O$ = 60 V
- $D = {}^{V_O}/_{V_{in}} = 0.6$
- $I_O$ = 100 A
- $R_L$ = 1 Ω
- L = 200 µH
- C = 18800 µF
- $R_C$ = 11.5 mΩ
- $R_i$ = 24 mΩ
- $F_S$ = 10 kHz

The inductor current waveform and PWM pulses were observed. The converter is operating at duty cycle of 60% (greater than 0.5). When no compensating ramp was added in the control loop, the sub-harmonic oscillation was observed in the inductor current waveform and is shown in Figure 13.

When a compensating ramp of peak-to-peak magnitude as calculated in Equation 10 is added in the control loop, the observed inductor current waveform and PWM pulses are as shown in Figure 14. The problem of sub-harmonic oscillation is eliminated with the addition of compensating ramp.

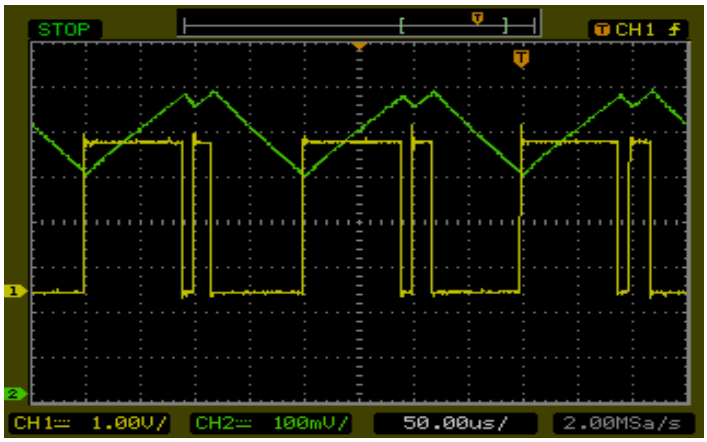


**Figure 13. Inductor current and PWM pulses without slope compensation**

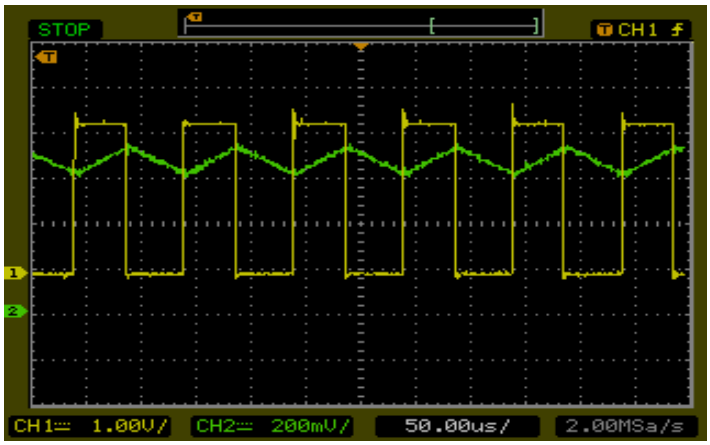


**Figure 14. Inductor current and PWM pulses with slope compensation**

# 8 Conclusion

This application note provides the details about implementing digital peak current mode control mechanism using Freescale's MC56F8257. By making use of the peripheral interfaces available on DSC, it is possible to implement reliable buck converter. The converter exhibits excellent performance characteristics like short-circuit protection, overcurrent protection, immunity towards input voltage variations, and quick response to the load variations.

# 9 References

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# 10 Revision history

**Table 1. Revision history**

| Revision No. | Date | Substantial changes |
|---|---|---|
| 0 | 04/2013 | Initial release |
| 1 | 05/2013 | • Removed one of the reference sources.<br>• Created the revision history table |

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