Fault Tolerant Multilevel Current Source Inverter

Miguel Aguirre[1]
CIDEI – ITBA
maguir@itba.edu.ar

Laura Calviño
CIDEI-ITBA
lcalvino@alu.itba.edu.ar

María Inés Valla
LEICI - UNLP
m.i.valla@ieee.org

Abstract – **This paper explores the issue of constructing a multilevel current source converter (MCSI) topology with fault tolerant capabilities. A novel modular single rating inductor MCSI topology is analyzed. The MCSI proposed is made by identical modules where all inductors carry the same amount of current. The current balance is achieved by a Phase-Shifted Carrier SPWM proper implementation. A new state machine approach, easy to implement on a FPGA, allows minimizing switching frequency by taking advantage of the three different zero-states of the topology. A protection circuit is proposed to avoid over voltages in case of a failure. The performance of a seven level, four modules, fault tolerant arrangement is analyzed and is thoroughly simulated with Matlab Simulink.**

I. INTRODUCTION

Multilevel voltage source converters have captured investigators attention and have been used in major applications involving high power, while current source inverters have not been in focus. Recent evolution of electronic switches, designed to rapidly turn on and off, such as IGBT, IGCT and ETO allow the implementation of PWM modulation and multilevel schemes powered by a current source, with ensuing low distortion and fast dynamic response in high power applications [1]-[2].

Classic CSI or thyristor converters have two degrees of freedom, hence only two branches of a three phase load are fed simultaneously, leaving the third one unplugged. Therefore, current through each phase is always univocally determined (I, 0, -I), the fulfillment of this is compulsory in CSIs, but implies using large capacitors to avoid harmful overshoots in switches and ease the thyristors switch off [2].

Multilevel topologies present several advantages regarding total harmonic distortion and stress on inductors and switches [1]. Moreover, multilevel CSI have more degrees of freedom, usually as many as inductors acting as current sources to impose different currents in the three phases depending on the topology. They are a smart choice to improve performance and efficiency in industrial applications where high power or low voltage and high current, is required, such as induction motor drives, FACTS and HVDC.

Several Multilevel-CSI topologies have been developed [3]. Multi-rating-inductor-MCSI requires only two balance inductors for two adjacent modules, and every pair of balance inductors carry different current values. There are no balance inductors in the paralleled H-bridge-MCSI although the use of multiple independent dc current sources is necessary [4].

In this paper a single-rating-inductor-MCSI is employed to feed a three phase load. The converter consists of a number of identical modules which determine the different current levels [5]. Each module uses two balance inductors and six power switches. All inductors of every module should carry the same current values. The current flowing through the inductors can be balanced and switching frequency can be reduced by applying a state machine modulation that properly uses redundant zero states [6]. Fault tolerant assembles are easy to develop and operate because all modules are identical.

The modulation and gate drives control logic are implemented on a Field-Programmable-Gate-Array, FPGA, [7] which is a powerful, cost-effective solution. It allows complex logical and control algorithms, fast speed and multiple I/O pins, which becomes especially attractive for multilevel converters control.

This paper presents a simple approach, showing that current balance can be provided by adapting a well known PWM strategy [8]-[9] while minimizing switching speed using a sequential machine approach. In detail, the paper is organized as follows. The circuit is described in Section II A, followed by a comprehensive analysis of the modulation method in sections II B through II D. Finally, Section III presents the evaluation of the performance of the proposed system with simulation results, including the protection circuit essential for secure operation and fault tolerant capabilities inherent of topology. A 3kW prototype is under construction.

II. NOVEL CSI ARRANGEMENT

A. *Switching structure*

The converter topology presented in Fig. 1, also known as "single-rating inductor MCSI", consists of multiple CSI sub circuits, connected in parallel with the load and sharing a common current source. Each group of six switches and two inductors will be referred as a *module*. Those *sharing inductors* split in equal shares the current from the main source.

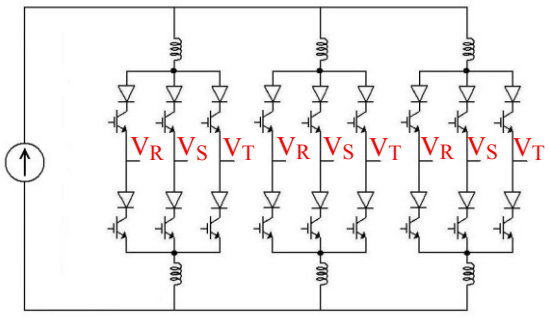

Fig. 1. Basic Multilevel CSI scheme.

[1]M. Aguirre is currently working toward the Doctor in Engineering degree at Universidad Nacional de La Plata.

The main advantage of this Multilevel CSI configuration is its modular structure, where each identical module handles only a fraction of the load current [6]. The number of levels in output current can be determined according to the number of modules *"m"* in (1)

$$i_n = \frac{m-n}{m} I_{DC} \qquad n=0,1,\ldots,2m \qquad (1)$$

where *m* represent the number of modules and n goes from 0 to 2*m*.

In this paper we consider *m*=3 to obtain seven levels of load current (2).

$$\frac{i_l}{I_{DC}} = 1,\ \frac{2}{3},\ \frac{1}{3},\ 0,\ -\frac{1}{3},\ -\frac{2}{3},-1 \qquad (2)$$

Seven levels in output current requires eighteen switches with bidirectional blocking capability. The switches can be implemented by MOS transistors, IGBT, ETO or IGCT, among others, with the addition of series diodes. The technology of the switch depends on the power and frequency required by the application. Fault tolerant capabilities can be achieved by adding hot spare modules.

Different load current levels can be obtained by turning on or off each switch. Two examples are shown in Fig. 2 and the corresponding switches states are presented in Table I. In example 1, the switches A1, B1 and C1 are on, while each branch conducts a third of supply current *"I"*. Current into phase R equals *"I"*. The current in phase S is *I*/3 flowing from the load to the source through switch A5 and the current on phase T is 2/3*I* flowing towards the source through switches B6 and C6. The analysis of example 2 is analogous, providing 2/3*I* and 1/3*I* into phases R and S respectively, while all current *I* flows outwards phase T. Solid lines in Fig. 3 show the current paths through the whole converter down to the load for the examples described previously.

It is worth to notice that each output current level can be generated by more than one combination of switches. This can be seen in Fig. 4 where an alternative switch configuration for example 1 is shown. Currents on the load, IR=*I*, IS=–1/3*I*, IT=–2/3*I* will be supplied as a result of turning on switches A1, B1, C1, A5, B6, C6 (Fig. 3a) as well as switches A1, B1, C1, A6, B6, C5 (Fig. 4). This redundancy gives some degree of freedom to work on the current balance of all inductors and to minimize the switching frequency of the converter.

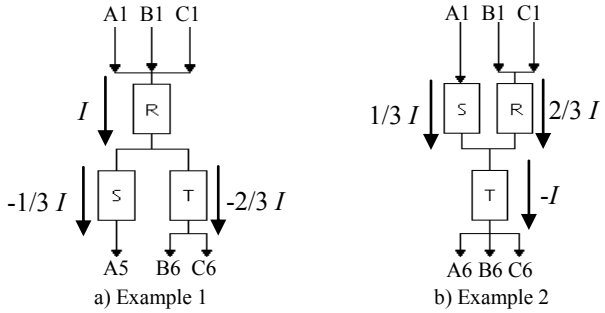

Fig. 2. Current Flow according to switches in on-state.

TABLE I
SWITCHING COMBINATIONS FOR EXAMPLES IN FIG. 2.

	A1	A2	A3	A4	A5	A6	B1	B2	B3	B4	B5	B6	C1	C2	C3	C4	C5	C6
Ex1	1	0	0	0	1	0	1	0	0	0	0	1	1	0	0	0	0	1
Ex2	0	1	0	0	0	1	1	0	0	0	0	1	1	0	0	0	0	1

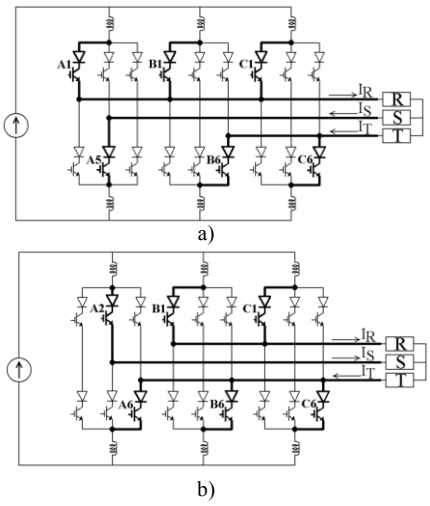

Fig. 3. Current flow, a) example 1, b) example 2.

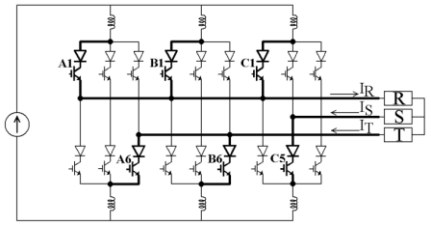

Fig. 4. Alternative switching combination providing same output currents as Fig. 3a (I_R=*I*, I_S=-1/3*I*, I_T=-2/3*I*).

B. SPWM of one module

SPWM Modulation is based on the comparison of a sinusoidal control signal with a triangular carrier. The switches on a single branch are turned on or off depending on whether the control signal is greater or smaller than the carrier. Working with three phase loads, the control signals must be standard three phase sine waves.

In SPWM for voltage source inverters (VSI), the signals, P_R, P_S, P_T (Fig. 5b), generated by comparison of one triangular with three sine waves (Fig. 5a), are directly used to drive the switches of each leg of the VSI. But this is not so easy to implement in CSI, in order to guarantee that the current of the module is imposed to a certain phase of the load. The driving signals are obtained with some more manipulation of the signals. First an XOR of P_R, P_S, P_T two at a time ($P_R \oplus P_S$, $P_S \oplus P_T$, $P_T \oplus P_R$) is performed to identify which of the branches have equal levels and L_R, L_S, L_T (Fig. 5c) are obtained. These signals indicate when each phase should deliver current but they have no information of their polarity. This means that signals *Li* combine both upper and lower switch signals in each branch ($L_R \rightarrow A1$ and $A4$, $L_S \rightarrow A2$ and $A5$, $L_T \rightarrow A3$ and $A6$).

Nunca deberían estar prendidas LR, LS y LT al mismo tiempo, eso es algo que técnicamente nunca se podría cumplir. Lo que si podés tener es dos de estas al mismo tiempo, si tienen 2 polaridades distintas.

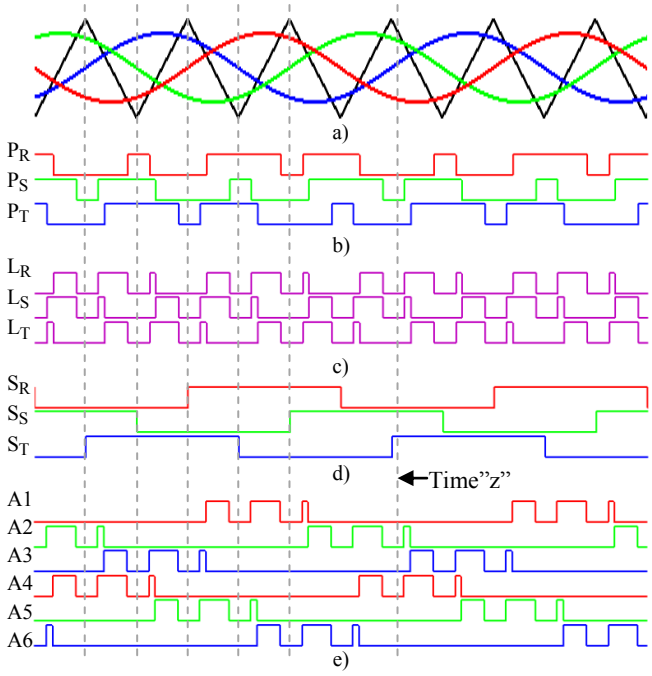

Fig. 5. SPWM modulation.

It is still necessary to identify whether the upper or the lower switch should carry the current. This is performed with the help of signals *Si* (Fig. 5d) which represent the polarity of the reference currents of each leg. Upper switch gate signal is obtained by performing a logical AND of *Li* with *Si*. Lower switch gate signal is the logical AND of *Li* with logical complement of *Si* [5]. The resulting six active states are shown in table II. Fig. 6 shows the corresponding logic diagram. A glitch-free logic is mandatory in real FPGA implementation to avoid spurious firing of the switches.

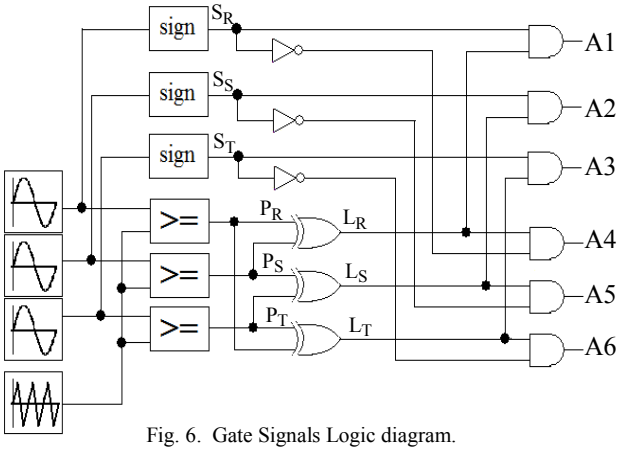

Fig. 6. Gate Signals Logic diagram.

TABLE II
DIRECT SPWM GATE SIGNALS

State	A1	A2	A3	A4	A5	A6	I_R	I_S	I_T
1		1				1	0	*I/3*	*- I/3*
2	1				1		*I/3*	*- I/3*	0
3	1					1	*I/3*	0	*- I/3*
4			1	1			*- I/3*	0	*I/3*
5		1		1			*- I/3*	*I/3*	0
6			1		1		0	*- I/3*	*I/3*

Los otros estados son zero-states ó no son válidos

C. *Minimum switching frequency Zero State selection*

Firing signals generated in Fig. 5e cannot directly drive IGBT's gates since they generate zero states by turning off all switches. This does not allow inductor's current continuity in a CSI, e. g. time "z" in Fig. 5. Zero states generated by the SPWM logic should be recognized and replaced by adequate zero states according to the CSI topology as is developed in this section.

A CSI module can generate zero states in seven different ways as shown in Fig. 7 (where on switches are highlighted). Closing all six switches (Fig. 7a) is the simplest implementation at the expense of greater losses. Closing only the two switches of a branch (Fig. 7b) is the most efficient solution in terms of switching frequency although requesting more calculation complexity. The combination of switches shown in Fig. 7c is the worst case of switching losses and calculation complexity, hence it will not be considered.

Performing a detailed analysis of the commutation signals (A1…A6) generated with SPWM (Fig. 5e) it is easy to identify six main sequences as shown in Fig. 8, e.g. sequence A is a string of states 6, 2 and 0 in the form "…0 2 6 0 6 2 0 2 6 0 6 2 0…". Each active state (1 to 6) is generated as described in section II-B and represents a combination of switches in a module according to table II.

Each sequence (A to F) is a state of the sequential machine displayed in Fig. 9. The jump from one sequence to the next is performed by detecting a switching state that does not belong to the current sequence, e.g. *sequence B* will run until a *state 1* is generated by the PWM logic, then *sequence C* will be initiated.

There are three zero state combinations (Fig. 7b) whose selection allows to minimize the switching frequency.

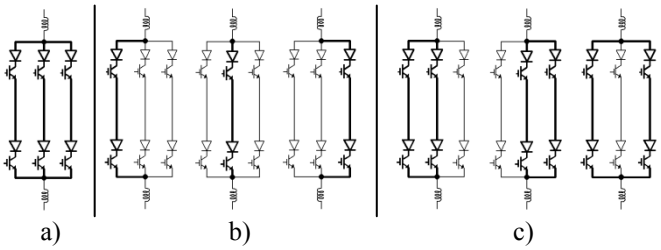

Fig. 7. Seven zero state posibilities for one CSI module

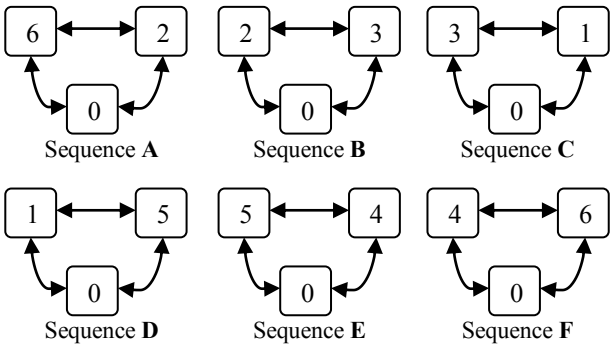

Fig. 8. Six conmutation secuences.

Correct zero state implementation is mandatory when minimizing switching frequency, avoiding unnecessary switches' changes inside a sequence thus lowering power dissipation. Minimum switching frequency can be accomplished by correctly choosing the zero state in each sequence.

The table III shows that only one zero combination is assigned to each sequence in order to minimize the switching frequency. For example, during sequence *B*, turning on switches A1 and A4 as zero state avoids that A1, A2 and A3 have to change state while the sequence is active.

Logic state machine replaces zero states generated by SPWM (all switches closed) by optimal zero combination according to the active sequence. The active states are not affected by the state machine and pass through unchanged. Fig. 10 shows the gate signals of switch A1 as an example of the effect of the sequential machine on commutation of the power switches. Gate signals generated with the state machine zero selection (Fig. 10b) have much less commutations per cycle than all switches closed (Fig. 7a) zero approach (Fig. 10a). The asynchronous sequential state machine is implemented with StateFlow in Matlab Simulink. Its actual behavior has been checked by FPGA implementation in a Cylcone EP1C6T144C6.

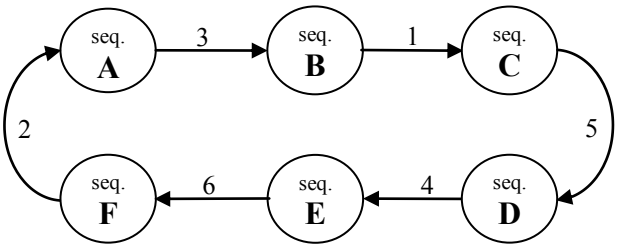

Fig. 9. Sequence of states.

TABLE III
MINIMUM SWITCHING FREQUENCY GATE SIGNALS

Sequence	Module A Switch state							Output Current		
	State	A1	A2	A3	A4	A5	A6	IR	IS	IT
A	2	1				1		*I*/3	- *I*/3	0
	6			1		1		0	- *I*/3	*I*/3
	0		1			1		0	0	0
B	2	1				1		*I*/3	- *I*/3	0
	3	1					1	*I*/3	0	- *I*/3
	0	1			1			0	0	0
C	3	1					1	*I*/3	0	- *I*/3
	1		1				1	0	*I*/3	- *I*/3
	0			1			1	0	0	0
D	1		1				1	0	*I*/3	- *I*/3
	5		1		1			- *I*/3	*I*/3	0
	0		1			1		0	0	0
E	5		1		1			- *I*/3	*I*/3	0
	4			1	1			- *I*/3	0	*I*/3
	0	1			1			0	0	0
F	4			1	1			- *I*/3	0	*I*/3
	6			1		1		0	- *I*/3	*I*/3
	0			1			1	0	0	0

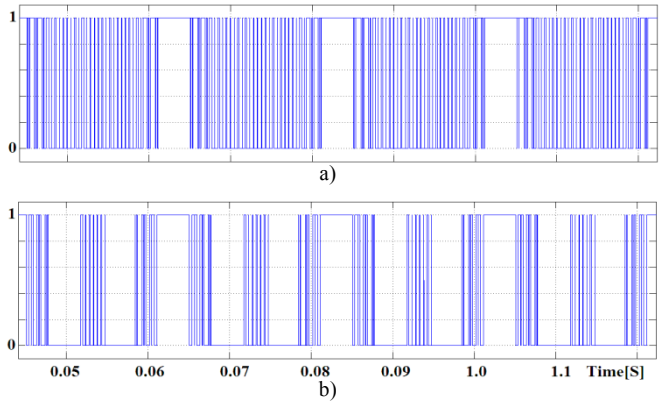

Fig. 10. Gate signal for switch A1 a) SPWM b) sequential state machine.

D. Multilevel operation - Phase-Shifted Carrier SPWM

Multiple modules are arranged to produce a multilevel output current. Since load voltage may affect the current balance over the sharing inductors a careful choice of the PWM should be performed. The simplest way is to adopt a Phase-Shifted Carrier SPWM [4]. The PSC-SPWM uses as many triangular carriers as modules have the converter. These carrier waves are delayed an angle

$$\varphi_k = \frac{2\pi}{m}k \tag{3}$$

where m=3 and k goes from 1 to m as shown in Fig. 11.

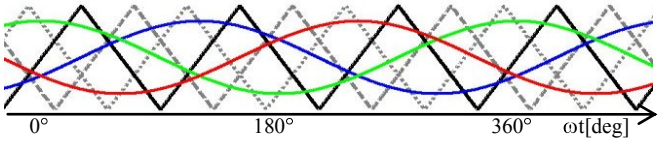

Fig. 11. PSC-SPWM modulation.

The same modulation procedure described in the previous section is reproduced for each module using the corresponding carrier. The output current level is controlled by setting the reference sine waves amplitude. The amplitude modulation index m_a is then defined as,

$$m_a = \frac{\hat{v}_{sine}}{\hat{v}_{triangular}} \tag{4}$$

E. Fault Tolerant Capability And Protection

Fault tolerant capabilities are reached by adding a hot spare module, as shown in Fig. 12. When a failure is detected all switches in a damaged module should be turned off. Two thyristors per module allow sharing inductor's current to flow through main inductors in order to maintain current continuity and avoid switches damage. Only the thyristors arrangement in module A is shown in Fig. 12 for simplicity.

Fault detection is accomplished by measuring output currents and voltage in each module. Comparison of measured and expected values in an FPGA table indicates if a switch is in a wrong state. Momentary over voltages caused by calculation delays are avoided by attaching Metal Oxide Varistors (MOV) to each module's terminals.

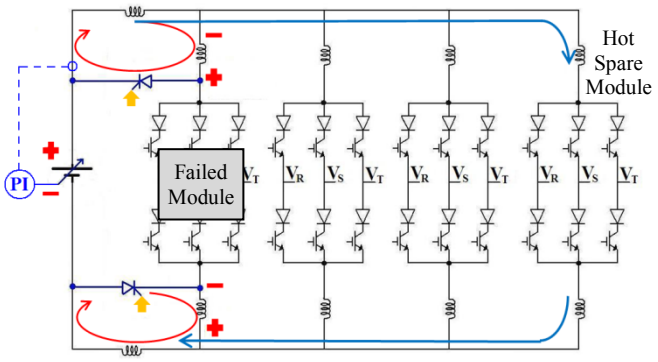

Fig. 12. Multilevel CSI protection circuit and fault tolerant arrangement. Currents paths under transient fail conditions.

In case of failure thyristors are fired, allowing the inductor's current to flow through main inductors as shown in Fig. 12. A current control (PI) of the input rectifier is introduced to avoid the rise of main inductors' current. This control reduces the rectifier voltage, forcing the inductors of the failed module to discharge.. Meanwhile, gate signals from damaged module are routed to spare module whose current will grow to its nominal value causing only a momentary distortion in the load current.

Thyristors clamp failed module voltage to V_{DC} as long as there's energy on its sharing inductors. Once such energy reaches zero, thyristors turn off and the module is ready to be safely replaced or repaired.

Spare modules can be cycled to ensure fully operational behavior in case of failure, and also to perform preventive maintenance and reduce switches' stress.

III. Simulation Results

The performance of the proposed converter is simulated with Matlab Simulink. The fault tolerant converter arrangement is composed by four identical modules. Each module is built with six IGBT's, with series diodes. The PSC-SPWM logic and the sequential state machine for each module are implemented with the StateFlow tool. The hot spare module remains disconnected until a failure is detected. A three phase controlled rectifier provides the energy to the main inductors. The load is composed by a three phase R-L series connection. A capacitor bank is used to filter the output current. Its capacitance is calculated to avoid that the resonant frequency matches the harmonics generated by the converter. The main parameters of the converter are summarized on Table IV.

TABLE IV
Simulation Parameters

Main source	SCR controlled rectifier ±300V
Main current inductors	L = 200 mH
Main current (nominal)	500 A
Sharing inductors	L = 165 mH
Load frequency	50 Hz
Filter capacitors	5µF
Switching frequency	1065 Hz

The currents in main inductors are regulated with a PI control, acting on the firing angle of input rectifier's thyristors. The reverse power capability of the input rectifier allows four-quadrant operation or regenerative braking of the load.

The inverter output current is shown in Fig. 13a, where the seven levels (I, $2/3I$, $1/3I$, 0, $-1/3I$, $-2/3I$, $-I$) can be recognized. The output current is filtered by a small capacitor bank delivering a sinusoidal current to the load (Fig. 13b) with low distortion whose spectrum can be seen in Fig. 13c.

Fig. 14 shows the balance operation of all sharing inductors. It is clear that each inductor carries one third of the main current. A detail of one of these currents is shown in Fig. 14b. The output current is regulated by changing m_a presenting a linear dependency. The current of the sharing inductors remains under balance at different values of m_a.

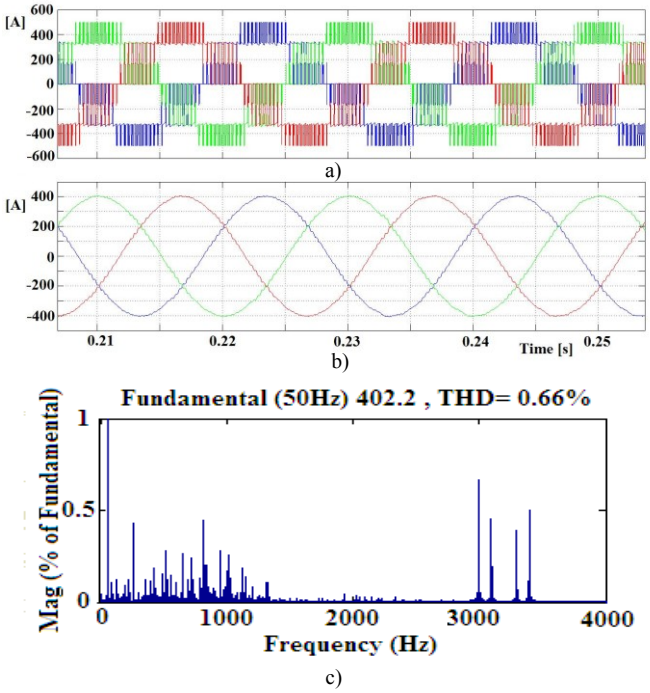

Fig. 13. a) Inverter output current. b) Load current. c) Load current spectrum.

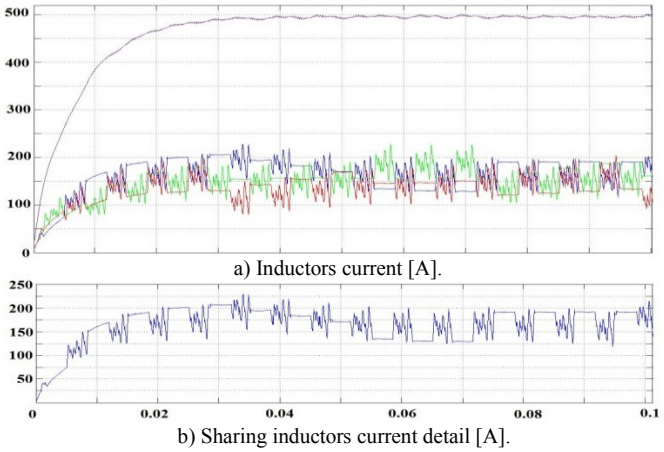

Fig. 14. Inductors current balance.

Fig. 15 shows the load current and inductor current for each module different values of m_a.

In Fig. 16 the open loop load regulation under different load conditions is shown. First, only the load resistance is change and then both resistance and inductance are reduced showing a very good dynamic response. Increments in resistance and inductance do not affect output current either. The current balance is not affected by load changes.

A failure in module A is simulated in Fig. 17. When a fault condition is detected, all switches in the damaged module are turned off and the thyristors are fired. The gate signals from the damaged module are routed to the IGBTs of the spare module. The current provided by the input rectifier (Fig. 17a) is reduced due to the discharge of failed module's sharing inductors into main current path. Failed module inductors' current (Fig. 17b) falls down to zero while the current of the spare module (Fig. 17c) rises to its nominal value. The load current (Fig. 17d) suffers a small disturbance only while the current in the inductors of the spare module rises to its nominal values.

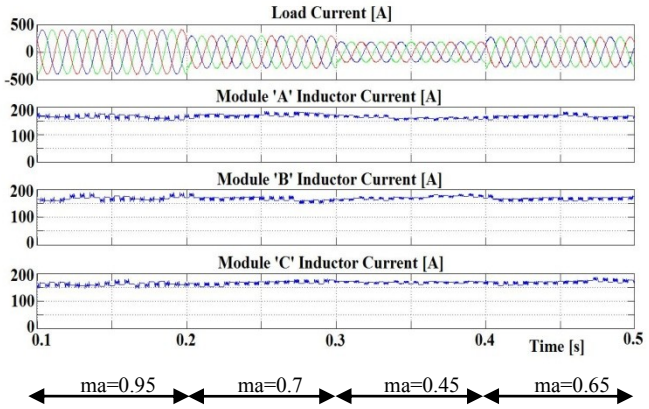

Fig. 15. Output linearity and sharing inductor's current balance for different m_a values.

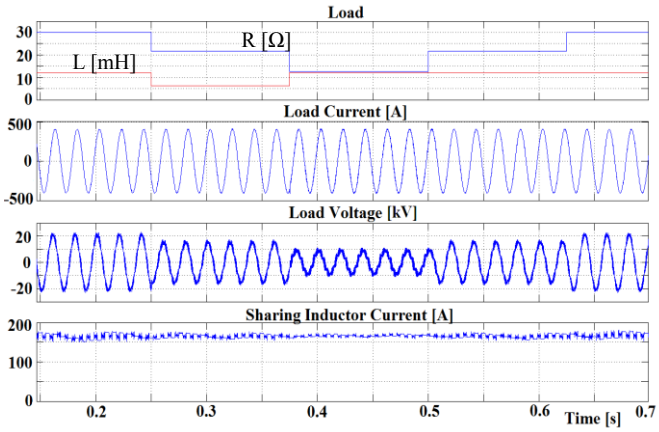

Fig. 16. Output regulation against load variation.

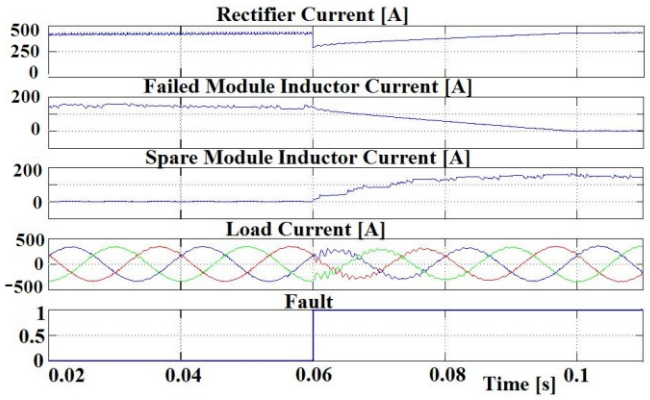

Fig. 17. Fault tolerant behavior.

IV. Conclusions

A novel modular single rating inductor MCSI topology was analyzed in this paper. The behavior of a seven level, four modules, fault tolerant arrangement was simulated showing excellent conditions of load regulation, linearity and dynamic response. Fault tolerance was achieved by adding a hot-spare module and a protection circuit to handle the current of the inductors in case of a failure. As a result of circuit topology and PSC-SPWM utilization, current balance was achieved in both main and sharing inductors, even under load and operation point changes. The switching frequency was minimized with a new state-machine approach, taking the advantage of the three different zero-states of the topology.

References

[1] B. P. McGrath, D. G.Holmes, "Natural current balancing of multicell current source converters", IEEE Transactions On Power Electronics, Vol. 23, No. 3, May 2008

[2] Mitsuyuki Hombu, Shigeta Ueda, Akjteru Ueda and Yasuo Matsuda, "A new current source GTO inverter with sinusoidal output voltage and current" IEEE Transactions on Industry Applications, Vol. IA-21 no. 5, september/october, 1985.

[3] ZhiHong Bai and ZhongChao Zhang. "Conformation of multilevel current source converter topologies using the duality principle", IEEE Transactions On Power Electronics, Vol. 23, No. 5, September 2008.

[4] Zhihong Bai; Zhongchao Zhang; Yao Zhang; "A generalized three-phase multilevel current source inverter with carrier phase-shifted SPWM", PESC 2007, IEEE 17-21, pp. 2055-2060. June 2007.

[5] Yu Xiong, Danjiang Chen, Xin Yang, Changsheng Hu and Zhongchao Zhang, "Analysis and experimentation of a new three-phase multilevel current-source inverter" 35th Annual IEEE Power Electronics Specialistr Conference, Aachen, Germany, 2004.

[6] D. N. Zmood, and D.G. Holmes, "A generalised approach to the modulation of current source inverters" PESC98, Vol. 1, pp. 739-745, May, 1998.

[7] Zhihong Bai; Zhongchao Zhang; "Digital control technique for multi-module current source converter", ICIT 2008, pp. 1-5, April 2008.

[8] Xiao Wang and Boon-Teck Ooi, "Unity pf current-source rectifier based on dynamic trilogic PWM", IEEE Transactions On Power Electronics, Vol. 8, No. 3, July 1993.

[9] Zhihong Bai, Zhongchao Zhang, Guozhu Chen, "Development of a three-phase high power factor multilevel current-source rectifier", PESC2008, pp. 574-578. 15-19 June, 2008.