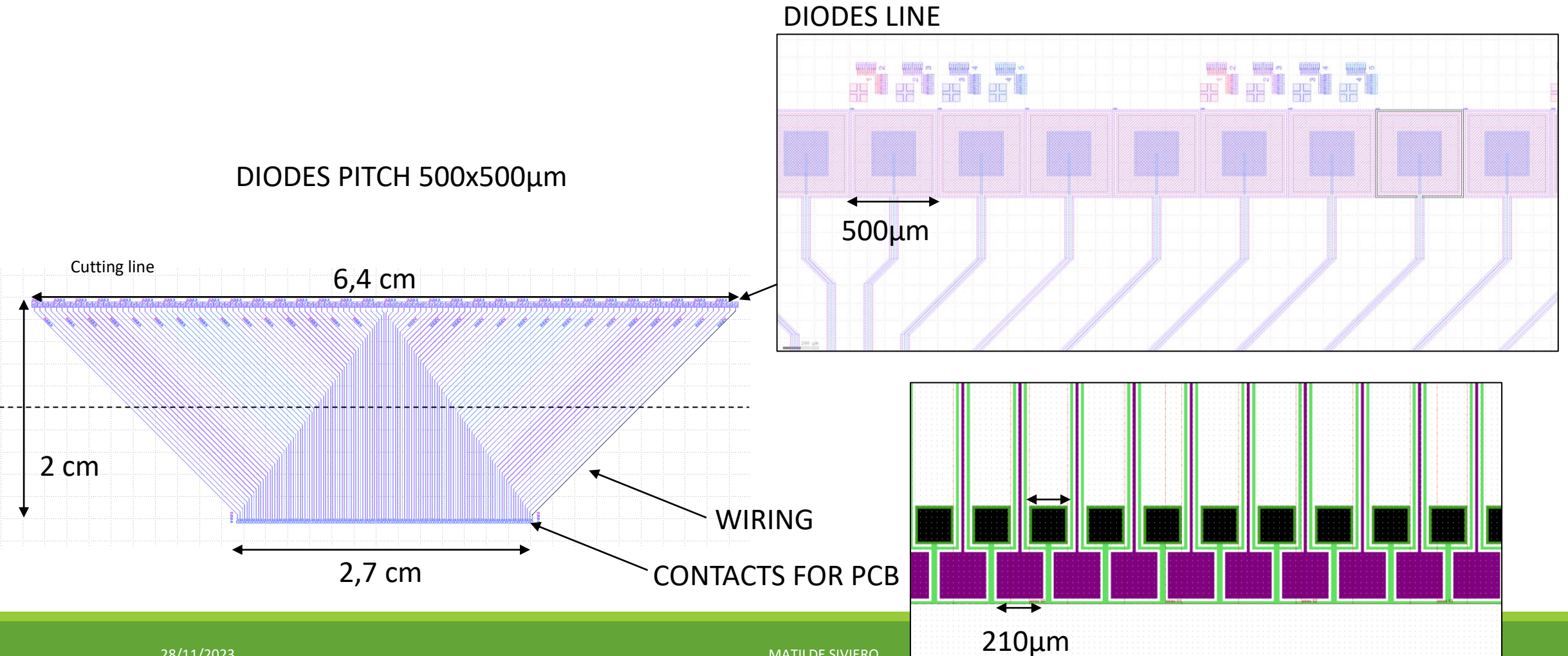


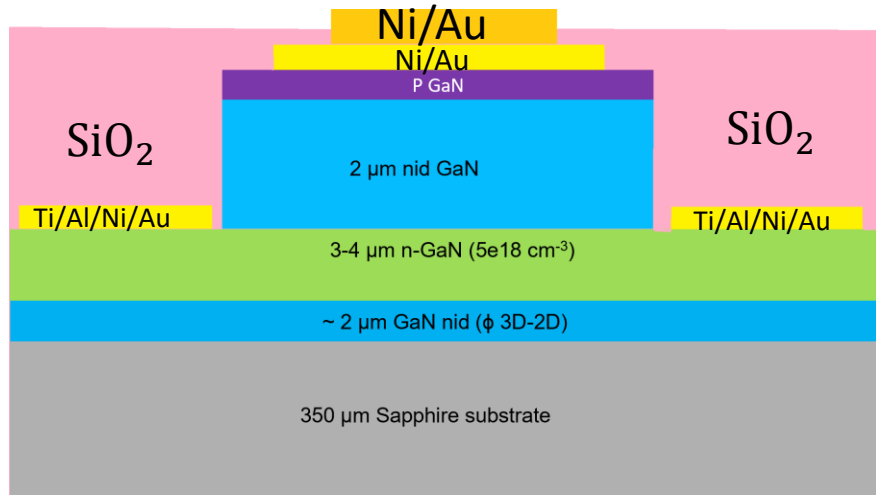
LATEST FABRICATED SAMPLES

MATILDE SIVIERO
CRHEA

FIRST 128 LINEAR ARRAY



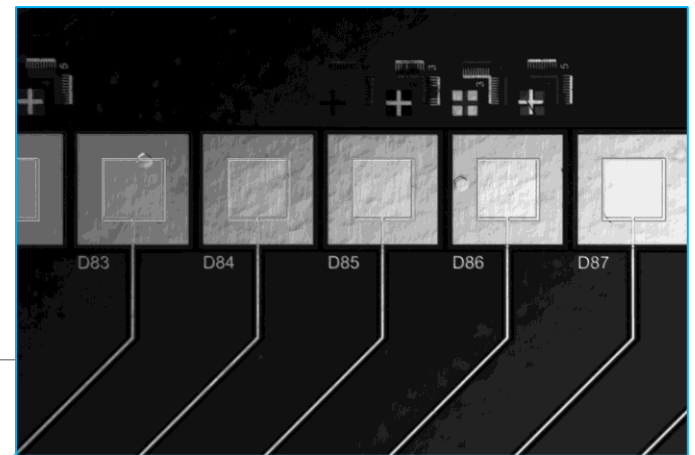
FIRST 128 LINEAR ARRAY



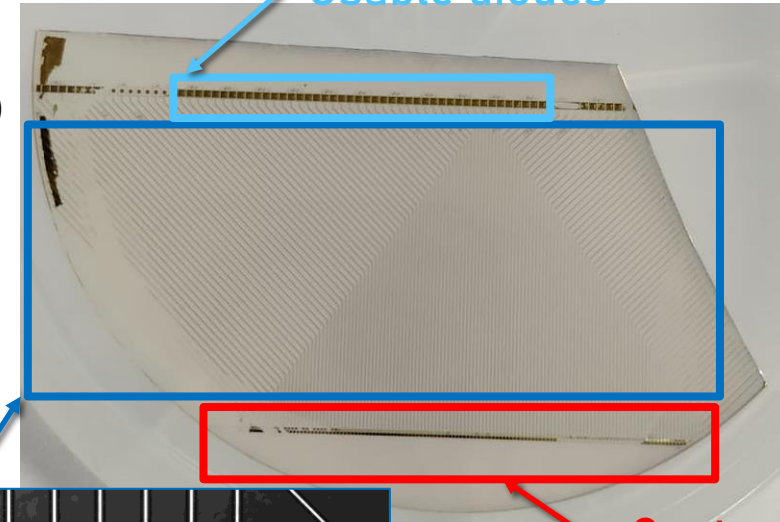
(Pin diode)

5 photolithography steps:

1. Mesa (litho+ plasma etch)
2. N contact(litho+metal dep)
3. P contact(litho+metal dep)
4. SiO₂ (deposition+opening)
5. Gold deposition

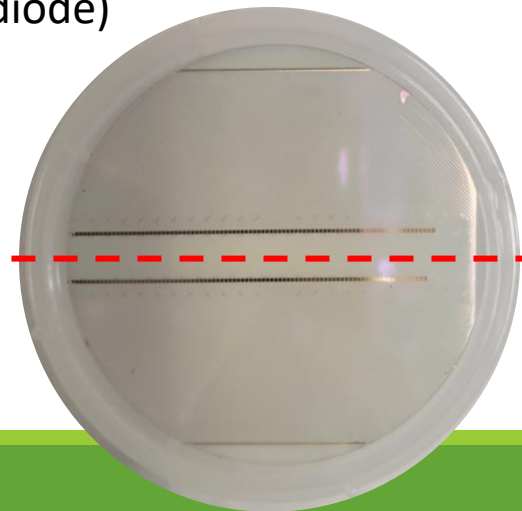


Usable diodes



Diodes line

Contacts for wiring

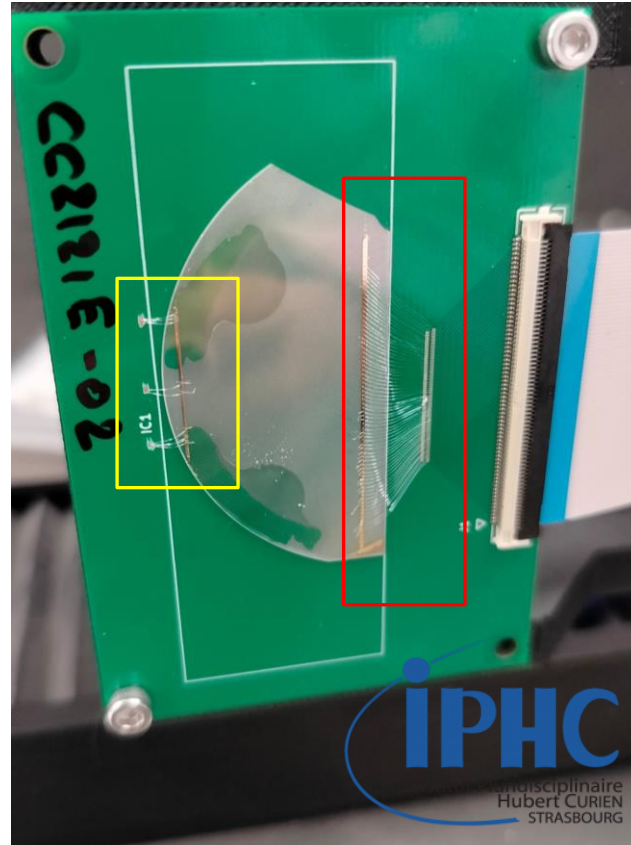


2 arrays on 1 wafer of 2"

YIELD: about 70
working diodes over 90

Not only the gold lines were useless...

Only the ground was bonded using the contact pads

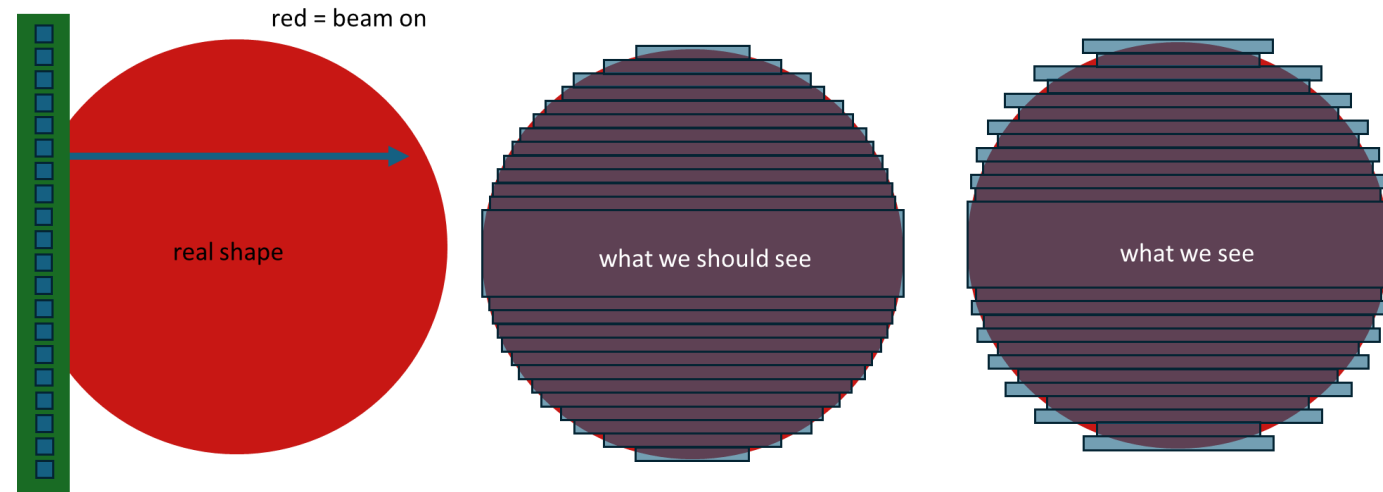
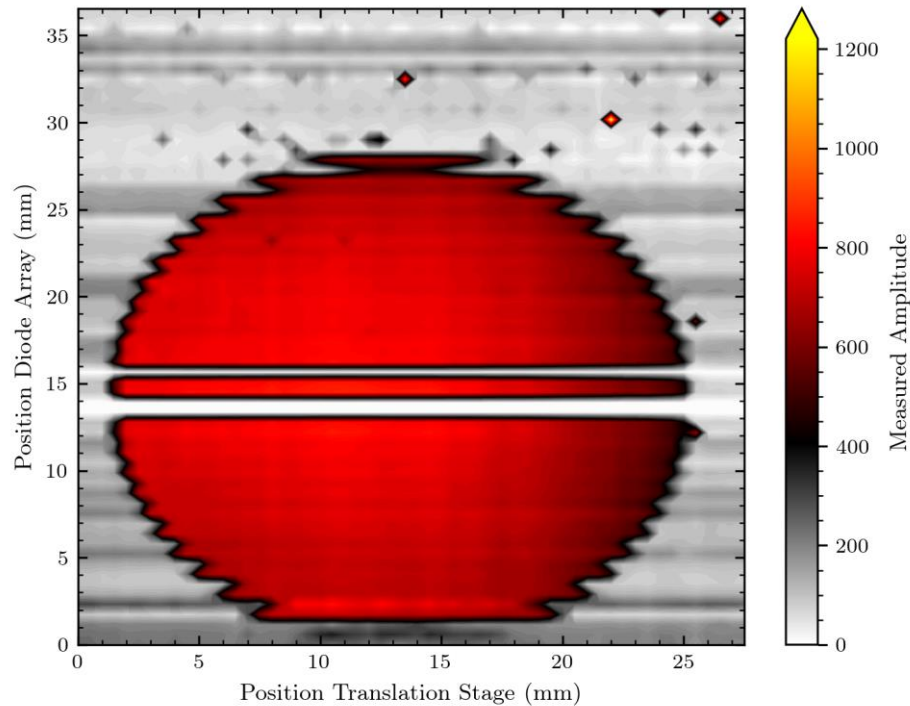


The diodes bonding to the PCB was done directly on top of the diodes

So the diodes pitch of $500\mu\text{m}$ was not a problem at all!
The bonding worked great

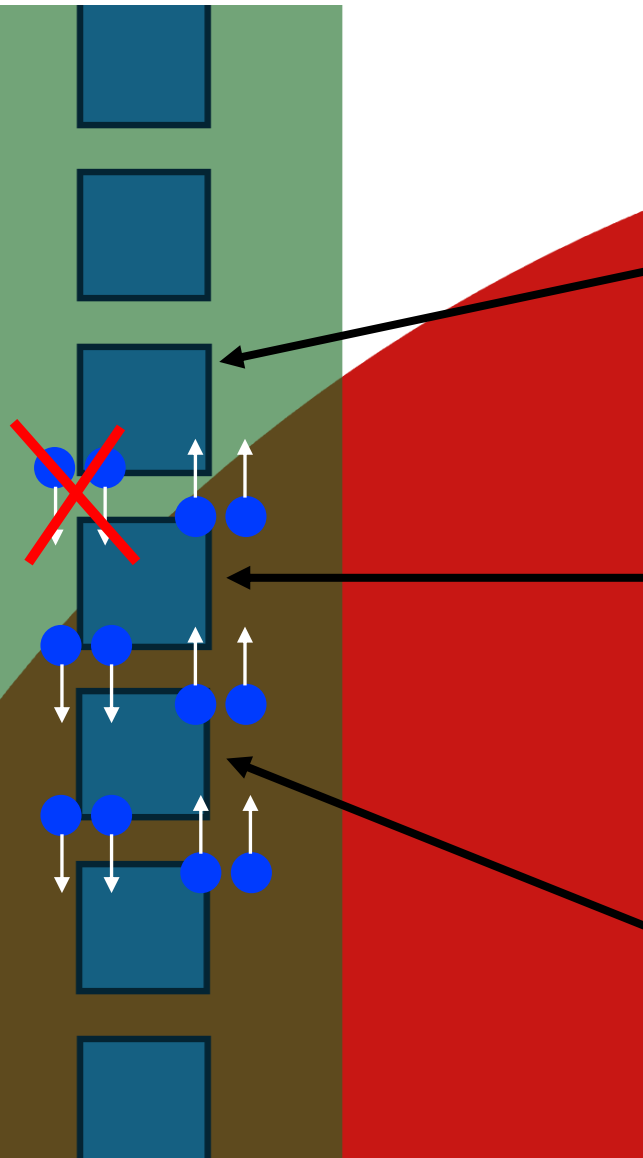
...the gold lines only created issues

Gold wires generate a parasitic signal once irradiated leading to periodic line artifacts



Images from Nico Brosda

Red = proton beam exposure



Diode n+1:

Electrons from diode n arrive = $+ N_e$

No electrons are lost

 $+ N_e$ signal gained

Diode n:

Electrons from diode n-1 arrive = $+ N_e$

Electrons are lost to diode n-1 and diode n+1 = $- 2 \times N_e$

No electrons from diode n+1 arrive

 $- N_e$ Signal lost

Diode n-1:

Electrons from diode n-2 and n arrive = $+ 2 \times N_e$

Electrons are lost to diode n-2 and diode n = $- 2 \times N_e$

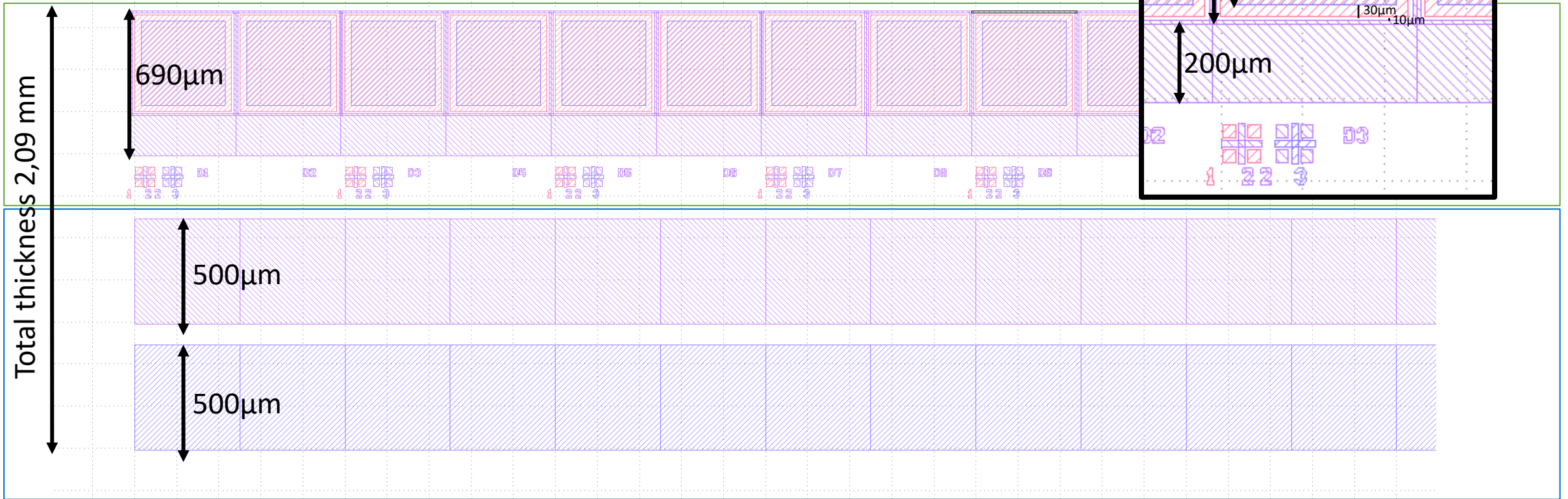
0

NEW LINEAR ARRAY MASK

128 DIODES ON 3 INCHES WAFERS

500x500 μm

DIODES LINE (x140) Maximum total length 500 μm x140=7cm



TESTING LINES FOR WIRE BONDING

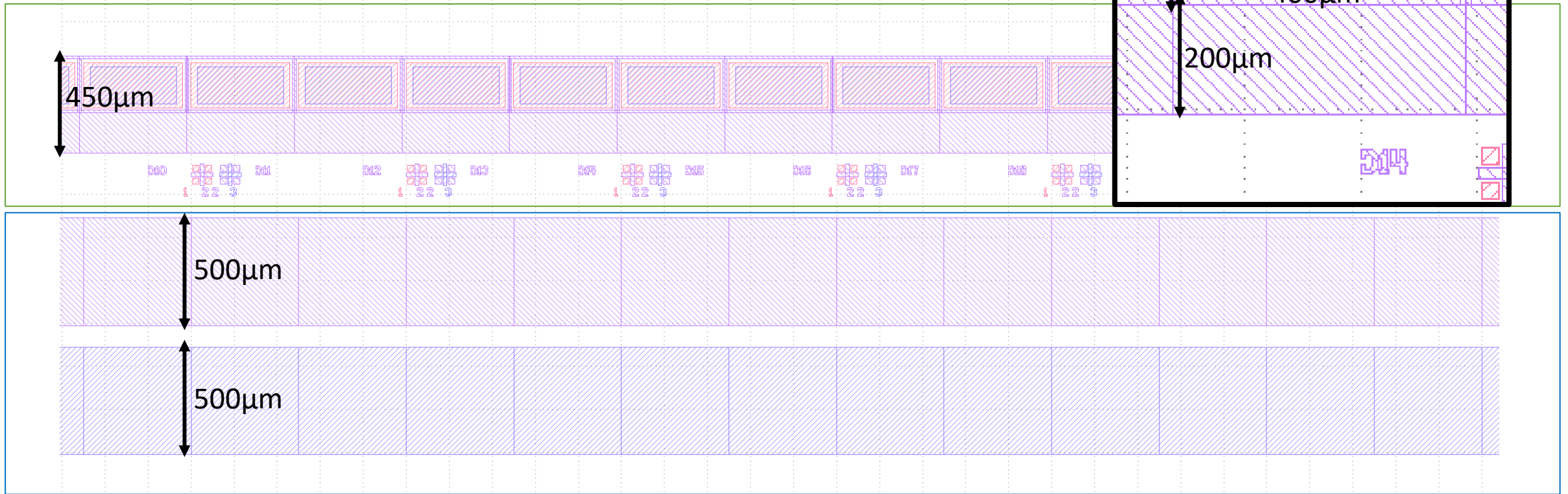
500x250 μm

n CONTACT = GROUND

SINGLE DIODE

DIODES LINE (x140) Maximum total length $500\mu\text{m} \times 140 = 7\text{cm}$

Total thickness = 1,85mm

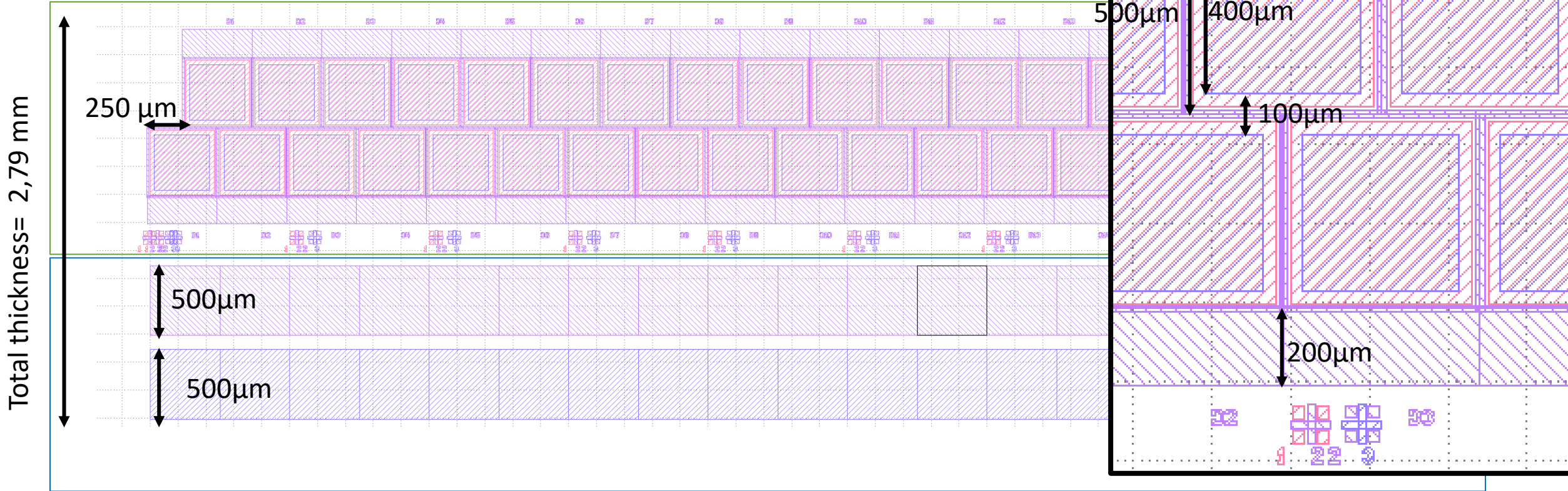


TESTING LINES FOR WIRE BONDING

(one continuous line for p contact and one of ground contact bonding test)

DOUBLE LINE 500x500 μm

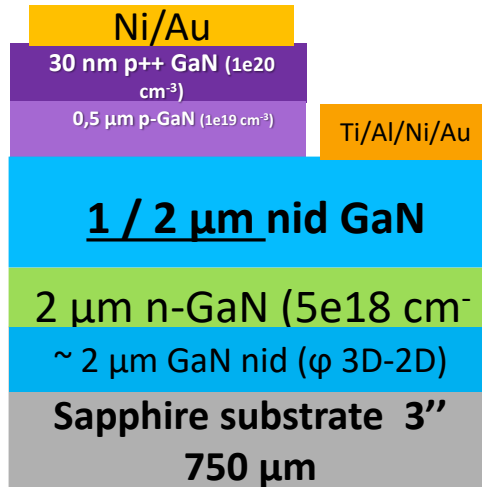
DIODES LINE (x140) Maximum total length 500 μm x70=3,5cm



TESTING LINES FOR WIRE BONDING

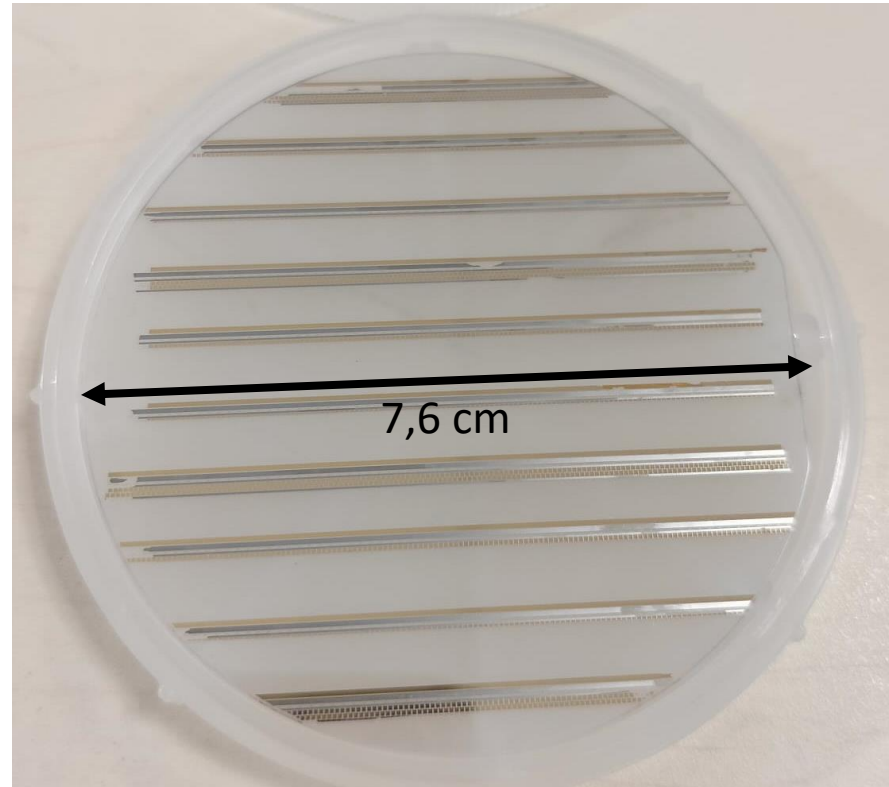
FABRICATION ON 3"

PIN diode



Only 3 fabrication steps:

1. Mesa (litho+plasma etch)
2. N contact (litho+metal dep)
3. P contact (litho + metal dep)



10 ARRAYS ON A SINGLE 3 INCHES WAFER
3 GEOMETRIES

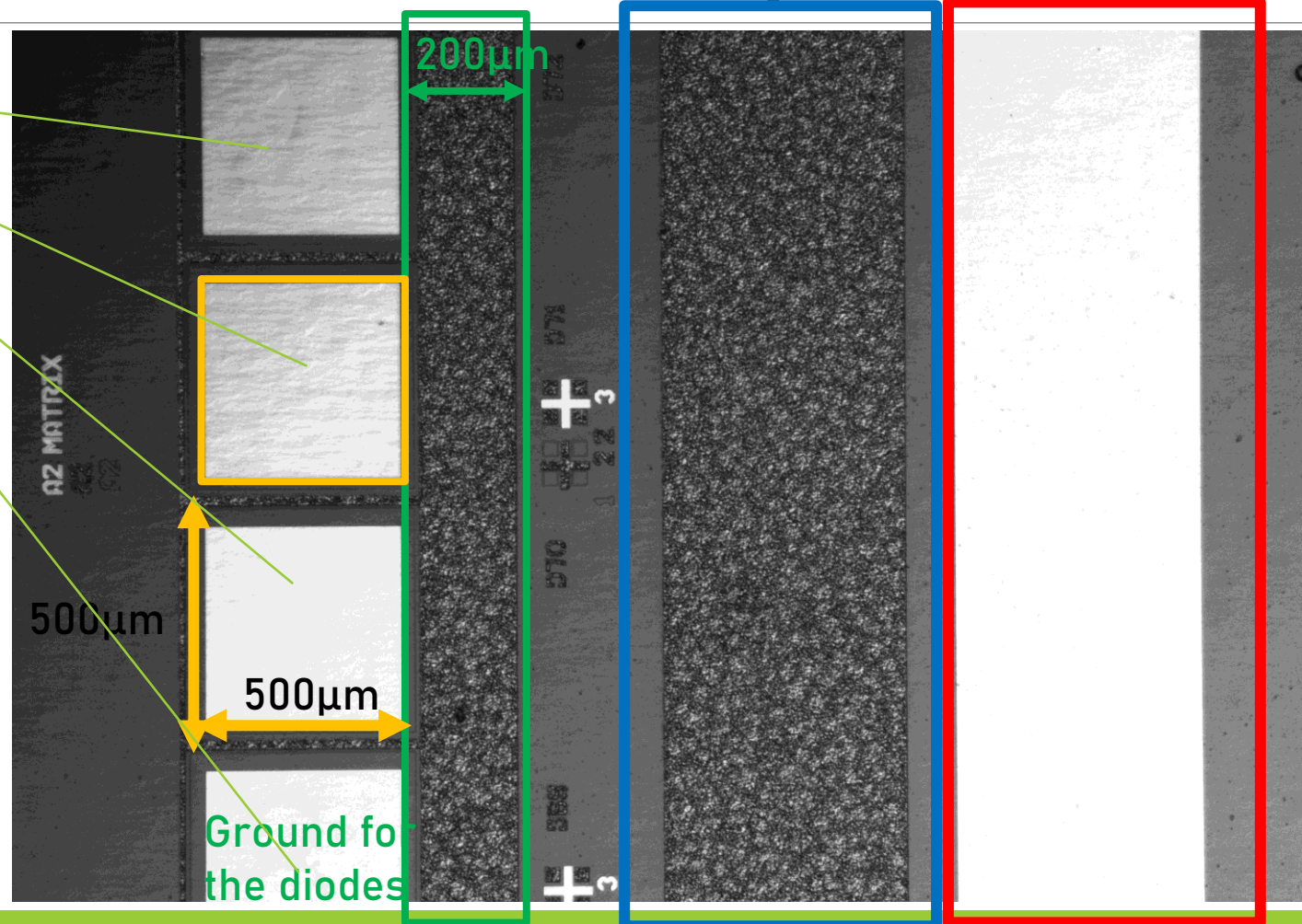


Single line 500x500 μm

P contact line for bonding tests

P contact
of diodes

Period between
diodes : 500 μm



Ideal: to bond
128 consecutive
diodes

Ground line for bonding tests

Double line 500x500μm

P contact line for bonding tests

P contact of diodes

Period between diodes : 500 μm

500 μm

500μm

500 μm

Ground for the diodes

200 μm

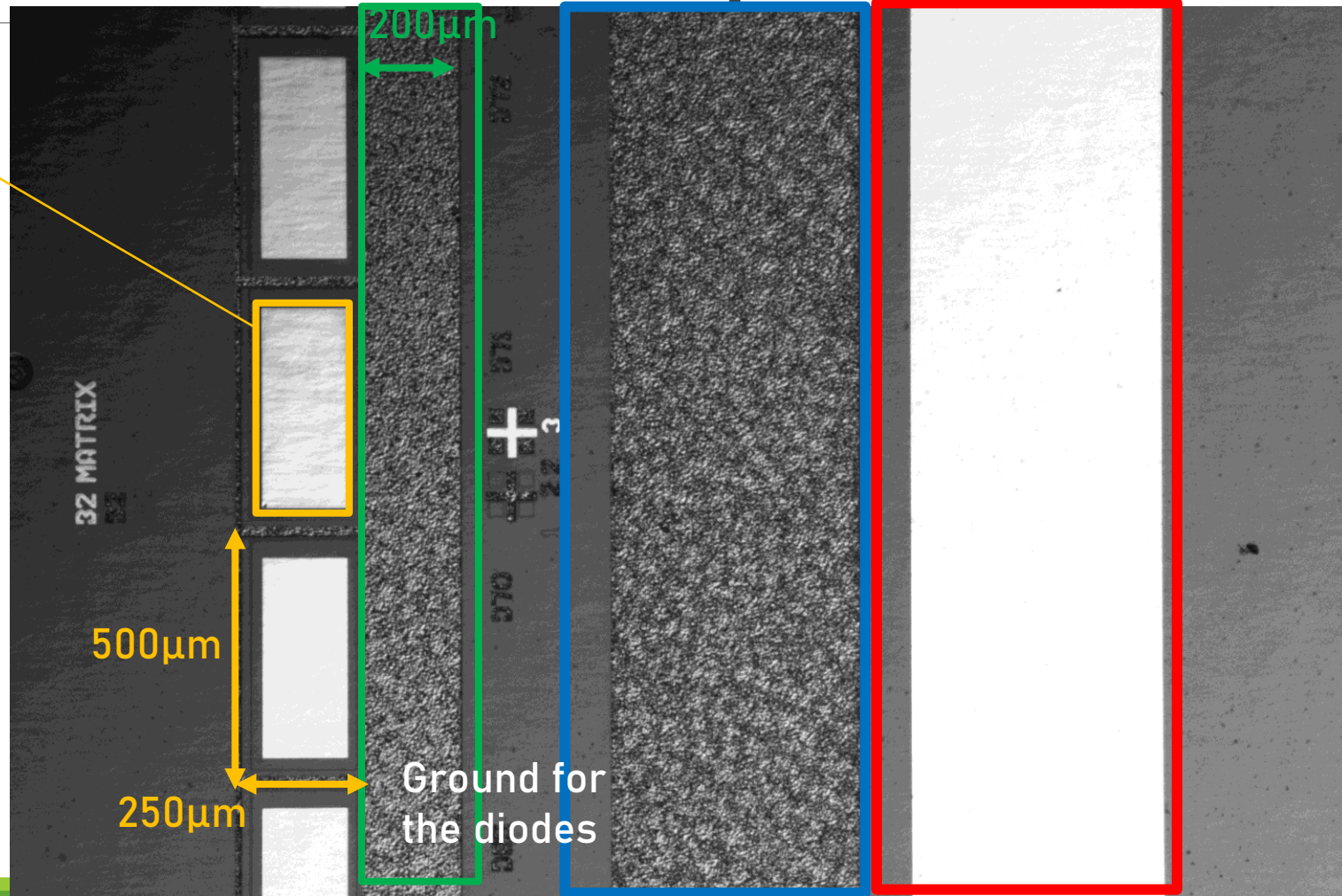
Ground line for bonding tests

**Ideal: to
bond 64
diodes on
the first line
and 64 on
the second**

Single line 250x500 μm

P contact of diodes

Period between diodes : 500 μm

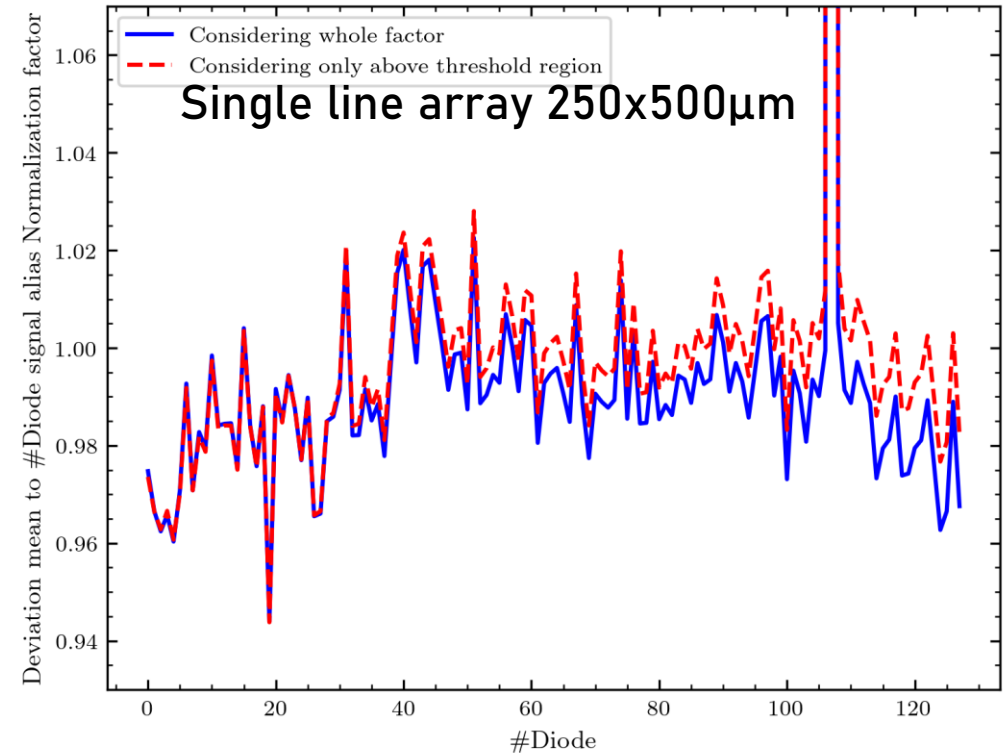
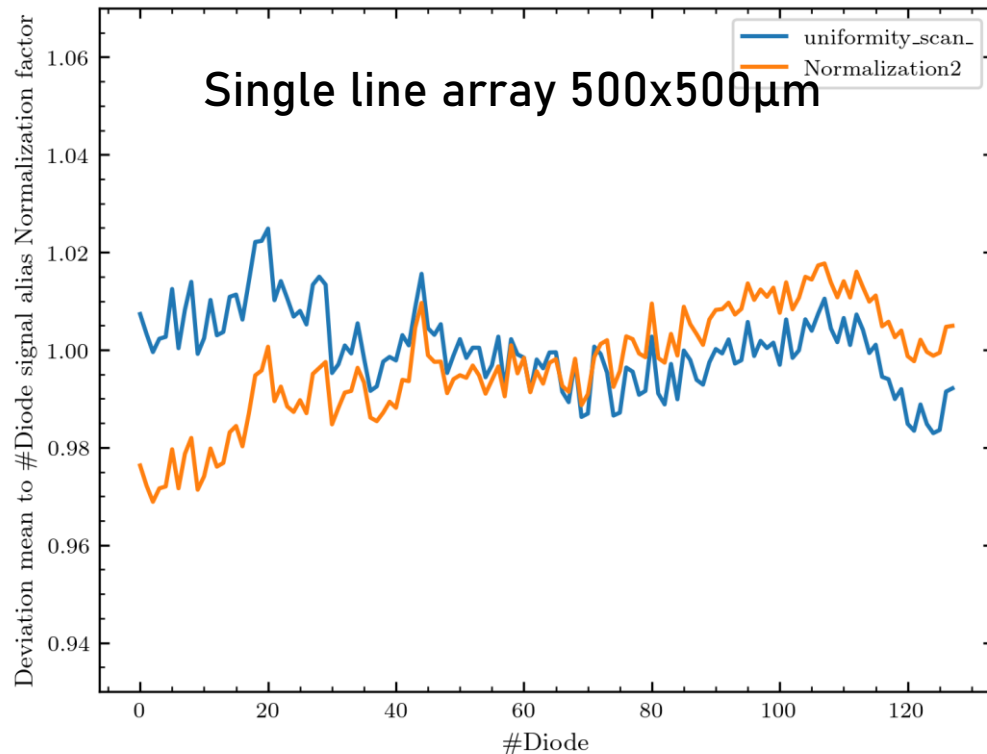
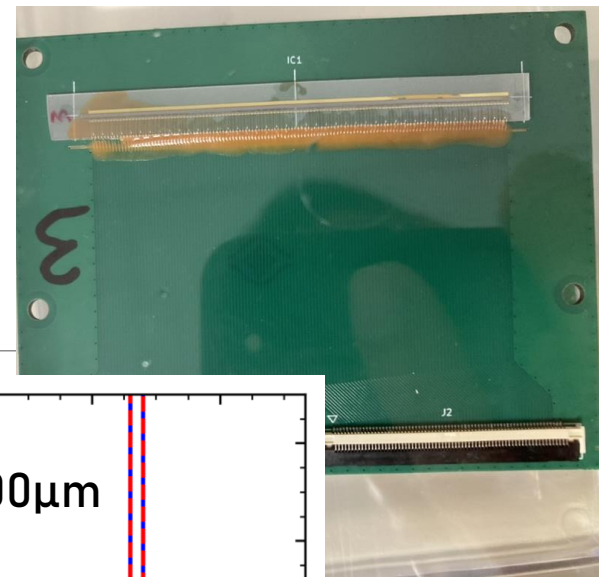


P contact line for bonding tests

Ideal: to bond
128
consecutive
diodes

Ground line for bonding tests

Homogeneity of the response

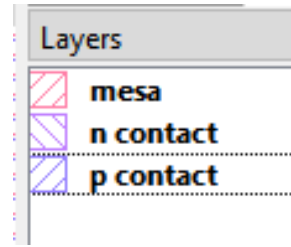


Homogeneity <2 % before normalization 😊

First 2D array mask

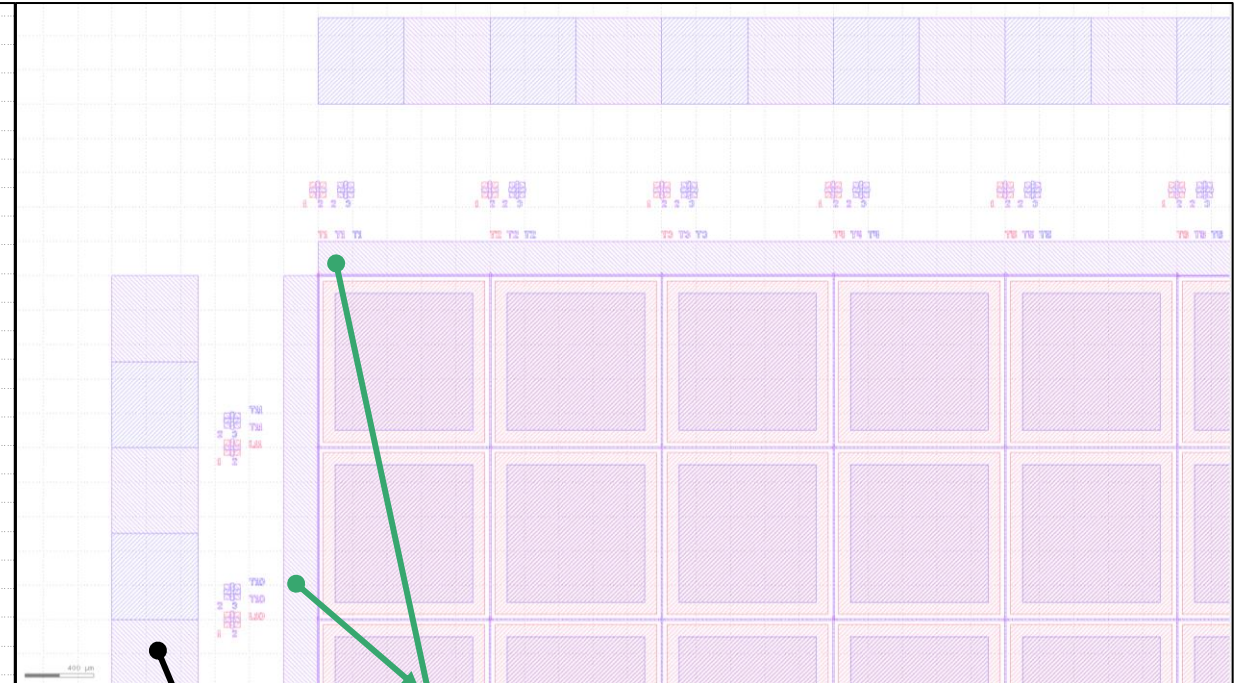
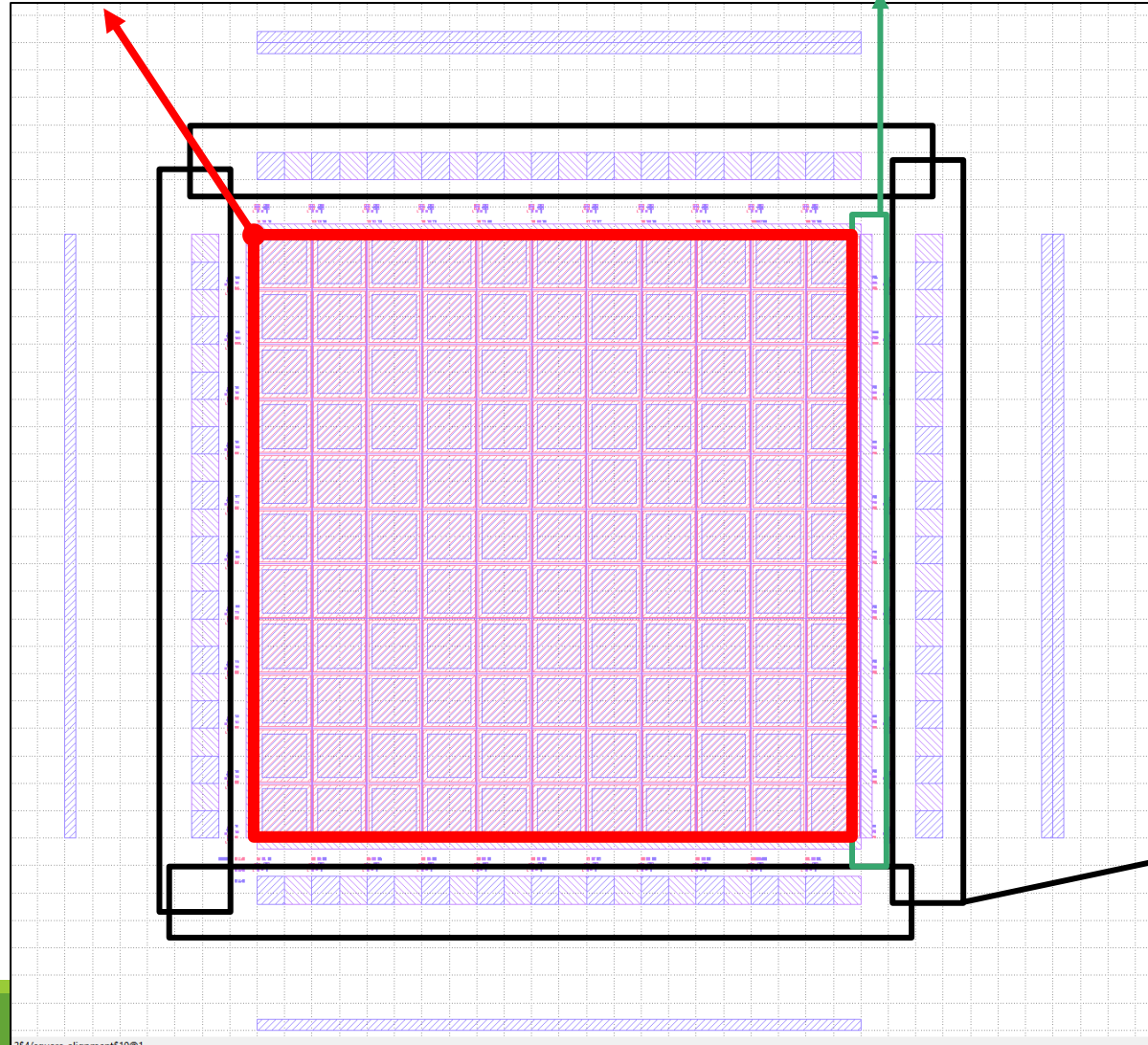
11X11 MATRIX

BECAUSE WE ONLY HAVE 128 CONTACTS ON THE OSRAM CIRCUIT



Matrix of diodes

Ground bar

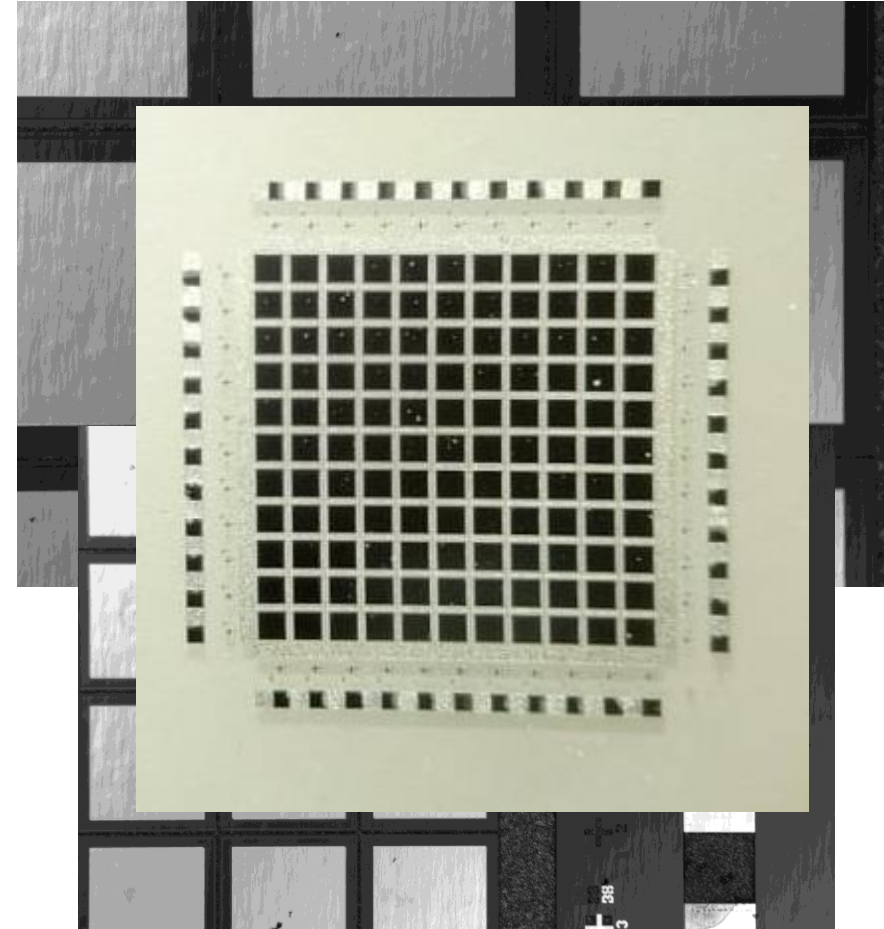
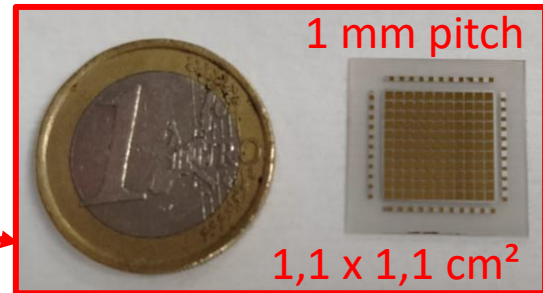
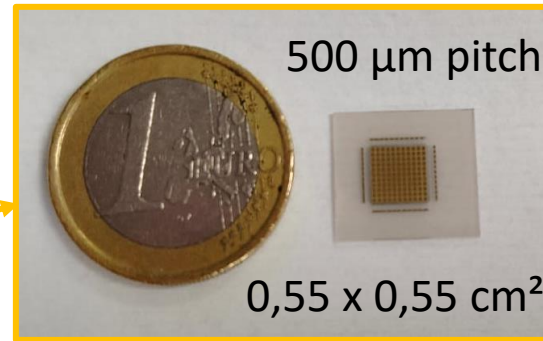
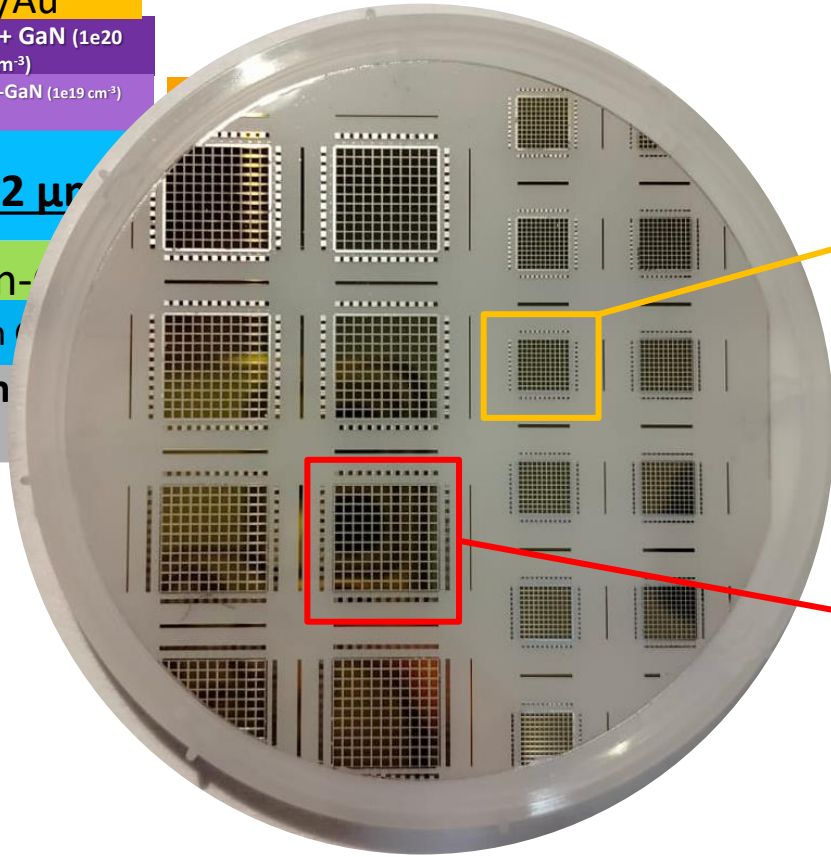


Ground bar (one on each side)
Thickness = 200 μm

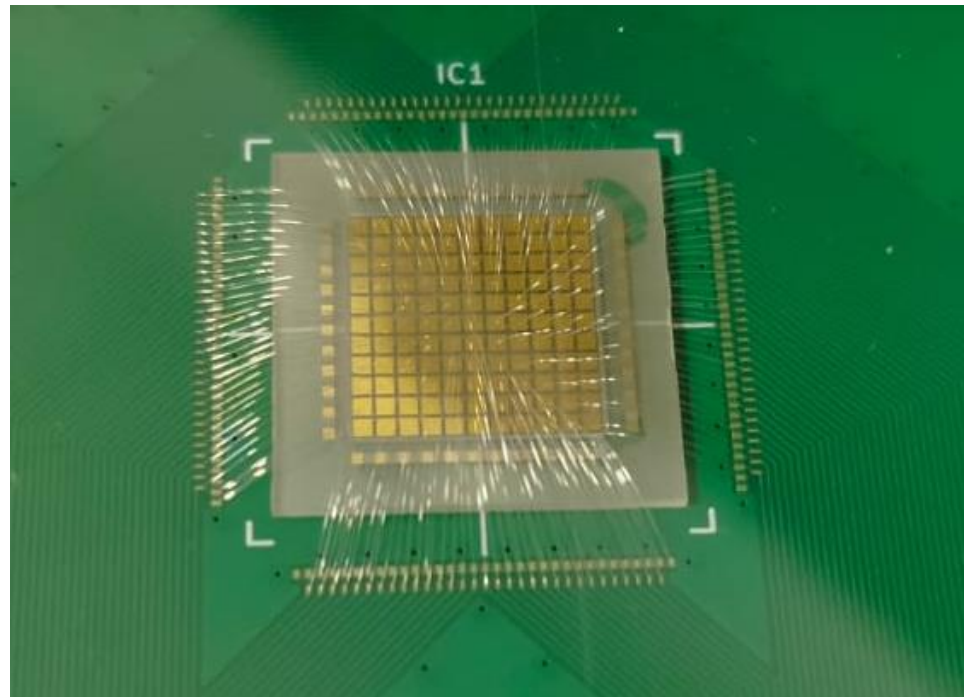
Contact testing pads (one on each side)
500x500 μm
(p contact and ground are alternated, period 500 μm)

Fabrication on 3 inches

Ni/Au
30 nm p++ GaN ($1e20 \text{ cm}^{-3}$)
0,5 μm p-GaN ($1e19 \text{ cm}^{-3}$)
1 / 2 μm
2 μm n-
~ 2 μm /
Sapph

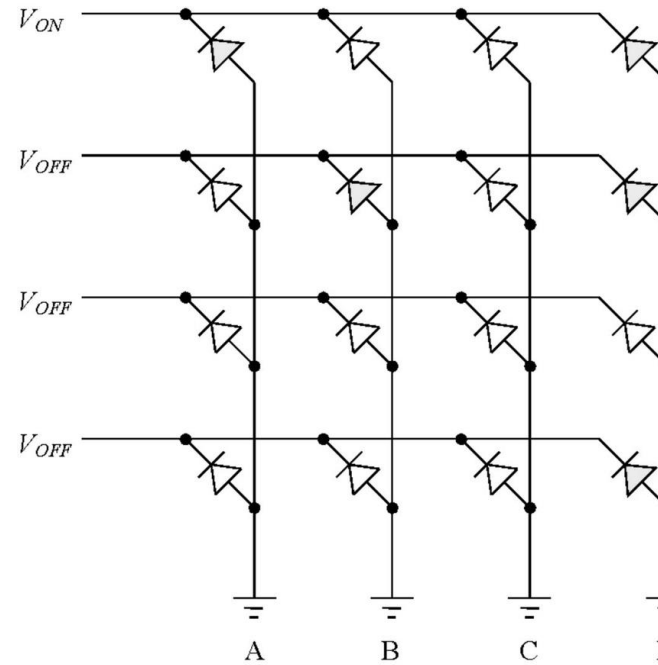
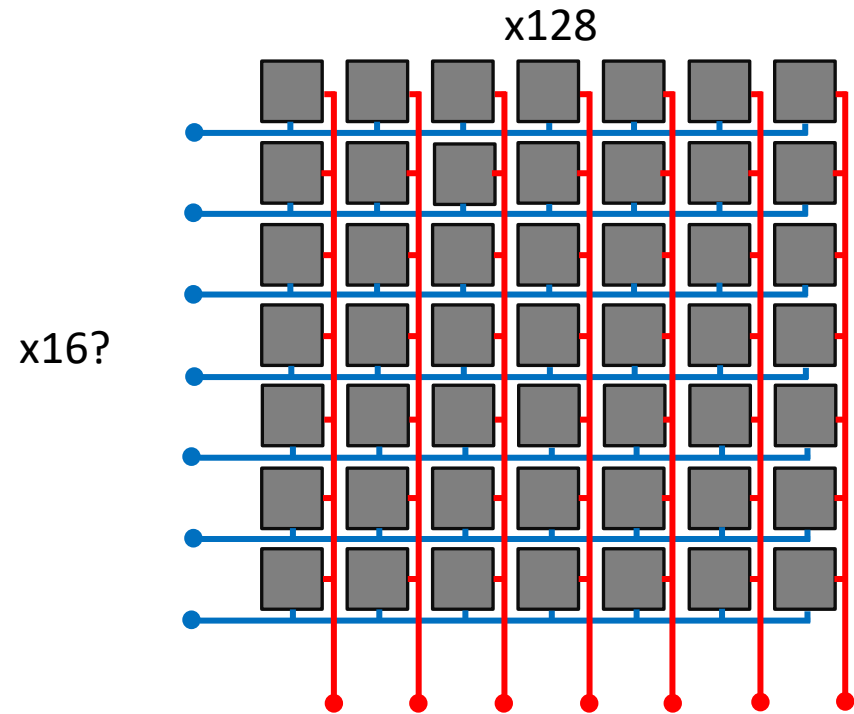


Bonding of 121 diodes

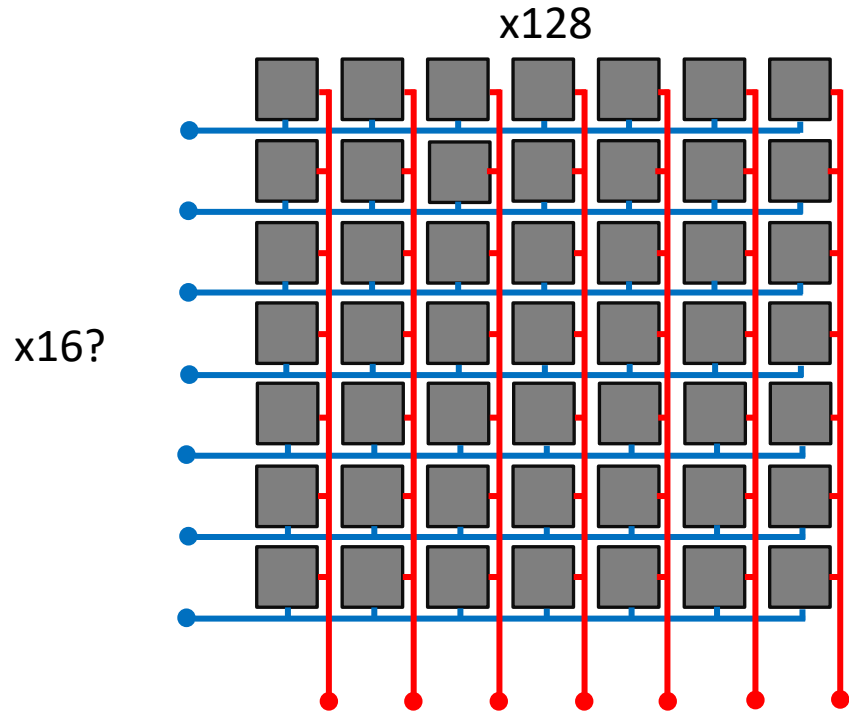


Yield: 1-2 broken diodes or contacts over 121

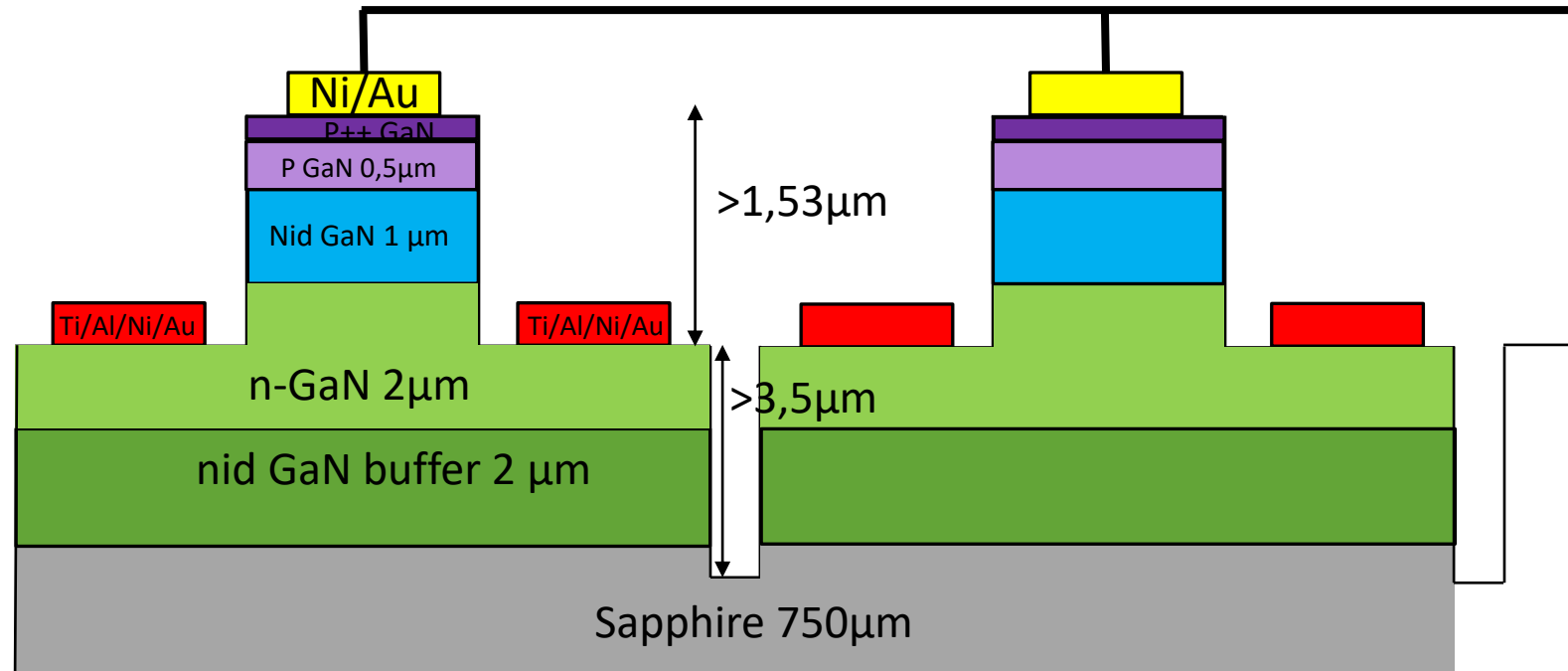
Next: 128xN diodes matrix



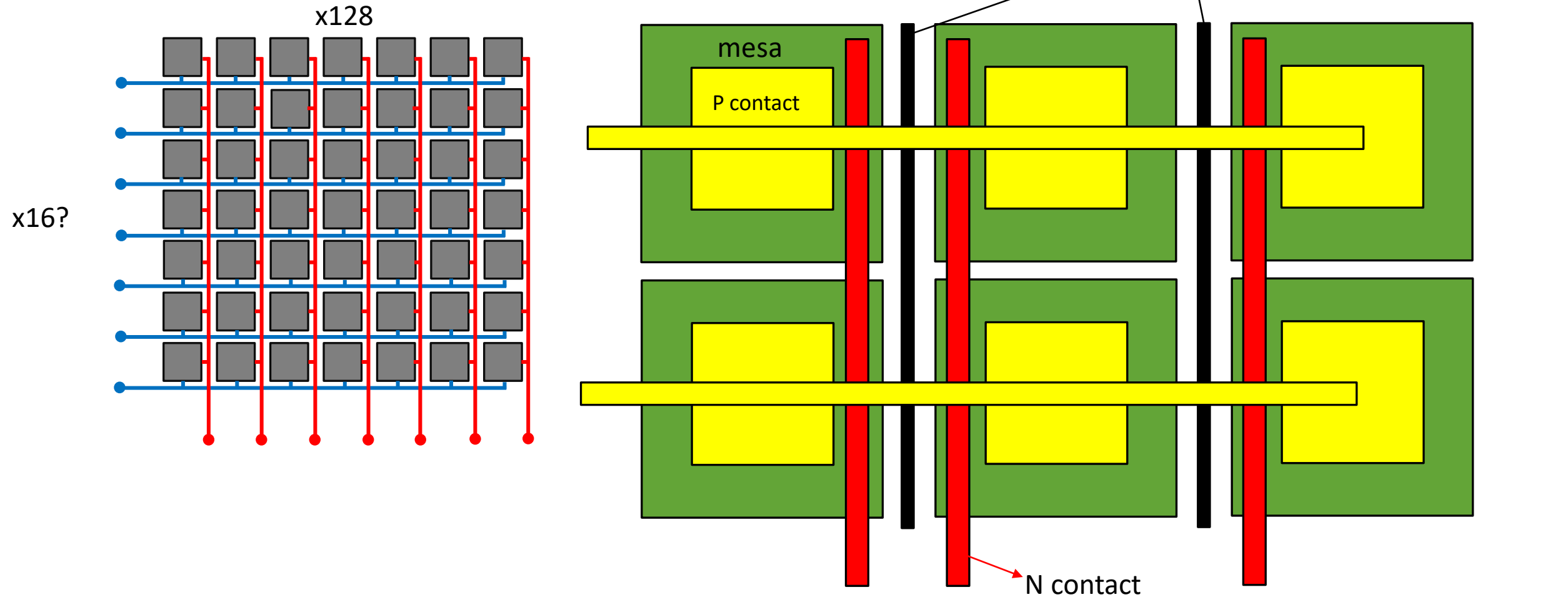
Next: 128xN diodes matrix



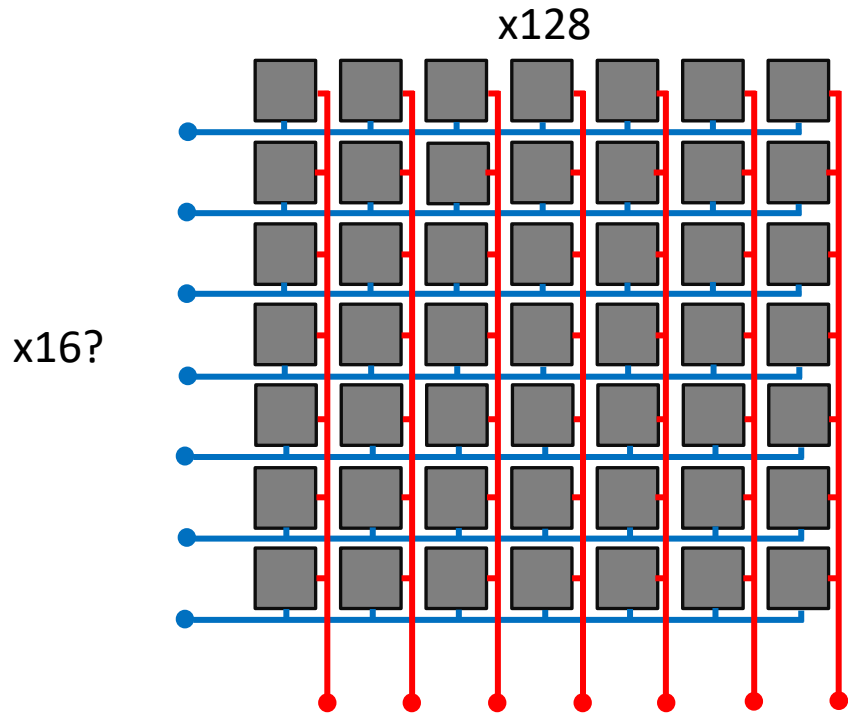
Cross section view:



Next: 128xN diodes matrix



Next: 128xN diodes matrix



For this kind of design we need more fabrication steps:

1. Mesa (litho + etch)
2. N contact (litho + metal deposition)
3. P contact (litho + metal deposition)
4. Deep etching between lines (?) (litho + etch)
5. Insulator coating (SiO₂)
6. Insulator opening (plasma etch)
7. Ni/Au line deposition (red ones)
8. Insulator coating (SiO₂)
9. Insulator opening (plasma etch)
10. Ni/Au line deposition (blue ones)

7-8 lithography masks

(for the last samples I had 3 masks)

Issues:

1. Higher number of photolithography masks (=more steps): lower yield
2. Periodic parasite signal due to gold lines