Design and Analysis of a Three-Phase Three-Level Flying Capacitor

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***Abstract*—This paper presents the design and analysis of a three-phase three-level flying-capacitor inverter (FCI) developed for railway applications requiring operation at non-standard frequencies. The main objective is to design a solution that combines energy efficiency, waveform quality, and thermal reliability, according to the specific requirements of the German railway system. The simulation was carried out using the PLECS software, enabling the implementation of a detailed system model, including power device loss modeling and thermal analysis of the semiconductors.**

***Index Terms*—FCI, PS-SPWM, pole voltage, line to line voltage, phase voltage, phase current, flying capacitors, spectral analysis, THD, efficiency, losses.**

I. Introduction

MODERN railway traction systems require static power converters capable of ensuring high standards of reliability, energy efficiency, and power quality, even under specific operating conditions such as those imposed by the German railway network, which operates at a frequency of $16.7\,\mathrm{Hz}$ [1]. In this context, the choice of inverter architecture and power device technology is crucial.

To meet these requirements, a three-phase three-level FCI topology was adopted. This configuration reduces the voltage stress on individual switching devices, improving efficiency and lowering the total harmonic distortion (THD) of voltage and current waveforms [2]. In combination with this topology, a Phase-Shifted Sinusoidal PWM modulation (PS-SPWM) was implemented. The control technique greatly reduces the oscillation of the voltage and enables natural balancing of the flying capacitor voltages within the FCI. Silicon Carbide (SiC) MOSFETs were selected for their excellent high-frequency switching characteristics, low conduction resistance, and ability to operate at high junction temperatures without compromising reliability. The system was designed to supply a three-phase load of $15\,\mathrm{kW}$, with a line-to-line AC voltage of $400\,\mathrm{V}$, starting from a $1000\,\mathrm{V}$ DC-link. The design process considered an ambient temperature of $40°$, with a maximum junction temperature constraint of $100°$. The power factor was required to fall within the range [0.8, 1], and a value of 0.9 was specifically chosen. In accordance with the provided specifications, only switching and conduction losses in the power devices were considered for efficiency estimation, neglecting losses associated with capacitors and magnetic components. The analyses carried out included the generation and evaluation of the main electrical waveforms, namely pole voltages, phase voltages, line-to-line voltages, phase currents, and voltages across DC-link capacitors. In addition, a spectral analysis of the phase voltage and current was performed to determine harmonic distortion. Moreover, a detailed analysis of the loss distribution among the various power devices was performed. Finally, inverter efficiency was assessed throughout the load range, from $10\,\%$ to $100\,\%$ of nominal power, by plotting the efficiency curve and calculating efficiency values at the four standard load points (4-point efficiency), as well as European efficiency according to relevant standards.

II. Three phase Three Level Flying Capacitor Inverter

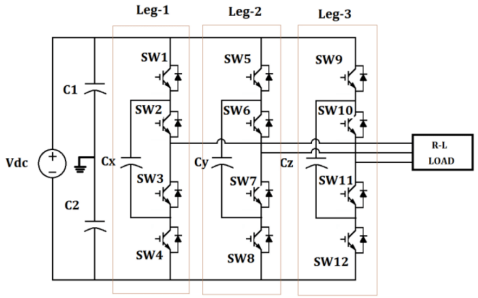

Fig. 1: Topology of Three phase Three level FCI

Multilevel inverters have advantages such as low inductor current harmonics, hence a better approximation of the AC voltage that leads to a easier filtering actions, and reduced voltage stress on power switches for high performance applications compared to conventional two-level designs. In this paper, we explore the use of the FCI in three-phase applications that is shown in Fig. 1.

Four power switching devices are connected in series to form one leg of the inverter. In this topology, the capacitors Cx, Cy, Cz are connected between the series power switching devices, moreover they have no connection to a common DC link and are therefore referred to as *flying capacitors* [5]. Extra capacitors hold controlled direct voltages to provide the additional voltage levels. Changing power switching devices states depending on the specific modulation, the DC-link voltage and the capacitor are connected in different ways. And, pole voltage output can produce three-level.

The mode of the FCI is shown in Table I. The top and bottom switches as well as the two middle ones are complimentary. When SW1 and SW2 are turning-on and other switches are

Active Switches	Mode	Pole Voltage v_{A0}
SW1 ON, SW2 ON	(1)	$+\frac{V_{dc}}{2}$
SW1 ON, SW3 ON	(2)	0
SW2 ON, SW4 ON	(3)	0
SW3 ON, SW4 ON	(4)	$-\frac{V_{dc}}{2}$

TABLE I: Operating Mode

turning-off, pole voltage becomes $\frac{V_{dc}}{2}$. When SW3 and SW4 are tuning on and other switches are turning-off, output voltage becomes $-\frac{V_{dc}}{2}$. In addition, when SW1 and SW3 are tuning on and other switches are turning-off, or SW2 and SW4 are tuning on and other switches are turning off, pole voltage becomes 0. Mode 2 and Mode 3 force the output current pass through the AC terminal to flow through the flying capacitor, hence they are redundant as they produce the same zero-voltage level [7]. However, the current direction is different in the two cases enabling the balance of the capacitor voltage by choosing the appropriate state whenever zero voltage should be imposed. Therefore, the capacitor is charged or discharged according to the output current polarity; if the current has positive polarity, Mode 2 is that the capacitor is charged and Mode 3 is that the capacitor is discharged. If the current has negative polarity, Mode 2 is that the capacitor is discharged and Mode 3 is that the capacitor is charged. In order to obtain three-level output, the voltage of capacitor must be maintained in this process at $\frac{V_{dc}}{2}$.

In order to ensure stable three-level operation and effective voltage balancing of the flying capacitor, a careful selection of circuit parameters was carried out. The inverter operates with a DC-link voltage of $1000\,\mathrm{V}$, which is split across two DC-link capacitors of $100\,\mu\mathrm{F}$ each. These capacitors are sized in order to equally split the **DC-link voltage** as shown in Fig. 2 and minimize ripple under dynamic load conditions.

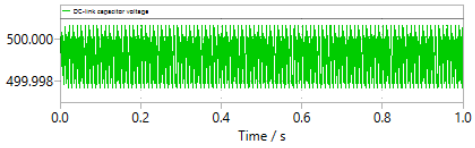

Fig. 2: DC link capacitor voltage

For the flying capacitors, voltage balancing is intrinsically achieved through the current path during zero-voltage switching states (Mode 2 and Mode 3), as previously discussed. In order to guarantee a proper charge/discharge cycle of the flying capacitor without excessive voltage ripple, the value of the flying capacitor was also selected as $100\,\mu\mathrm{F}$. This allows maintaining the capacitor voltage around $\frac{V_{dc}}{2} = 500\,\mathrm{V}$, which is essential to achieve symmetric output levels. The power switches employed in the simulation are SiC MOSFETs, which offer high-speed switching capability and low conduction losses. To reflect realistic device characteristics, an ON-resistance R_{on} of $10\,\mathrm{m}\Omega$ was assigned. This low value reduces conduction losses significantly while preserving the voltage balancing functionality of the inverter. Additionally, a high switching frequency of $20\,\mathrm{kHz}$ was adopted, which is well supported by SiC technology and enables improved output voltage waveform quality with reduced harmonic distortion. This frequency ensures faster response of the flying capacitor voltage, but it also results in increased switching losses, which must be considered in the thermal design phase.

The inverter is connected to a balanced three-phase R–L load, with a total output active power of $15\,\mathrm{kW}$ as shown in Fig. 3.

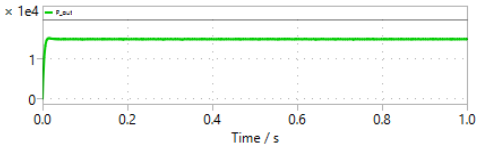

Fig. 3: Output Power

The system operates with a line-to-line RMS voltage of $400\,\mathrm{V}$. A power factor of 0.9 was selected to reflect a realistic operating condition, where part of the power is consumed as reactive power due to the inductive nature of the load. The power factor is shown in Fig. 4, defined as the cosine of the phase angle between voltage and current ($\cos\varphi$), is a measure of how effectively the electrical power is converted into useful mechanical or thermal work. A power factor of 1 indicates that all supplied power is active, whereas a lower value implies the presence of reactive power, which does not perform useful work but contributes to the overall current flow. Maintaining a high power factor is desirable, as it reduces losses, improves voltage regulation, and enhances the efficiency of the power delivery system.

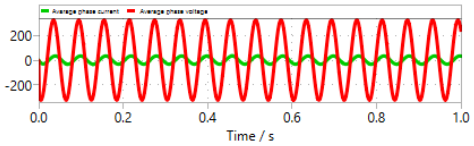

Fig. 4: Power Factor

To determine the appropriate values for the load resistance and inductance, we apply the formulas for balanced three-phase systems. The total active power is given by:

$$P = \sqrt{3} \cdot V_{LL} \cdot I_{\mathrm{ph}} \cdot \cos\varphi \tag{1}$$

Solving for the phase current:

$$I_{\mathrm{ph}} = \frac{P}{\sqrt{3} \cdot V_{LL} \cdot \cos\varphi} = \frac{15\,000}{\sqrt{3} \cdot 400 \cdot 0.9} \approx 24.06\,\mathrm{A} \tag{2}$$

The corresponding phase voltage is calculated as:

$$V_{\mathrm{ph}} = \frac{V_{LL}}{\sqrt{3}} \approx 230.94\,\mathrm{V} \tag{3}$$

From this, the impedance per phase becomes:

$$Z_{\mathrm{ph}} = \frac{V_{\mathrm{ph}}}{I_{\mathrm{ph}}} \approx 9.60\,\Omega \tag{4}$$

Given the power factor, we compute the impedance angle:

$$\varphi = \cos^{-1}(0.9) \approx 28.71^\circ \tag{5}$$

The resistance and inductive reactance per phase are then calculated as:

$$R = Z_{\text{ph}} \cdot \cos\varphi \approx 8.65\,\Omega \tag{6}$$

$$X_L = Z_{\text{ph}} \cdot \sin\varphi \approx 4.17\,\Omega \tag{7}$$

The corresponding inductance, based on a fundamental frequency of 16.7 Hz, is:

$$L = \frac{X_L}{2\pi f} = \frac{4.17}{2\pi \cdot 16.7} \approx 39.7\,\text{mH} \tag{8}$$

These values define the equivalent R–L load that the inverter must supply. They represent a realistic load condition for our application context, namely a German railway traction system.

III. Phase-Shift Sinusoidal PWM

To control the switching of the FCI, a *Phase-Shifted Sinusoidal Pulse Width Modulation* technique is adopted, as specified for this application. This strategy is particularly effective in multilevel inverters, where it contributes to harmonic reduction, improved waveform quality, and capacitor voltage balancing.

In the PS-SPWM scheme used here, the switching signals are generated by comparing a set of sinusoidal modulating waveforms, one for each phase, with two triangular carrier waveforms. These carriers have the same amplitude and frequency but are horizontally phase-shifted with respect to each other (180°) as shown in Fig. 5. Furthermore, with this modulation technique the switches commutate over the whole fundamental period and consequently we would have higher switching losses with respect to Level-Shift phase disposition PWM (LS-PD PWM) [7].

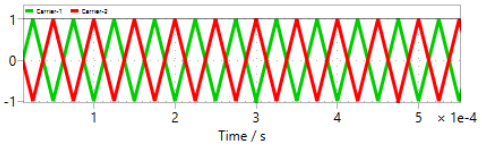

Fig. 5: Phase-shifted carriers

Each modulating waveform corresponds to a desired phase voltage (A, B, and C), and they are phase-shifted by 120° to represent a balanced three-phase system as shown in Fig. 6.

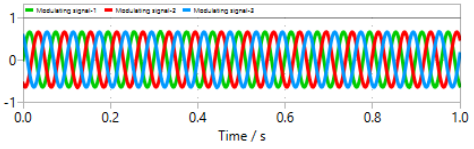

Fig. 6: Modulating signals

For this application, the fundamental frequency of the sinusoidal modulating waveforms is set to 16.7 Hz. The triangular carriers, on the other hand, operate at a frequency of 20 kHz, which is suitable given the high-speed switching capability of the SiC MOSFETs used.

The comparison between the sinusoidal references and the phase-shifted carriers produces PWM signals as shown in Fig. 7 that directly control the gate of each switch in the inverter.

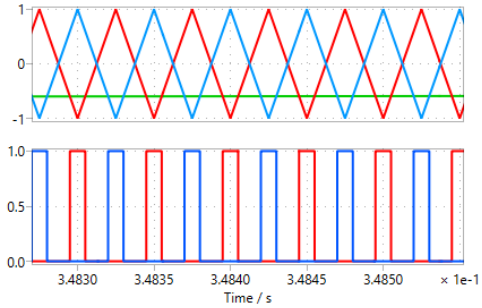

Fig. 7: Gate signals

At each instant, the sinusoidal reference (modulating signal) is compared with the phase-shifted triangular carrier waveforms. When the reference is greater than the carrier, a logic high signal is generated, turning on the corresponding MOSFETs and allowing current to flow through the selected path. Instead, when the reference is lower than the carrier, a logic low signal is produced, turning off the corresponding switches. This comparison process generates a sequence of gate pulses that control the switches' operation. This process results in a staircase-like output voltage that approximates the desired AC waveform [3].

A key parameter in this modulation scheme is the *modulation index* m, defined as follows:

$$m = \frac{V_{\text{phase, peak}}}{V_{dc}/2} = 0.654 \tag{9}$$

This expression indicates that the peak value of the desired phase voltage is normalized with respect to half of the DC-link voltage. Maintaining the modulation index within the linear region ensures correct operation and avoids waveform distortion due to overmodulation.

The modulation index m directly influences the THD of the inverter's output voltage. In general, when operating within the *linear modulation region* ($0 < m < 1$), increasing m leads to a higher amplitude of the fundamental component and a reduction in harmonic content. This results in improved waveform quality and lower THD, as the available DC-link voltage is more effectively utilized.

At very low values of m, the output waveform contains a relatively weak fundamental and is dominated by switching harmonics, leading to high THD. As m approaches unity, THD decreases, reaching its minimum just before the transition into overmodulation. Beyond $m = 1$, however, the inverter operates in the *overmodulation region*, where the sinusoidal reference waveform exceeds the bounds of the carrier signal, causing it to be clipped during the portions of the cycle where the reference surpasses the carrier limits. This results in a distorted output waveform and a loss of linearity between the

modulation index and the output voltage amplitude. Although the amplitude of the fundamental component may increase slightly, the output waveform includes increased low-order harmonic distortion, which can adversely affect the power quality and the operation of connected loads [4].

In our case, the chosen modulation index is $m = 0.654$, which lies well within the linear region. This value provides a good compromise between output voltage amplitude and waveform generation. It is important to note that, since no output filter has been applied, the **phase voltage** waveform exhibits a relatively high **THD**. However, due to the R-L nature of the load, the resulting **phase current** maintains a low **THD**, see the Fig. 8. This ensures suitable current quality for the application, even in the absence of dedicated output filtering.

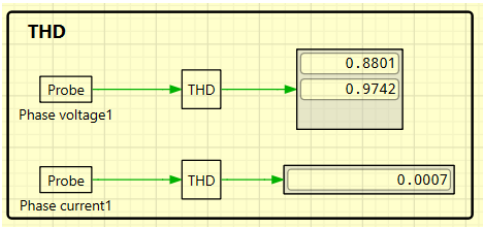

Fig. 8: Phase Voltage and Phase Current THDs

The effectiveness of the implemented PS-SPWM strategy can be clearly observed through the waveforms obtained from the simulation. The following figures illustrate the inverter's electrical waveforms behaviors.

Fig. 9 shows the **pole voltages**, that exhibits three distinct levels: $-\frac{V_{dc}}{2}$,0, and $\frac{V_{dc}}{2}$. The red line represent the average voltages.

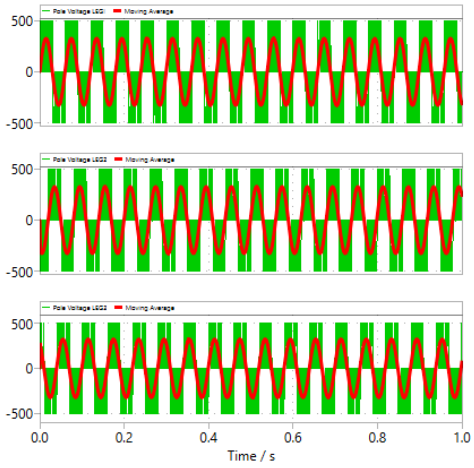

Fig. 9: Pole Voltages

Fig. 10 shows the **line-to-line voltages**, that presents five levels: $-V_{dc}$, $-\frac{V_{dc}}{2}$, 0, $\frac{V_{dc}}{2}$, and V_{dc}. The peak value is 565 V.

Fig. 11 shows the **phase voltage**, which have seven discrete levels: $-\frac{2}{3}V_{dc}$, $-\frac{1}{2}V_{dc}$, $-\frac{1}{3}V_{dc}$, 0, $\frac{1}{3}V_{dc}$, $\frac{1}{2}V_{dc}$, and $\frac{2}{3}V_{dc}$. The peak value is 327 V.

Finally, Fig. 12 illustrates the **phase current**. The current reaches a peak amplitude of about 33.7 A.

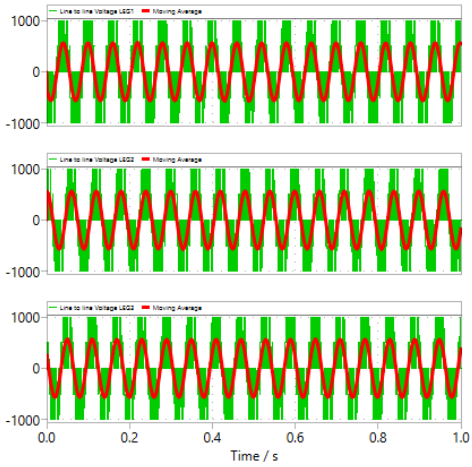

Fig. 10: Line-to-line voltages

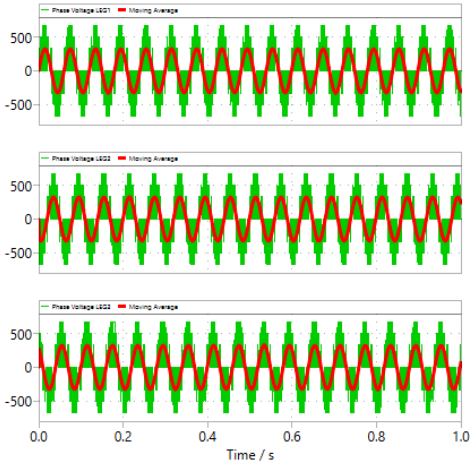

Fig. 11: Phase voltages

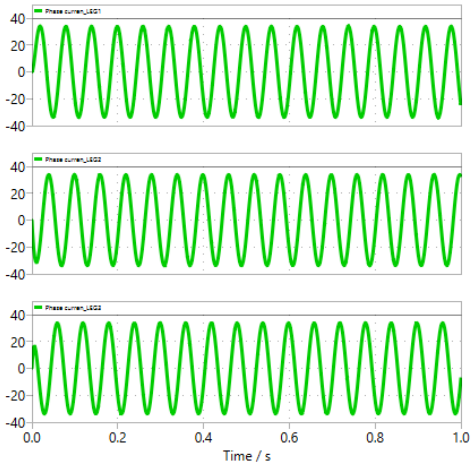

Fig. 12: Phase current

Now, lets move on to the *spectral analysis* that is a fundamental tool in power electronics for evaluating waveform quality in the frequency domain. It allows to visualize how a periodic signal spreads across different frequencies, making it possible to detect and quantify harmonic distortion introduced by switching operations, nonlinearities, or control strategies.

In systems using sinusoidal PWM, particularly with a high switching frequency, the spectral content of the output signal is composed of the fundamental frequency and a series of harmonics, mainly centered around the switching frequency and its multiples. Generally, we expect the largest peak at the fundamental frequency (in our case, 16.7 Hz), followed by smaller harmonic components at integer multiples of the switching frequency such as 20 KHz, 40 kHz, 60 kHz, etc.

However, in our system, we apply PS-SPWM using two triangular carriers of identical frequency (20 KHz) and amplitude, but with a horizontal phase shift between them. This introduces a specific symmetry, known as *half-wave symmetry*, in the generated PWM signals. As a result of this symmetry, the odd harmonics of the carrier frequency cancel out, and the spectrum contains only the even harmonics of the switching frequency [8].

This behavior is clearly observed in the **phase voltage spectrum**, where the fundamental peak appears at 16.7 Hz, as shown in Fig. 13, but subsequent peaks are found not at 20 kHz, 60 kHz, or 100 kHz, but rather at 40 kHz, 80 kHz, 120 kHz, and so on, at the even multiples of the carrier frequency, see the Fig. 14

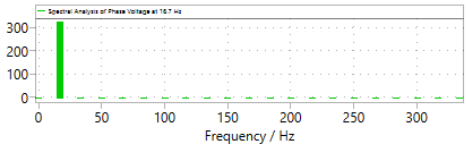

Fig. 13: Phase voltage spectrum at fundamental frequency

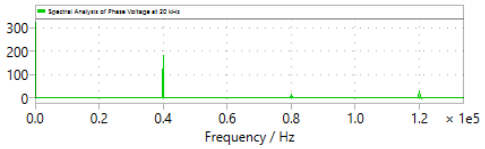

Fig. 14: Phase voltage spectrum at switching frequency and its multiples

This phenomenon is advantageous from a filtering standpoint. Since the dominant high-frequency harmonics are further away from the fundamental frequency, they are easier to suppress with smaller or less complex filters.

In contrast, the **phase current spectrum** appears much cleaner. The R-L nature of the load acts as a natural low-pass filter, significantly attenuating the high-frequency components present in the voltage. As a result, the current waveform remains almost purely sinusoidal, dominated by the 16.7 Hz fundamental as shown in Fig. 15 and Fig. 16, and exhibits very low harmonic distortion.

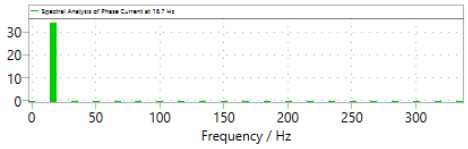

Fig. 15: Phase current spectrum at fundamental frequency

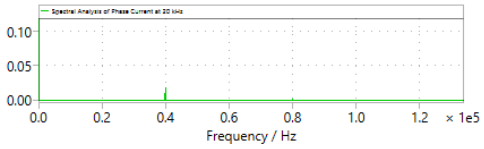

Fig. 16: Phase current spectrum at switching frequency and its multiples

In summary, the spectral analysis confirms the effectiveness of the PS-SPWM strategy.

IV. Thermal Design

The power switch selected for this application is the Hitachi Energy (ABB) 5SFG 0780B12000x_Rth66lmin45C_MOSFET, a 1200 V SiC-based device with high current capability and excellent thermal characteristics. The corresponding antiparallel diode (5SFG 0780B12000x_Rth66lmin45C_BodyDiode) is also used to support reverse conduction.

From a thermal perspective, the heat generated inside the MOSFET (due to conduction and switching losses) follows a path from the junction to the surrounding environment. This thermal path includes multiple stages: junction-to-case, case-to-heatsink, and heatsink-to-ambient. The junction-to-case resistance is already included in the device specification. The rest of the thermal path can be modeled using a simplified Cauer thermal network, where each physical interface is represented as a thermal resistance and a thermal capacitance [6]. This approach helps estimate the junction temperature over time.

According to the application constraints, the system must operate in an ambient temperature of $40°$, while ensuring that the junction temperature of the device does not exceed $100°$. Thanks to the SiC technology, the chosen MOSFET maintains a moderate temperature rise. This allows for relatively simple cooling solutions and provides a comfortable safety margin.

The phase current RMS value is approximately 24 A, with a peak current reaching about 33 A. Considering this, the chosen MOSFET module is still somewhat oversized relative to the operating current, but this is a deliberate and justifiable design choice. The conservative sizing ensures improved thermal headroom and enhanced reliability.

It is important to note that the thermal simulation of the **junction temperature** typically requires a long transient period to reach steady state, where the temperature stabilizes and no longer increases. In our case, the simulation results show a continuous temperature rise over the simulated time window, see the Fig. 17, making it challenging to precisely determine the final steady-state junction temperature. However, this does

not imply that the temperature will increase indefinitely in real operation; rather, it reflects the fact that the simulation has not yet reached thermal equilibrium. Given the conservative design margins of the selected MOSFET and the relatively low current levels compared to its rating, it is reasonable to expect that the junction temperature will remain within safe limits in actual operation. Therefore, despite the ongoing temperature increase observed in the simulation, the system is not expected to encounter thermal issues under the specified conditions.

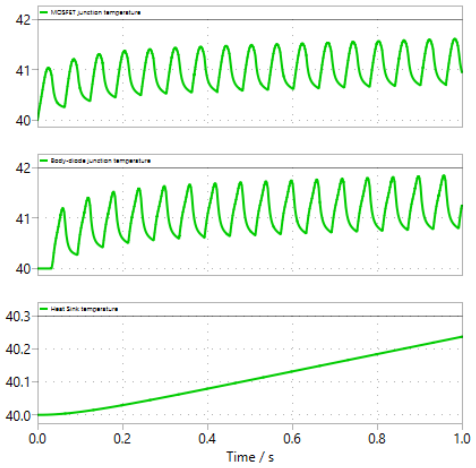

Fig. 17: Mosfet, Body-diode and Heatsink temeprature behaviours

In a static power conversion system such as the FCI considered, power losses are the primary source of heat that must be dissipated to maintain the devices within their safe thermal operating range. The **total losses** can be mainly divided into conduction losses and switching losses.

Conduction losses occur when the power devices, such as MOSFETs and diodes, are in the ON state and are conducting current. These losses depend on the on-state resistance R_{on}, the RMS value of the current, and the duty cycle, since a higher conduction time leads to greater energy dissipation. Essentially, the longer a device stays ON, the more Joule losses it accumulates.

Switching losses, on the other hand, take place during the ON-OFF transitions and are determined by the energy lost in each switching event. These losses are strongly influenced by the switching frequency, the voltage across the device, the current at the moment of switching, the speed of the transition and the dynamic characteristic of the device. In our case, the switching frequency is $20\,\mathrm{kHz}$, a relatively high value that improves waveform quality but significantly increases dynamic losses due to the large number of switching events per second.

From our simulation, the total conduction losses are approximately $110\,\mathrm{W}$, while the switching losses reach about $270\,\mathrm{W}$. This balance reflects the operational characteristics of our system: a low phase RMS current results in moderate conduction losses, particularly due to the low R_{on} of the selected SiC MOSFETs. However, the high switching frequency substantially contributes to the total power dissipation, making switching losses the dominant component.

The total losses generated by all active components of the inverter (12 MOSFETs and 12 diodes) define the thermal power that must be effectively dissipated through appropriate thermal design. These losses have been monitored throughout the simulation as it's represented in the Fig. 18. Therefore, efficient loss management not only improves overall efficiency but also ensures reliability and longevity of the system.

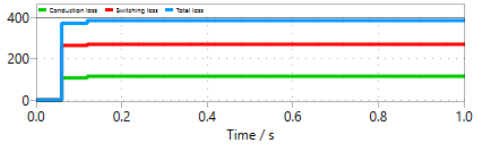

Fig. 18: Conduction, switching and Total losses

V. Efficiency Analysis and Results

The efficiency of a power conversion system is a key performance indicator, reflecting how effectively the converter transforms input electrical energy into usable output power. It is defined as the ratio between the output power and the total input power, where the input power includes the output power and the total losses in the system:

$$\eta = \frac{P_{\text{out}}}{P_{\text{out}} + P_{\text{loss}}} = 97.45 \tag{10}$$

In this study, only conduction and switching losses have been considered in the computation of total losses. These losses have been computed over the entire operating range, from 0% to 100% of the rated output power ($15\,\mathrm{kW}$), and the efficiency has been calculated accordingly.

Below is the Table II summarizing the performance data used to build the **efficiency curve** of the inverter system:

(%)	P(W)	i(A)	$Z(\Omega)$	$R(\Omega)$	L(mH)	Eff(%)
0	0	0.00	0.00	0.00	0.0	0.00
5	750	1.20	192.20	173.00	795.2	74.64
10	1500	2.40	96.10	86.50	397.6	86.60
20	3000	4.81	48.03	43.26	198.8	92.65
25	3750	6.01	38.42	34.60	159.0	93.86
30	4500	7.21	32.04	28.84	132.5	94.67
40	6000	9.62	24.01	21.63	99.4	95.68
50	7500	12.02	19.22	17.30	79.5	96.28
60	9000	14.42	16.02	14.42	66.3	96.67
70	10500	16.83	13.73	12.35	56.7	96.96
75	11250	18.03	12.81	11.53	52.9	97.07
80	12000	19.23	12.01	10.79	49.7	97.16
90	13500	21.63	10.68	9.61	44.2	97.32
100	15000	24.06	9.60	8.65	39.7	97.45

TABLE II: Efficiency measurements at different load levels

From this data, the efficiency curve demonstrates a rapid increase at low loads and gradual stabilization beyond 50% load. The maximum efficiency achieved is approximately 97.45% at full load, see the Fig. 19.

To further characterize the inverter performance under realistic usage profiles, two widely accepted metrics have been calculated:

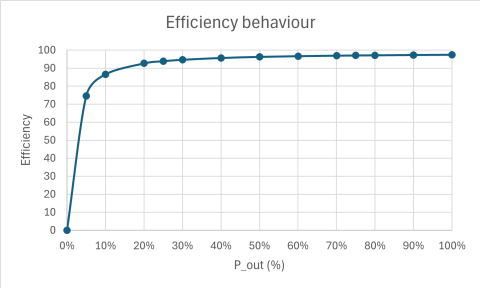

Fig. 19: Efficiency curve from 10% to 100% of the rated power

Four Point Efficiency

The **Four Point Efficiency** evaluates the inverter efficiency at 25%, 50%, 75%, and 100% of the rated power, assuming equal weight for each point. It provides a balanced view across a typical operational range.

$$\eta_{4p} = \frac{1}{4}(\eta_{25\%} + \eta_{50\%} + \eta_{75\%} + \eta_{100\%}) = 96.17\% \quad (11)$$

European Efficiency

The **European Efficiency** is an averaged operating efficiency over a yearly power distribution corresponding to middle-Europe climate [6]. The value of this weighted efficiency is obtained by assigning a percentage of time the inverter resides in a given operating range. It is calculated as:

$$\begin{aligned}\eta_{\text{European}} &= 0.03 \cdot \eta_{5\%} + 0.06 \cdot \eta_{10\%} + 0.13 \cdot \eta_{20\%} \\ &\quad + 0.10 \cdot \eta_{30\%} + 0.48 \cdot \eta_{50\%} + 0.20 \cdot \eta_{100\%} \\ &= 94.80\% \end{aligned} \quad (12)$$

These two efficiency values offer insights into inverter behavior under various load conditions, helping validate the design under different operating scenarios.

In conclusion, the inverter design meets the project's performance expectations, delivering high efficiency across a wide load range. The inclusion of SiC MOSFETs, careful thermal considerations, and optimized modulation contribute to the excellent energy conversion performance, making this solution well-suited for German railway traction applications.

VI. Zip File Attachment

The attached ZIP file contains the project materials related to the PLECS simulation. This includes simulation models, plots, and supporting documentation.

References

[1] UIC, *Energy efficiency technologies for railways*, International Union of Railways, 2015.

[2] P. Ladoux, "Flying capacitor multilevel inverters and their applications," *IEEE Transactions on Industrial Electronics*, vol. 49, no. 4, pp. 764–774, 2002.

[3] H. Akagi, "Classification, Terminology, and Application of the Modular Multilevel Converter (MMC)," *IEEE Transactions on Power Electronics*, 2017.

[4] M. Vancini *et al.*, "Carrier-Based PWM Overmodulation Strategies for Five-Phase Inverters," *IEEE Transactions on Power Electronics*, 2020. Definisce chiaramente le regioni "linear", "extended linear" e "overmodulation", con esempi specifici per inverter a cinque fasi.

[5] Y.-L. Syu, Z. Liao, P. Assem, D. Chou and R. C. N. Pilawa-Podgurski, "Phase-Shifted PWM with Dynamic Phase Shift Control and Zero Sequence Injection to Minimize Inductor Current Ripple in Three-Phase Flying Capacitor Multilevel Converters," in *2020 IEEE 21st Workshop on Control and Modeling for Power Electronics (COMPEL)*, Aalborg, Denmark, 2020, pp. 1–7. doi: 10.1109/COMPEL49091.2020.9265783.

[6] R. Mandrioli, *Conduction, commutation and losses*, slides del corso Power Electronic Circuits M, Unibo.

[7] M. Ricco, *Three phase inverter, Multilevel inverter*, slides del corso Power Electronic Circuits M, Unibo.

[8] P.G. Abdul Rahiman Beig etal., *Space vector based synchronized PWM algorithm for three level voltage source inverters*, IECON 2002