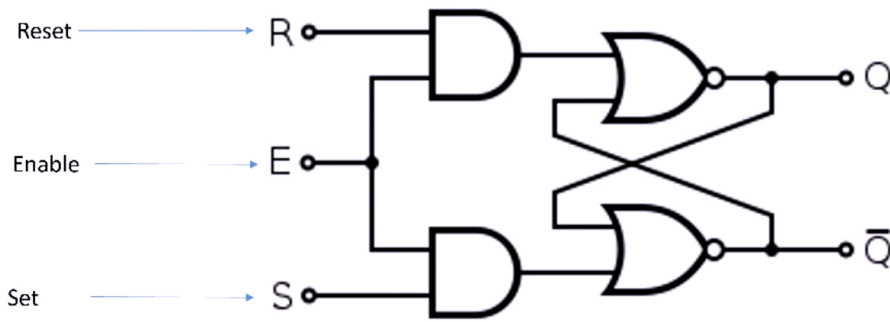


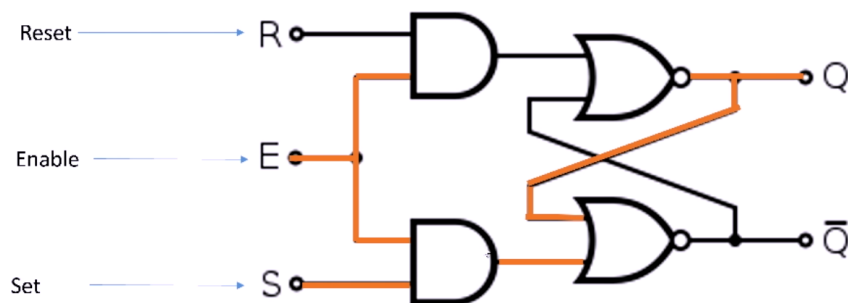
Motivation

- [[Combinational Circuits]] are not capable of storing data
 - changes to input lead to change at output
- storage by creating a feedback loop

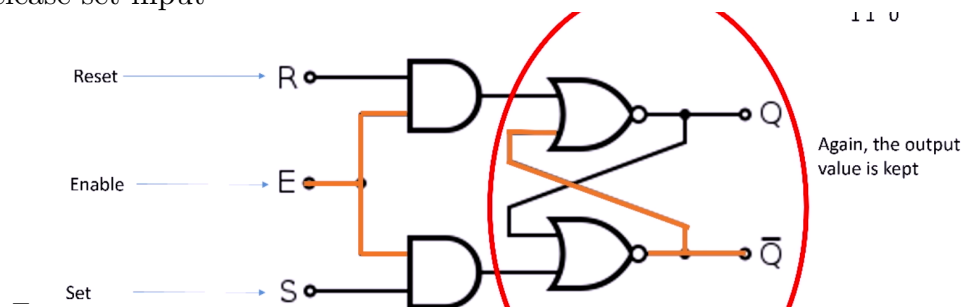
Set-Reset Latch - NOR Version



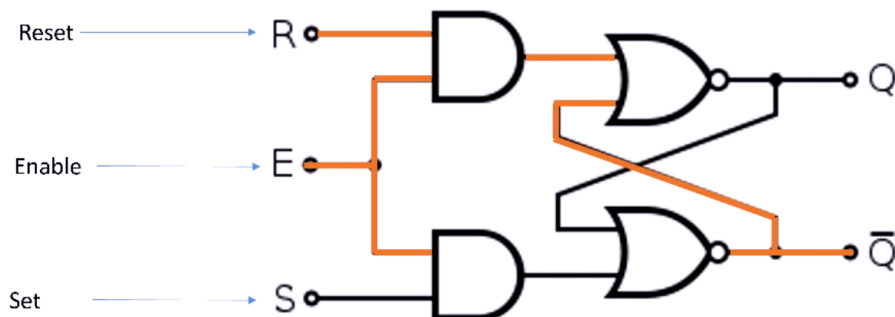
-
- set



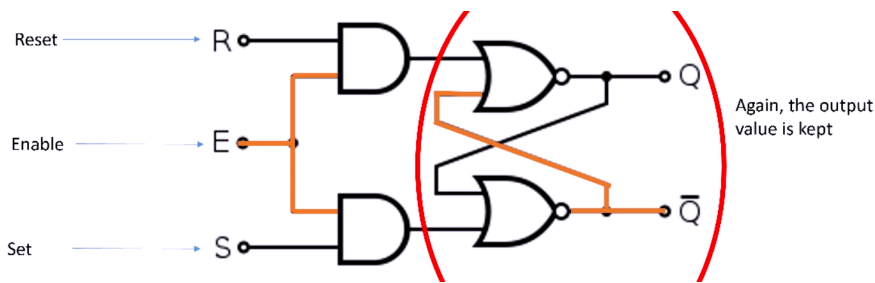
- release set input



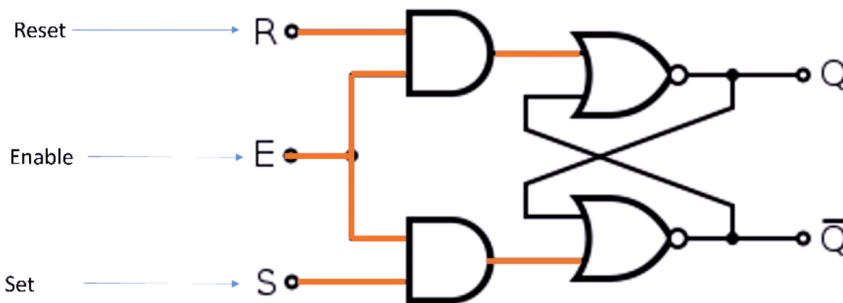
- reset



- release reset



- illegal action



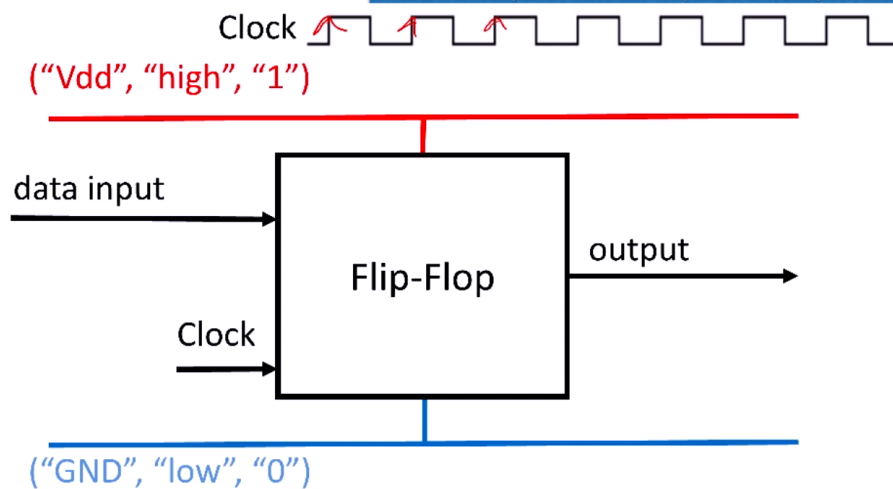
(A)synchronous circuits

- synchronous circuits with global clock signal
 - most commonly used
 - no latches as storage
 - instead uses flip-flops or registers

* sets output to data input on each rising clock edge

- The flip-flop sets output = input when the clock switches from low to high;
- In all other cases, the input is ignored; the last "sampled" value is kept at the output

Storage



*

- 1-bit storage - flip-flop
- n-bit storage - register
- asynchronous circuits

– very rare

Combination of Registers and [[Combinational Circuits]]

