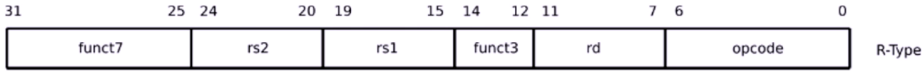
RISC-V

- [[Instruction Set Architecture]]
- properties
  - is open
  - developed at UC Berkeley
  - An instruction family from low-end 32bit devices to large 64bit CPUs
  - Significant momentum in industry and academia
  - More information and full specs available at https://riscv.org/
- Instruction Set
  - **Base instruction sets**
    - **RV32I** (RV32E is the same as RV32I, except the fact that it only allows 16 registers)
    - RV64I
    - RV128I
  - **Extensions**
    - "M" Standard Extension for Integer Multiplication and Division
    - "A" Standard Extension for Atomic Instructions
    - "Zicsr", Control and Status Register (CSR) Instructions
    - "F" Standard Extension for Single-Precision Floating-Point
- ALU and register file are 32-bit
- register files consists of 32 registers
  - register x0 always stores zero
  - allows transformation of operations
    - add(destination,a,b) => add(dest, a, 0) = move(a, dest)

Instruction Encoding

- stores operation to execute and parameters
- terminology
  - **Opcode, funct3, funct7:** definition of the functionality
  - **Imm:** immediate values (constants)
  - **rs1, rs2:** source registers
  - **rd:** destination register
- instruction types
  - R-Type
    - perform arithmetic and logic operations based on two input registers
    -



IR ADD, R3, R2, R1

*
  - I-Type
  - S-Type
  - U-Type