Finite State Machines - Automaton

- synchronous FSM clocked by clock signal and [[Clock Frequency]]
- each clock period has defined current state
- machine advances into next defined state after each rising edge

State Diagram

- defines sequence of states
- initial state defined
- circle with symbolic names for each state
- arrows define sequence
  - can be described in state transition table

present state	in	next state
A	0	B
A	1	B
B	0	A
B	1	C
C	0	A
C	1	C

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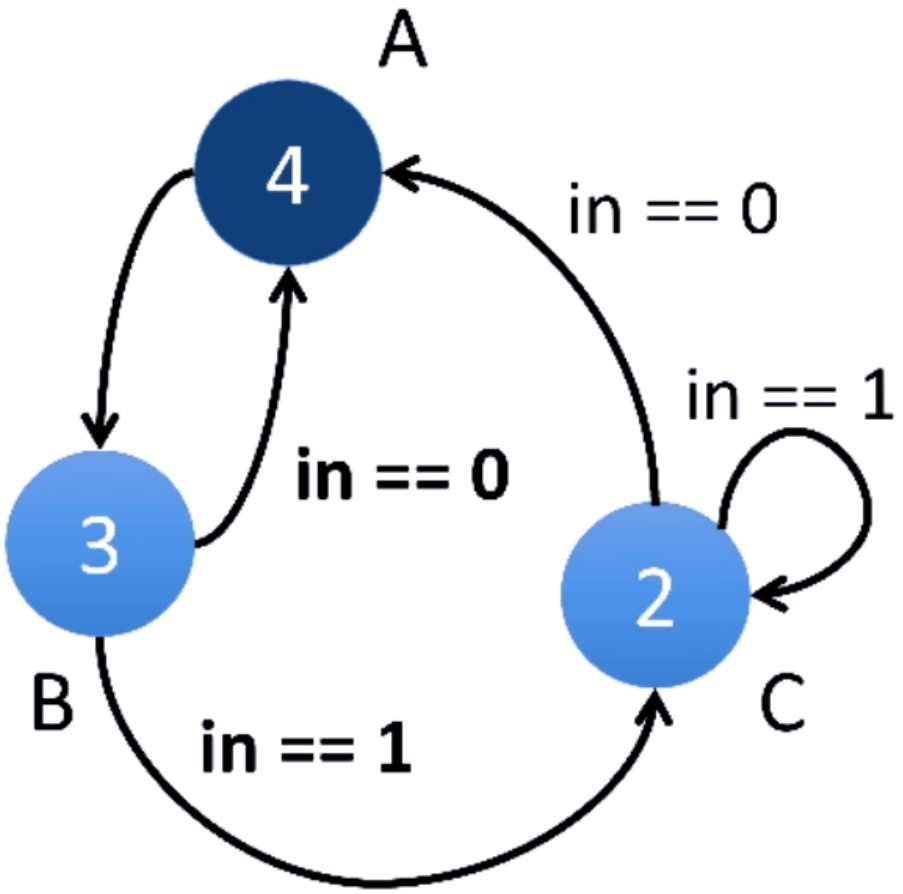
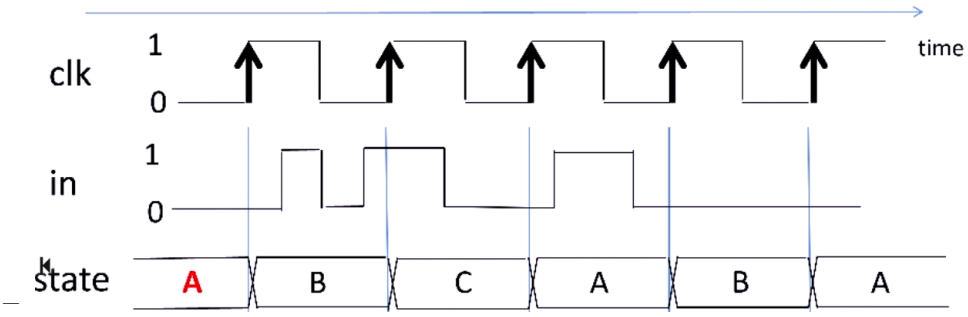
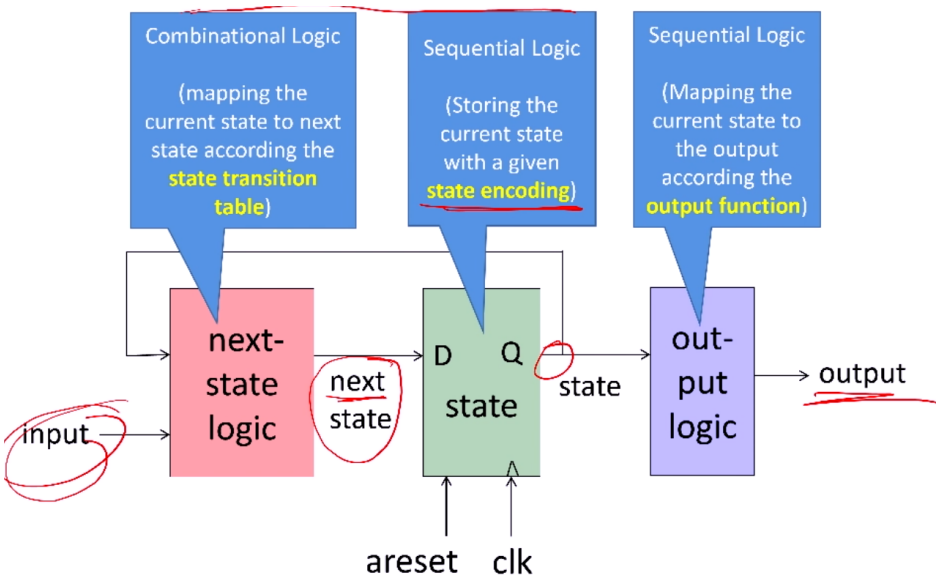
- may have inputs which influence next state
- may also have outputs
  - written into state circles
  - called Moore machines



- timing diagram



Mapping State Diagram to Hardware



- state encoding

state	encoding
A	00
B	01
C	10

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- state transition table
  - next state logic
    - next s0 = ((~s1) & (~s0) & (~in)) | ((~s1) & (~s0) & in)
    - next s1 = ((~s1) & s0 & in) | (s1 & (~s0) & in)

present		in	next	
s1	s0		s1	s0
0	0	0	0	1
0	0	1	0	1
0	1	0	0	0
0	1	1	1	0
1	0	0	0	0
1	0	1	1	0
1	1	0	x	x
1	1	1	x	x

- output function
  - 2, 3, 4 => 3 bit output

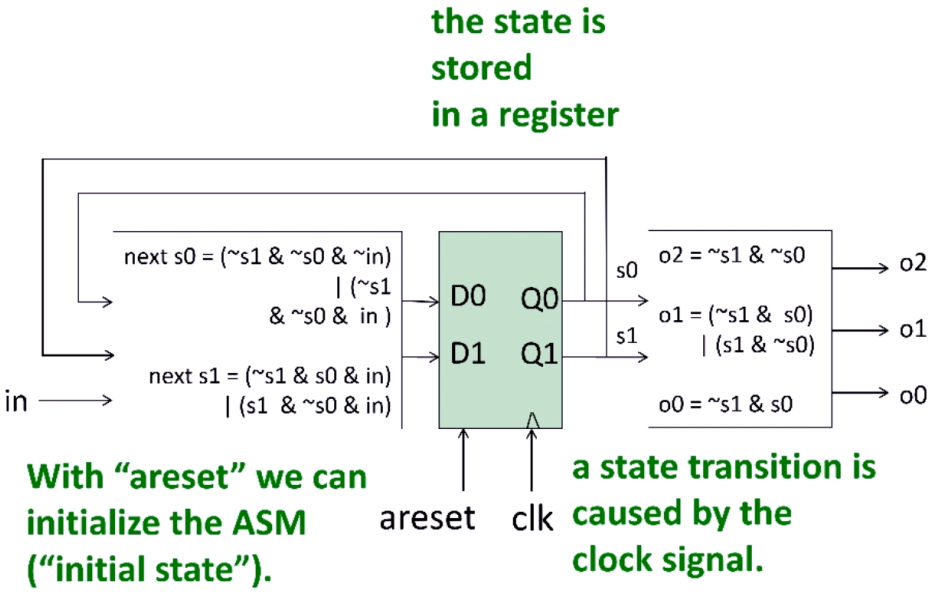
s1	s0	o2	o1	o0
0	0	1	0	0
0	1	0	1	1
1	0	0	1	0

o2 = ~s1 & ~s0

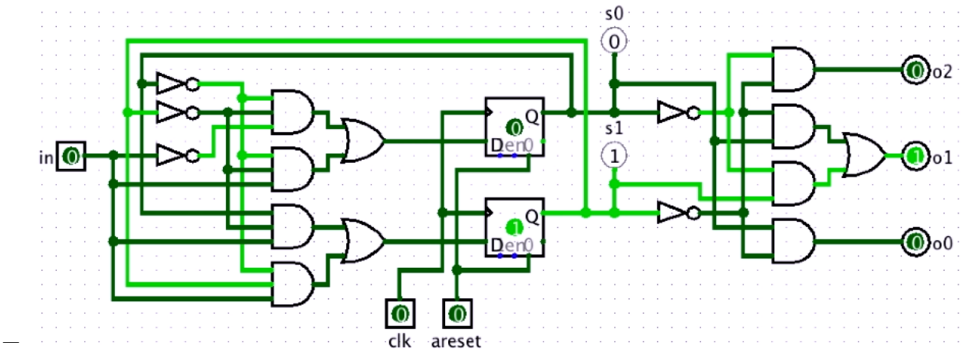
o1 = (~s1 & s0) | (s1 & ~s0)

o0 = ~s1 & s0

- structural diagram of FSM



- hardware implementation



SystemVerilog Implementation