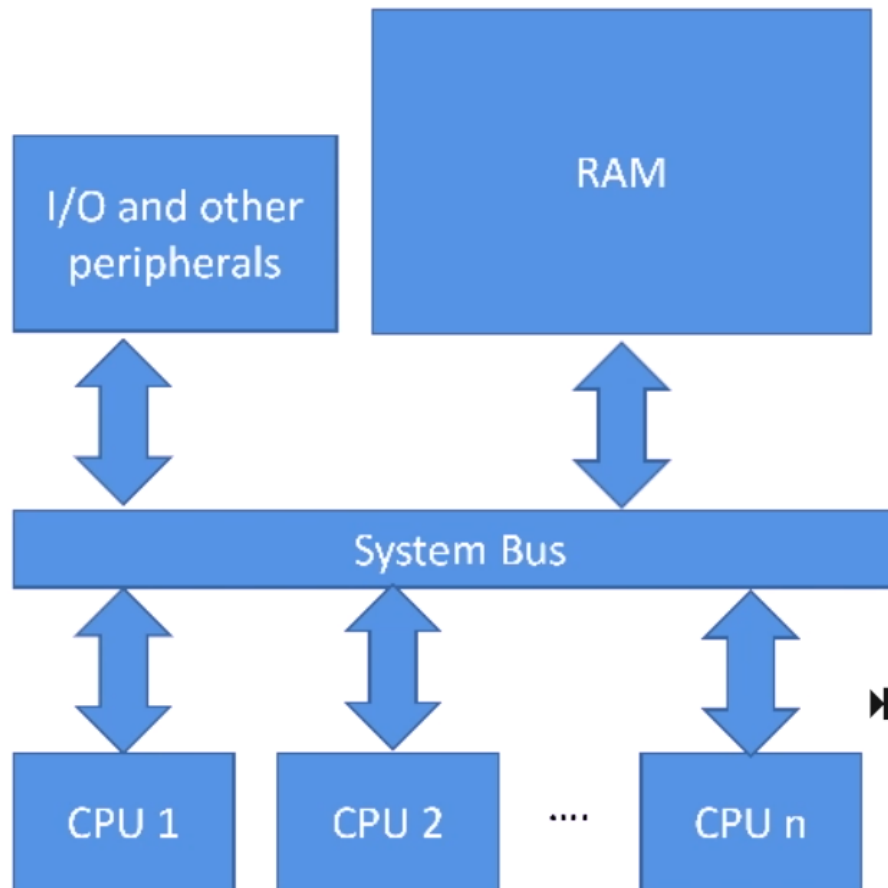Basic Idea

- add hardware to handle multiple instructions truly parallel
  - fetch multiple instructions simulatenously
  - schedule [[Multi-Cycle Execution]]
  - • Put multiple CPU cores on one chip
  - • Typical setup is symmetric: all CPUs are equal
- • All are connected to a shared memory

  -
- superscalar pipeline for each CPU core
- bottle neck
  - slow memory access
  - single memory access could take hundreds of CPU cycles
  - solution: [[Caching]]

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