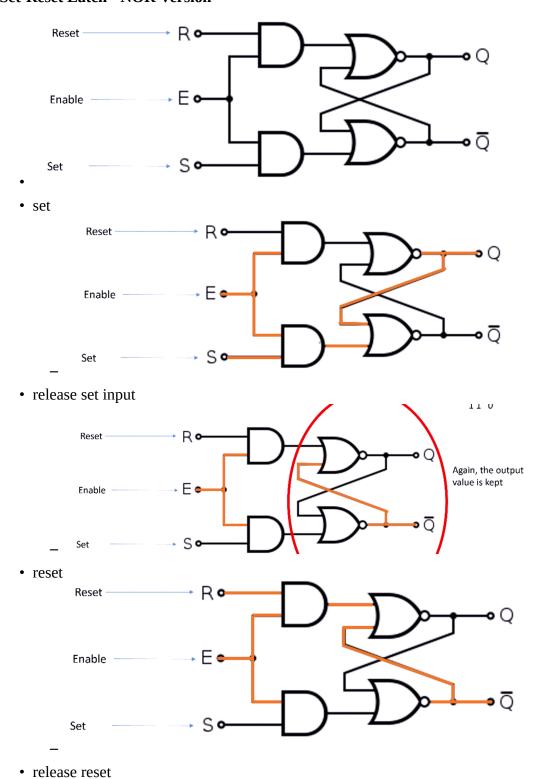
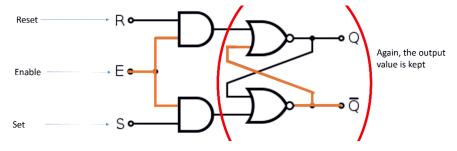
Motivation

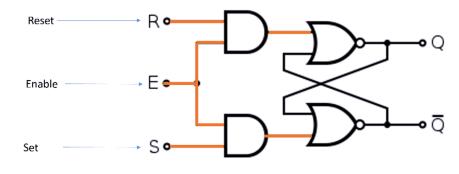
- [[Combinational Circuits]] are not capable of storing data
 - changes to input lead to change at output
- storage by creating a feedback loop

Set-Reset Latch - NOR Version





illegal action



(A)synchronous circuits

- · synchronous circuits with global clock signal
 - most commonly used
 - no latches as storage
 - instead uses flip-flops or registers
 - * sets output to data input on each rising clock edge

 The flip-flop sets output = input when the clock switches from low to high;

 In all other cases, the input is ignored; the last "sampled" value is kept at the output

 Clock

 ("Vdd", "high", "1")

 data input

 Flip-Flop

 Clock

 ("GND", "low", "0")
 - 1-bit storage flip-flop
 - n-bit storage register
- · asychronous circuits

very rare

Combination of Registers and [[Combinational Circuits]]

