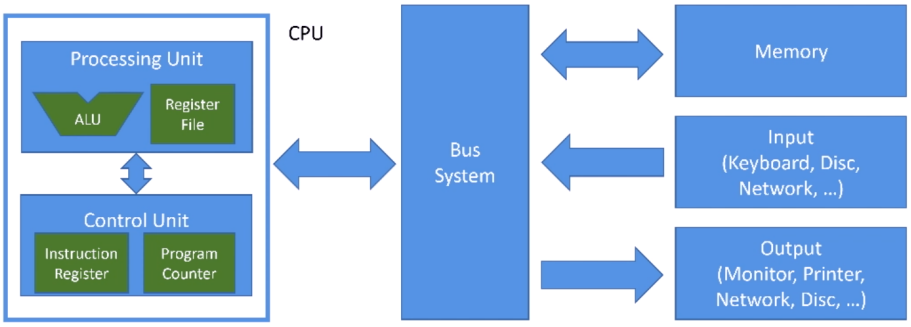
Limitations of [[Finite State Machines]]

- previous state machines designed for specific application
- application changes require new state machine, new hardware
- general-purpose machine wanted

Von Neumann Model

- architecture with following components
  - Processing Unit
  - Control Unit
  - Memory
  - Input
  - Output
  - Buses
- CPU connected via bus system to memory and I/O



- Hardvard Architecture Variation
  - Memory split into Data and Instruction Memory

Arithmetic Logic Unit

- ALUs are [[Combinational Circuits]] performing calculation operations
- basic properties

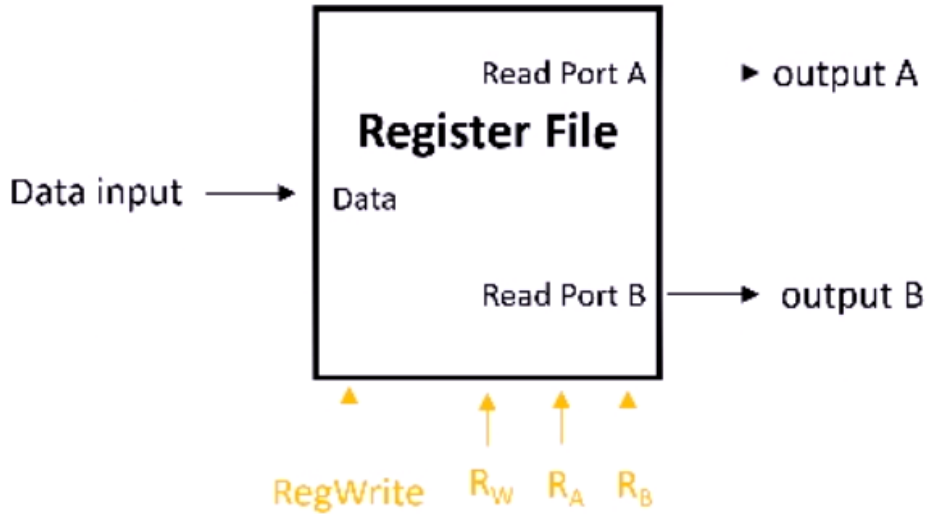
  Takes two n-bit inputs (A, B); today typically 32 bit or 64 bit

  Performs an operation based on one or both inputs; the performed operation is selected by the control input alu_sel

  Returns an n-bit output; It typically also provides a status output with flags to e.g. indicate overflows or relations of A and B, such as A==B or A<B

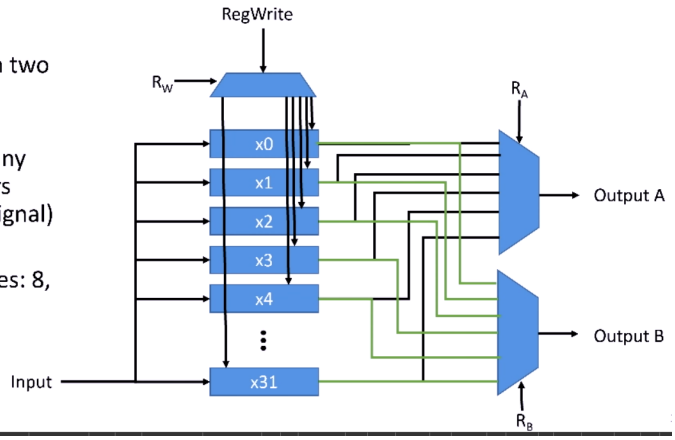
Register File

- contatins m n-bit registers
- write one n-bit value per clock cycle
  - register selected via R_W
  - does not write if low
- read two registers per clock cycle
  - provided at outputs A and B
  - registers selected via R_A and R_B
- basically memory with
  - one write port
  - two read ports



- register file with 32 registers

- Basic Properties
  - Data registers with two output MUX
  - Input is stored in any one of the registers (selection via R_W signal)
  - Typical register sizes: 8, 16, 32, 64 bit



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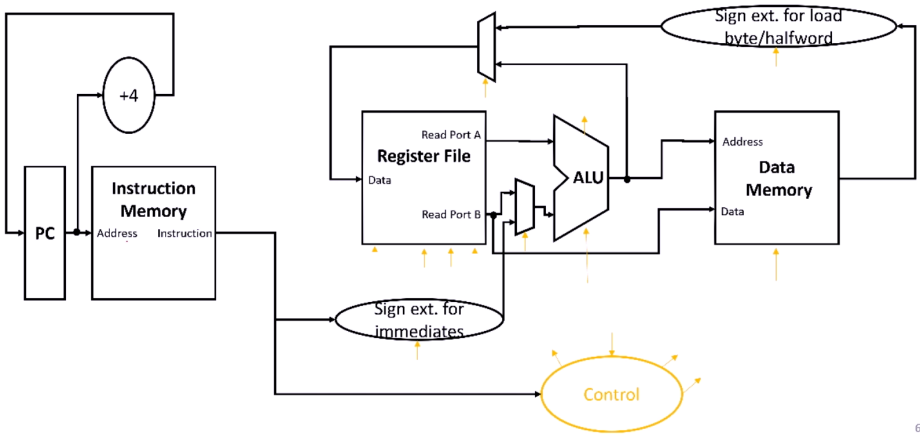
Processing Unit

- combines ALU and register file



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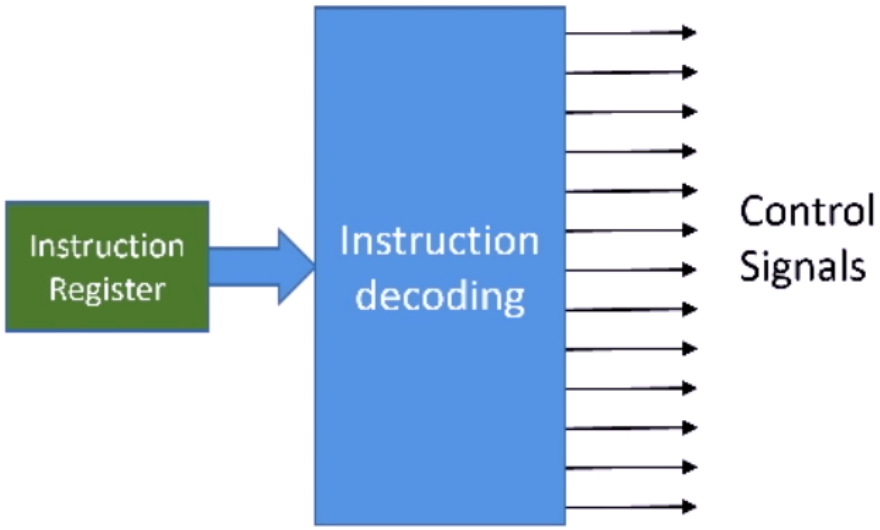
- instruction register
  - stores instruction to execute and parameters
  - mapped to control signals by instruction encoder



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