

a-Si TFT LCD Single Chip Driver 132RGBx162 Resolution and 262K color

Specification

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1. Introduction

ILI9163C is a 262,144-color one-chip SoC driver for a-TFT liquid crystal display with resolution of 132RGBx162 dots, comprising a 396-channel source driver, a 162-channel gate driver, 48,114bytes GRAM for graphic data of 132RGBx162 dots, and power supply circuit.

The ILI9163C supports 18-/16-/9-/8-bit data bus interface and serial peripheral interfaces (SPI). It also supplies 18-bit, 16-bit or 6-bit RGB interface for driving video signal directly from application controller. The moving picture area can be specified in internal GRAM by window address function. The specified window area can be updated selectively, so that moving picture can be displayed simultaneously independent of still picture area.

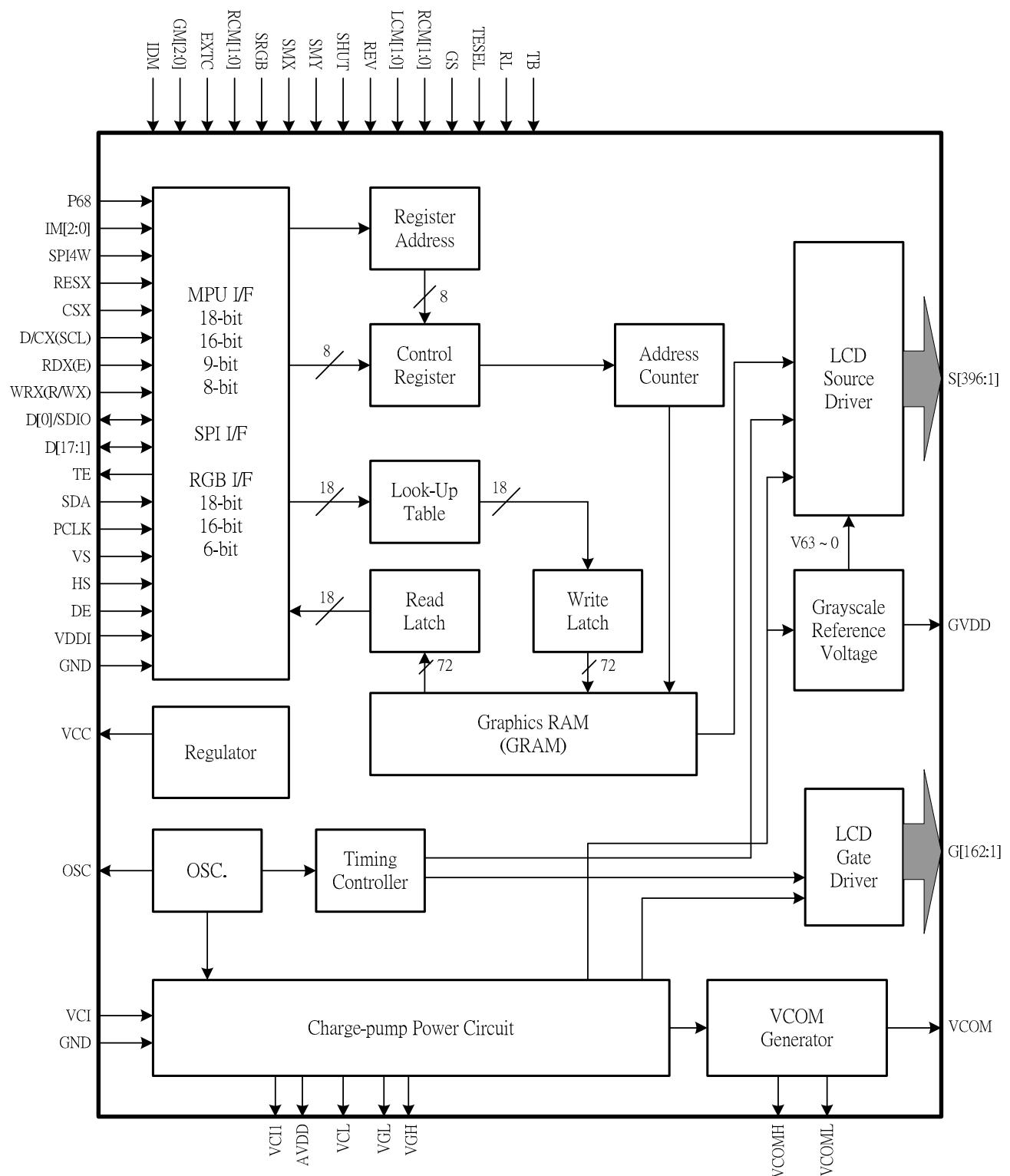
ILI9163C can operate with 1.65V I/O interface voltage, and an incorporated voltage follower circuit to generate voltage levels for driving an LCD. The ILI9163C also supports a function to display in 8 colors and a sleep mode, allowing for precise power control by software and these features make the ILI9163C an ideal LCD driver for medium or small size portable products such as digital cellular phones, smart phone, MP3 and PMP where long battery life is a major concern.

2. Features

- ◆ Display resolution: [132xRGB](H) x 162(V)
- ◆ Output:
 - 396 source outputs
 - 162 gate outputs
 - Common electrode output
- ◆ AM-LCD driver with on-chip full display RAM: 48,114 bytes
- ◆ System Interfaces
 - 8-bits, 9-bits, 16-bits, 18-bits interface with 8080-series MCU
 - 8-bits, 9-bits, 16-bits, 18-bits interface with 6800-series MCU
 - 6-bits, 16-bits, 18-bits RGB interface
 - 3-pin/4-pin serial interface
- ◆ Display mode:
 - Full color mode (idle mode off): 262K-colors
 - Reduced color mode (idle mode on): 8-colors (3-bits MSB bits mode)
- ◆ On chip functions:
 - VCOM generator and adjustment
 - Timing generator
 - Oscillator
 - DC/DC converter
 - 4 preset gamma curve selectable
 - Line/frame inversion
 - MTP to store initialization register setting
 - Factory default value(Contrast, Module ID, Module version, etc) are stored on the display module

- ◆ MTP:
 - 8-bits for ID2
 - 8-bits for ID3
 - 7-bits for VCOM adjustment
- ◆ Low –power consumption architecture
 - Low operating power supplies:
 - VDDI = 1.65V ~ 3.3 V (interface I/O)
 - VCI = 2.5V ~ 4.0 V (analog)
- ◆ LCD Voltage drive:
 - Source/VCOM power supply voltage
 - AVDD – GND = 4.5V ~ 6.0V
 - VCL – GND = -1.0V ~ -3.0V
 - VCI1 – VCL \leq 6.0V
 - Gate driver output voltage
 - VGH – GND = 10V ~ 16V
 - VGL – GND = -6V ~ -12V
 - VGH – VGL \leq 30V
 - VCOM driver output voltage
 - VCOMH = 2.5V ~5V
 - VCOML = -2.5V ~ 0V
 - VCOMH-VCOML \leq 6.0V
- ◆ Operate temperature range: -40°C to 85°C

3. Block Diagram



4. Pin Descriptions

Pin Name	I/O	Descriptions															
P68	I	8080/6800 MCU Interface mode selection. P68='1': select 6800-MCU parallel interface P68='0': select 8080-MCU parallel interface If not used, please fix this pin at GND level.															
IM2	I	MCU Parallel interface bus and Serial interface select - IM2='1';Parallel Interface - IM2='0';Serial Interface															
IM1, IM0	I	MCU parallel interface type selection <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>IM1</th> <th>IM0</th> <th>Parallel interface</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>MCU 8-bit Parallel</td> </tr> <tr> <td>0</td> <td>1</td> <td>MCU 16-bit Parallel</td> </tr> <tr> <td>1</td> <td>0</td> <td>MCU 9-bit Parallel</td> </tr> <tr> <td>1</td> <td>1</td> <td>MCU 18-bit Parallel</td> </tr> </tbody> </table>	IM1	IM0	Parallel interface	0	0	MCU 8-bit Parallel	0	1	MCU 16-bit Parallel	1	0	MCU 9-bit Parallel	1	1	MCU 18-bit Parallel
IM1	IM0	Parallel interface															
0	0	MCU 8-bit Parallel															
0	1	MCU 16-bit Parallel															
1	0	MCU 9-bit Parallel															
1	1	MCU 18-bit Parallel															
SPI4W	I	SPI interface selection pin SPI4W='0': 3-wire SPI. (default) SPI4W='1': 4-wire SPI. This pin is internal pull low.															
RESX	I	Chip reset pin (“Low Active”). This signal low will reset the device and must be applied to properly initialize the chip.															
CSX	I	Chip select input pin (“Low” enable). This pin can be permanently fixed “Low” in MCU interface mode only.															
D/CX (SCL)	I	Display data / Command selection pin in parallel and SCL in 3-pin SPI interface. D/CX='1': Display data. D/CX='0': Command data. If not used, please connect this pin to GND.															
RDX (E)	I	Read enable in 8080-parallel interface and Read/ Write operation enable pin in 6800-parallel interface. In 8080-parallel interface, if not used, please connect this pin to VDDI. In 6800-parallel interface, if not used, please connect this pin to VDDI or GND.															
WRX (R/WX)(D/CX)	I	Write enable in parallel interface. WRX: for 8080 MCU R/WX: for 6800 MCU D/CX: for 4-wire SPI If not used, please connect this pin to VDDI or GND.															
D[17:1] D[0]/SDIO	I/O	When RCM1='0' (MCU I/F), D[17:0] are used to MCU parallel interface data bus, and D0 is also the serial input/ output signal in SPI interface mode. In serial interface, D[17:1] are not used and should be connected to ground. When RCM1='1' (RGB I/F), D[17:0] are used to RGB interface data bus.															

Pin Name	I/O	Descriptions																												
TE	O	Tearing effect output pin to synchronies MCU to frame writing, activated by S/W command. When this pin is not activated, this pin is low. If not used, please open this pin.																												
SDA	I/O	When RCM1,RCM0='1X'(RGB I/F), serial input/output signal in serial I/F mode. The data is input on the rising edge of the SCL signal. The data is output on the falling edge of the SCL signal. When RCM1,RCM0='0X'(MCU I/F), this pin is not used, and fix at VDDI or GND level. If not used, please fix this pin at VDDI or GND level.																												
PCLK	I	Pixel clock signal in RGB I/F mode. -If it's not used, please fix this pin at GND level.																												
VS	I	Vertical sync. Signal in RGB I/F mode. -If it's not used, please fix this pin at GND level.																												
HS	I	Horizontal sync. Signal in RGB I/F mode. -If it's not used, please fix this pin at GND level.																												
DE	I	Data enable signal in RGB I/F mode. -If it's not used, please fix this pin at GND level.																												
OSC	O	Oscillator output or test purpose.																												
EXTC	I	To use extended command set, please connect this pin to VDDI. During normal operation, please open this pin. (It has an internal pull low resistor.) EXTC='1', all the command can be used. EXTC='0', only Command (00h~3Ah, DAh~DCh) can be used																												
IDM	I	Normal mode and Idle mode control pin(Only for RGB interface(2)) <table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <th>IDM</th> <th>Idle mode H/W controller</th> </tr> <tr> <td>0</td> <td>Normal display (can be changed to Idle mode by S/W)</td> </tr> <tr> <td>1</td> <td>Idle mode</td> </tr> </table>	IDM	Idle mode H/W controller	0	Normal display (can be changed to Idle mode by S/W)	1	Idle mode																						
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GM2,GM1,GM0	I	Panel Resolution selection pins <table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <th>GM2</th> <th>GM1</th> <th>GM0</th> <th>Resolution selection</th> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td>132RGB x 162(S1~396 and G1~ G162 output)</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>128RGB x 128(S7~390 and G2~ G129 output)</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>120RGB x 160(S7~366 and G2~ G161 output)</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>128RGB x 160(S7~390 and G2~ G161 output)</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>130RGB x 130(S7~396 and G2~ G131 output)</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>132RGB x 132(S1~396 and G2~ G133 output)</td> </tr> </table>	GM2	GM1	GM0	Resolution selection	0	0	0	132RGB x 162(S1~396 and G1~ G162 output)	0	0	1	128RGB x 128(S7~390 and G2~ G129 output)	0	1	0	120RGB x 160(S7~366 and G2~ G161 output)	0	1	1	128RGB x 160(S7~390 and G2~ G161 output)	1	0	0	130RGB x 130(S7~396 and G2~ G131 output)	1	0	1	132RGB x 132(S1~396 and G2~ G133 output)
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RCM[1:0]	I	RGB and MCU interface mode selection pin <table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <th>RCM1</th> <th>RCM0</th> <th>Resolution selection</th> </tr> <tr> <td>0</td> <td>X</td> <td>MCU interface mode</td> </tr> <tr> <td>1</td> <td>0</td> <td>RGB interface(1)</td> </tr> <tr> <td>1</td> <td>1</td> <td>RGB interface(2)</td> </tr> </table>	RCM1	RCM0	Resolution selection	0	X	MCU interface mode	1	0	RGB interface(1)	1	1	RGB interface(2)																
RCM1	RCM0	Resolution selection																												
0	X	MCU interface mode																												
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SRGB	I	RGB direction select H/W pin for Color filter default setting. <table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <th>SRGB</th> <th>Color mapping selection</th> </tr> <tr> <td>0</td> <td>S1, S2, S3 filter order = 'R', 'G', 'B'</td> </tr> <tr> <td>1</td> <td>S1, S2, S3 filter order = 'B', 'G', 'R'</td> </tr> </table>	SRGB	Color mapping selection	0	S1, S2, S3 filter order = 'R', 'G', 'B'	1	S1, S2, S3 filter order = 'B', 'G', 'R'																						
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Pin Name	I/O	Descriptions																												
		If the register is not changed, this H/W pin is always valid. If the register be changed, should be following registers setting. When Power On or H/W reset, this function follow H/W pins setting first.																												
SMX	I	Source output direction H/W select pin <table border="1"> <thead> <tr> <th>SMX</th><th colspan="6">Source Output Direction</th></tr> <tr> <th></th><th>GM='101'</th><th>GM='100'</th><th>GM='011'</th><th>GM='010'</th><th>GM='001'</th><th>GM='000'</th></tr> </thead> <tbody> <tr> <td>0</td><td>S1 → S396</td><td>S7 → S396</td><td>S7 → S390</td><td>S7 → S366</td><td>S7 → S390</td><td>S1 → S396</td></tr> <tr> <td>1</td><td>S396 → S1</td><td>S396 → S7</td><td>S390 → S7</td><td>S366 → S7</td><td>S390 → S7</td><td>S396 → S1</td></tr> </tbody> </table> If the register is not changed, this H/W pin is always valid. If the register be changed, should be following registers setting and H/W operation (XOR). When Power On or H/W reset, this function follow H/W pins setting first.	SMX	Source Output Direction							GM='101'	GM='100'	GM='011'	GM='010'	GM='001'	GM='000'	0	S1 → S396	S7 → S396	S7 → S390	S7 → S366	S7 → S390	S1 → S396	1	S396 → S1	S396 → S7	S390 → S7	S366 → S7	S390 → S7	S396 → S1
SMX	Source Output Direction																													
	GM='101'	GM='100'	GM='011'	GM='010'	GM='001'	GM='000'																								
0	S1 → S396	S7 → S396	S7 → S390	S7 → S366	S7 → S390	S1 → S396																								
1	S396 → S1	S396 → S7	S390 → S7	S366 → S7	S390 → S7	S396 → S1																								
SMY	I	Gate output direction H/W select pin <table border="1"> <thead> <tr> <th>SMY</th><th colspan="5">Gate Output Direction</th></tr> <tr> <th></th><th>GM='101'</th><th>GM='100'</th><th>GM='011','010'</th><th>GM='001'</th><th>GM='000'</th></tr> </thead> <tbody> <tr> <td>0</td><td>G2 → G133</td><td>G2 → G131</td><td>G2 → G161</td><td>G2 → G129</td><td>G1 → G162</td></tr> <tr> <td>1</td><td>G133 → G2</td><td>G131 → G2</td><td>G161 → G2</td><td>G129 → G2</td><td>G162 → G1</td></tr> </tbody> </table> If the register is not changed, this H/W pin is always valid. If the register be changed, should be following registers setting and H/W operation(XOR). When Power On or H/W reset, this function follow H/W pins setting first.	SMY	Gate Output Direction						GM='101'	GM='100'	GM='011','010'	GM='001'	GM='000'	0	G2 → G133	G2 → G131	G2 → G161	G2 → G129	G1 → G162	1	G133 → G2	G131 → G2	G161 → G2	G129 → G2	G162 → G1				
SMY	Gate Output Direction																													
	GM='101'	GM='100'	GM='011','010'	GM='001'	GM='000'																									
0	G2 → G133	G2 → G131	G2 → G161	G2 → G129	G1 → G162																									
1	G133 → G2	G131 → G2	G161 → G2	G129 → G2	G162 → G1																									
SHUT	I	Display On/ Off H/W control pin In RGB I/F(Only for RGB interface(2)) <table border="1"> <thead> <tr> <th>SHUT</th><th>Display On/Off in RGB interface</th></tr> </thead> <tbody> <tr> <td>0</td><td>Display on</td></tr> <tr> <td>1</td><td>Display off</td></tr> </tbody> </table> Please refer RGB I/F for detail using.	SHUT	Display On/Off in RGB interface	0	Display on	1	Display off																						
SHUT	Display On/Off in RGB interface																													
0	Display on																													
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REV	I	Source output data polarity select H/W pin. <table border="1"> <thead> <tr> <th>REV</th><th>Source output data polarity</th></tr> </thead> <tbody> <tr> <td>0</td><td>Data not reverse</td></tr> <tr> <td>1</td><td>Data reverse</td></tr> </tbody> </table> If the register is not changed, this H/W pin is always valid. If the register be changed, should be following registers setting. When Power On or H/W reset, this function follow H/W pins setting first.	REV	Source output data polarity	0	Data not reverse	1	Data reverse																						
REV	Source output data polarity																													
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LCM[1:0]	I	Different Liquid Crystal type selection pins. There is a pull-low resistor only in LCM1 pin <table border="1"> <thead> <tr> <th>LCM1</th><th>LCM0</th><th>LC Type Selection</th></tr> </thead> <tbody> <tr> <td>0</td><td>0</td><td rowspan="4">TM (Transmission) LC Type2</td></tr> <tr> <td>0</td><td>1</td></tr> <tr> <td>1</td><td>0</td></tr> <tr> <td>1</td><td>1</td></tr> </tbody> </table>	LCM1	LCM0	LC Type Selection	0	0	TM (Transmission) LC Type2	0	1	1	0	1	1																
LCM1	LCM0	LC Type Selection																												
0	0	TM (Transmission) LC Type2																												
0	1																													
1	0																													
1	1																													
GS	I	Input pin to select the gamma curve order Connect to VDDI for GC0(2,2), GC1(1.8), GC2(2.5), GC3(1.0) Connect to GND for GC0(1,0), GC1(2.5), GC2(2.2), GC3(1.8)																												

Pin Name	I/O	Descriptions																																																						
TESEL	I	<p>Default is internal pull high.</p> <p>This pin is only for GM[2:0] = '000' mode</p> <p>Connect to VDDI (Disable scroll function)</p> <p>Connect to GND (Enable scroll function)</p>																																																						
RL	I	<p>Source output direction H/W select pin in RGB interface(2)</p> <p>When SMX=0</p> <table border="1"> <thead> <tr> <th rowspan="2">RL</th> <th colspan="6">Module source output direction</th> </tr> <tr> <th>GM='101'</th> <th>GM='100'</th> <th>GM='011'</th> <th>GM='010'</th> <th>GM='001'</th> <th>GM='000'</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>S1 → S396</td> <td>S7 → S396</td> <td>S7 → S390</td> <td>S7 → S366</td> <td>S7 → S390</td> <td>S1 → S396</td> </tr> <tr> <td>1</td> <td>S396 → S1</td> <td>S396 → S7</td> <td>S390 → S7</td> <td>S366 → S7</td> <td>S390 → S7</td> <td>S396 → S1</td> </tr> </tbody> </table> <p>When SMX=1</p> <table border="1"> <thead> <tr> <th rowspan="2">RL</th> <th colspan="6">Module source output direction</th> </tr> <tr> <th>GM='101'</th> <th>GM='100'</th> <th>GM='011'</th> <th>GM='010'</th> <th>GM='001'</th> <th>GM='000'</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>S396 → S1</td> <td>S396 → S7</td> <td>S390 → S7</td> <td>S366 → S7</td> <td>S390 → S7</td> <td>S396 → S1</td> </tr> <tr> <td>1</td> <td>S1 → S396</td> <td>S7 → S396</td> <td>S7 → S390</td> <td>S7 → S366</td> <td>S7 → S390</td> <td>S1 → S396</td> </tr> </tbody> </table>	RL	Module source output direction						GM='101'	GM='100'	GM='011'	GM='010'	GM='001'	GM='000'	0	S1 → S396	S7 → S396	S7 → S390	S7 → S366	S7 → S390	S1 → S396	1	S396 → S1	S396 → S7	S390 → S7	S366 → S7	S390 → S7	S396 → S1	RL	Module source output direction						GM='101'	GM='100'	GM='011'	GM='010'	GM='001'	GM='000'	0	S396 → S1	S396 → S7	S390 → S7	S366 → S7	S390 → S7	S396 → S1	1	S1 → S396	S7 → S396	S7 → S390	S7 → S366	S7 → S390	S1 → S396
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TB	I	<p>Gate output direction H/W select pin on RGB interface(2)</p> <p>When SMY=0</p> <table border="1"> <thead> <tr> <th rowspan="2">TB</th> <th colspan="5">Module gate output direction</th> </tr> <tr> <th>GM='101'</th> <th>GM='100'</th> <th>GM='011', '010'</th> <th>GM='001'</th> <th>GM='000'</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>G2 → G133</td> <td>G2 → G131</td> <td>G2 → G161</td> <td>G2 → G129</td> <td>G1 → G162</td> </tr> <tr> <td>1</td> <td>G133 → G2</td> <td>G131 → G2</td> <td>G161 → G2</td> <td>G129 → G2</td> <td>G162 → G1</td> </tr> </tbody> </table> <p>When SMY=1</p> <table border="1"> <thead> <tr> <th rowspan="2">TB</th> <th colspan="5">Module gate output direction</th> </tr> <tr> <th>GM='101'</th> <th>GM='100'</th> <th>GM='011', '010'</th> <th>GM='001'</th> <th>GM='000'</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>G133 → G2</td> <td>G131 → G2</td> <td>G161 → G2</td> <td>G129 → G2</td> <td>G162 → G1</td> </tr> <tr> <td>1</td> <td>G2 → G133</td> <td>G2 → G131</td> <td>G2 → G161</td> <td>G2 → G129</td> <td>G1 → G162</td> </tr> </tbody> </table>	TB	Module gate output direction					GM='101'	GM='100'	GM='011', '010'	GM='001'	GM='000'	0	G2 → G133	G2 → G131	G2 → G161	G2 → G129	G1 → G162	1	G133 → G2	G131 → G2	G161 → G2	G129 → G2	G162 → G1	TB	Module gate output direction					GM='101'	GM='100'	GM='011', '010'	GM='001'	GM='000'	0	G133 → G2	G131 → G2	G161 → G2	G129 → G2	G162 → G1	1	G2 → G133	G2 → G131	G2 → G161	G2 → G129	G1 → G162								
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S1 ~ S396	O	Source driver output pins.																																																						
G1 ~ G162	O	Gate driver output pins.																																																						
VCI	P	<p>Power supply for analog circuit.</p> <p>Could connect to external power supply (VCI=2.5~4.8V).</p>																																																						
VDDI	P	Power supply for interface logic circuits (1.65 ~ 3.3 V)																																																						
VCC	P	Power supply for internal logic regulator.																																																						
GND	P	GND voltage output level for control pins.																																																						
VDDIO	P	VDDI voltage output level for control pins using.																																																						
GNDO	P	GND voltage output level for control pins using.																																																						
VCI1	P	A reference voltage in step-up circuit 1																																																						
AVDD	P	A power output pin for source driver block that is generated from power block.																																																						

Pin Name	I/O	Descriptions
		Output of booster 1 circuit (output of 2-times output of VCI) Connect a capacitor for stabilization.
VCL	P	A power supply pin for generating VCOML
GVDD	P	A standard level for grayscale voltage generator.
VGH	P	Positive power supply for the gate driver.
VGL	P	Negative power supply for the gate driver. Connect a capacitor for stabilization
VCOM	O	TFT display common electrode power supply. Alternates between voltage levels between VCOMH-VCOML. Registers set the alternating cycle for operating or halting VCOM.
VCOMH	O	The high level of VCOM AC voltage.
VCOML	O	The low level of VCOM AC voltage.
TESTOSC	I	These test pins for Driver vendor test used. Please open these pins or fix to GND.
TESTDA[5:0] TEST_MODE[2:0]	O	These test pins for Driver vendor test used. Please open these pins.
DUMMYR1-DUMMYR2	-	DUMMYR1 and DUMMYR2 are short-circuited within the chip for COG contact resistance measurement. Please leave them open when not used.
DUMMY1-DUMMY18 DUMMY	-	Dummy pins. During normal operation, leave these pads open.

Liquid crystal power supply specifications Table 1

No.	Item	Description	
1	TFT Source Driver	396 pins (132 x RGB)	
2	TFT Gate Driver	162 pins	
3	TFT Display's Capacitor Structure	Cst structure only (Common VCOM)	
4	Liquid Crystal Drive Output	S1 ~ S396	V0 ~ V63 grayscales
		G1 ~ G162	VGH – VGL
		VCOM	VCOMH – VCOML: Amplitude = electronic volumes
5	Input Voltage	VDDI	1.65 ~ 3.30V
		VCI	2.50 ~ 4.00V
6	Liquid Crystal Drive Voltages	AVDD	4.5V ~ 6.0V
		VGH	10V ~ 16V
		VGL	-6V ~ -12V
		VCL	-1.0V ~ -3.0V
		VGH – VGL	Max. 30V
		VCI – VCL	Max. 6.0V
	Internal Step-up Circuits	AVDD	VCI x2
		VGH	AVDD x2.5, x3
		VGL	AVDD -x2.5, -x3
		VCL	VCI1 x-1

5. Pad Arrangement and Coordination

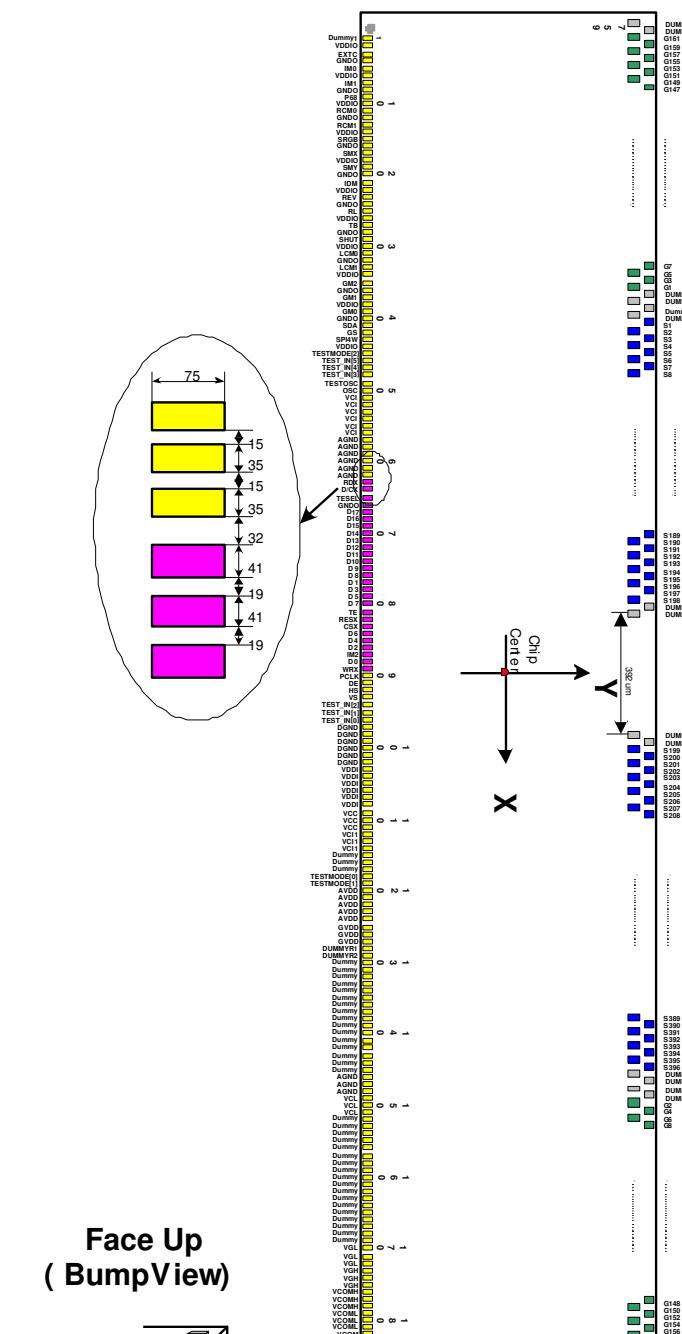
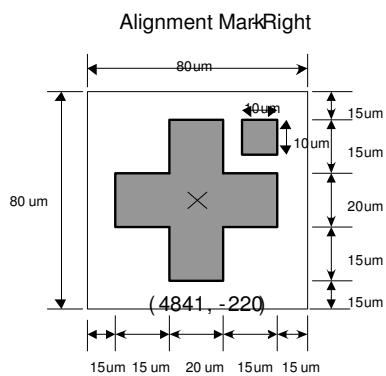
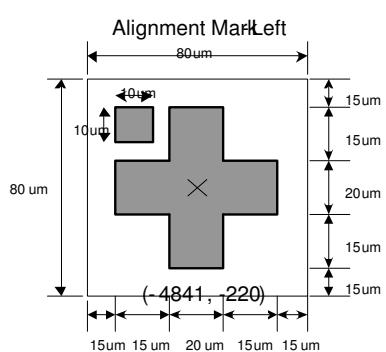
Chip Size 9900um x670um

Chip thickness 280 um(typ.)/300um

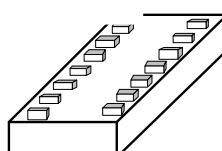
Pad Location Pad Center

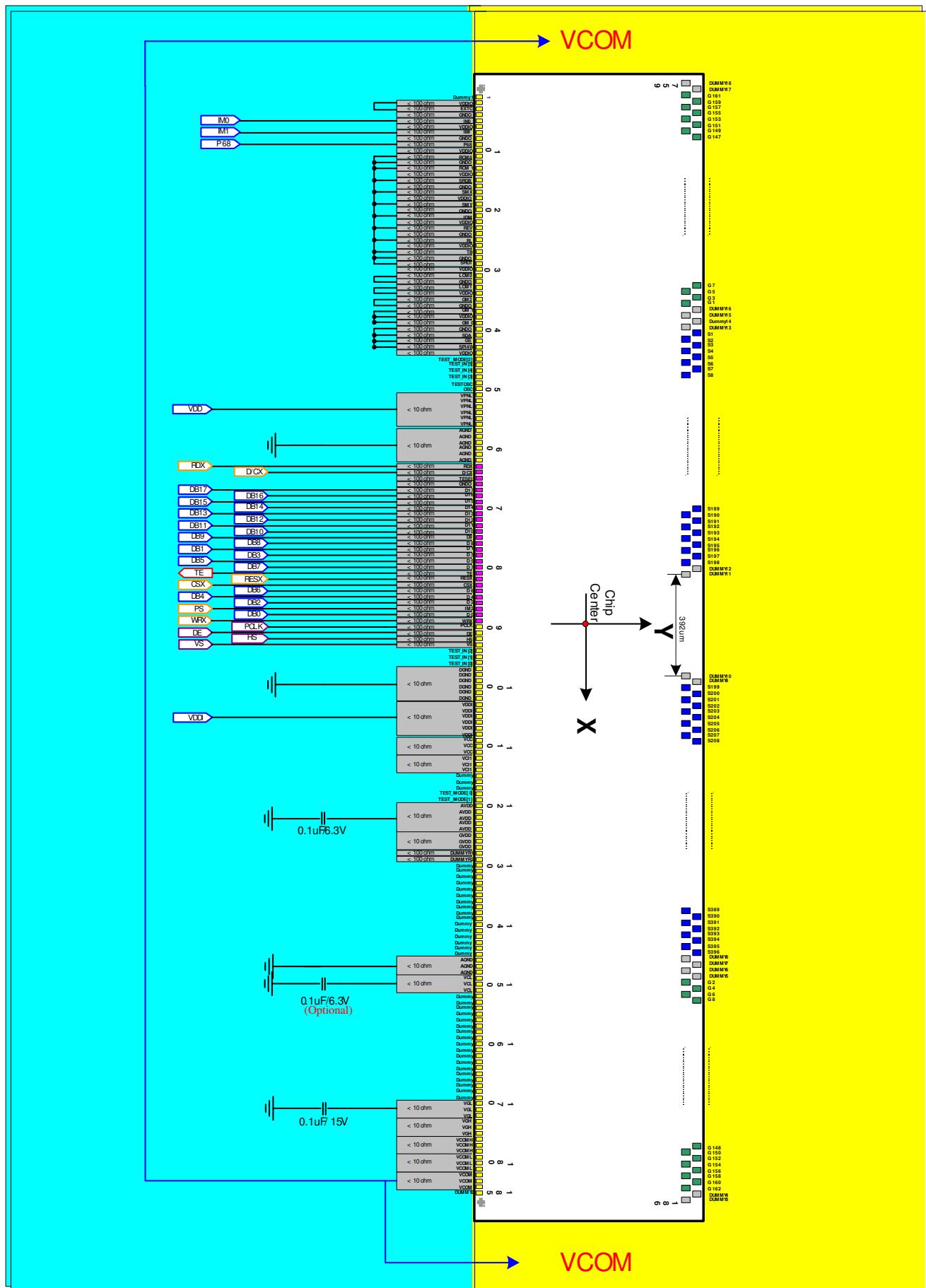
Coordinate Origin Chip Center

Au bump height 12+- 2 um



Face Up (BumpView)

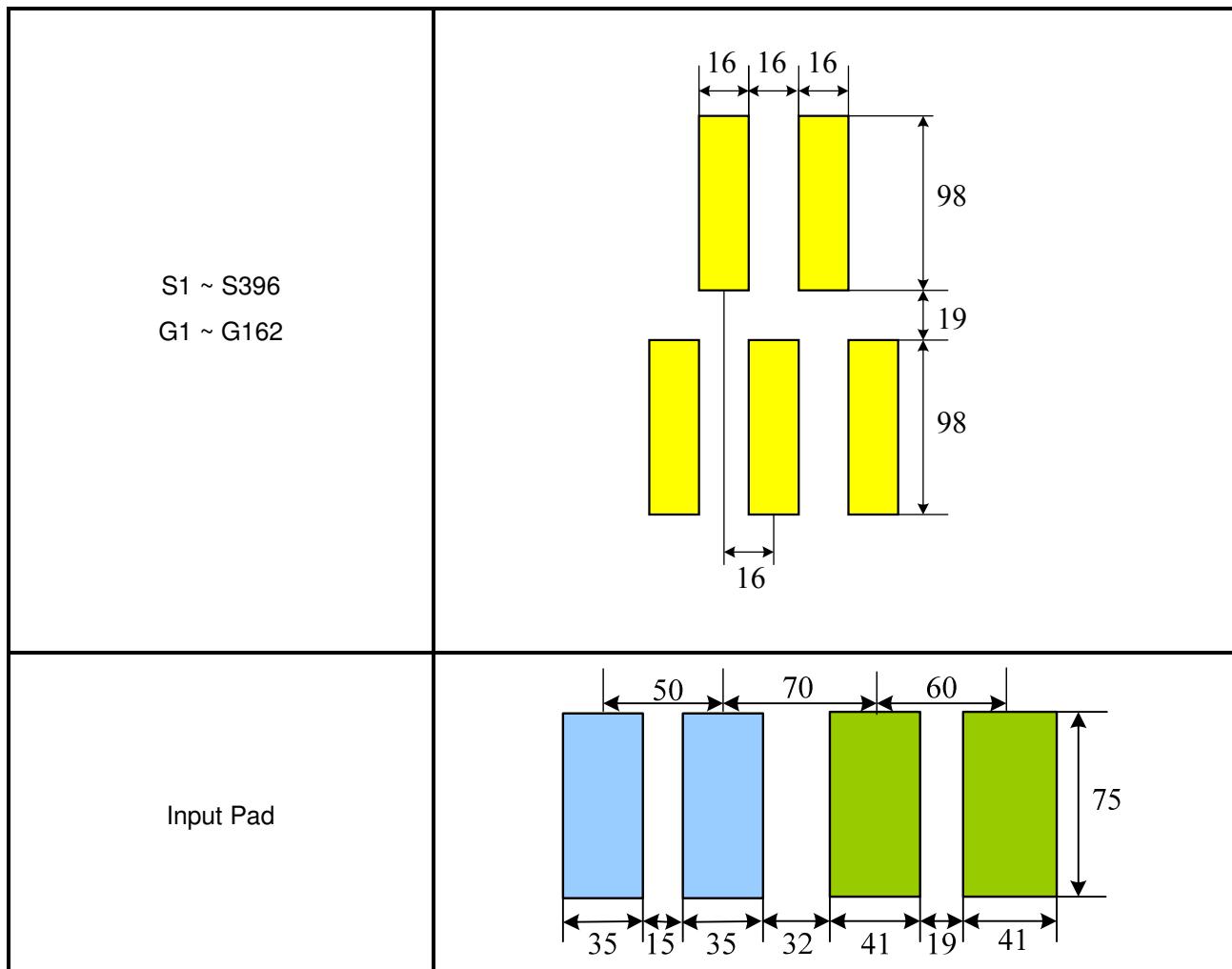




No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
1	Dummy1	-4750	-238.5	61	AGND	-1750	-238.5	121	AVDD	1550	-238.5	181	VCOML	4550	-238.5	241	G56	3892	227
2	VDDIO	-4700	-238.5	62	AGND	-1700	-238.5	122	AVDD	1600	-238.5	182	VCOM	4600	-238.5	242	G54	3876	110
3	EXTC	-4650	-238.5	63	RDX	-1630	-238.5	123	AVDD	1650	-238.5	183	VCOM	4650	-238.5	243	G52	3860	227
4	GNDO	-4600	-238.5	64	D/CX	-1570	-238.5	124	AVDD	1700	-238.5	184	VCOM	4700	-238.5	244	G50	3844	110
5	IM0	-4550	-238.5	65	TESEL	-1510	-238.5	125	GVDD	1750	-238.5	185	DUMMY2	4750	-238.5	245	G48	3828	227
6	VDDIO	-4500	-238.5	66	GNDO	-1450	-238.5	126	GVDD	1800	-238.5	186	DUMMY3	4772	110	246	G46	3812	110
7	IM1	-4450	-238.5	67	D17	-1390	-238.5	127	GVDD	1850	-238.5	187	DUMMY4	4756	227	247	G44	3796	227
8	GNDO	-4400	-238.5	68	D16	-1330	-238.5	128	DUMMYR1	1900	-238.5	188	G162	4740	110	248	G42	3780	110
9	P68	-4350	-238.5	69	D15	-1270	-238.5	129	DUMMYR2	1950	-238.5	189	G160	4724	227	249	G40	3764	227
10	VDDIO	-4300	-238.5	70	D14	-1210	-238.5	130	Dummy	2000	-238.5	190	G158	4708	110	250	G38	3748	110
11	RCM0	-4250	-238.5	71	D13	-1150	-238.5	131	Dummy	2050	-238.5	191	G156	4692	227	251	G36	3732	227
12	GNDO	-4200	-238.5	72	D12	-1090	-238.5	132	Dummy	2100	-238.5	192	G154	4676	110	252	G34	3716	110
13	RCM1	-4150	-238.5	73	D11	-1030	-238.5	133	Dummy	2150	-238.5	193	G152	4660	227	253	G32	3700	227
14	VDDIO	-4100	-238.5	74	D10	-970	-238.5	134	Dummy	2200	-238.5	194	G150	4644	110	254	G30	3684	110
15	SRGB	-4050	-238.5	75	D9	-910	-238.5	135	Dummy	2250	-238.5	195	G148	4628	227	255	G28	3668	227
16	GNDO	-4000	-238.5	76	D8	-850	-238.5	136	Dummy	2300	-238.5	196	G146	4612	110	256	G26	3652	110
17	SMX	-3950	-238.5	77	D1	-790	-238.5	137	Dummy	2350	-238.5	197	G144	4596	227	257	G24	3636	227
18	VDDIO	-3900	-238.5	78	D3	-730	-238.5	138	Dummy	2400	-238.5	198	G142	4580	110	258	G22	3620	110
19	SMY	-3850	-238.5	79	D5	-670	-238.5	139	Dummy	2450	-238.5	199	G140	4564	227	259	G20	3604	227
20	GNDO	-3800	-238.5	80	D7	-610	-238.5	140	Dummy	2500	-238.5	200	G138	4548	110	260	G18	3588	110
21	IDM	-3750	-238.5	81	TE	-550	-238.5	141	Dummy	2550	-238.5	201	G136	4532	227	261	G16	3572	227
22	VDDIO	-3700	-238.5	82	RESX	-490	-238.5	142	Dummy	2600	-238.5	202	G134	4516	110	262	G14	3556	110
23	REV	-3650	-238.5	83	CSX	-430	-238.5	143	Dummy	2650	-238.5	203	G132	4500	227	263	G12	3540	227
24	GNDO	-3600	-238.5	84	D6	-370	-238.5	144	Dummy	2700	-238.5	204	G130	4484	110	264	G10	3524	110
25	RL	-3550	-238.5	85	D4	-310	-238.5	145	Dummy	2750	-238.5	205	G128	4468	227	265	G8	3508	227
26	VDDIO	-3500	-238.5	86	D2	-250	-238.5	146	AGND	2800	-238.5	206	G126	4452	110	266	G6	3492	110
27	TB	-3450	-238.5	87	IM2	-190	-238.5	147	AGND	2850	-238.5	207	G124	4436	227	267	G4	3476	227
28	GNDO	-3400	-238.5	88	D0	-130	-238.5	148	AGND	2900	-238.5	208	G122	4420	110	268	G2	3460	110
29	SHUT	-3350	-238.5	89	WRX	-70	-238.5	149	VCL	2950	-238.5	209	G120	4404	227	269	DUMMY5	3444	227
30	VDDIO	-3300	-238.5	90	PCLK	0	-238.5	150	VCL	3000	-238.5	210	G118	4388	110	270	DUMMY6	3428	110
31	LCM0	-3250	-238.5	91	DE	50	-238.5	151	VCL	3050	-238.5	211	G116	4372	227	271	DUMMY7	3412	227
32	GNDO	-3200	-238.5	92	HS	100	-238.5	152	Dummy	3100	-238.5	212	G114	4356	110	272	DUMMY8	3396	110
33	LCM1	-3150	-238.5	93	VS	150	-238.5	153	Dummy	3150	-238.5	213	G112	4340	227	273	S396	3380	227
34	VDDIO	-3100	-238.5	94	TESTDA[2]	200	-238.5	154	Dummy	3200	-238.5	214	G110	4324	110	274	S395	3364	110
35	GM2	-3050	-238.5	95	TESTDA[1]	250	-238.5	155	Dummy	3250	-238.5	215	G108	4308	227	275	S394	3348	227
36	GNDO	-3000	-238.5	96	TESTDA[0]	300	-238.5	156	Dummy	3300	-238.5	216	G106	4292	110	276	S393	3332	110
37	GM1	-2950	-238.5	97	DGND	350	-238.5	157	Dummy	3350	-238.5	217	G104	4276	227	277	S392	3316	227
38	VDDIO	-2900	-238.5	98	DGND	400	-238.5	158	Dummy	3400	-238.5	218	G102	4260	110	278	S391	3300	110
39	GM0	-2850	-238.5	99	DGND	450	-238.5	159	Dummy	3450	-238.5	219	G100	4244	227	279	S390	3284	227
40	GNDO	-2800	-238.5	100	DGND	500	-238.5	160	Dummy	3500	-238.5	220	G98	4228	110	280	S389	3268	110
41	SDA	-2750	-238.5	101	DGND	550	-238.5	161	Dummy	3550	-238.5	221	G96	4212	227	281	S388	3252	227
42	GS	-2700	-238.5	102	DGND	600	-238.5	162	Dummy	3600	-238.5	222	G94	4196	110	282	S387	3236	110
43	SPI4W	-2650	-238.5	103	VDDI	650	-238.5	163	Dummy	3650	-238.5	223	G92	4180	227	283	S386	3220	227
44	VDDIO	-2600	-238.5	104	VDDI	700	-238.5	164	Dummy	3700	-238.5	224	G90	4164	110	284	S385	3204	110
45	TESTMODE[2]	-2550	-238.5	105	VDDI	750	-238.5	165	Dummy	3750	-238.5	225	G88	4148	227	285	S384	3188	227
46	TESTDA[5]	-2500	-238.5	106	VDDI	800	-238.5	166	Dummy	3800	-238.5	226	G86	4132	110	286	S383	3172	110
47	TESTDA[4]	-2450	-238.5	107	VDDI	850	-238.5	167	Dummy	3850	-238.5	227	G84	4116	227	287	S382	3156	227
48	TESTDA[3]	-2400	-238.5	108	VDDI	900	-238.5	168	Dummy	3900	-238.5	228	G82	4100	110	288	S381	3140	110
49	TESTOSC	-2350	-238.5	109	VCC	950	-238.5	169	Dummy	3950	-238.5	229	G80	4084	227	289	S380	3124	227
50	OSC	-2300	-238.5	110	VCC	1000	-238.5	170	VGL	4000	-238.5	230	G78	4068	110	290	S379	3108	110
51	VCI	-2250	-238.5	111	VCC	1050	-238.5	171	VGL	4050	-238.5	231	G76	4052	227	291	S378	3092	227
52	VCI	-2200	-238.5	112	VCI1	1100	-238.5	172	VGL	4100	-238.5	232	G74	4036	110	292	S377	3076	110
53	VCI	-2150	-238.5	113	VCI1	1150	-238.5	173	VGH	4150	-238.5	233	G72	4020	227	293	S376	3060	227
54	VCI	-2100	-238.5	114	VCI1	1200	-238.5	174	VGH	4200	-238.5	234	G70	4004	110	294	S375	3044	110
55	VCI	-2050	-238.5	115	Dummy	1250	-238.5	175	VGH	4250	-238.5	235	G68	3988	227	295	S374	3028	227
56	VCI	-2000	-238.5	116	Dummy	1300	-238.5	176	VCOMH	4300	-238.5	236	G66	3972	110	296	S373	3012	110
57	AGND	-1950	-238.5	117	Dummy	1350	-238.5	177	VCOMH	4350	-238.5	237	G64	3956	227	297	S372	2996	227
58	AGND	-1900	-238.5	118	TEST_MODE[0]	1400	-238.5	178	VCOMH	4400	-238.5	238	G62	3940	110	298	S371	2980	110
59	AGND	-1850	-238.5	119	TEST_MODE[1]	1450	-238.5	179	VCOML	4450	-238.5	239	G60	3924	227	299	S370	2964	227
60	AGND	-1800	-238.5	120	AVDD	1500	-238.5	180	VCOML	4500	-238.5	240	G58	3908	110	300	S369	2948	110

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
301	S368	2932	227	361	S308	1972	227	421	S248	1012	227	481	S192	-324	110	541	S132	-1284	110
302	S367	2916	110	362	S307	1956	110	422	S247	996	110	482	S191	-340	227	542	S131	-1300	227
303	S366	2900	227	363	S306	1940	227	423	S246	980	227	483	S190	-356	110	543	S130	-1316	110
304	S365	2884	110	364	S305	1924	110	424	S245	964	110	484	S189	-372	227	544	S129	-1332	227
305	S364	2868	227	365	S304	1908	227	425	S244	948	227	485	S188	-388	110	545	S128	-1348	110
306	S363	2852	110	366	S303	1892	110	426	S243	932	110	486	S187	-404	227	546	S127	-1364	227
307	S362	2836	227	367	S302	1876	227	427	S242	916	227	487	S186	-420	110	547	S126	-1380	110
308	S361	2820	110	368	S301	1860	110	428	S241	900	110	488	S185	-436	227	548	S125	-1396	227
309	S360	2804	227	369	S300	1844	227	429	S240	884	227	489	S184	-452	110	549	S124	-1412	110
310	S359	2788	110	370	S299	1828	110	430	S239	868	110	490	S183	-468	227	550	S123	-1428	227
311	S358	2772	227	371	S298	1812	227	431	S238	852	227	491	S182	-484	110	551	S122	-1444	110
312	S357	2756	110	372	S297	1796	110	432	S237	836	110	492	S181	-500	227	552	S121	-1460	227
313	S356	2740	227	373	S296	1780	227	433	S236	820	227	493	S180	-516	110	553	S120	-1476	110
314	S355	2724	110	374	S295	1764	110	434	S235	804	110	494	S179	-532	227	554	S119	-1492	227
315	S354	2708	227	375	S294	1748	227	435	S234	788	227	495	S178	-548	110	555	S118	-1508	110
316	S353	2692	110	376	S293	1732	110	436	S233	772	110	496	S177	-564	227	556	S117	-1524	227
317	S352	2676	227	377	S292	1716	227	437	S232	756	227	497	S176	-580	110	557	S116	-1540	110
318	S351	2660	110	378	S291	1700	110	438	S231	740	110	498	S175	-596	227	558	S115	-1556	227
319	S350	2644	227	379	S290	1684	227	439	S230	724	227	499	S174	-612	110	559	S114	-1572	110
320	S349	2628	110	380	S289	1668	110	440	S229	708	110	500	S173	-628	227	560	S113	-1588	227
321	S348	2612	227	381	S288	1652	227	441	S228	692	227	501	S172	-644	110	561	S112	-1604	110
322	S347	2596	110	382	S287	1636	110	442	S227	676	110	502	S171	-660	227	562	S111	-1620	227
323	S346	2580	227	383	S286	1620	227	443	S226	660	227	503	S170	-676	110	563	S110	-1636	110
324	S345	2564	110	384	S285	1604	110	444	S225	644	110	504	S169	-692	227	564	S109	-1652	227
325	S344	2548	227	385	S284	1588	227	445	S224	628	227	505	S168	-708	110	565	S108	-1668	110
326	S343	2532	110	386	S283	1572	110	446	S223	612	110	506	S167	-724	227	566	S107	-1684	227
327	S342	2516	227	387	S282	1556	227	447	S222	596	227	507	S166	-740	110	567	S106	-1700	110
328	S341	2500	110	388	S281	1540	110	448	S221	580	110	508	S165	-756	227	568	S105	-1716	227
329	S340	2484	227	389	S280	1524	227	449	S220	564	227	509	S164	-772	110	569	S104	-1732	110
330	S339	2468	110	390	S279	1508	110	450	S219	548	110	510	S163	-788	227	570	S103	-1748	227
331	S338	2452	227	391	S278	1492	227	451	S218	532	227	511	S162	-804	110	571	S102	-1764	110
332	S337	2436	110	392	S277	1476	110	452	S217	516	110	512	S161	-820	227	572	S101	-1780	227
333	S336	2420	227	393	S276	1460	227	453	S216	500	227	513	S160	-836	110	573	S100	-1796	110
334	S335	2404	110	394	S275	1444	110	454	S215	484	110	514	S159	-852	227	574	S99	-1812	227
335	S334	2388	227	395	S274	1428	227	455	S214	468	227	515	S158	-868	110	575	S98	-1828	110
336	S333	2372	110	396	S273	1412	110	456	S213	452	110	516	S157	-884	227	576	S97	-1844	227
337	S332	2356	227	397	S272	1396	227	457	S212	436	227	517	S156	-900	110	577	S96	-1860	110
338	S331	2340	110	398	S271	1380	110	458	S211	420	110	518	S155	-916	227	578	S95	-1876	227
339	S330	2324	227	399	S270	1364	227	459	S210	404	227	519	S154	-932	110	579	S94	-1892	110
340	S329	2308	110	400	S269	1348	110	460	S209	388	110	520	S153	-948	227	580	S93	-1908	227
341	S328	2292	227	401	S268	1332	227	461	S208	372	227	521	S152	-964	110	581	S92	-1924	110
342	S327	2276	110	402	S267	1316	110	462	S207	356	110	522	S151	-980	227	582	S91	-1940	227
343	S326	2260	227	403	S266	1300	227	463	S206	340	227	523	S150	-996	110	583	S90	-1956	110
344	S325	2244	110	404	S265	1284	110	464	S205	324	110	524	S149	-1012	227	584	S89	-1972	227
345	S324	2228	227	405	S264	1268	227	465	S204	308	227	525	S148	-1028	110	585	S88	-1988	110
346	S323	2212	110	406	S263	1252	110	466	S203	292	110	526	S147	-1044	227	586	S87	-2004	227
347	S322	2196	227	407	S262	1236	227	467	S202	276	227	527	S146	-1060	110	587	S86	-2020	110
348	S321	2180	110	408	S261	1220	110	468	S201	260	110	528	S145	-1076	227	588	S85	-2036	227
349	S320	2164	227	409	S260	1204	227	469	S200	244	227	529	S144	-1092	110	589	S84	-2052	110
350	S319	2148	110	410	S259	1188	110	470	S199	228	110	530	S143	-1108	227	590	S83	-2068	227
351	S318	2132	227	411	S258	1172	227	471	Dummy9	212	227	531	S142	-1124	110	591	S82	-2084	110
352	S317	2116	110	412	S257	1156	110	472	Dummy10	196	110	532	S141	-1140	227	592	S81	-2100	227
353	S316	2100	227	413	S256	1140	227	473	Dummy11	-196	110	533	S140	-1156	110	593	S80	-2116	110
354	S315	2084	110	414	S255	1124	110	474	Dummy12	-212	227	534	S139	-1172	227	594	S79	-2132	227
355	S314	2068	227	415	S254	1108	227	475	S198	-228	110	535	S138	-1188	110	595	S78	-2148	110
356	S313	2052	110	416	S253	1092	110	476	S197	-244	227	536	S137	-1204	227	596	S77	-2164	227
357	S312	2036	227	417	S252	1076	227	477	S196	-260	110	537	S136	-1220	110	597	S76	-2180	110
358	S311	2020	110	418	S251	1060	110	478	S195	-276	227	538	S135	-1236	227	598	S75	-2196	227
359	S310	2004	227	419	S250	1044	227	479	S194	-292	110	539	S134	-1252	110	599	S74	-2212	110
360	S309	1988	110	420	S249	1028	110	480	S193	-308	227	540	S133	-1268	227	600	S73	-2228	227

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
601	S72	-2244	110	661	S12	-3204	110	721	G89	-4164	110
602	S71	-2260	227	662	S11	-3220	227	722	G91	-4180	227
603	S70	-2276	110	663	S10	-3236	110	723	G93	-4196	110
604	S69	-2292	227	664	S9	-3252	227	724	G95	-4212	227
605	S68	-2308	110	665	S8	-3268	110	725	G97	-4228	110
606	S67	-2324	227	666	S7	-3284	227	726	G99	-4244	227
607	S66	-2340	110	667	S6	-3300	110	727	G101	-4260	110
608	S65	-2356	227	668	S5	-3316	227	728	G103	-4276	227
609	S64	-2372	110	669	S4	-3332	110	729	G105	-4292	110
610	S63	-2388	227	670	S3	-3348	227	730	G107	-4308	227
611	S62	-2404	110	671	S2	-3364	110	731	G109	-4324	110
612	S61	-2420	227	672	S1	-3380	227	732	G111	-4340	227
613	S60	-2436	110	673	Dummy13	-3396	110	733	G113	-4356	110
614	S59	-2452	227	674	Dummy14	-3412	227	734	G115	-4372	227
615	S58	-2468	110	675	Dummy15	-3428	110	735	G117	-4388	110
616	S57	-2484	227	676	Dummy16	-3444	227	736	G119	-4404	227
617	S56	-2500	110	677	G1	-3460	110	737	G121	-4420	110
618	S55	-2516	227	678	G3	-3476	227	738	G123	-4436	227
619	S54	-2532	110	679	G5	-3492	110	739	G125	-4452	110
620	S53	-2548	227	680	G7	-3508	227	740	G127	-4468	227
621	S52	-2564	110	681	G9	-3524	110	741	G129	-4484	110
622	S51	-2580	227	682	G11	-3540	227	742	G131	-4500	227
623	S50	-2596	110	683	G13	-3556	110	743	G133	-4516	110
624	S49	-2612	227	684	G15	-3572	227	744	G135	-4532	227
625	S48	-2628	110	685	G17	-3588	110	745	G137	-4548	110
626	S47	-2644	227	686	G19	-3604	227	746	G139	-4564	227
627	S46	-2660	110	687	G21	-3620	110	747	G141	-4580	110
628	S45	-2676	227	688	G23	-3636	227	748	G143	-4596	227
629	S44	-2692	110	689	G25	-3652	110	749	G145	-4612	110
630	S43	-2708	227	690	G27	-3668	227	750	G147	-4628	227
631	S42	-2724	110	691	G29	-3684	110	751	G149	-4644	110
632	S41	-2740	227	692	G31	-3700	227	752	G151	-4660	227
633	S40	-2756	110	693	G33	-3716	110	753	G153	-4676	110
634	S39	-2772	227	694	G35	-3732	227	754	G155	-4692	227
635	S38	-2788	110	695	G37	-3748	110	755	G157	-4708	110
636	S37	-2804	227	696	G39	-3764	227	756	G159	-4724	227
637	S36	-2820	110	697	G41	-3780	110	757	G161	-4740	110
638	S35	-2836	227	698	G43	-3796	227	758	Dummy17	-4756	227
639	S34	-2852	110	699	G45	-3812	110	759	Dummy18	-4772	110
640	S33	-2868	227	700	G47	-3828	227				
641	S32	-2884	110	701	G49	-3844	110		ALK-R	4841	-220
642	S31	-2900	227	702	G51	-3860	227		ALK-L	-4841	-220
643	S30	-2916	110	703	G53	-3876	110				
644	S29	-2932	227	704	G55	-3892	227				
645	S28	-2948	110	705	G57	-3908	110				
646	S27	-2964	227	706	G59	-3924	227				
647	S26	-2980	110	707	G61	-3940	110				
648	S25	-2996	227	708	G63	-3956	227				
649	S24	-3012	110	709	G65	-3972	110				
650	S23	-3028	227	710	G67	-3988	227				
651	S22	-3044	110	711	G69	-4004	110				
652	S21	-3060	227	712	G71	-4020	227				
653	S20	-3076	110	713	G73	-4036	110				
654	S19	-3092	227	714	G75	-4052	227				
655	S18	-3108	110	715	G77	-4068	110				
656	S17	-3124	227	716	G79	-4084	227				
657	S16	-3140	110	717	G81	-4100	110				
658	S15	-3156	227	718	G83	-4116	227				
659	S14	-3172	110	719	G85	-4132	110				
660	S13	-3188	227	720	G87	-4148	227				



6. Function Description

6.1 MCU Interface Type Selection

The selection of a given interfaces are done by setting P68, IM2, IM1, and IM0 pins as show in below tables.

Table 6.1.1 MCU Interface Type Selection

P68	IM2	IM1	IM0	Interface	Read back selection
-	0	-	-	Serial interface	Via the read instruction (8-bit, 24-bit and 32-bit read parameter)
0	1	0	0	8080 MCU 8-bit Parallel	RDX strobe(8-bit read data and 8-bit read parameter)
0	1	0	1	8080 MCU 16-bit Parallel	RDX strobe(16-bit read data and 8-bit read parameter)
0	1	1	0	8080 MCU 9-bit Parallel	RDX strobe(9-bit read data and 8-bit read parameter)
0	1	1	1	8080 MCU 18-bit Parallel	RDX strobe(18-bit read data and 8-bit read parameter)
1	1	0	0	6800 MCU 8-bit Parallel	E strobe(8-bit read data and 8-bit read parameter)
1	1	0	1	6800 MCU 16-bit Parallel	E strobe(9-bit read data and 8-bit read parameter)
1	1	1	0	6800 MCU 9-bit Parallel	E strobe(16-bit read data and 8-bit read parameter)
1	1	1	1	6800 MCU 18-bit Parallel	E strobe(18-bit read data and 8-bit read parameter)

6.2 Serial Interface

The Module uses a 3-wire 9-bit serial interface or 4-pins/8-bit bi-directional interface for communication between the micro controller and the LCD driver chip. The 3-pins serial use: CSX (chip enable), SCL(serial clock) and SDA(serial data input/output) and the 4-pins serial use: CSX(chip enable), D/CX(data/ command select), SCL(serial clock), and SDA(serial data input/output).

Table 6.2.1 Serial Interface Type Selection

IM2	4WSPI	Interface	Read back selection
0	0	3-Pins Serial Interface	Via the read instruction(8-bit, 24-bit and 32-bit read parameter)
0	1	4-Pins Serial Interface	Via the read instruction(8-bit, 24-bit and 32-bit read parameter)

6.2.1 Command Write

The write mode of the interface means the micro controller writes commands and data to the LCD driver. 3-pins serial data packet contains a control bit D/CX and a transmission byte and in 4-pins serial case, data packet contains just transmission byte and control bit D/CX is transferred by the D/CX pin. If D/CX is “low”, the transmission byte is interpreted as a command byte. If D/CX is “high”, the transmission byte is stored in the display data RAM (Memory write command), or command register as parameter.

Any instruction can be sent in any orders to the Driver. The MSB is transmitted first. The serial interface is initialized when CSX is high status. In this state, SCL clock pulse or SDA data have no effect. A falling edge on CSX enables the serial interface and indicated the start of data transmission.

Figure1: 3-pins Serial Data Stream Format

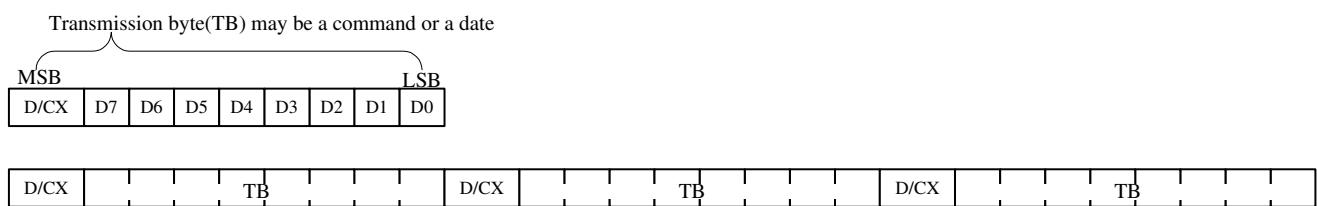
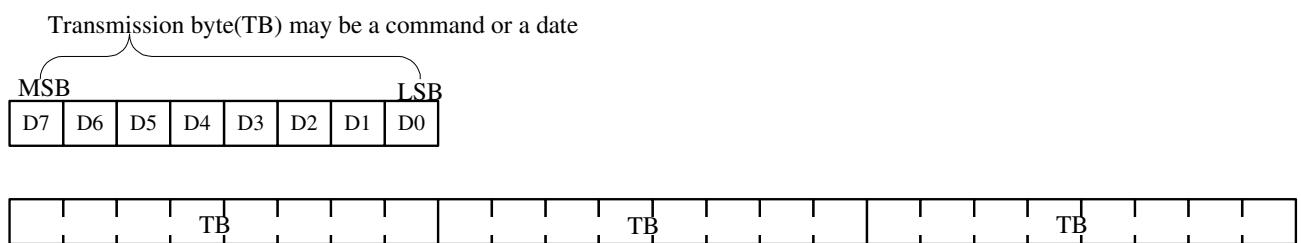
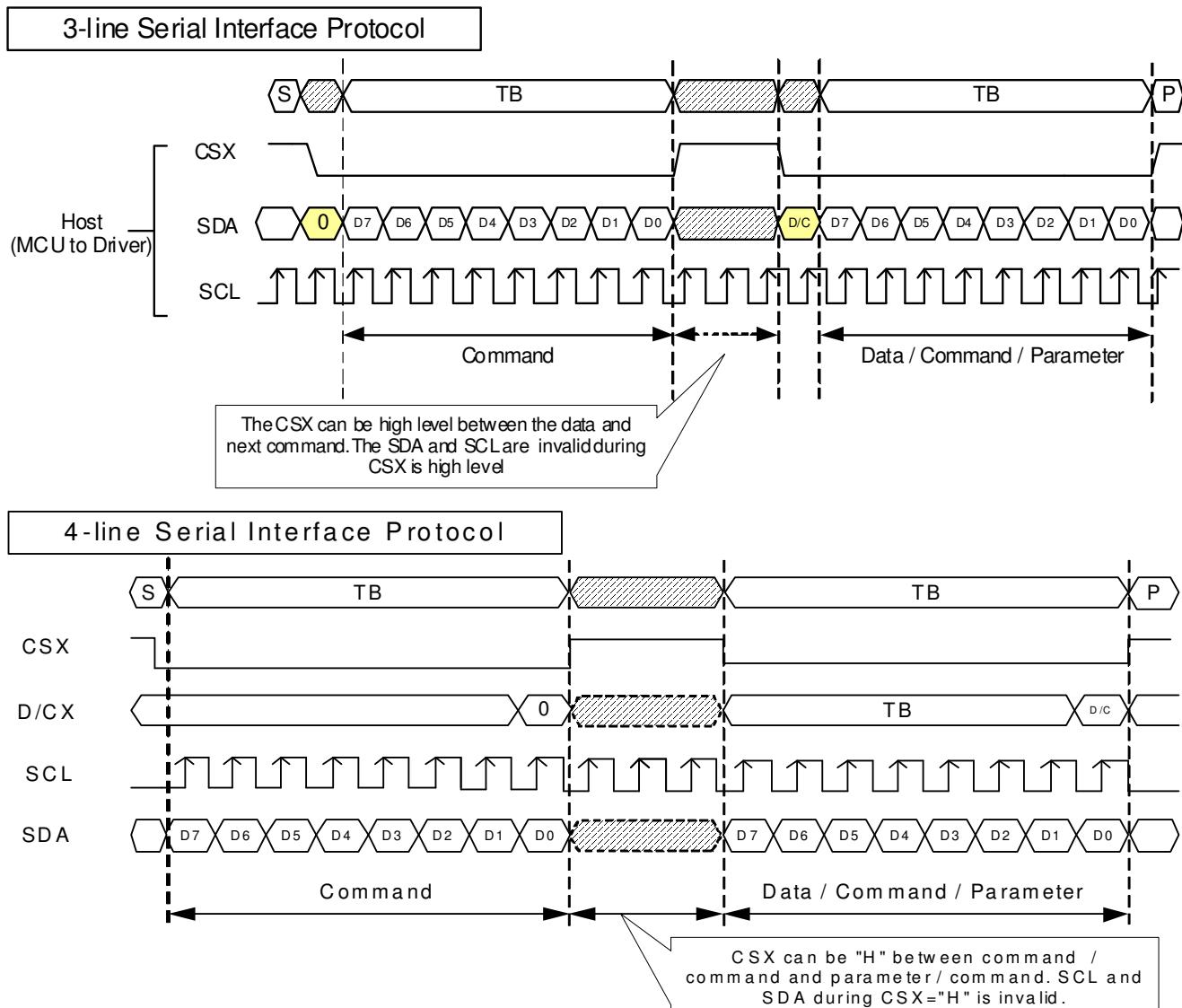


Figure2: 4-pins Serial Data Stream Format



When CSX is “high”, SCL clock is ignored. At the falling edge of CSX, SCL can be high or low. SDA is sampled at the rising edge of CSX. D/CX indicates, whether the byte is command code (D/CX='0') or parameter/RAM data (D/CX='1'). If CSX stays low after the last bit of command/data byte, the serial interface expects the D/CX bit (3-pin serial interface) or D7(4-pins serial interface) of the next byte at the next rising edge of SCL.



6.2.2 Read Function

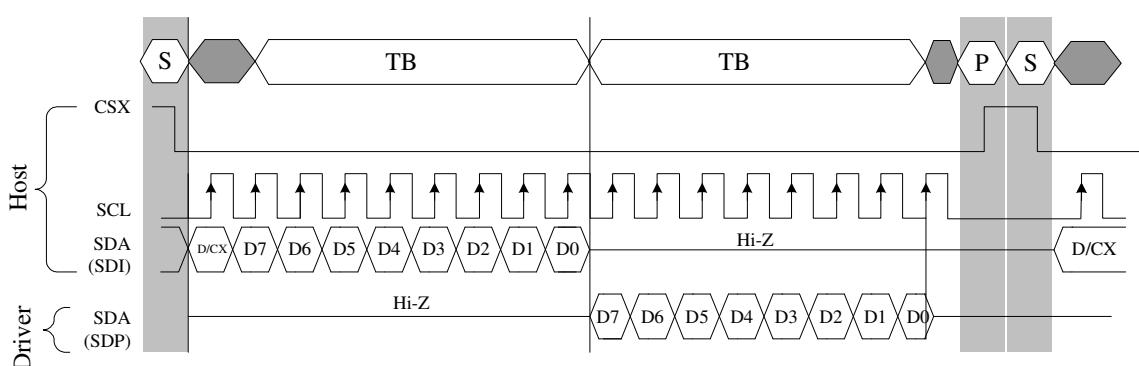


Figure3: 3-Pins Serial Protocol (for DAH/DBH/DCH/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh command: 8-bit read)

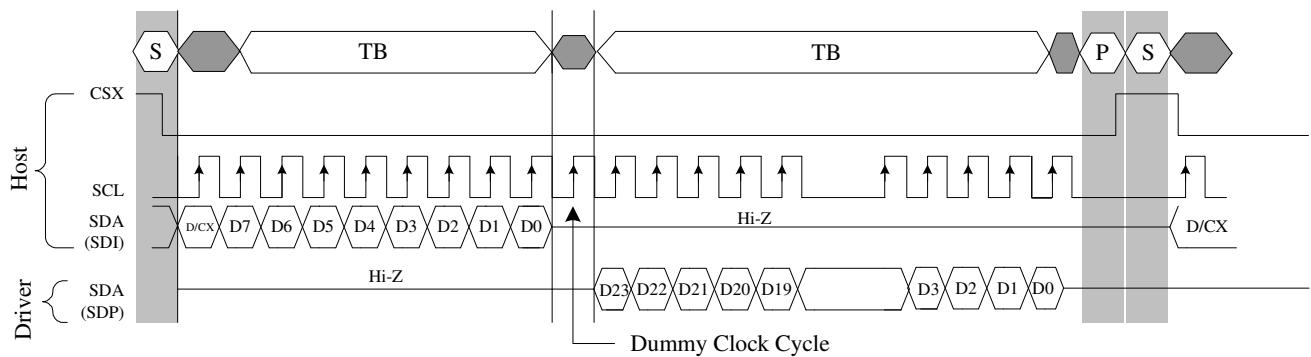


Figure4: 3-Pins Serial Protocol (for 04H command: 24-bit read)

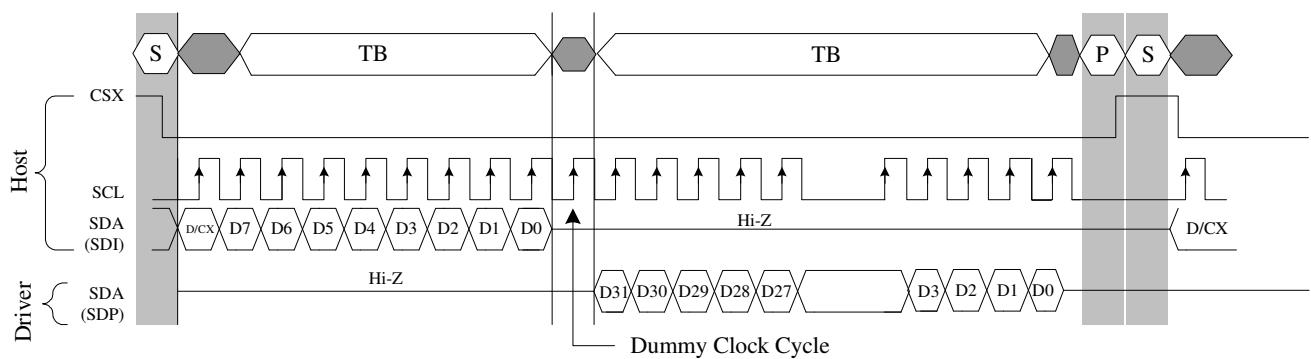


Figure5: 3-Pins Serial Protocol (for 09H command: 32-bit read)

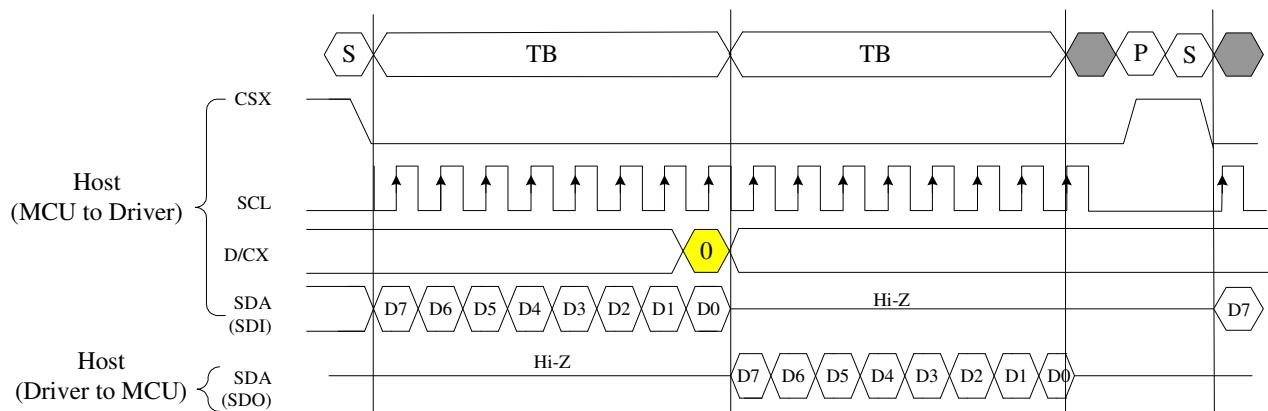


Figure6: 4-pins Serial Protocol (for DAH/DBH/DCH/0AH/0BH/0CH/0DH/0EH/0FH command: 8-bit read)

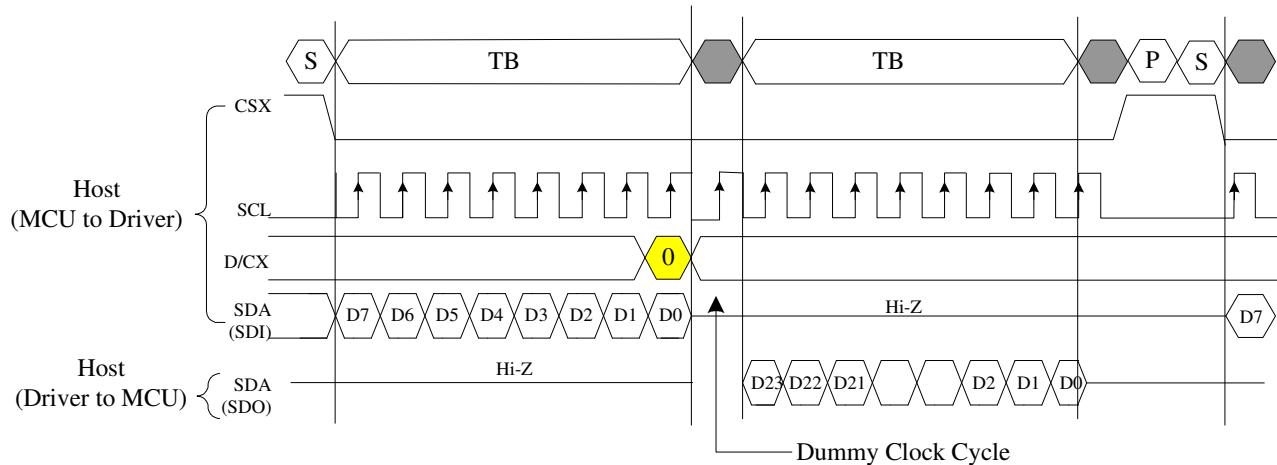


Figure7: 4-pins Serial Protocol (for 04H command: 24-bit read)

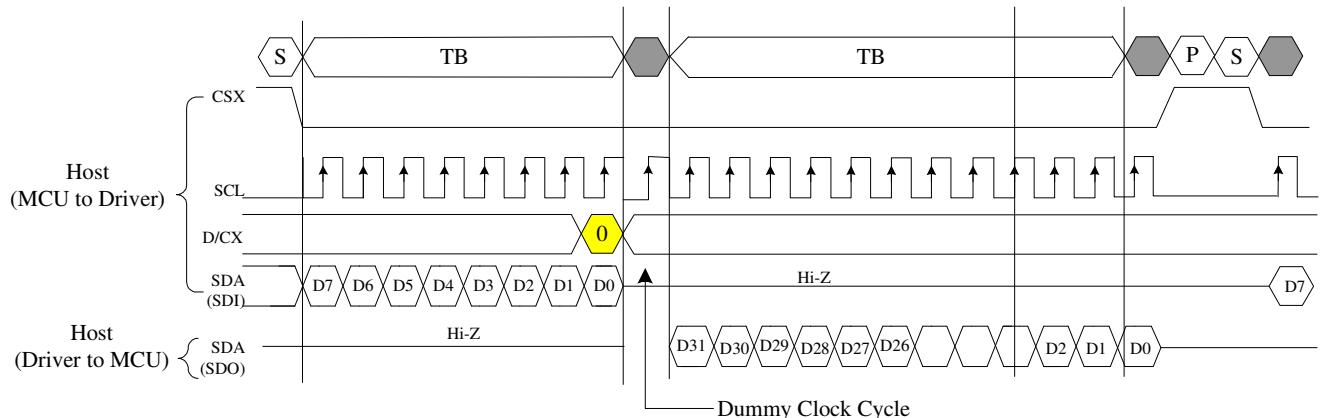


Figure8: 4-pins Serial Protocol (for 09H command: 32-bit read)

6.3 8080-Series Parallel Interface (P68='0')

The MCU uses a 11-wires 8-data parallel interface or 12-wires 9-data parallel interface or 19-wires 16-data parallel interface or 21-wires 18-data parallel interface. The chip-select CSX (active low) enables and disables the parallel interface. RESX (active low) is an external reset signal. WRX is the parallel data write, RDX is the parallel data read and D[17:0] is parallel data.

The graphics controller chip reads the data at the rising edge of WRX signal. The D/CX is the data/command flag. When D/CX='1', D[17,0] bits are display RAM data or command parameters. When D/C='0', D[17,0] bits are commands.

The 8080-series bi-direction interface can be used for communication between the micro controller and LCD driver chip. The selection of this interface is done when P68 pin is low state (GND). Interface bus width can be selected with IM2, IM1 and IM0. The interface function of 8080-series parallel interface are given in Table 6.3.1.

Table 6.3.1The function of 8080-series parallel interface

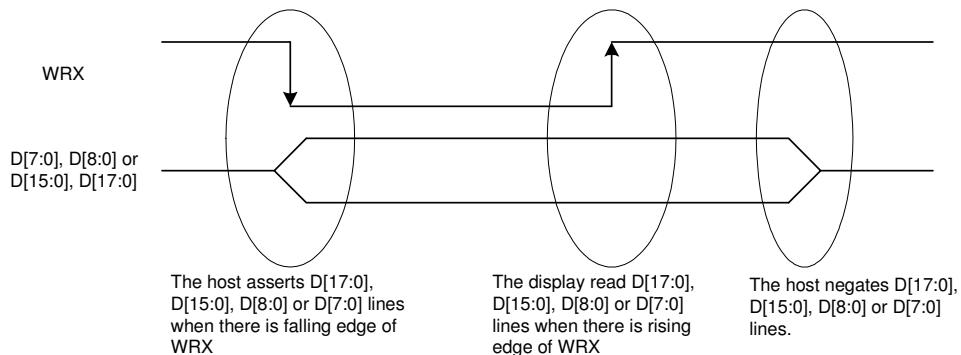
P68	IM2	IM1	IM0	Interface	D/CX	RDX	WRX	Function
0	1	0	0	8-bit Parallel	0	1	↑	Write 8-bit command(D7 to D0)
					1	1	↑	Write 8-bit display data or 8-bit parameter(D7 to D0)
					1	↑	1	Read 8-bit display data(D7 to D0)
					1	↑	1	Read 8-bit parameter or status(D7 to D0)
0	1	0	1	16-bit Parallel	0	1	↑	Write 8-bit command(D7 to D0)
					1	1	↑	Write 16-bit display data or 8-bit parameter(D15 to D0)
					1	↑	1	Read 16-bit display data(D15 to D0)
					1	↑	1	Read 8-bit parameter or status(D7 to D0)
0	1	1	0	9-bit Parallel	0	1	↑	Write 8-bit command(D7 to D0)
					1	1	↑	Write 9-bit display data or 8-bit parameter(D8 to D0)
					1	↑	1	Read 9-bit display data (D8 to D0)
					1	↑	1	Read 8-bit parameter or status(D7 to D0)
0	1	1	1	18-bit Parallel	0	1	↑	Write 8-bit command(D7 to D0)
					1	1	↑	Write 18-bit display data or 8-bit parameter(D17 to D0)
					1	↑	1	Read 18-bit display data(D17 to D0)
					1	↑	1	Read 8-bit parameter or status(D7 to D0)

Note: Reading operation applied for command code: DAh, DBh, DCh, 04h, 09h, 0Ah, 0Bh, 0Ch, 0Dh, 0Eh, 0Fh

6.3.1 Write Cycle/Sequence

The write cycle means that the host writes information (command or/and data) to the display via the interface.

Each write cycle (WRX high-low-high sequence) consists of 3 control (D/CX, RDX, WRX) and data signals (D[17...0]). D/CX bit is a control signal, which tells if the data is a command or a data. The data signals are a command if the control signal is low (= '0') and vice versa it is data (= '1'). The write cycle is described in the following figure.



Note: WRX is an unsynchronized signal (it can be stopped)

Figure9: 8080-Series WRX Protocol

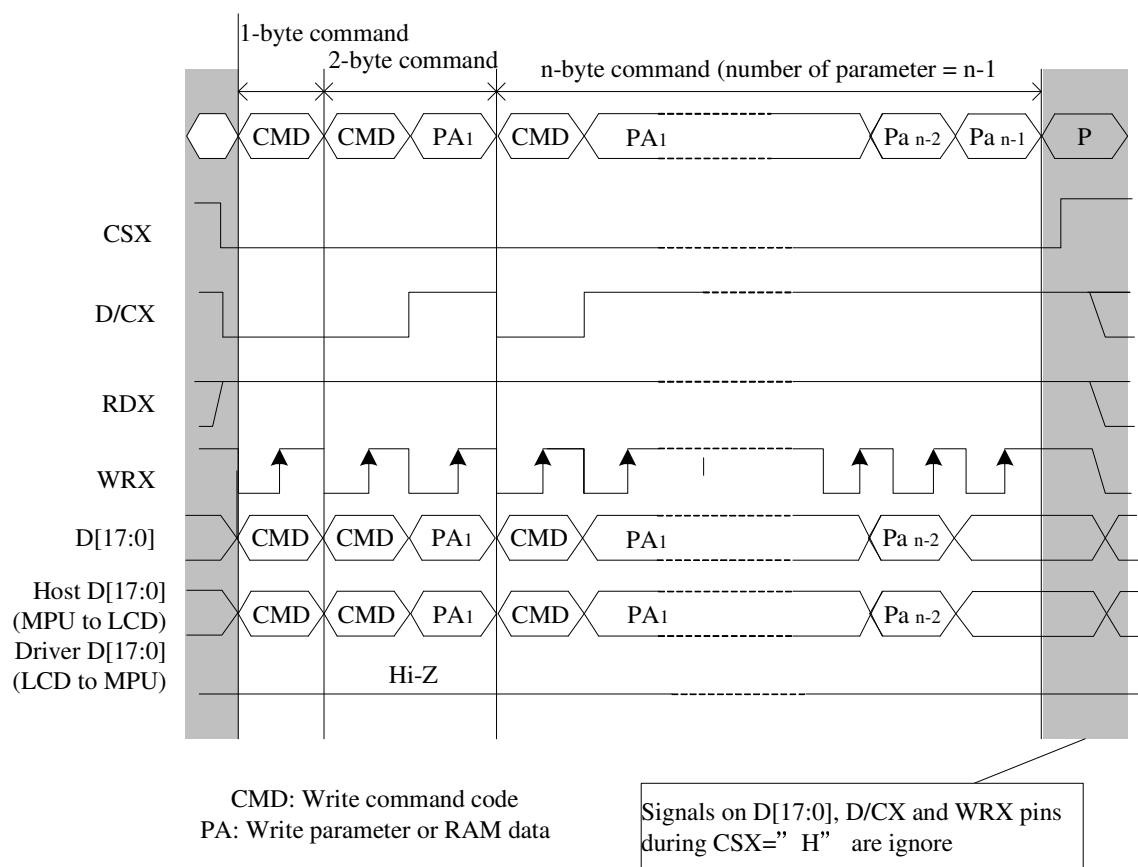
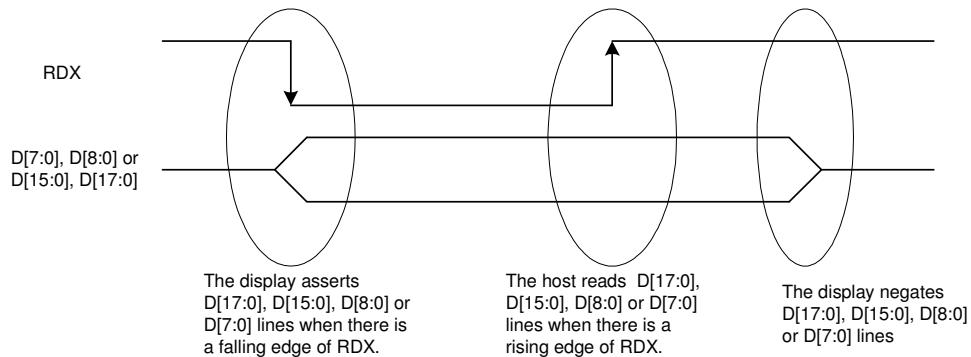


Figure10: 8080-Series Parallel bus protocol (write to register or display RAM)

6.3.2 Read Cycle/Sequence

The read cycle (RDX high-low-high sequence) means that the host reads information from the display via interface. The display sends data (D[17...0]) to the host when there is a falling edge of RDX and the host reads data when there is a rising edge of RDX.



Note: RDX is an unsynchronized signal (It can be stopped).

Figure11: 8080-Series RDX Protocol

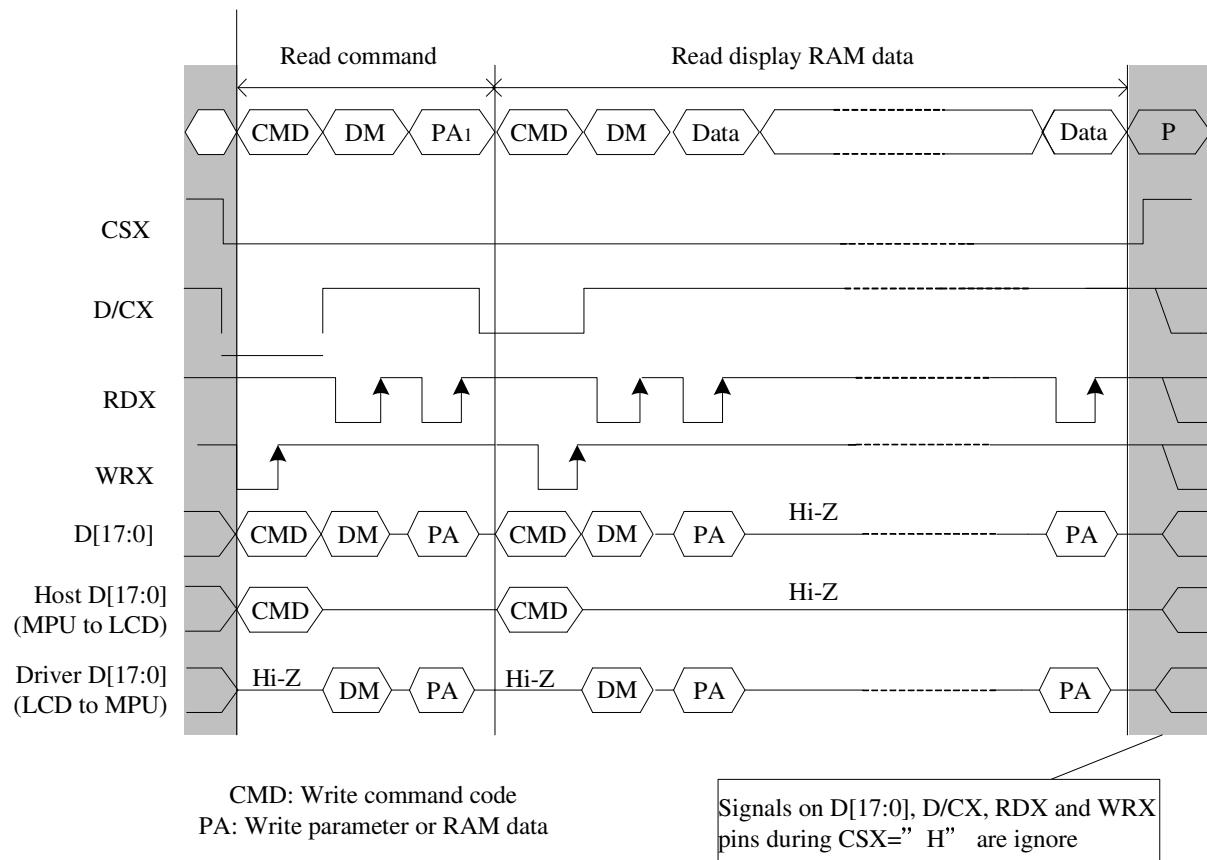


Figure12: 8080-Series parallel bus protocol (Read from register or display RAM)

6.4 6800-Series Parallel Interface (P68='1')

The MCU uses a 11-wires 8-data parallel interface or 12-wires 9-data parallel interface or 19-wires 16-data parallel interface or 21-wires 18-data parallel interface. The chip-select CSX(active low) enables and disables the parallel interface. RESX(active low) is an external reset signal. WRX is the parallel data write, RDX is the parallel data read and D[17:0] is parallel data.

The Graphics Controller Chip reads the data at the falling edge of E signal when R/WX='1' and writes the data at the falling of the E signal when R/WX='0'. The D/CX is the data/command flag. When D/CX='1', D[17,0] bits are display RAM data or command parameters. When D/C='0', D[17,0] bits are commands.

The 6800-series bi-direction interface can be used for communication between the micro controller and LCD driver chip. The selection of this interface is done when P68 pin is high state (VDDI). Interface bus width can be selected with IM2, IM1 and IM0. The interface function of 6800-series parallel interface are given in Table 6.4.1.

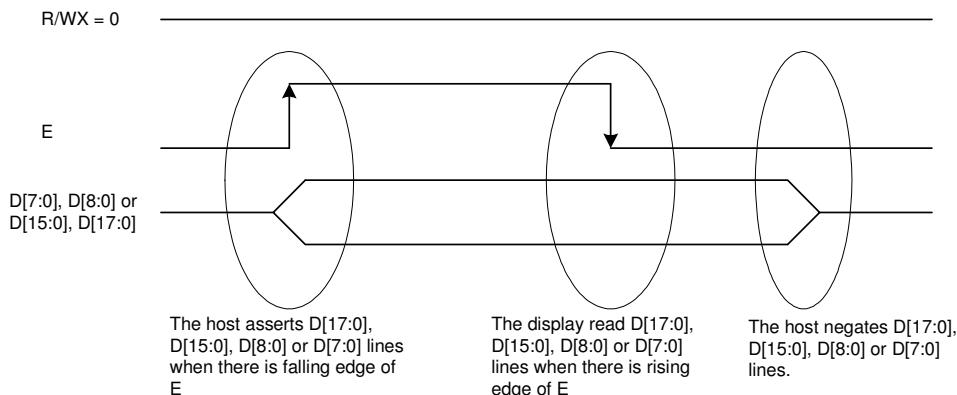
Table 6.4.1 The function of 6800-series parallel interface

P68	IM2	IM1	IM0	Interface	D/CX	RDX	E	Function
1	1	0	0	8-bit Parallel	0	1	↓	Write 8-bit command(D7 to D0)
					1	1	↓	Write 8-bit display data or 8-bit parameter(D7 to D0)
					1	↓	1	Read 8-bit display data(D7 to D0)
					1	↓	1	Read 8-bit parameter or status(D7 to D0)
1	1	0	1	16-bit Parallel	0	1	↓	Write 8-bit command(D7 to D0)
					1	1	↓	Write 16-bit display data or 8-bit parameter(D15 to D0)
					1	↓	1	Read 16-bit display data(D15 to D0)
					1	↓	1	Read 8-bit parameter or status(D7 to D0)
1	1	1	0	9-bit Parallel	0	1	↓	Write 8-bit command(D7 to D0)
					1	1	↓	Write 9-bit display data or 8-bit parameter(D8 to D0)
					1	↓	1	Read 9-bit display data (D8 to D0)
					1	↓	1	Read 8-bit parameter or status(D7 to D0)
1	1	1	1	18-bit Parallel	0	1	↓	Write 8-bit command(D7 to D0)
					1	1	↓	Write 18-bit display data or 8-bit parameter(D17 to D0)
					1	↓	1	Read 18-bit display data(D17 to D0)
					1	↓	1	Read 8-bit parameter or status(D7 to D0)

Note : Reading operation applied for command code : DAh, DBh, DCh, 04h, 09h, 0Ah, 0Bh, 0Ch, 0Dh, 0Eh, 0Fh

6.4.1 Write Cycle/Sequence

The write cycle means that the host writes information (command or/and data) to the display via the interface. Each write cycle (E low-high-low sequence) consists of 3 control (D/CX, E, R/WX) and data signals (D[17...0]). D/CX bit is a control signal, which tells if the data is a command or a data. The data signals are a command if the control signal is low (= '0') and vice versa it is data (= '1'). The write cycle is described in the following figure.



Note: E is unsynchronized signal (it can be stopped)

Figure13: 6800-Series Write Protocol

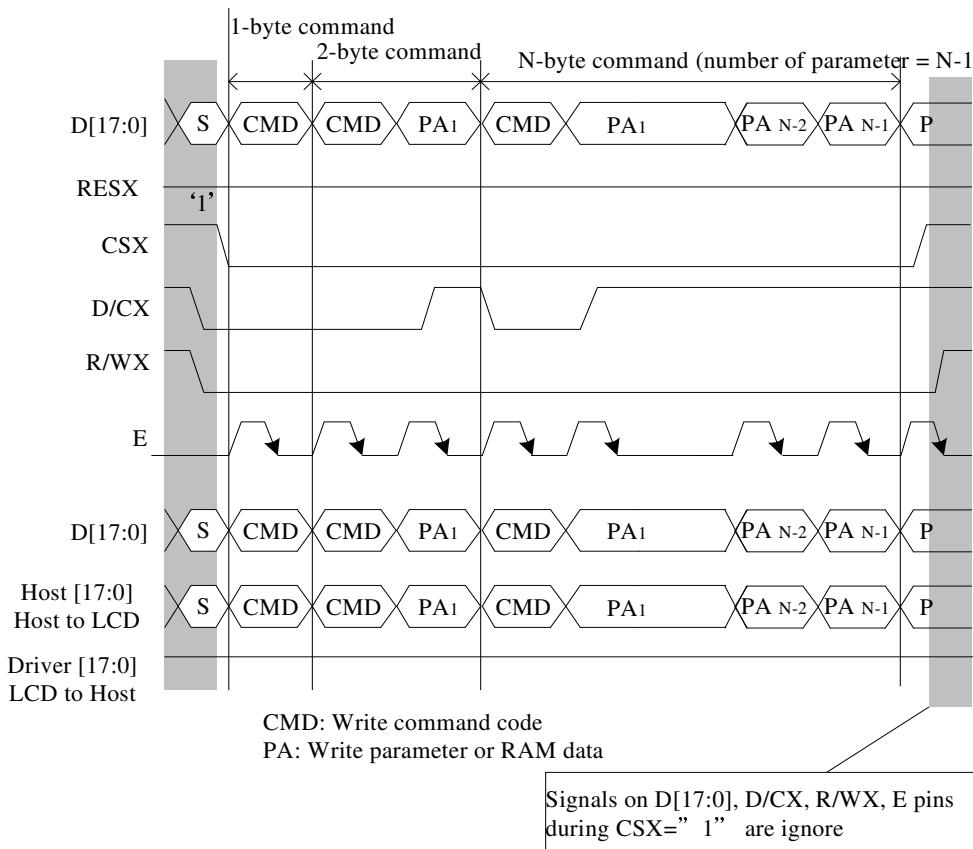
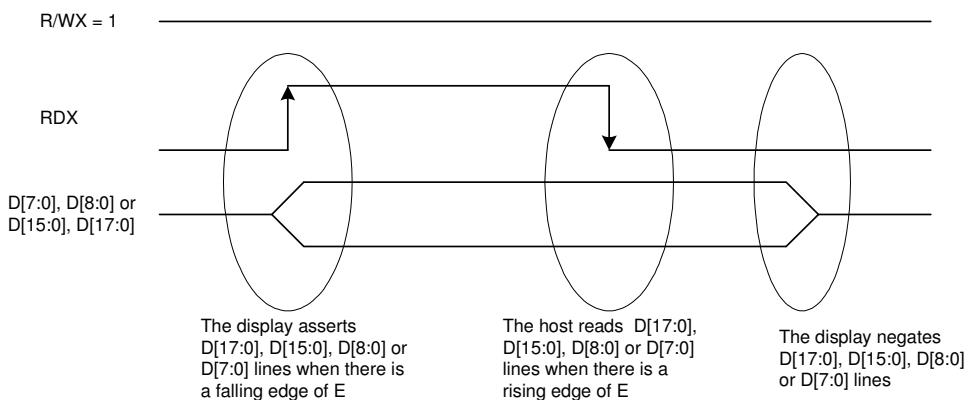


Figure14: 6800-Series parallel bus protocol (write to register or display RAM)

6.4.2 Read Cycle/Sequence

The read cycle means that the host reads information (command or/and data) to the display via the interface. Each read cycle (E low-high-low sequence) consists of 3 control (D/CX, E, R/WX) and data (D[17...0]). D/CX bit is control signal, which tells if the data is a command or a data. The data signals are the command if the control signal is low ($='0'$) and vice versa it is data ($='1'$)



Note: E is an unsynchronized signal (It can be stopped).

Figure15: 6800-Series Read Protocol

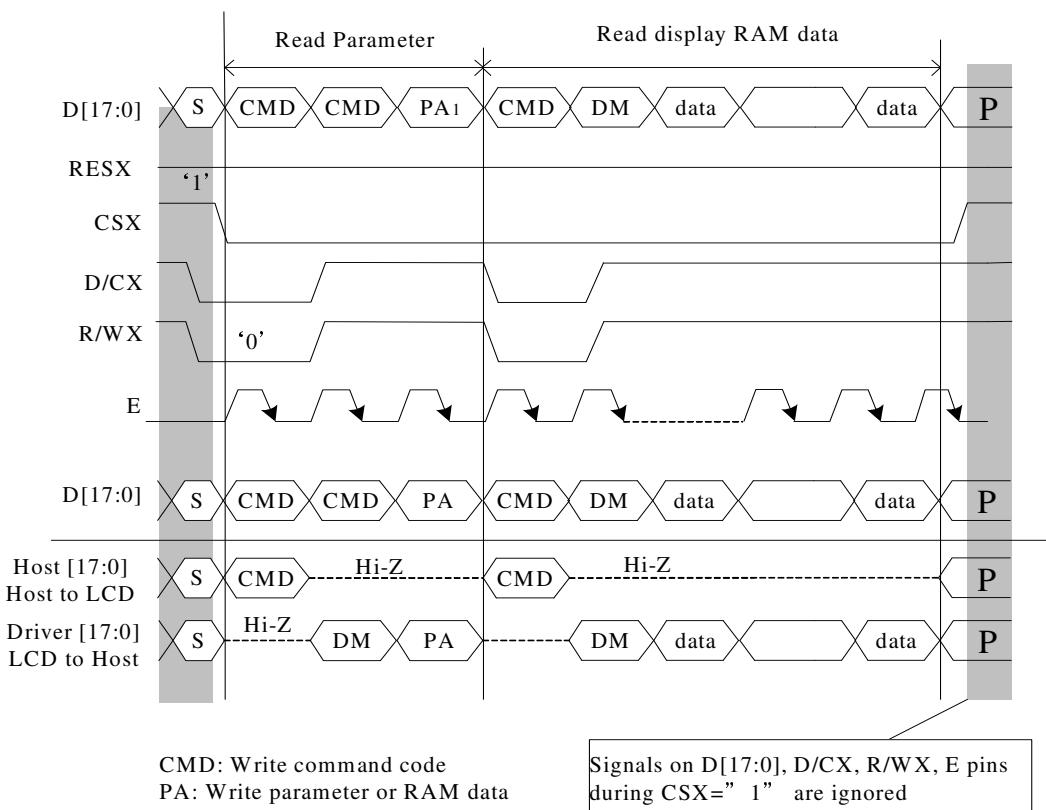


Figure16: 6800-Series Parallel bus protocol (Read from register or display RAM)

6.5 Display Data Transfer Recovery

If there is a break in data transmission by RESX pulse, while transferring a Command or Frame Memory Data or Multiple Parameter command Data, before Bit D0 of the byte has been completed, then DRIVER will reject the previous bits and have reset the interface such that it will be ready to receive command data again when the chip select line (CSX) is next activated after RESX have been High state. See the following example.

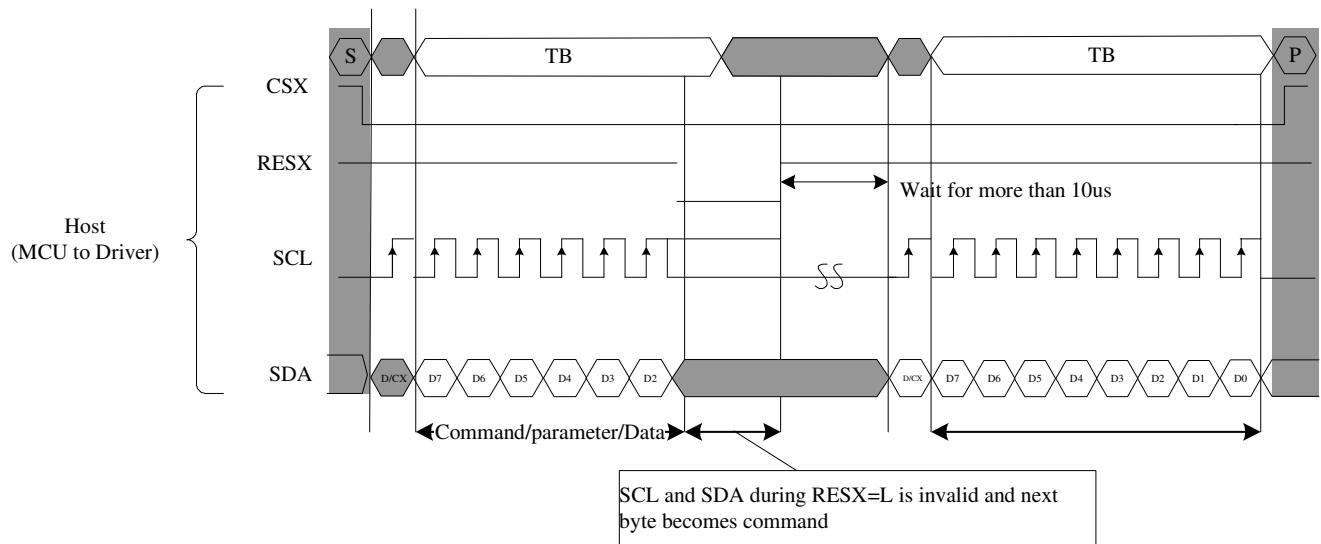


Figure17: Serial bus protocol, write mode – interrupted by RESX

If there is a break in data transmission by CSX pulse, while transferring a Command or Frame Memory Data or Multiple Parameter command data, before Bit D0 of the byte has been completed. Then the DRIVER will reject the previous bits and have reset the interface such that it will be ready to receive the same byte re-transmitted when the chip select line(CSX) is next activated. See the following example.

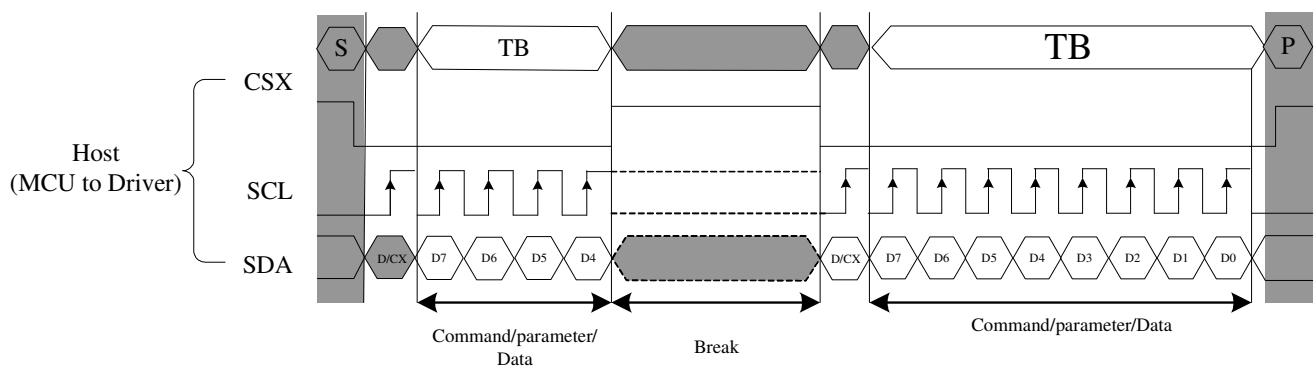


Figure18: Serial bus protocol, write mode – interrupted by CSX

If 1, 2 or more parameter command is being sent and a break occurs while sending any parameter before the last one and if the host then sends a new command rather than re-transmitting the parameter that was interrupted, then the parameters that were successfully sent are stored and the parameter where the break occurred is rejected. The interface is ready to receive next byte as show below.

Note: Break can be e.g. another command or noise pulse.

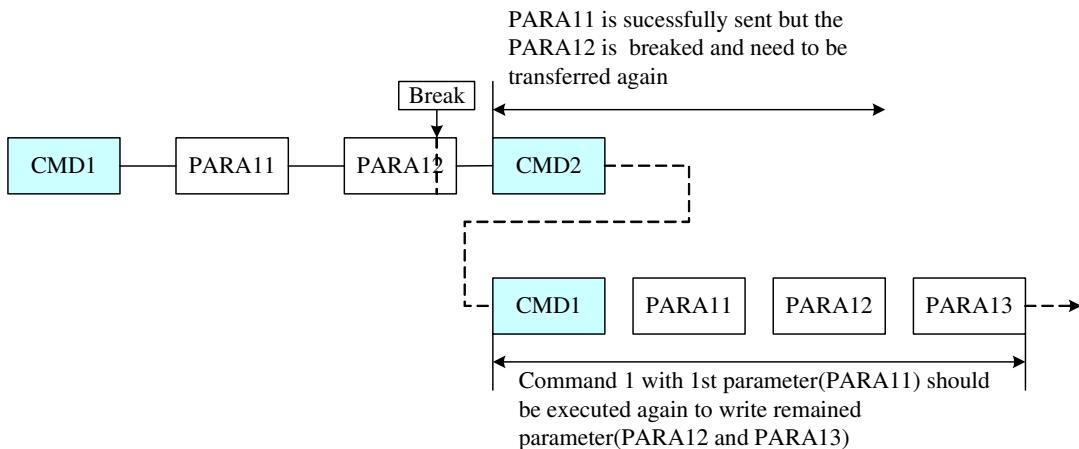


Figure19: Write interrupts recovery (serial interface)

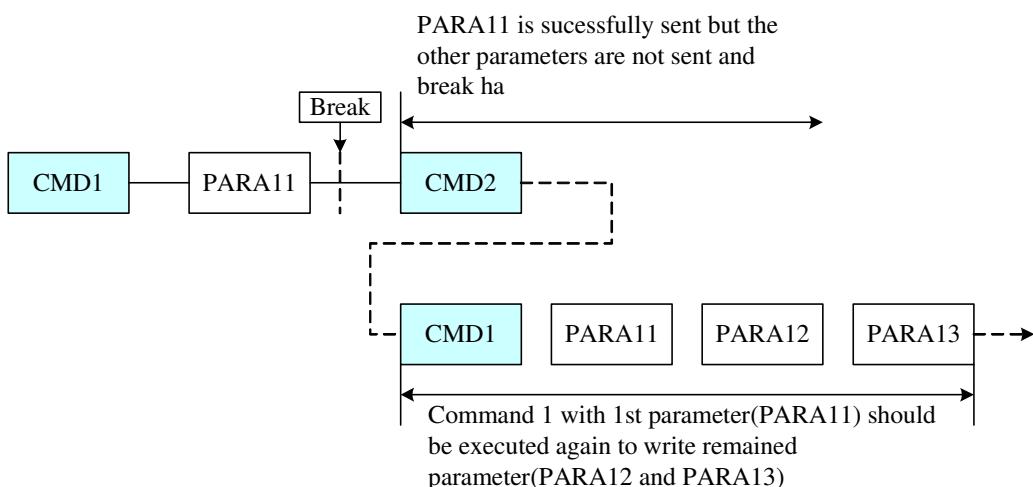


Figure20: Write interrupts recovery (both serial and parallel interface)

6.6 Display Data Transfer Pause

It will be possible when transferring a Command, Frame Memory Data or Multiple Parameter Data to invoke a pause in the data transmission. If the Chip Select Line is released after a whole byte of a Frame Memory Data or Multiple Parameter Data has been completed, then the Display Module will wait and continue the Frame Memory Data or Parameter Data Transmission from the point where it was paused. If the Chip Select Line is released after a whole byte of a command has been completed, then the Display Module will receive either the command's parameters (if appropriate) or a new command when the Chip Select Line is next enabled as shown below:

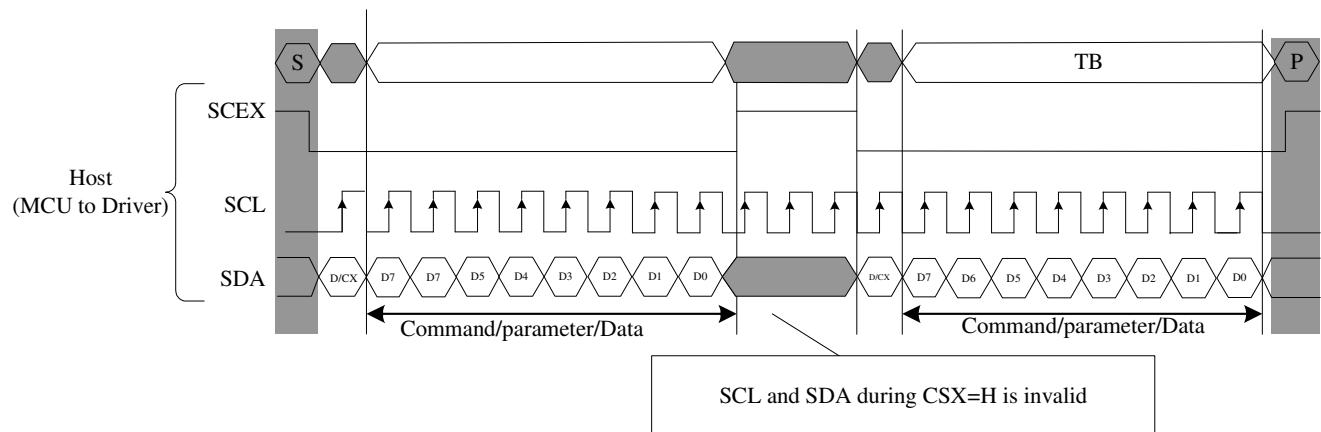


Figure21: Serial interface Pause Protocol (pause by CSX)

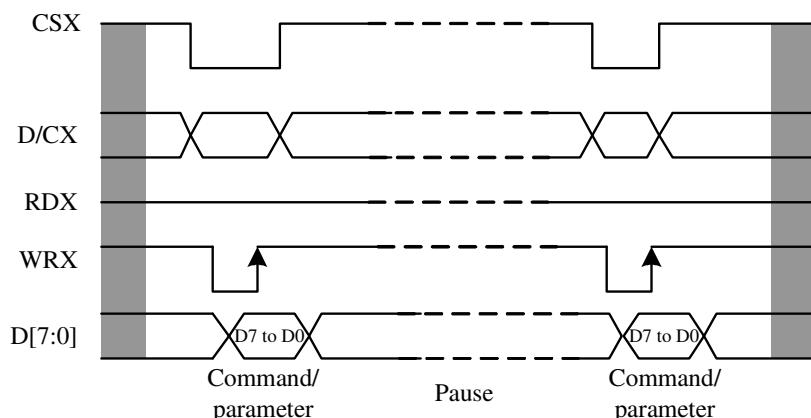


Figure22: Parallel bus Pause Protocol (paused by CSX)

This applies to the following 4 conditions:

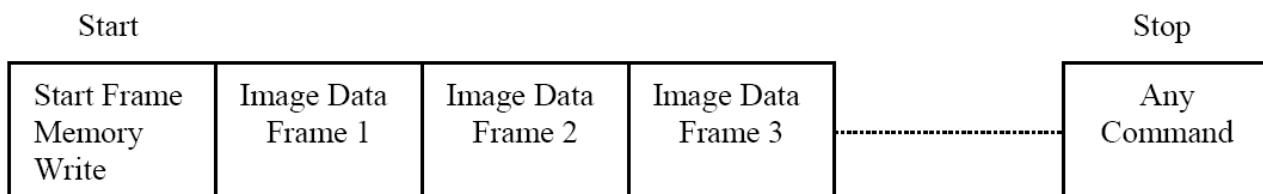
1. Command-Pause-Command
2. Command-Pause-Parameter
3. Parameter-Pause-Command
4. Parameter-Pause-Parameter

6.7 Display Data Transfer Mode

The data format is described for each interface. Data can be downloaded to the Frame Memory by 2 methods.

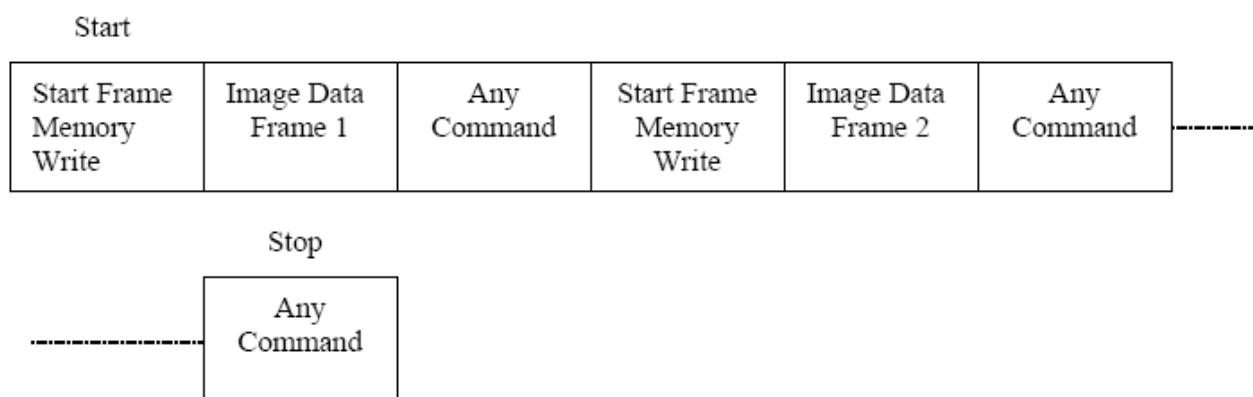
Method 1:

The Image data is sent to the Frame Memory in successive Frame writes, each time the Frame Memory is filled, the Frame Memory pointer is reset to the start point and the next Frame is written.



Method 2:

Image Data is sent and at the end of each Frame Memory download, a command is sent to stop Frame Memory Write. Then Start Memory Write command is sent, and a new Frame is downloaded.



Note:

1. These apply to this Data Transfer Color mode on both Serial and Parallel interfaces.
2. The Frame Memory can contain both odd and even number of pixels for both Methods. Only complete pixel data will be stored in the Frame Memory.

6.8 RGB Interface

6.8.1 RGB Interface Selection

The RGB interface mode is available for ILI9163C and the interface is selected by setting the VIPF[3:0] bits as following table.

VIPF[3:0]				RGB Interface	Data Bus
0	1	1	0	18-bit RGB interface	D[17:0]
0	1	0	1	16-bit RGB interface	D[17:13], D[11:1]
1	1	1	0	6-bitRGB interface	D[7:2]
Others		Setting prohibited			

The display operation via RGB interface is synchronized with the VS, HS and PCLK signals. The RGB interface transfers the updated data to GRAM and the update area is defined by the window address function. The back porch and back porch are used to set the RGB interface timing.

Parallel RGB Interface Set Table

18-bit data bus interface (D[17:0] is used) , VIPF[3:0] = 0110

	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
18bpp Frame Memory Write	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]

16-bit data bus interface (D[17:13] and D[11:1] are used) , VIPF[3:0] = 0101

	D17	D16	D15	D14	D13	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1
16bpp Frame Memory Write	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]

6-bit data bus interface (D[7:2] is used) , VIPF[3] = 1110

	First Transfer						Second Transfer						Third Transfer					
	D7	D6	D5	D4	D3	D2	D7	D6	D5	D4	D3	D2	D7	D6	D5	D4	D3	D2
18bpp Frame Memory Write	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]

Pixel clock (PCLK) is running all the time without stopping and it is used to entering VS, HS, EN and D[17:0] states when there is a rising edge of the PCLK. The PCLK can not be used as continues internal clock for other functions of the display module.

Vertical synchronization (VS) is used to tell when there is received a new frame of the display. This is high enable and its state is read to the display module by a rising edge of the PCLK signal.

Horizontal synchronization (HS) is used to tell when there is received a new line of the frame. This is low enable and its state is read to the display module by a rising edge of the PCLK signal.

Data Enable (EN) is used to tell when there is received RGB information that should be transferred on the display. This is a high enable and its state is read to the display module by a rising edge of the PCLK signal. D[17:0] are used to tell what is the information of the image that is transferred on the display (When EN= '1' and there is a rising edge of PCLK). D[17:0] can be '0' (low) or '1' (high). These lines are read by a rising edge of the PCLK signal.

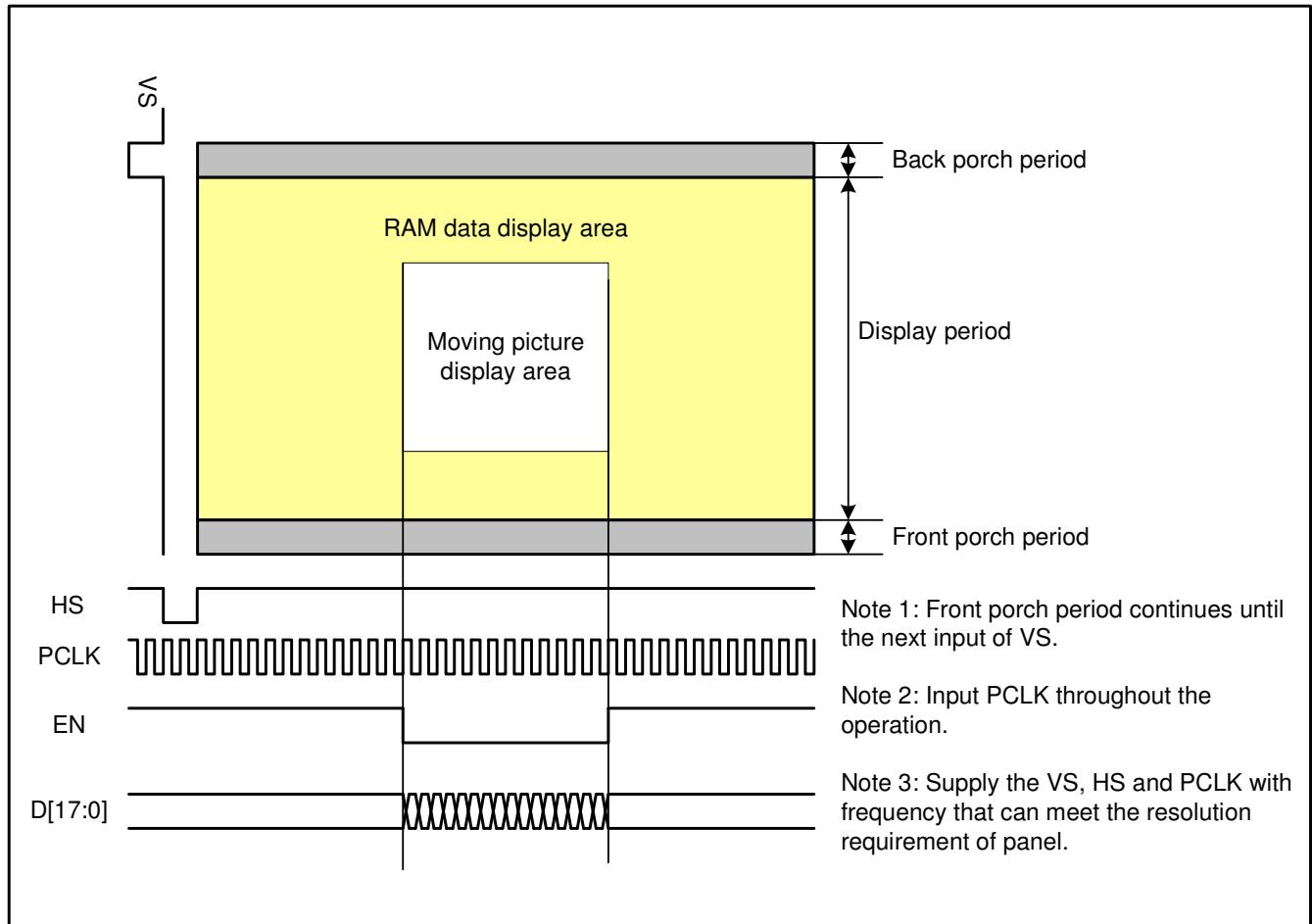


Figure23: GRAM Access Area by RGB Interface

6.8.2 RGB Interface Timing

The timing chart of 18-/16-bit RGB interface mode is shown as below.

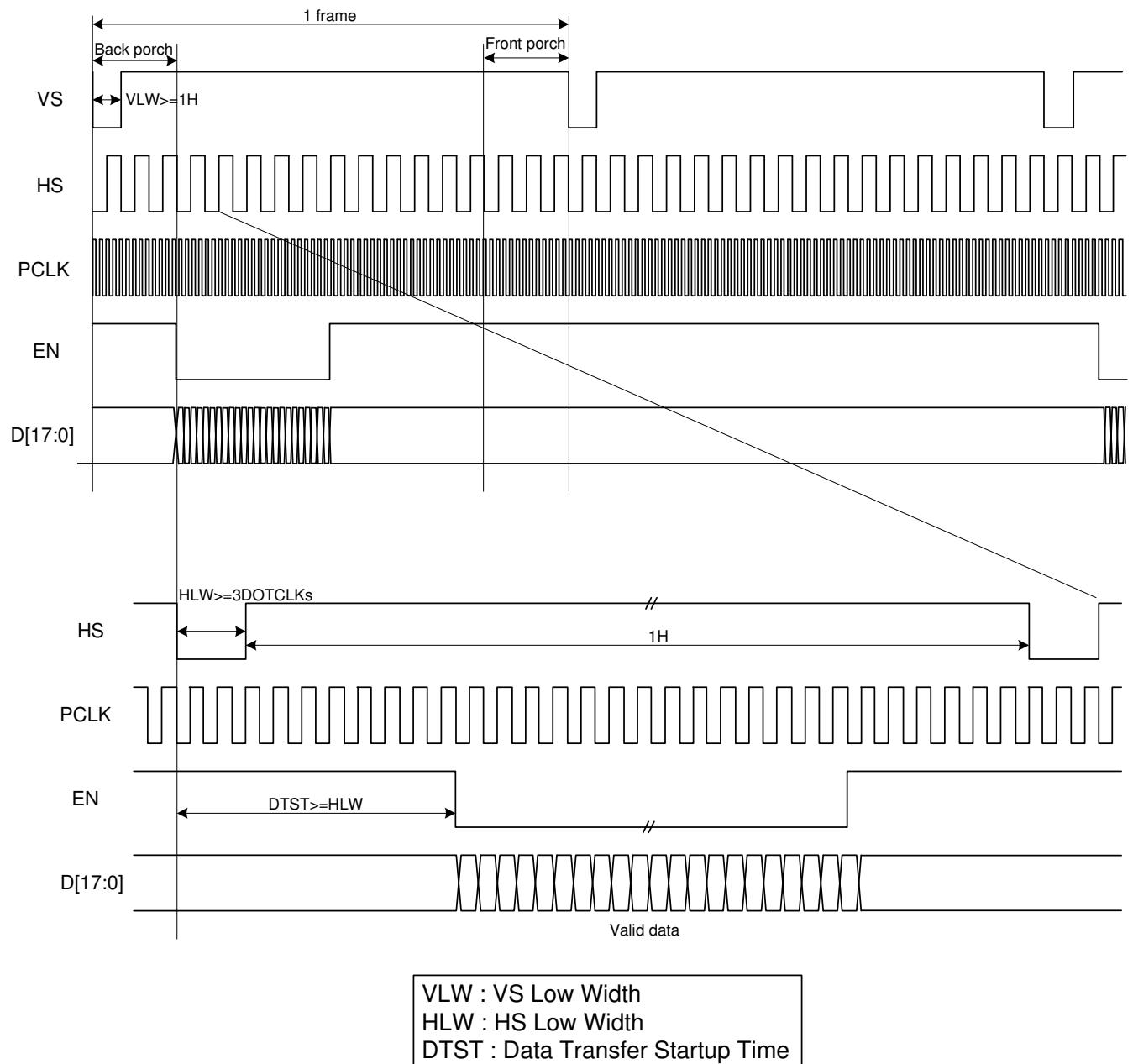
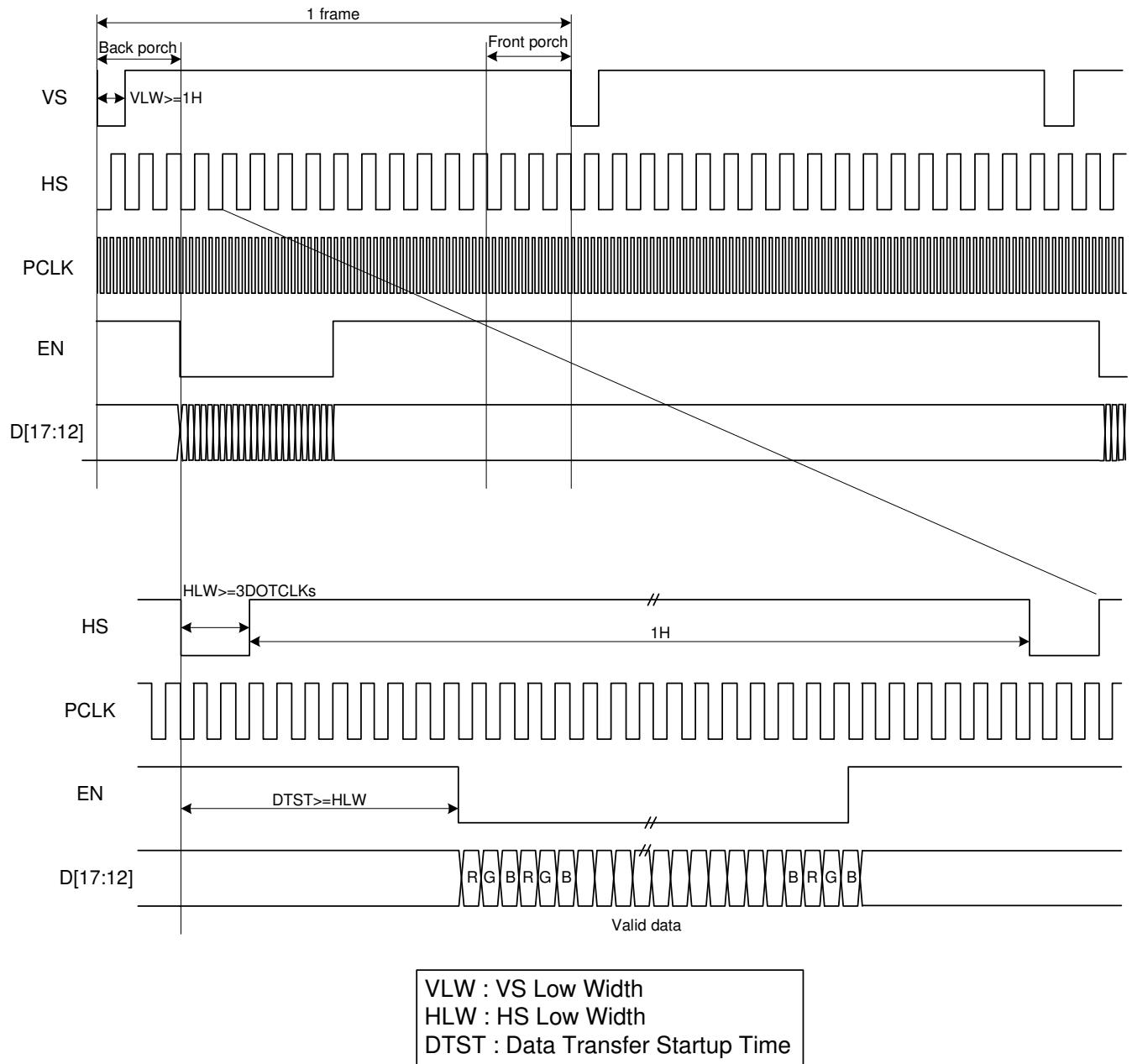


Figure24: Timing Chart of Signals in 18-/16-bit RGB Interface Mode

The timing chart of 6-bit RGB interface mode is shown as below:



Note 1: In 6-bit RGB interface mode, each dot of one pixel (R, G and B) is transferred in synchronization with PCLK.

Note 2: In 6-bit RGB interface mode, set the cycles of VS, HS and EN to 3 multiples of PCLK.

Figure25: Timing Chart of Signals in 6-bit RGB Interface Mode

6.8.3 RGB Interface Mode Set

ILI9163C supplies a RGB interface with DE mode and can be controlled by external RCM[1:0] pins.

RCM1	RCM0	Resolution selection
0	X	MCU interface mode
1	0	RGB interface(1)
1	1	RGB interface(2)

There are 2-kinds of RGB mode which is selected by RCM1 & RCM0 hardware pins.

In RGB interface 1 : (RCM1, RCM0 = “10”), writing data to frame memory is done by PCLK and Video Data Bus , when DE is high state. The external synchronization signals (PCLK, VS and HS) are used for internal display signals. So, controller (host) must always transfer PCLK, VS, HS and DE signals to driver.

In RGB interface 2 : (RCM1, RCM0 = “11”), blanking porch setting of VS and HS signals are defined by RGBBPCTR (B5h)command. DE pin is used for data making. When DE pin is high, valid data is directly stored to frame memory. In the contrast, if DE pin is low, valid data will becomes “00” and stored to frame memory.

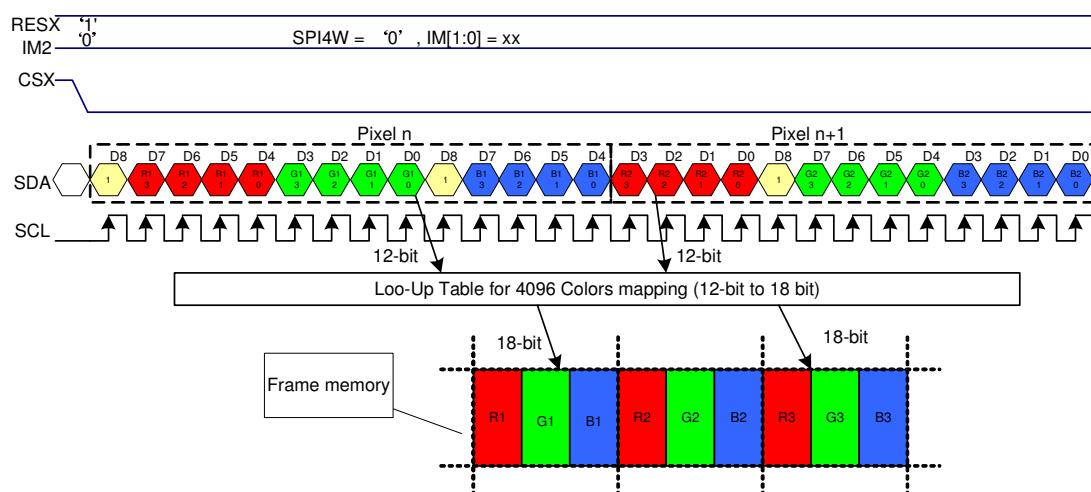
6.9 Display Data Color Coding

6.9.1 Serial Interface

Different display data formats are available for three colors depth supported by the LCM listed below.

- ❖ 4k colors, RGB 4-4-4-bits input
- ❖ 65K colors, RGB 5-6-5-bits input
- ❖ 262K colors, RGB 6-6-6-bits input

3-pin 9-bit data protocol



Note 1: pixel data with the 12-bits color depth information.

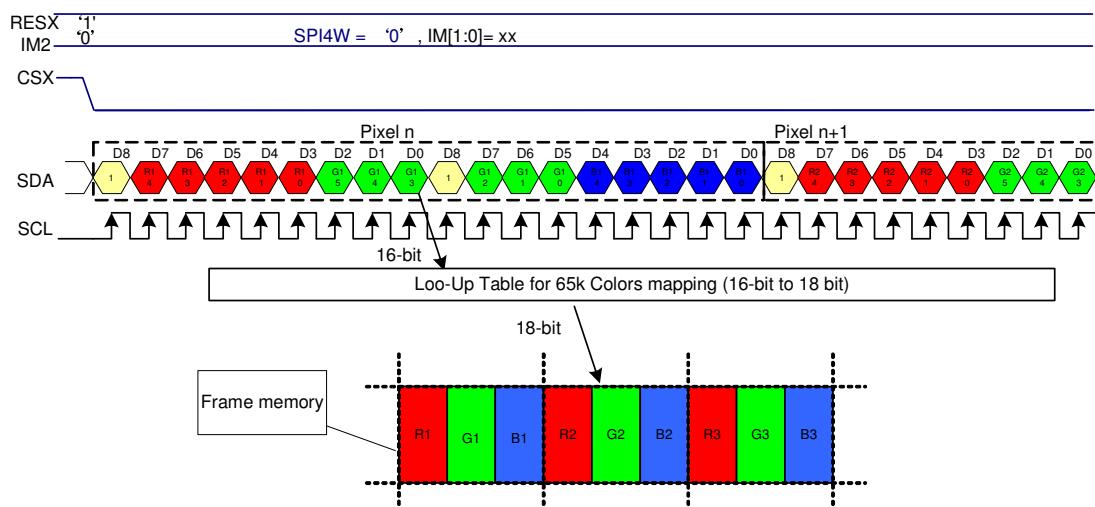
Note 2: The most significant bits are: Rx[3], Gx³ and Bx³

Note 3: The least significant bits are: Rx⁰, Gx⁰ and Bx⁰

Note 4: X = don't care – Can be set to '0' or '1'

Figure26: Write data for RGB4-4-4 bits input

4-pin 8-bit Series data protocol



Note 1: pixel data with the 16-bits color depth information.

Note 2: The most significant bits are: Rx4, Gx5 and Bx4

Note 3: The least significant bits are: Rx0, Gx0 and Bx0

Note 4: X = Don't care – Can be set to '0' or '1'

Figure27: Write data for RGB 5-6-5-bits input

3-pin 9-bit Series data protocol

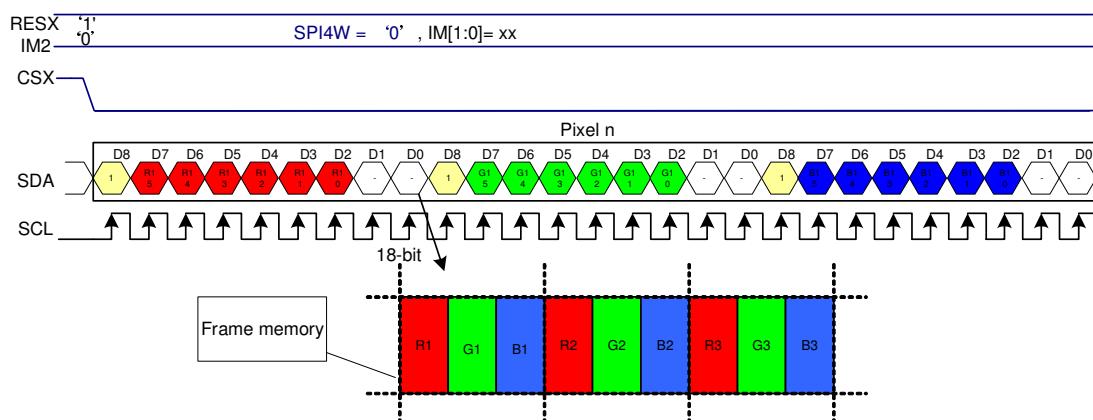
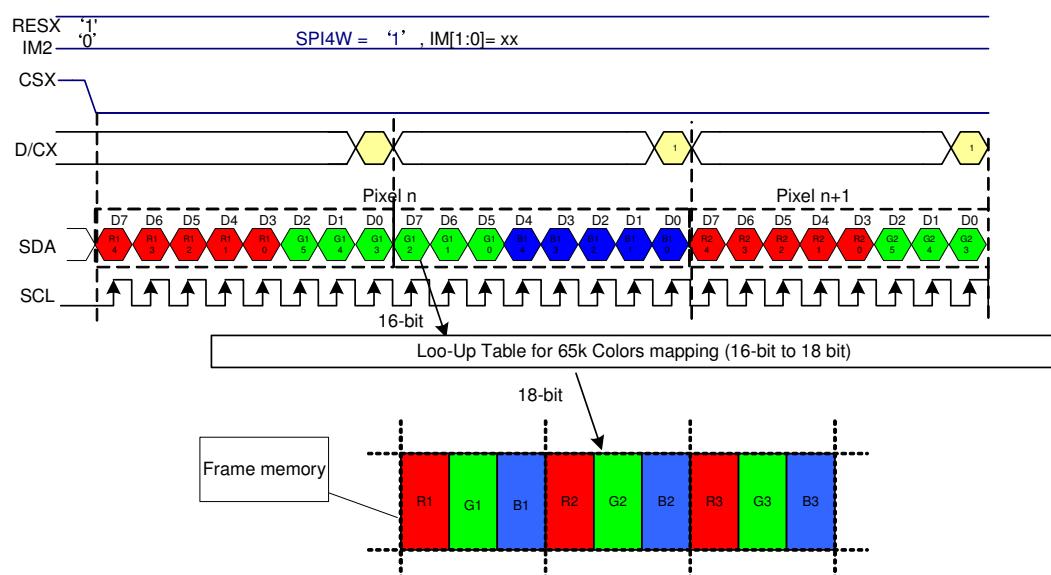


Figure28: Write data for RGB 6-6-6 bits input

4-pin 8-bit Series data protocol



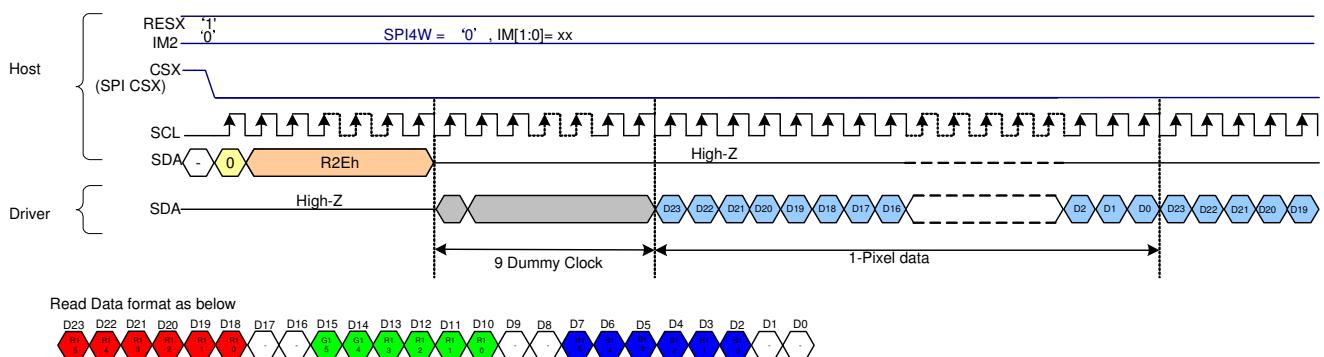
Note 1: pixel data with the 18-bits color depth information.

Note 2: The most significant bits are: Rx⁵, Gx⁵ and Bx⁵

Note 3: The least significant bits are: Rx⁰, Gx⁰ and Bx⁰

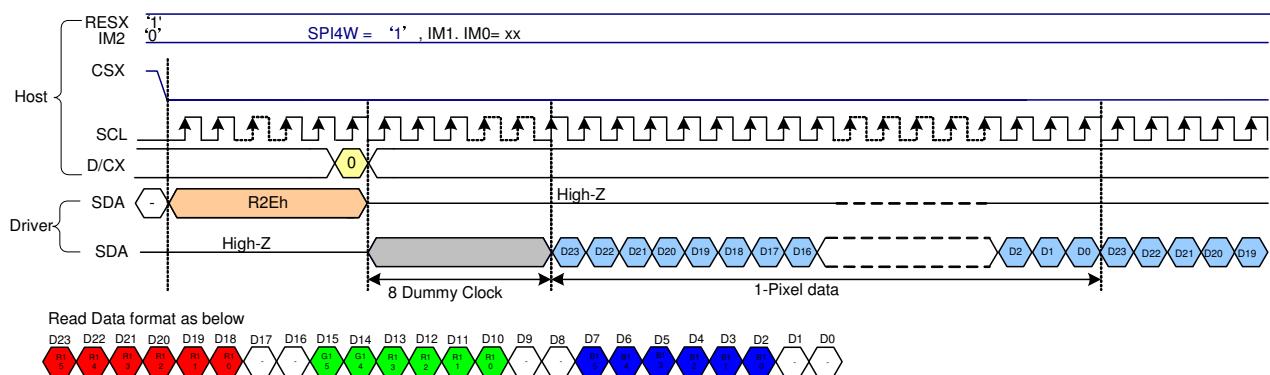
Note 4: X = Don't care – Can be set to '0' or '1'

Read data for 3-W SPI RGB



Note: X = Don't care – Can be set to '0' or '1'

Read data for 4-W SPI RGB



Note: X = Don't care – Can be set to '0' or '1'

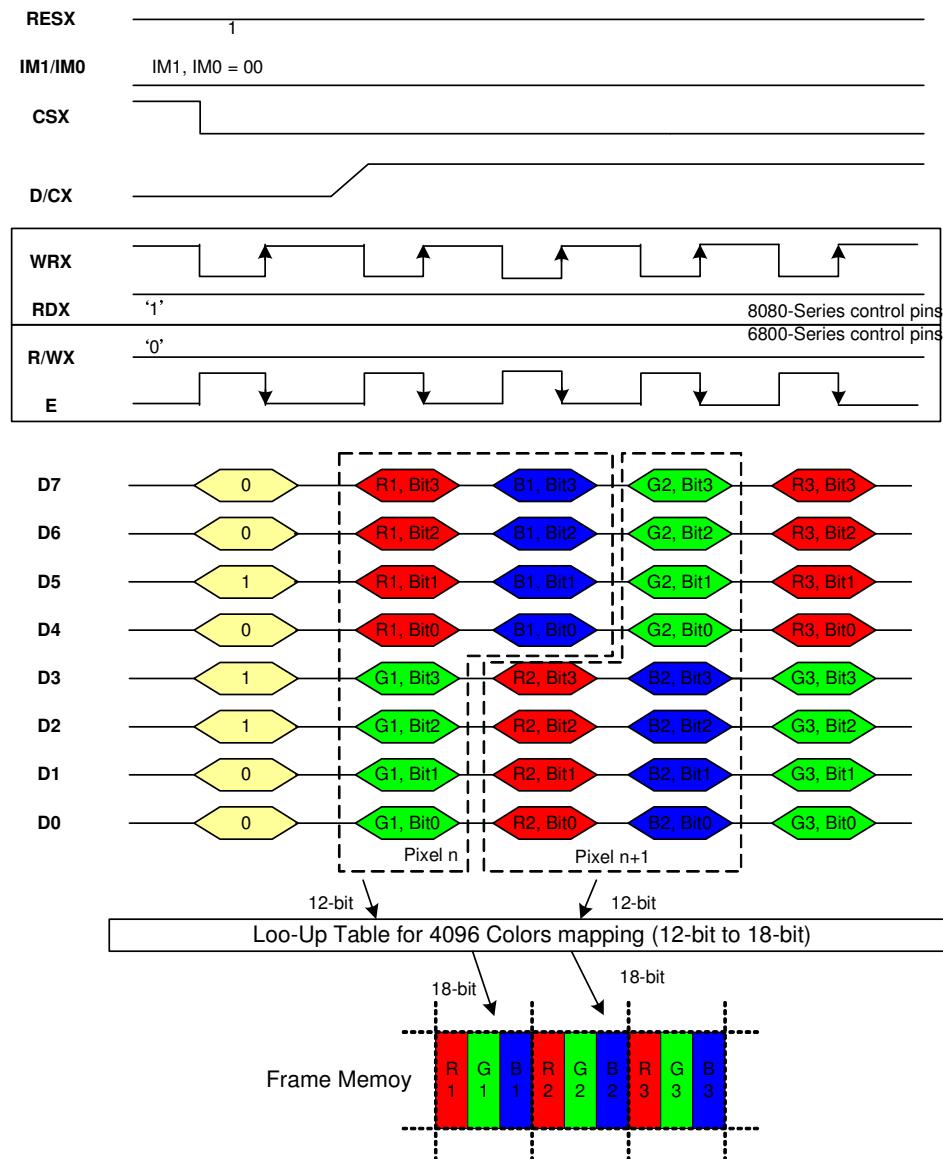
Figure29: Read data for SPI RGB 6-6-6-bits

6.9.2 8-bit Parallel Interface (IM2='1', IM[1:0] = "00")

Different display data formats are available for three colors depth supported by listed below

- ◇ 4k colors, RGB4-4-4-bits input
- ◇ 65K colors, RGB5-6-5-bits input
- ◇ 262K colors, RGB6-6-6-bits input

2 pixels (6 sub-pixels) per 3 transfer



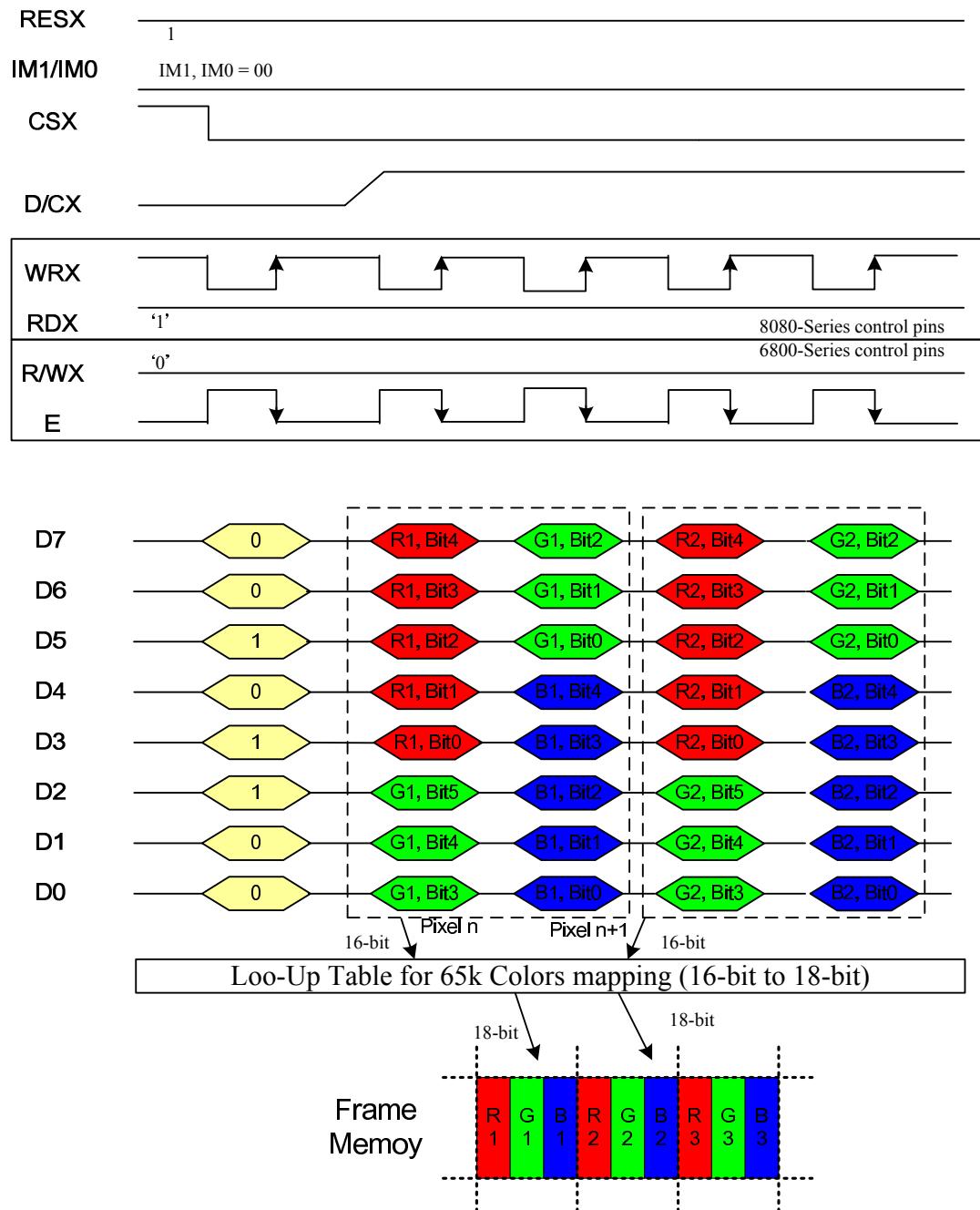
Note 1: The data order is as follows, MSB=D7, LSB=D0 and picture data is MSB=Bit3, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 3-times transfer is used to transmit 2 pixels data with the 12-bits color depth information.

Note 3: '-' = Don't care – Can be set to '0' or '1'

Figure30: Write 8-bit data for RGB 4-4-4-bits input

There is 1 pixel (3 sub-pixels) per 2 transfer



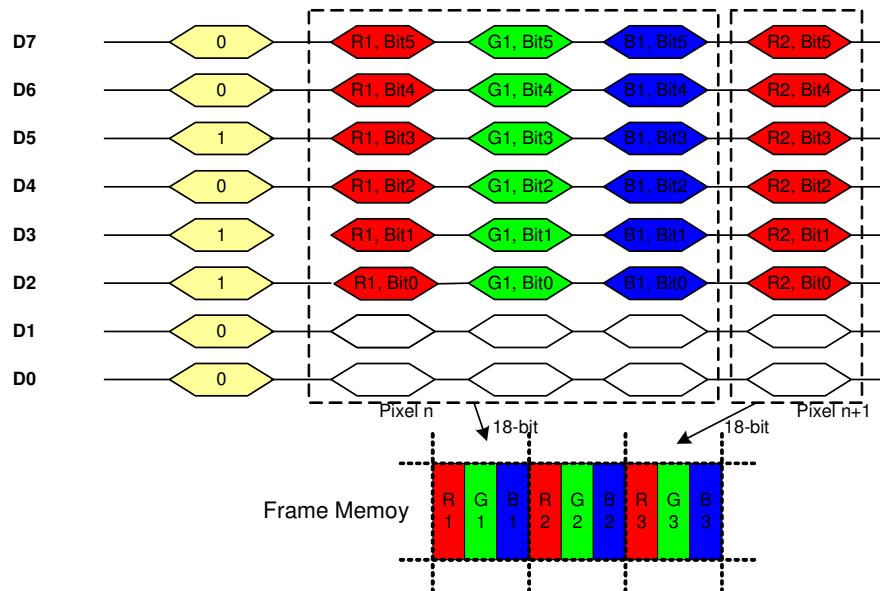
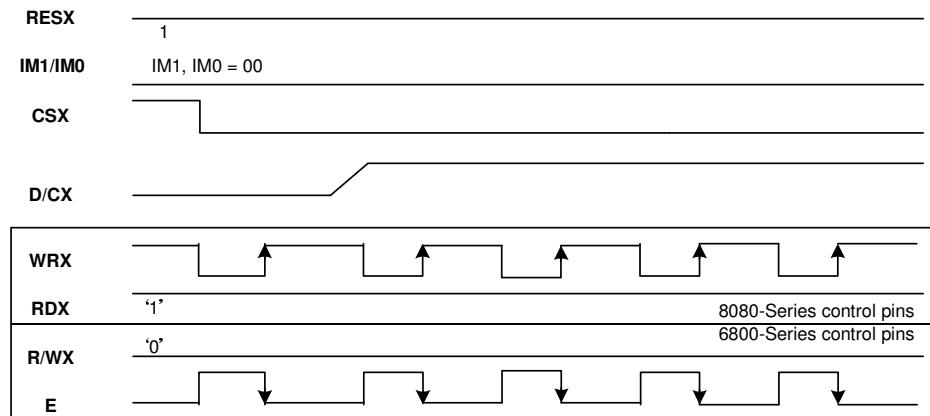
Note 1: The data order is as follows, MSB=D7, LSB=D0 and picture data is MSB=Bit5, LSB=Bit 0 for Green and MSB=Bit4, LSB=Bit0 for Red and Blue data.

Note 2: 2-times transfer is used to transmit 1 pixel data with the 16-bits color depth information.

Note 3: '-' = Don't care – Can be set to '0' or '1'

Figure31: Write 8-bits data for RGB 5-6-5-bits input

1 pixel (3 sub-pixels) per 3 transfer



Note 1: The data order is as follows, MSB=D7, LSB=D0 and picture data is MSB=Bit5, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 3-times transfer is used to transmit 1 pixel data with the 18-bits color depth information.

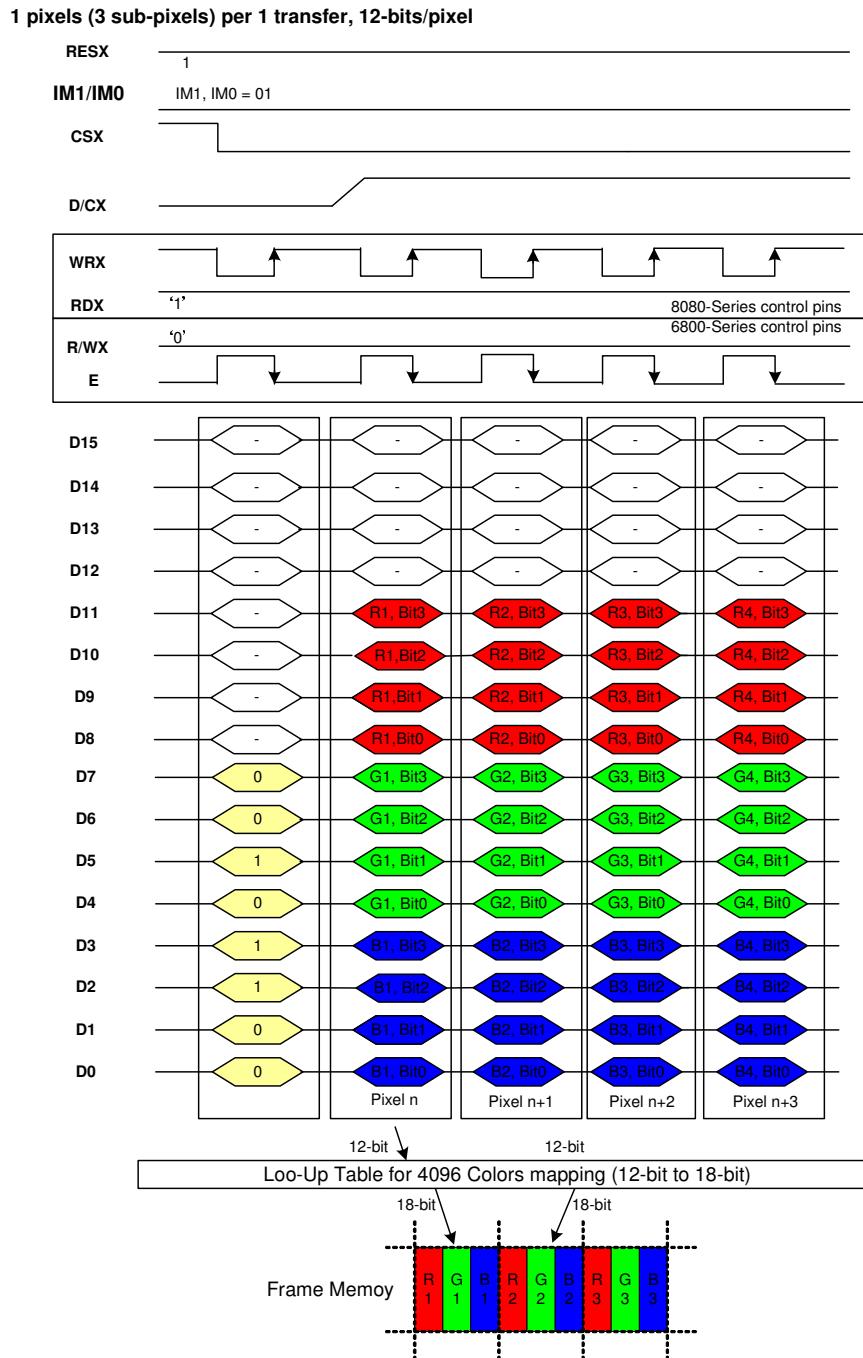
Note 3: '-' = Don't care – Can be set to '0' or '1'

Figure32: Write 8-bit data for RGB 6-6-6-bits input

6.9.3 16-bit Parallel Interface (IM2='1', IM1, IM0="01")

Different display data formats are available for three colors depth supported by listed below

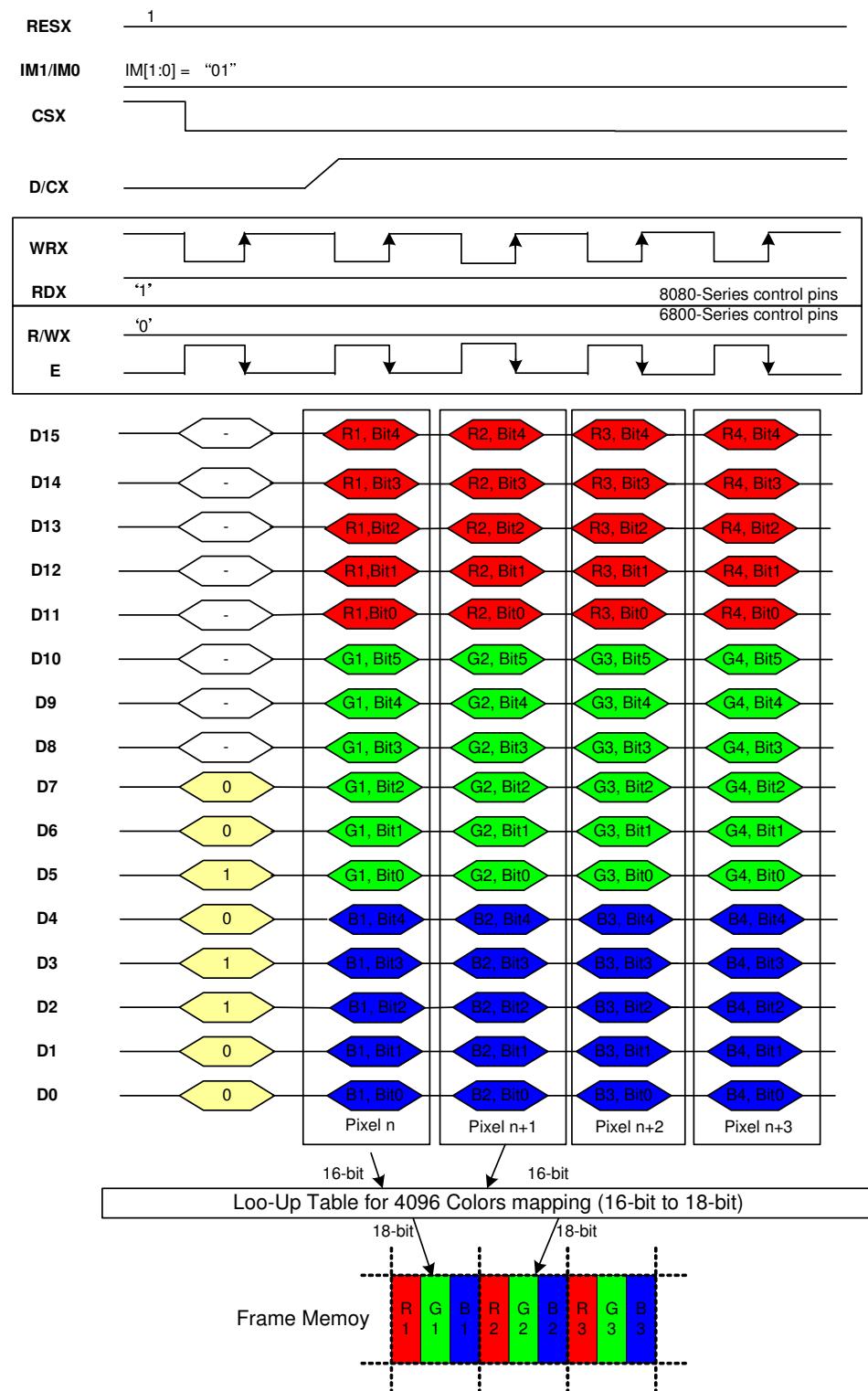
- ✧ 4k colors, RGB 4-4-4-bits input
- ✧ 65K colors, RGB 5-6-5-bits input
- ✧ 262K colors, RGB 6-6-6-bits input



Note1: The data order is as follows, MSB = D15, LSB = D0 and picture data is MSB = Bit3, LSB = Bit0 for Red, Green and Blue data.
Note 2: '=' Don't care – Can be set to '0' or '1'

Figure33: Write 16-bit data for RGB4-4-4-bits input (4k-color)

1 pixel (3 sub-pixels) per 1 transfer, 16-bits/pixel



Note1: The data order is as follows, MSB = D15, LSB = D0 and picture data is MSB = Bit5, LSB = Bit0 for Red and Blue and MSB=Bit5, LSB=Bit 0 for Green data.

Note 2: '=' Don't care – Can be set to '0' or '1'

Figure34: Write 16-bit data for RGB 5-6-5-bits input (65k colors)

2 pixels (6 sub-pixels) per 2 transfer, 18-bits/pixel

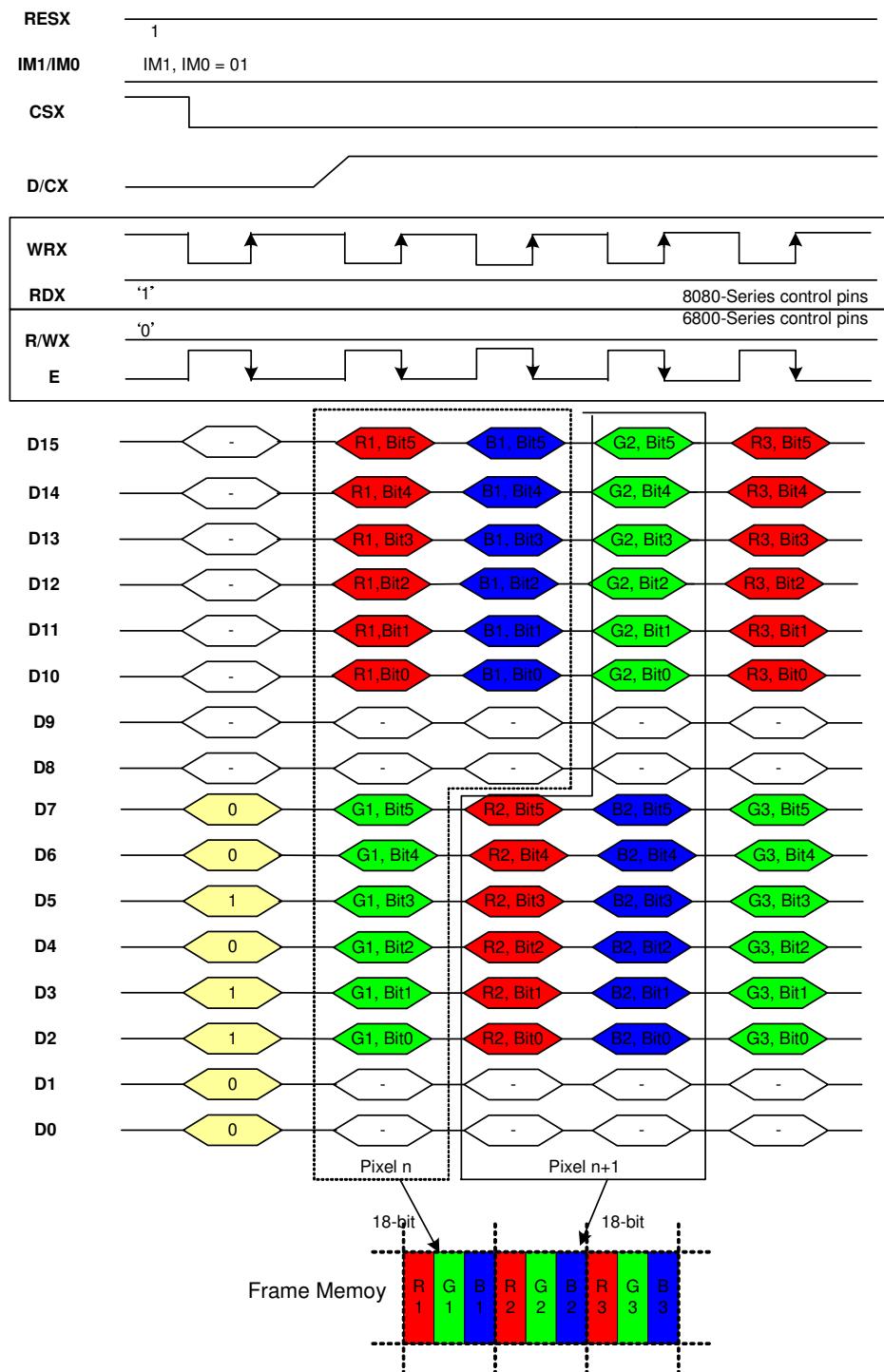


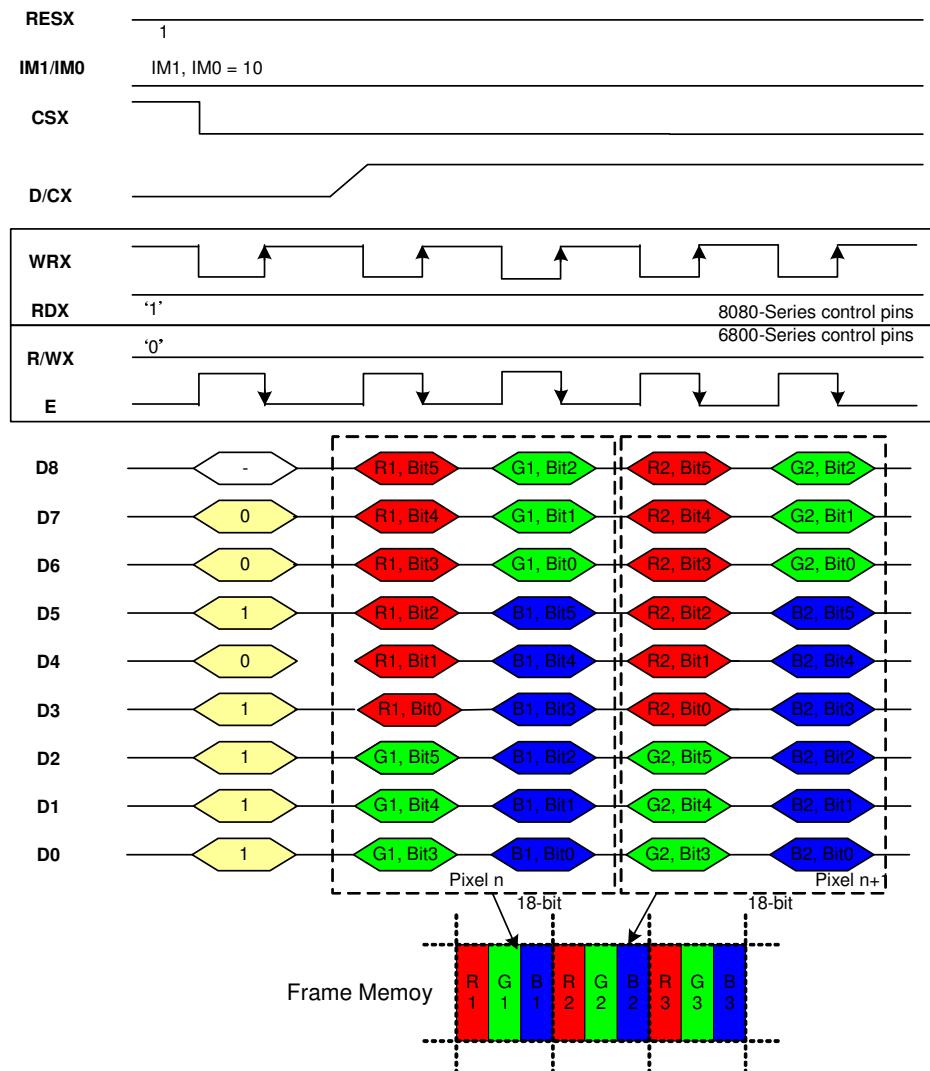
Figure35: Write 16-bit data for RGB 6-6-6-bits input (262K colors)

6.9.4 9-bit Parallel Interface (IM2='2', IM1, IM0="10")

Different display data formats are available for three colors depth supported by listed below

- ◇ 262K colors, RGB6-6-6-bits input

2 pixels (6 sub-pixels) per 4 transfer, 18-bits/pixel



Note1: The data order is as follows, MSB = D8, LSB = D0 and picture data is MSB = Bit5, LSB = Bit0 for Red and Green and Blue data.

Note 2: '=' Don't care – Can be set to '0' or '1'

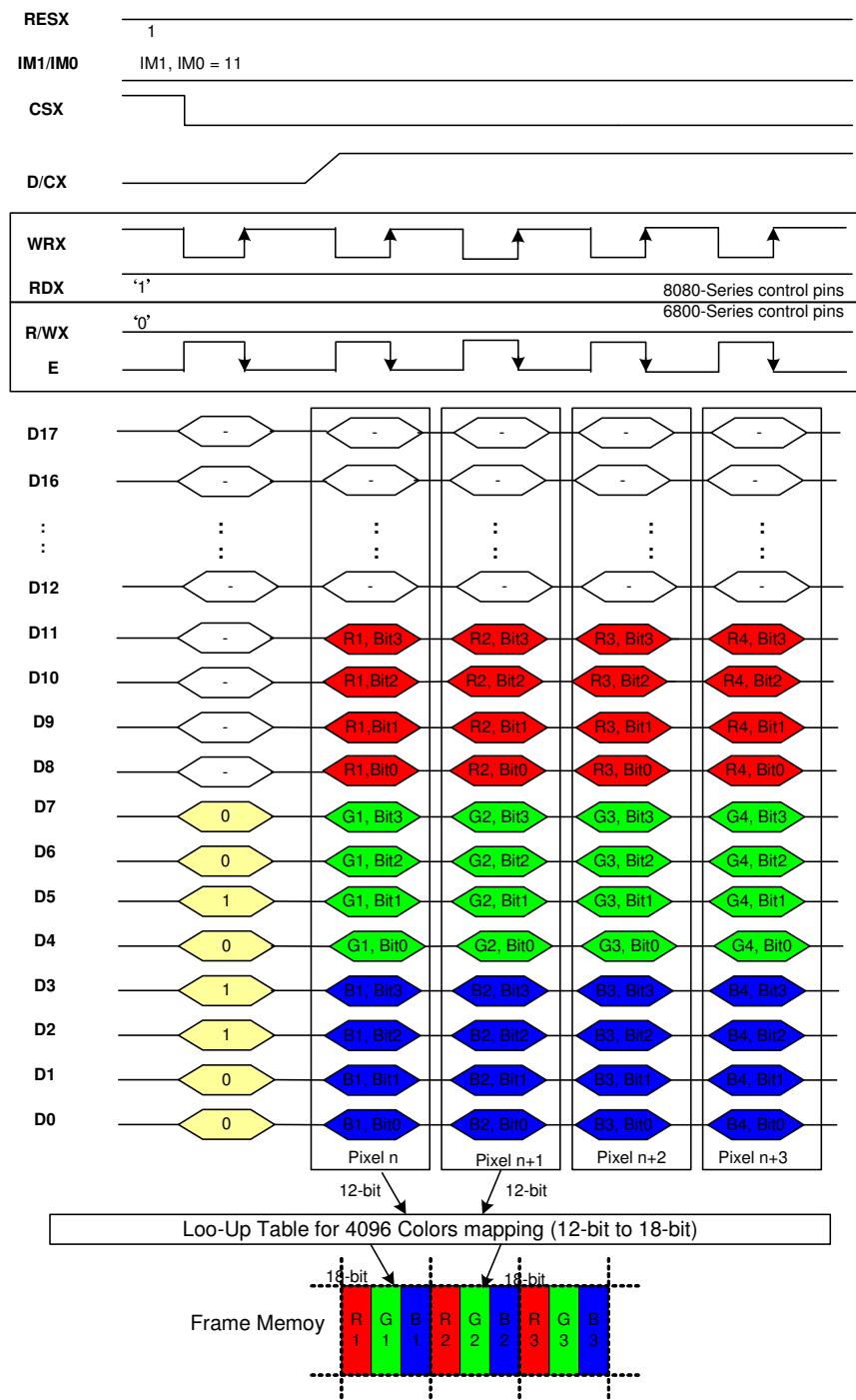
Figure36: Write 9-bit data for RGB 6-6-6-bits input(262k-color)

6.9.5 18-bit Parallel Interface (IM2='1', IM1, IM0="11")

Different display data formats are available for three colors depth supported by listed below

- ❖ 4k colors, RGB 4-4-4-bits input
- ❖ 65K colors, RGB 5-6-5-bits input
- ❖ 262K colors, RGB 6-6-6-bits input

1 pixel (3 sub-pixels) per 1 transfer, 12-bits/pixel

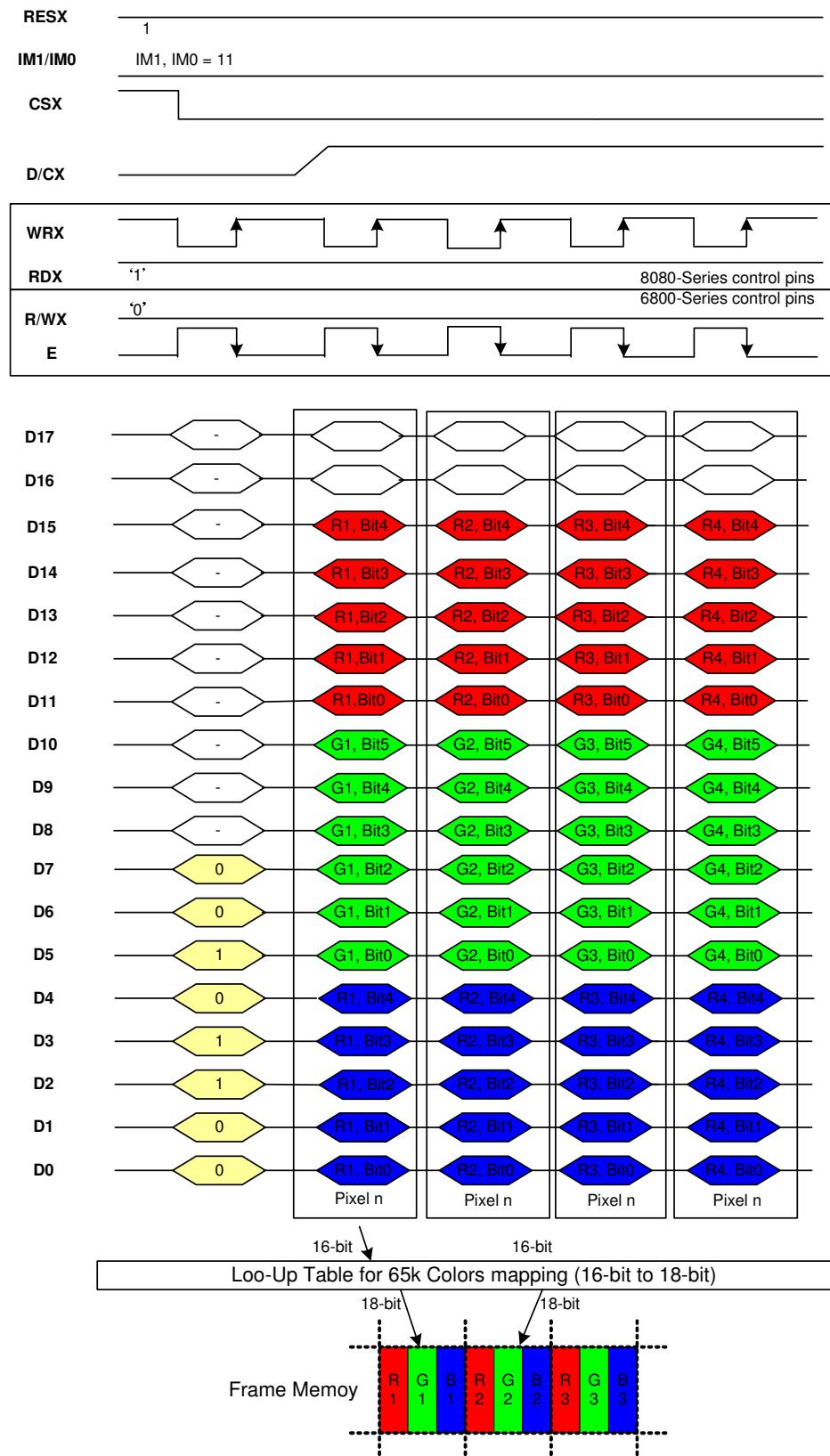


Note1: The data order is as follows, MSB = D11, LSB = D0 and picture data is MSB = Bit3, LSB = Bit0 for Red, Green and Blue data.

Note 2: '=' Don't care – Can be set to '0' or '1'

Figure37: Write 18-bits data for RGB 4-4-4-bits input (4k colors)

1 pixel (3 sub-pixels) per 1 transfer, 16-bits/pixel

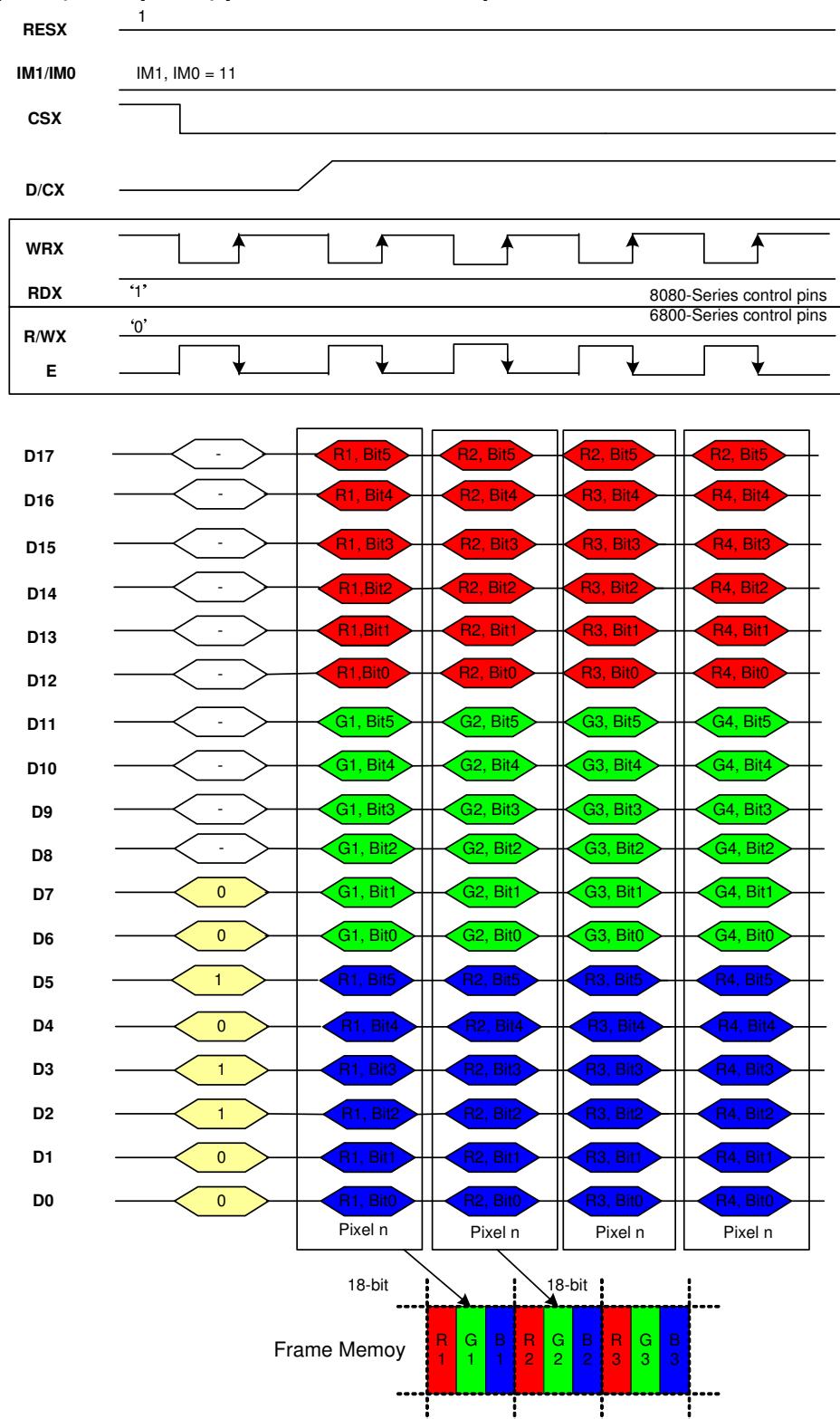


Note1: The data order is as follows, MSB = D15, LSB = D0 and picture data is MSB = Bit5, LSB = Bit0 for Green and MSB=Bit 4, LSB=Bit 0 for Blue data.

Note 2: '=' Don't care – Can be set to '0' or '1'

Figure38: Write 18-bits data for RGB 5-6-5-bits input (65k-color)

1 pixel (3 sub-pixels) per 1 transfer, 18-bits/pixel



Note1: The data order is as follows, MSB = D17, LSB = D0 and picture data is MSB = Bit5, LSB = Bit0 for Red, Green and Blue data.

Note 2: '=' Don't care – Can be set to '0' or '1'

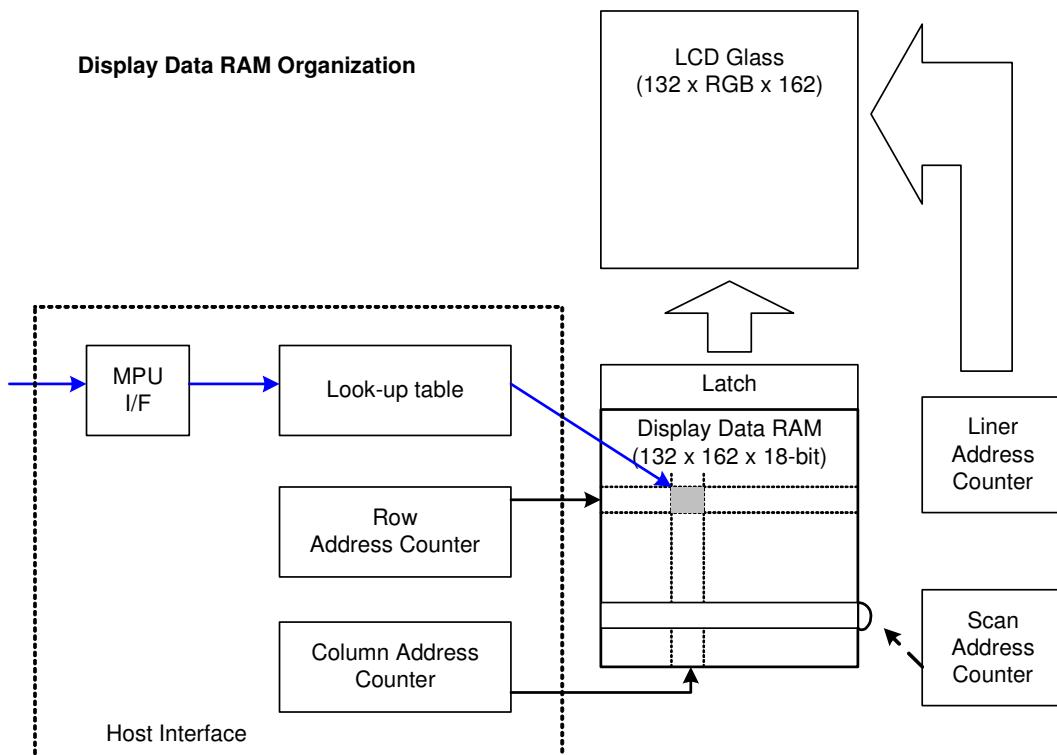
Figure39: Write 18-bit data for RGB 6-6-6-bits input (262K colors)

7. Display Data RAM

7.1 Configuration

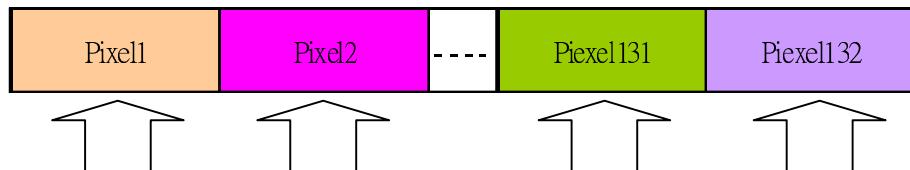
The display data RAM stores display dots and consists of 384,504 bits (132x18x162 bits). There is no restriction on access to the RAM even when the display data on the same address is loaded to DAC.

There will be no abnormal visible effect on the display when there is a simultaneous Panel Read and Interface Read or Write to the same location of the Frame Memory.



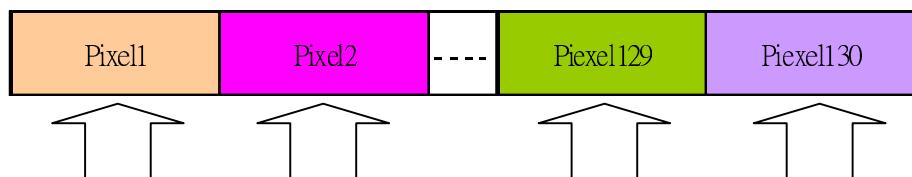
7.2 Memory to Display Address Mapping

7.2.1 132RGB x 132 resolution (GM[2:0] = “101”, SMX=SMY=SRGB=’0’)



Gate	Source Out	S1	S2	S3	S4	S5	S6	---	S391	S392	S393	S394	S395	S396	SA		
		RA	RGB=0	RGB=1													
	MY=0	MY=1													ML=0	ML=1	
1	1	132	R1	G1	B1	R2	G2	B2	---	R131	G131	B131	R132	G132	B132	1	132
2	2	131														2	131
3	3	130														3	130
4	4	129														4	129
5	5	128														5	128
6	6	127														6	127
7	7	126														7	126
8	8	125														8	125
9	9	124														9	124
10	10	123														10	123
11	11	122														11	122
12	12	121														12	121
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
125	125	8														125	8
126	126	7														126	7
127	127	6														127	6
128	128	5														128	5
129	129	4														129	4
130	130	3														130	3
131	131	2														131	2
132	132	1														132	1
CA	MX-0		1		2		---		131		132						
	MX-1		132		131		---		2		1						

7.2.2 130RGB x 130 resolution(GM[2:0] = “100”, SMX=SMY=SRGB=’0’)



Gate	Source Out	S7	S8	S9	S10	S11	S12	----	S391	S392	S393	S394	S395	S396	SA	
		RGB=1		RGB=1		RGB=1		RGB=1		RGB=1		RGB=1		RGB=1		
		RA														
		MY=0	MY=1													
1	1	130	R1	G1	B1	R2	G2	B2	----	R129	G129	B129	R130	G130	B130	1 130
2	2	129							----							2 129
3	3	128							----							3 128
4	4	127							----							4 127
5	5	126							----							5 126
6	6	125							----							6 125
7	7	124							----							7 124
8	8	123							----							8 123
9	9	122							----							9 122
10	10	121							----							10 121
11	11	120							----							11 120
12	12	119							----							12 119
:	:	:							----							:
:	:	:							----							:
:	:	:							----							:
:	:	:							----							:
123	123	8							----							123 8
124	124	7							----							124 7
125	125	6							----							125 6
126	126	5							----							126 5
127	127	4							----							127 4
128	128	3							----							128 3
129	129	2							----							129 2
130	130	1							----							130 1
CA	MX-0		1		2			----		129		130				
	MX-1		130		129			----		2		1				

7.2.3 128RGB x 160 resolution (GM[2:0] = “011”, SMX=SMY=SRGB=’0’)

Gate	Source Out	S7	S8	S9	S10	S11	S12	----	S385	S386	S387	S388	S389	S390	SA		
		RA RGB=0 MY=0	RA RGB=1 MY=1	RA RGB=0 MY=0	RA RGB=1 MY=1	RA RGB=0 MY=0	RA RGB=1 MY=1	RGB Order	RA RGB=0 MY=0	RA RGB=1 MY=1	RA RGB=0 MY=0	RA RGB=1 MY=1	RA RGB=0 MY=0	RA RGB=1 MY=1	ML=0	ML=1	
1	1	160	R1	G1	B1	R2	G2	B2	----	R127	G127	B127	R128	G128	B128	1	160
2	2	159							----							2	159
3	3	158							----							3	158
4	4	157							----							4	157
5	5	156							----							5	156
6	6	155							----							6	155
7	7	154							----							7	154
8	8	153							----							8	153
9	9	152							----							9	152
10	10	151							----							10	151
11	11	150							----							11	150
12	12	149							----							12	149
:	:	:	:	:	:	:	:	:	----	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:	----	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:	----	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:	----	:	:	:	:	:	:	:	:
153	153	8							----							153	8
154	154	7							----							154	7
155	155	6							----							155	6
156	156	5							----							156	5
157	157	4							----							157	4
158	158	3							----							158	3
159	159	2							----							159	2
160	160	1							----							160	1
CA	MX-0	1			2			----	127			128					
	MX-1	128			127			----	2			1					

Note

RA = Row Address

CA = Column Address

SA = Scan Address

MX = Mirror X-axis (Column address direction parameter), D6 parameter of MADCTL command

ML = Scan direction parameter, D4 parameter of MADCTL command

RGB = Red, Green and Blue pixel position change, D3 parameter of MADCTL command

7.2.4 120RGB x 160 resolution (GM[2:0] = “010”, SMX=SMY=SRGB=’0’)

The diagram illustrates the pixel mapping for a 120RGB x 160 resolution display onto a 132RGBx162 resolution. The top row shows four pixels: Pixel1 (orange), Pixel2 (magenta), followed by dashed lines for Pixel3 to Pixel119, and Pixel120 (purple). Below each pixel is a small upward-pointing arrow. The bottom section is a table with the following structure:

Gate	Source Out	S7	S8	S9	S10	S11	S12	-----	S361	S362	S363	S364	S365	S366			
		RA		RGB Order		SA											
	MY=0	MY=1	RGB=0	RGB=1	RGB=0	RGB=1	RGB=0	RGB=1	ML=0	ML=1							
1	1	160	R1	G1	B1	R2	G2	B2	-----	R119	G119	B119	R120	G120	B120	1	160
2	2	159							-----							2	159
3	3	158							-----							3	158
4	4	157							-----							4	157
5	5	156							-----							5	156
6	6	155							-----							6	155
7	7	154							-----							7	154
8	8	153							-----							8	153
9	9	152							-----							9	152
10	10	151							-----							10	151
11	11	150							-----							11	150
12	12	149							-----							12	149
:	:	:	:	:	:	:	:	:	-----	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:	-----	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:	-----	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:	-----	:	:	:	:	:	:	:	:
153	153	8							-----							153	8
154	154	7							-----							154	7
155	155	6							-----							155	6
156	156	5							-----							156	5
157	157	4							-----							157	4
158	158	3							-----							158	3
159	159	2							-----							159	2
160	160	1							-----							160	1
	CA	MX-0	1		2		-----	119			120						
		MX-1	120		119		-----	2			1						

Note

RA = Row Address

CA = Column Address

SA = Scan Address

MX = Mirror X-axis (Column address direction parameter), D6 parameter of MADCTL command

ML = Scan direction parameter, D4 parameter of MADCTL command

RGB = Red, Green and Blue pixel position change, D3 parameter of MADCTL command

7.2.5 128RGB x 128 resolution (GM[2:0] = “001”, SMX=SMY=SRGB=’0’)

		Pixel1			Pixel2			Pixel127			Pixel128						
Gate	Source Out	S7	S8	S9	S10	S11	S12	----	S385	S386	S387	S388	S389	S390			
		RA						RGB Order						SA			
		MY=0	MY=1					RGB=0						ML=0	ML=1		
1	1	128	R1	G1	B1	R2	G2	B2	----	R127	G127	B127	R128	G128	B128	1	128
2	2	127							----							2	127
3	3	126							----							3	126
4	4	125							----							4	125
5	5	124							----							5	124
6	6	123							----							6	123
7	7	122							----							7	122
8	8	121							----							8	121
9	9	120							----							9	120
10	10	119							----							10	119
11	11	118							----							11	118
12	12	117							----							12	117
:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
:	:	:	:	:	:	:	:	:	----	:	:	:	:	:	:	:	
:	:	:	:	:	:	:	:	:	----	:	:	:	:	:	:	:	
121	121	8							----							121	8
122	122	7							----							122	7
123	123	6							----							123	6
124	124	5							----							124	5
125	125	4							----							125	4
126	126	3							----							126	3
127	127	2							----							127	2
128	128	1							----							128	1
CA	MX-0	1			2			----	127			128					
	MX-1	128			127			----	2			1					

Note

RA = Row Address

CA = Column Address

SA = Scan Address

MX = Mirror X-axis (Column address direction parameter), D6 parameter of MADCTL command

ML = Scan direction parameter, D4 parameter of MADCTL command

RGB = Red, Green and Blue pixel position change, D3 parameter of MADCTL command

7.2.6 132RGB x 162 resolution (GM[2:0] = “000”, SMX=SMY=SRGB=’0’)

Gate	Source Out	S1	S2	S3	S4	S5	S6	-----	S391	S392	S393	S394	S395	S396	-----	SA	
RA		RGB=0	RGB=1	RGB=0	RGB=1	RGB=0	RGB=1	RGB Order	RGB=0	RGB=1	RGB=0	RGB=1	RGB=0	RGB=1	ML	ML	
		MY=0	MY=1													ML=0	ML=1
1	1	162	R1	G1	B1	R2	G2	B2	-----	R131	G131	B131	R132	G132	B132	1	162
2	2	161							-----							2	161
3	3	160							-----							3	160
4	4	159							-----							4	159
5	5	158							-----							5	158
6	6	157							-----							6	157
7	7	156							-----							7	156
8	8	155							-----							8	155
9	9	154							-----							9	154
10	10	153							-----							10	153
11	11	152							-----							11	152
12	12	151							-----							12	151
:	:	:	:	:	:	:	:	:	-----	:	:	:	:	:	-----	:	:
:	:	:	:	:	:	:	:	:	-----	:	:	:	:	:	-----	:	:
:	:	:	:	:	:	:	:	:	-----	:	:	:	:	:	-----	:	:
:	:	:	:	:	:	:	:	:	-----	:	:	:	:	:	-----	:	:
155	155	8							-----							155	8
156	156	7							-----							156	7
157	157	6							-----							157	6
158	158	5							-----							158	5
159	159	4							-----							159	4
160	160	3							-----							160	3
161	161	2							-----							161	2
162	162	1							-----							162	1
CA	MX-0	1		2		-----		131		132							
	MX-1	132		131		-----		2		1							

Note

RA = Row Address

CA = Column Address

SA = Scan Address

MX = Mirror X-axis (Column address direction parameter), D6 parameter of MADCTL command

ML = Scan direction parameter, D4 parameter of MADCTL command

RGB = Red, Green and Blue pixel position change, D3 parameter of MADCTL command

7.3 MCU to memory write/read direction (Address Counter)

The address counter set the addresses of the display data RAM for writing and reading.

Data is written pixel-wise into the RAM matrix of DRIVER. The data for one pixel or two pixels is collected(RGB 6-6-6-bit), according to the data formats. As soon as this pixel-data information is complete the "Write access" is activated on the RAM. The locations of RAM are addressed by the address pointers. When GM=011, 132RGB x 162, the address ranges are X=0 to X=131 (83h) and Y=0 to Y=161 (A1h). Addresses outside these ranges are not allowed. Before writing to the RAM a window must be defined into which will be written. The window is programmable via the command register XS, YS designating the start address and XE, YE designating the end address.

For example the whole display contents will be written, the window is defined by the following values: XS=0(0h) YS=0(0h) and XE=131(83h), YE=161(A1h)

In vertical addressing mode (MV=1), the Y-address increments after each byte, after the last Y-address (Y=YE), Y wraps around to YS and X increments to address the next column. In horizontal addressing mode (V=0), the X-address increments after each byte, after the last X-address(X=XE), X wraps around to XS and Y increments to address the next row. After the every last address (X=XE and Y=YE) the address pointers wrap around to address (X=XS and Y=YS)

For flexibility in handling a wide variety of display architectures, the commands "CASET, RASET" and "MADCTR", define flags MX and MY, which allows mirroring of the X-address and Y-address. All combinations of flags are allowed. Below table shows the available combinations of writing to the display RAM. When MX, MY and MV will be changed the data bust be rewritten to the display RAM.

For each image orientation, the controls for the column and page counters apply as below: -

Condition	Column Counter	Row Counter
When RAMWR/RAMRD command is accepted	Return to "Start Column (XS)"	Return to "Start Row (YS)"
Complete Pixel Read/Write action	Increment by 1	No change
The Column counter value is larger than "End Column(XE)"	Return to "Start Column (XS)"	Increment by 1
The Column counter value is larger than "End Column (XE)" and the Row counter value is larger than "End Row(YE)"	Return to "Start Column (XS)"	Return to "Start Row (YS)"

Figure40: Frame Data Write Direction According to the MADCTR parameters (MV, MX and MY)

Display Data Direction	MADCTR Parameter			Image in the Memory (MPU)	Image in the Driver (DDRAM)
	MV	MX	MY		
Normal	0	0	0		
Y-Mirror	0	0	1		
X-Mirror	0	1	0		
X-Mirror Y-Mirror	0	1	1		
X-Y Exchange	1	0	0		
X-Y Exchange Y-Mirror	1	0	1		
XY Exchange	1	1	0		
XY Exchange	1	1	1		

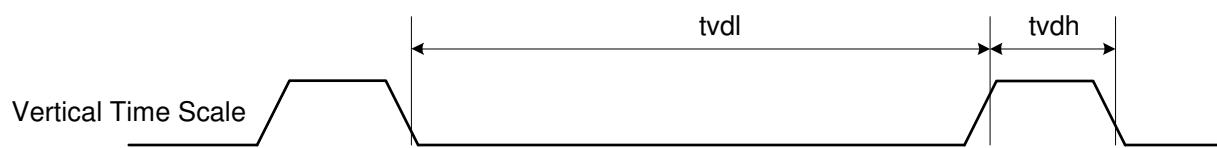
8. Tearing Effect Output Line

The Tearing Effect output line supplies to the MCU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect Signal is defined by the Parameter of the Tearing Effect Line On command.

The signal can be used by the MCU to synchronize Frame Memory Writing when displaying video images.

8.1 Tearing Effect Line Modes

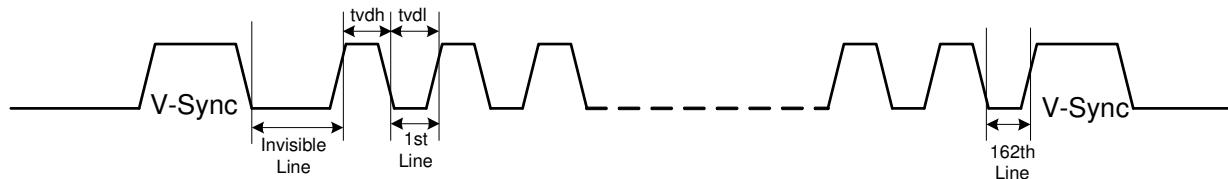
Mode 1, the Tearing Effect Output signal consists of V-Sync information only:



$tvdh$ = The LCD display is not updated from the Frame Memory.

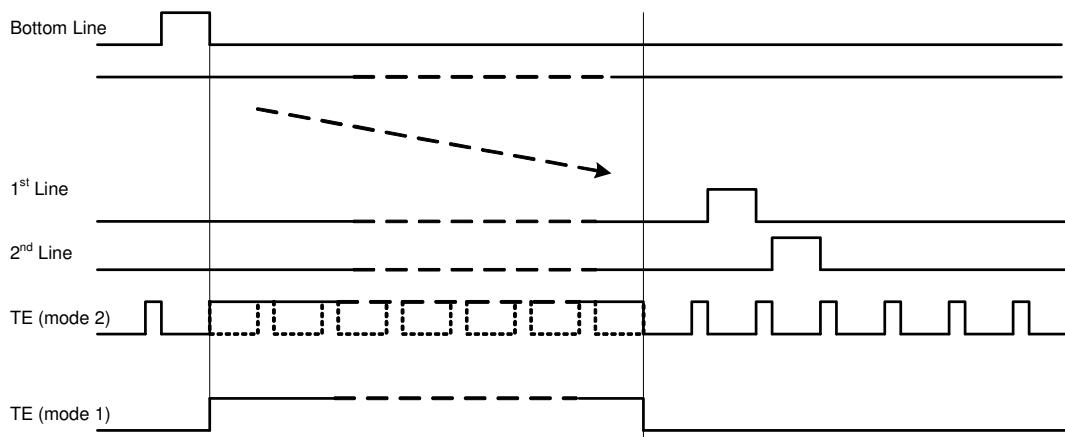
$tvdl$ = The LCD display is updated from the Frame Memory (except Invisible Line – see below).

Mode 2, the Tearing Effect Output signal consists of V-Sync and H-Sync information, There is one V-sync and 162 H-sync pulses per field:



t^{hdh} = The LCD display is not updated from the Frame Memory.

T^{hdl} = The LCD display is updated from the Frame Memory (except Invisible Line – see above).



Note: During Sleep In Mode, the Tearing Effect Output Pin is active Low.

8.2 Tearing Effect Line Timing

The Tearing Effect signal is described below:

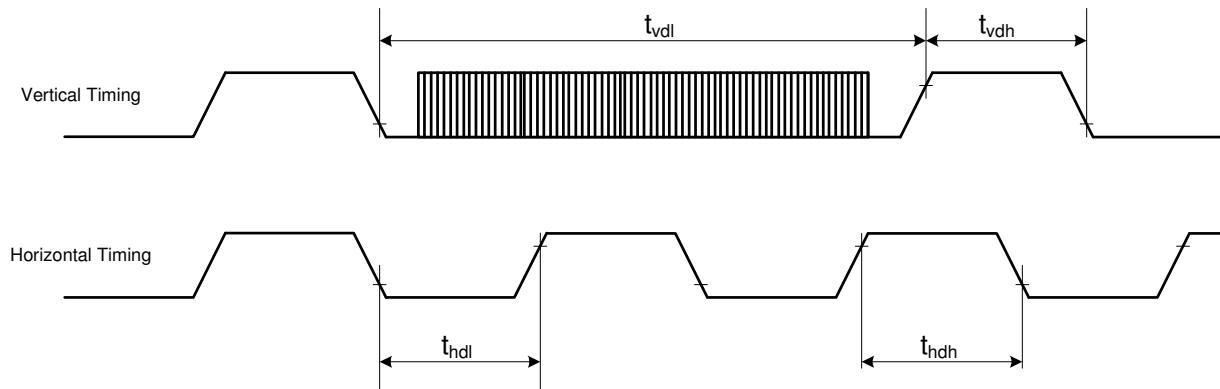


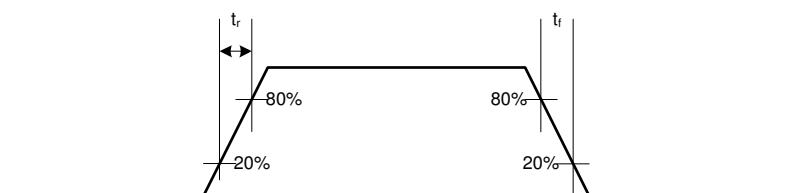
Table 8.2.1 AC characteristics of Tearing Effect Signal Idle Mode Off/On (Frame Rate = 58.9Hz)

Symbol	Parameter	min	max	unit	descripiton
t_{vdL}	Vertical Timing Low Duration	13	-	Ms	
t_{vdH}	Vertical Timing High Duration	1000	-	μs	
t_{hdl}	Horizontal Timing Low Duration	33	-	μs	
t_{hdH}	Horizontal Timing High Duration	25	500	μs	

Notes:

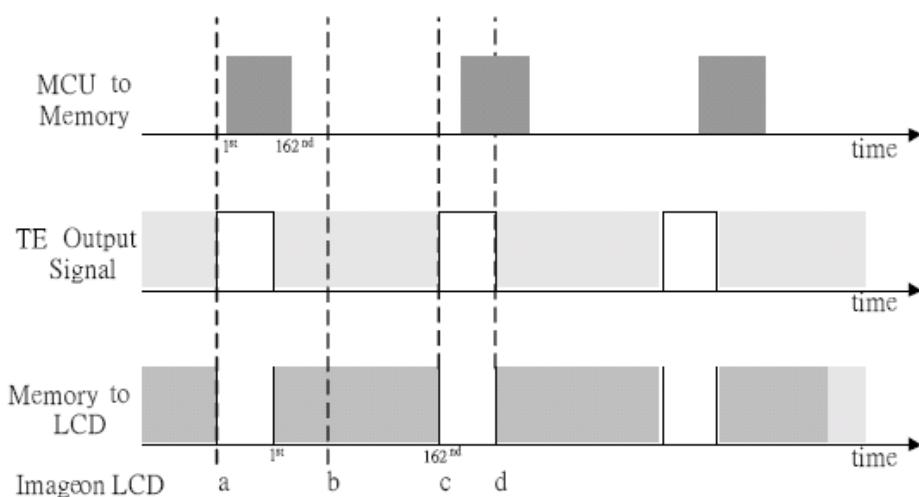
1. The timings in Table 8.2.1 apply when MADCTL B4=0 and B4=1
2. The signal's rise and fall times (t_f , t_r) are stipulated to be equal to or less than 15ns.

Figure41: Rise and fall times

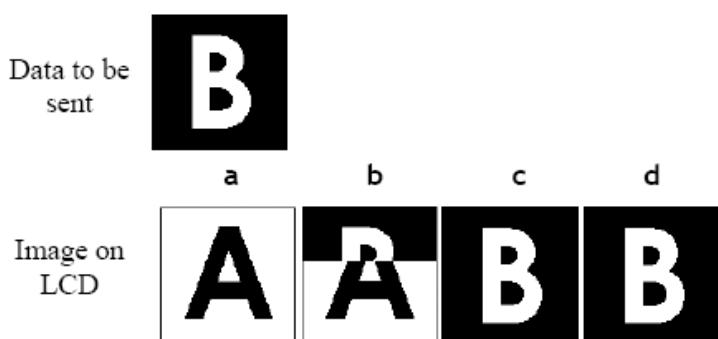


The Tearing Effect Output Line is fed back to the MCU and should be used as shown below to avoid Tearing Effect:

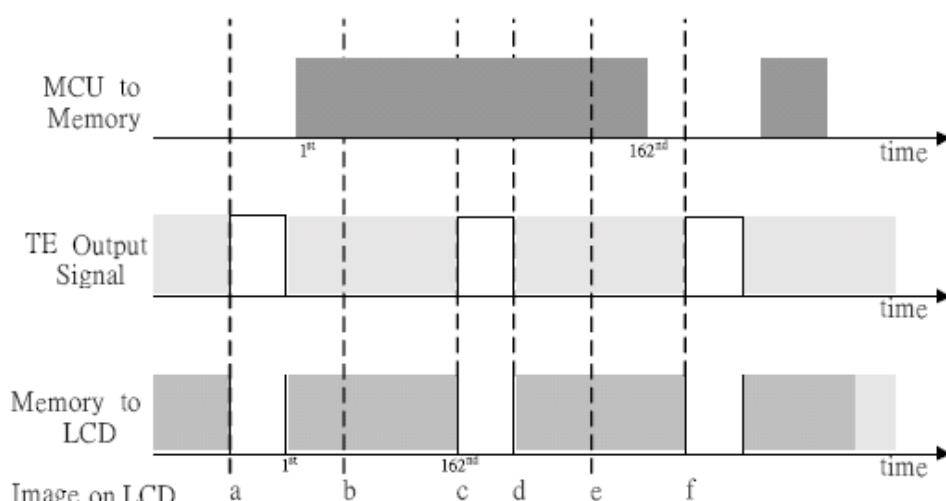
8.2.1 Example 1 MCU Write is Faster than Panel Read



Data write to Frame Memory is now synchronized to the Panel Scan. It should be written during the vertical sync pulse of the Tearing Effect Output Line. This ensures that data is always written ahead of the panel scan and each Panel Frame refresh has a complete new image:

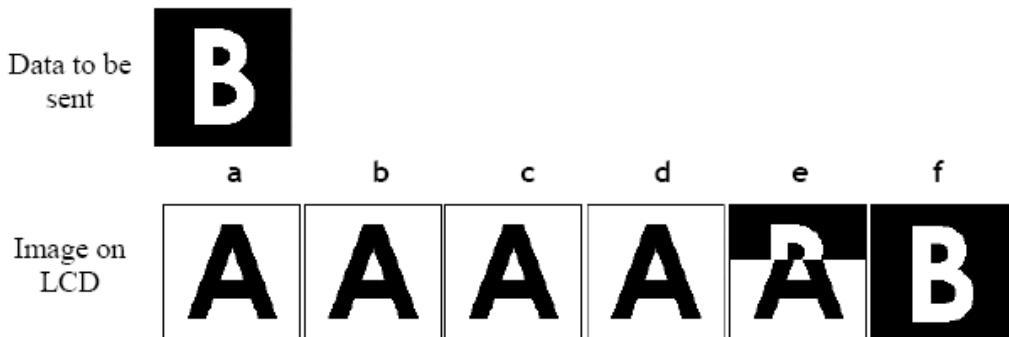


8.2.2 Example 2 MCU Write is slower than Panel Read



The MCU to Frame Memory write begins just after Panel Read has commenced i.e. after one horizontal sync

pulse of the Tearing Effect Output Line. This allows time for the image to download behind the Panel Read pointer and finishing download during the subsequent Frame before the Read Pointer “catches” the MCU to Frame memory write position.



9. Power ON/OFF Sequence

VDDI and VCI can be applied in any order.

VCI and VDDI can be powered down in any order.

During power off, if LCD is in the Sleep Out mode, VCI and VDDI must be powered down minimum 120msec after RESX has been released.

During power off, if LCD is in the Sleep In mode, VDDI or VCI can be powered down minimum 0msec after RESX has been released.

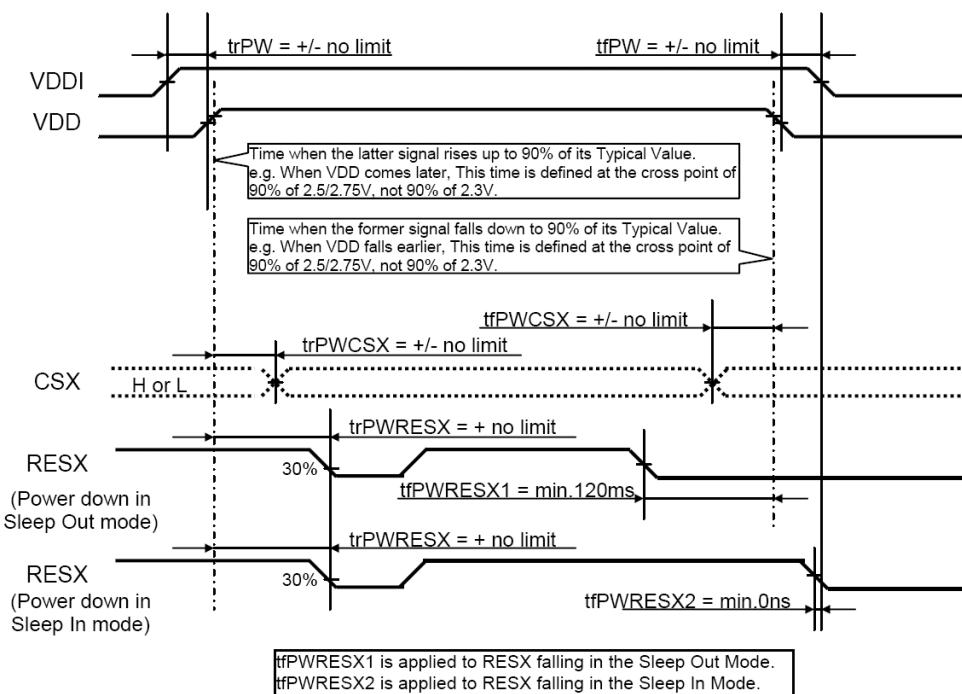
CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX.

Notes:

1. There will be no damage to the display module if the power sequences are not met.
2. There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.
3. There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.
4. If RESX line is not held stable by host during Power On Sequence as defined in Sections 9.1 and 9.2, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.

9.1 Case 1 – RESX line is held high or Unstable by Host at Power –On

If RESX line is held high or unstable by the host during Power On, then a Hardware Reset must be applied after both VCI and VDDI have been applied – otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.

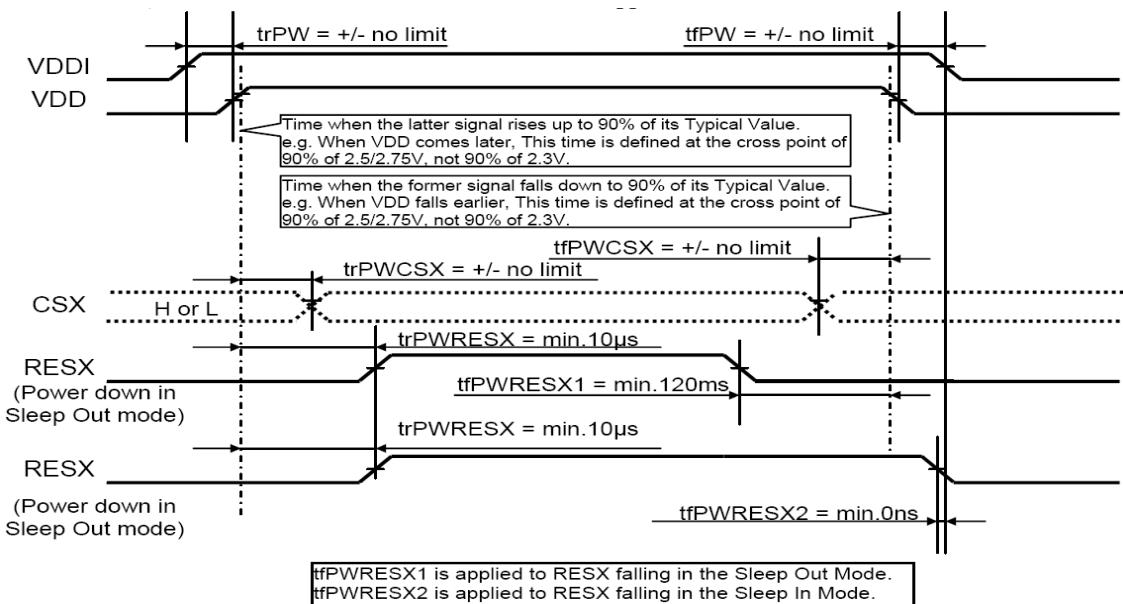


Note: Unless otherwise specified, timings herein show cross point at 50% of signal/power level.

9.2 Case 2 – RESX line is held Low by Host at Power On

If RESX line is held Low (and stable) by the host during Power On, then the RESX must be held low for minimum

10μsec after both VCI and VDDI have been applied.



Note: Unless otherwise specified, timings herein show cross point at 50% of signal/power level.

9.3 Uncontrolled Power Off

The uncontrolled power off means a situation when e.g. there is removed a battery without the controlled power off sequence. The display module must meet following requirements:

1. There cannot be any damages for the display module or the display module cannot cause any damages for the host or lines of the interface.
2. There cannot be any abnormal visible effects (= Display must be blank) within 1 second on the display and remains blank until "Power On Sequence" powers it up.

10. Power Level Definition

10.1 Power Levels

6 level modes are defined they are in order of Maximum Power consumption to Minimum Power Consumption:

1. Normal Mode On (full display), Idle Mode Off, Sleep Out.

In this mode, the display is able to show maximum 262,144 colors.

2. Partial Mode On, Idle Mode Off, Sleep Out.

In this mode part of the display is used with maximum 262,144 colors.

3. Normal Mode On (full display), Idle Mode On, Sleep Out.

In this mode, the full display area is used but with 8 colors.

4. Partial Mode On, Idle Mode On, Sleep Out.

In this mode, part of the display is used but with 8 colors.

5. Sleep In Mode.

In this mode, the DC:DC converter, Internal oscillator and panel driver circuit are stopped. Only the MCU interface and memory works with VDDI power supply. Contents of the memory are safe.

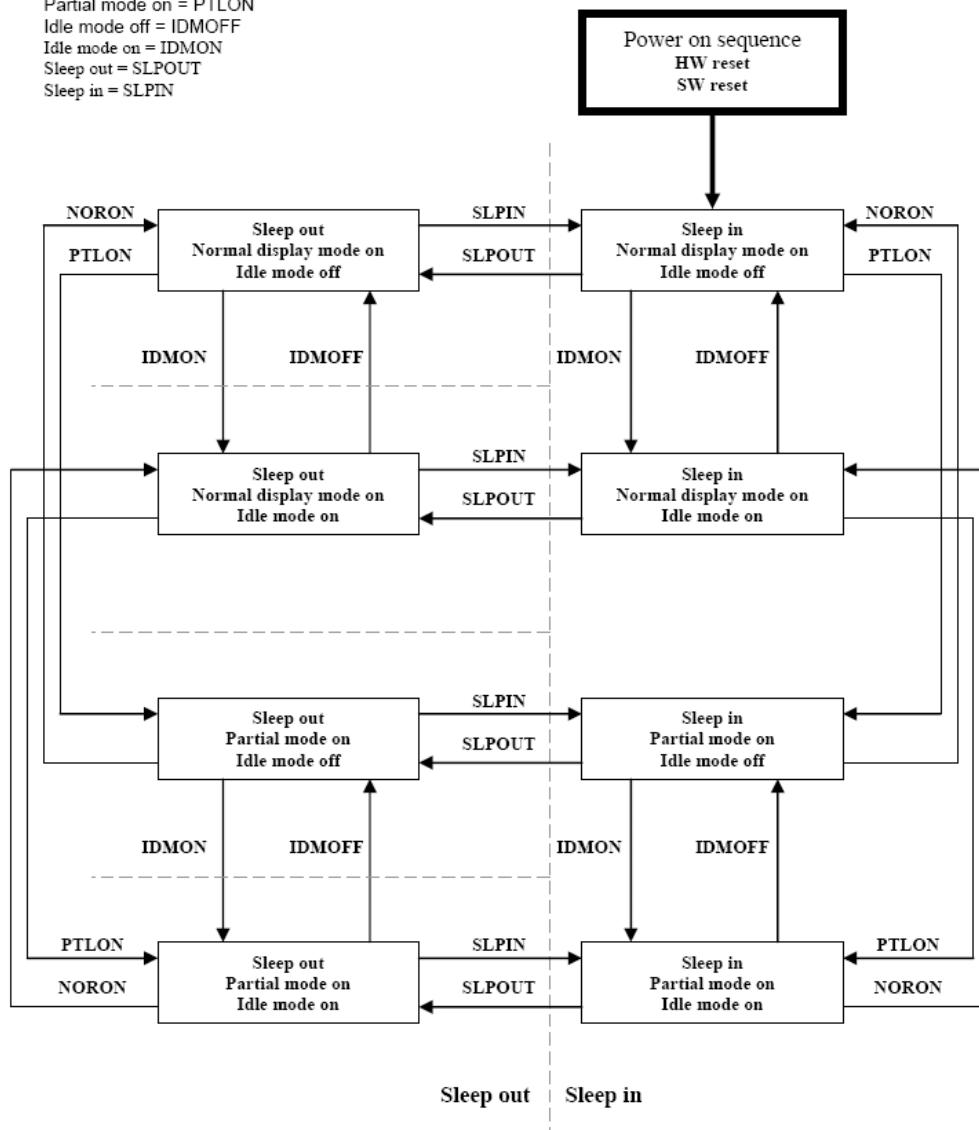
- V. .₁ Power Off Mode.

In this mode, both VCI and VDDI are removed.

Note: Transition between modes 1-5 is controllable by MCU commands. Mode 6 is entered only when both Power supplies are removed.

10.2 Power Flow Chart

Normal display mode on = NORON
Partial mode on = PTLON
Idle mode off = IDMOFF
Idle mode on = IDMON
Sleep out = SLPOUT
Sleep in = SLPIN



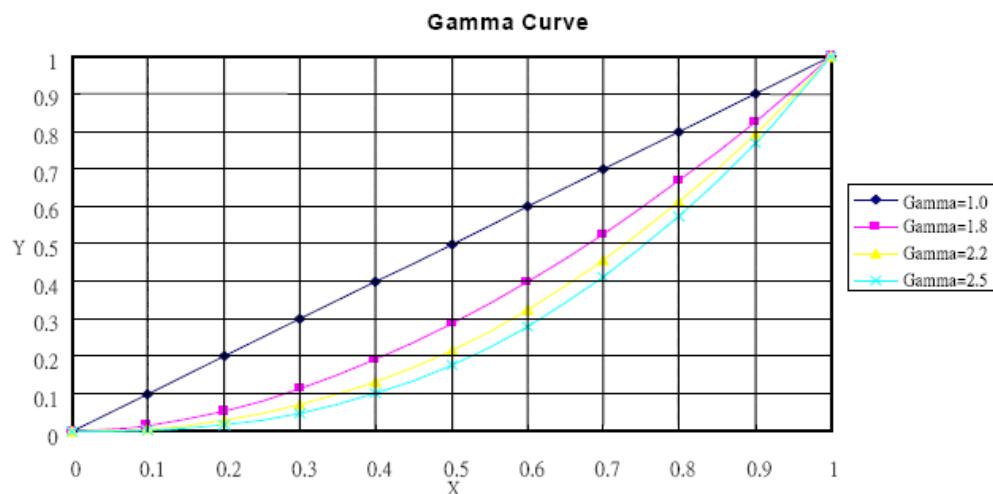
Note 1: There is not any abnormal visual effect when there is changing from one power mode to another power mode.

Note 2: There is not any limitation, which is not specified by Nokia, when there is changing from one power mode to another power mode.

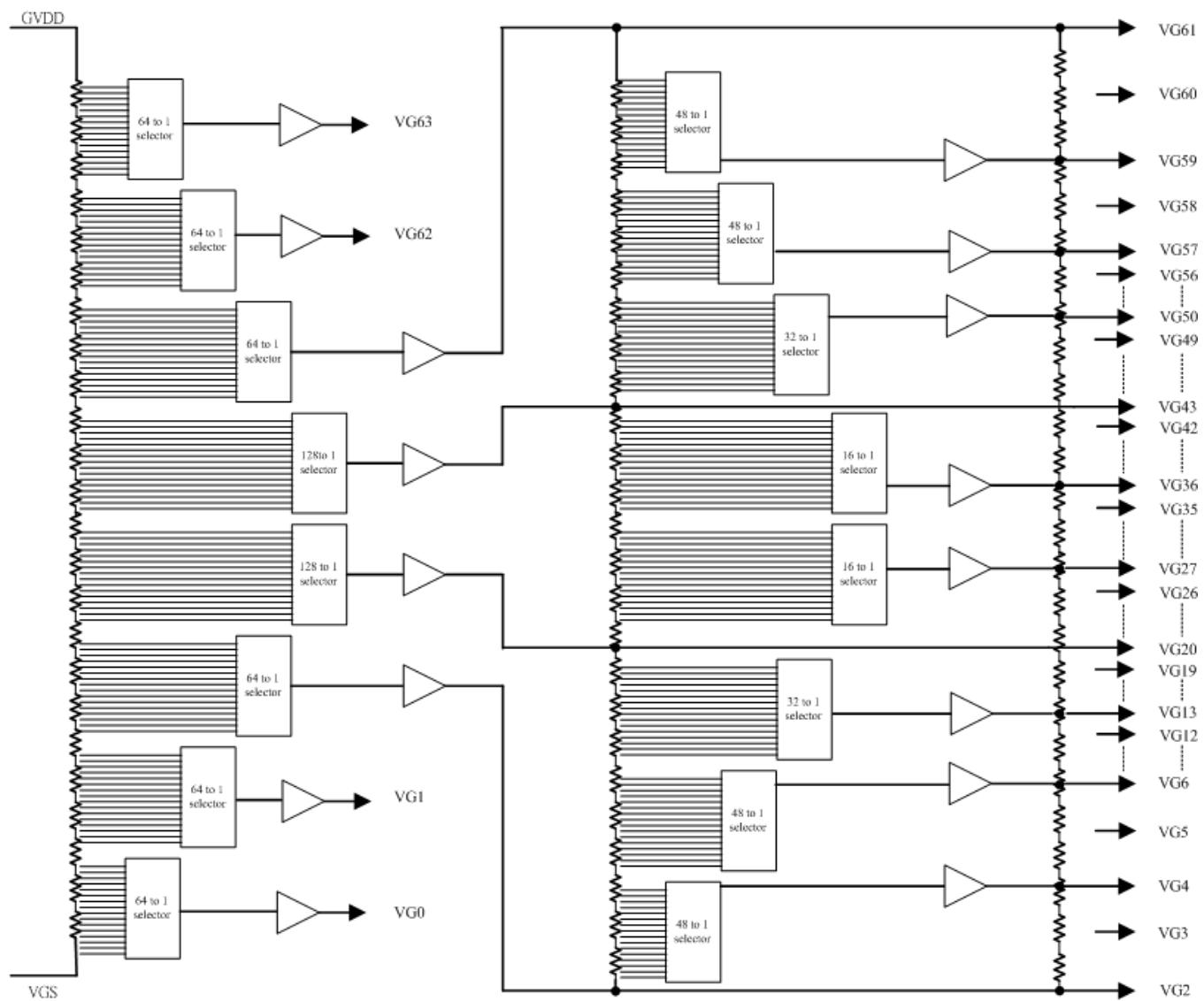
Note 3: It is recommended that it should be enter Sleep in before power off.

11. Gamma Curves

11.1 Gamma curve according to the Gamma1.0/1.8/2.2/2.5



11.2 Gamma Structure



Positive Gamma Correction

Grayscale	Value "X" in Formula	Input Range	Formula
VP0	VP0[5:0]	0 - 63	$((130R-X^R)/130R) * (GVDD-VGS) + VGS$
VP1	VP1[5:0]	0 - 63	$((130R-X^R)/130R) * (GVDD-VGS) + VGS$
VP2	VP2[5:0]	0 - 63	$((130R-X^R)/130R) * (GVDD-VGS) + VGS$
VP4	VP4[5:0]	0 - 47	$((47R-X^R)/47R) * (VP2-VP20) + VP20$
VP6	VP6[5:0]	0 - 47	$((47R-X^R)/47R) * (VP2-VP20) + VP20$
VP13	VP13[4:0]	0 - 31	$((32R-X^R)/47R) * (VP2-VP20) + VP20$
VP20	VP20[6:0]	0 - 127	$((130R-X^R)/130R) * (GVDD-VGS) + VGS$
VP27	VP27[3:0]	0 - 15	$((36R-X^R)/39R) * (VP20-VP43) + VP43$
VP36	VP36[3:0]	0 - 15	$((18R-X^R)/39R) * (VP20-VP43) + VP43$
VP43	VP43[6:0]	0 - 127	$((130R-X^R)/130R) * (GVDD-VGS) + VGS$
VP50	VP50[4:0]	0 - 31	$((46R-X^R)/47R) * (VP43-VP61) + VP61$
VP57	VP57[5:0]	0 - 47	$((47R-X^R)/47R) * (VP43-VP61) + VP61$
VP59	VP59[5:0]	0 - 47	$((47R-X^R)/47R) * (VP43-VP61) + VP61$
VP61	VP61[5:0]	0 - 63	$((66R-X^R)/130R) * (GVDD-VGS) + VGS$
VP62	VP62[5:0]	0 - 63	$((66R-X^R)/130R) * (GVDD-VGS) + VGS$
VP63	VP63[5:0]	0 - 63	$((66R-X^R)/130R) * (GVDD-VGS) + VGS$

Negative Gamma Correction

Grayscale	Value "X" in Formula	Input Range	Formula
VN63	VN63[5:0]	0 - 63	$((66R-X^R)/130R) * (GVDD-VGS) + VGS$
VN62	VN62[5:0]	0 - 63	$((66R-X^R)/130R) * (GVDD-VGS) + VGS$
VN61	VN61[5:0]	0 - 63	$((66R-X^R)/130R) * (GVDD-VGS) + VGS$
VN59	VN59[5:0]	0 - 47	$((47R-X^R)/47R) * (VN43-VN61) + VN61$
VN57	VN57[5:0]	0 - 47	$((47R-X^R)/47R) * (VN43-VN61) + VN61$
VN50	VN50[4:0]	0 - 31	$((46R-X^R)/47R) * (VN43-VN61) + VN61$
VN43	VN43[6:0]	0 - 127	$((130R-X^R)/130R) * (GVDD-VGS) + VGS$
VN36	VN36[3:0]	0 - 15	$((18R-X^R)/39R) * (VN20-VN43) + VN43$
VN27	VN27[3:0]	0 - 15	$((36R-X^R)/39R) * (VN20-VN43) + VN43$
VN20	VN20[6:0]	0 - 127	$((130R-X^R)/130R) * (GVDD-VGS) + VGS$
VN13	VN13[4:0]	0 - 31	$((32R-X^R)/47R) * (VN2-VN20) + VN20$
VN6	VN6[5:0]	0 - 47	$((47R-X^R)/47R) * (VN2-VN20) + VN20$
VN4	VN4[5:0]	0 - 47	$((47R-X^R)/47R) * (VN2-VN20) + VN20$
VN2	VN2[5:0]	0 - 63	$((130R-X^R)/130R) * (GVDD-VGS) + VGS$
VN1	VN1[5:0]	0 - 63	$((130R-X^R)/130R) * (GVDD-VGS) + VGS$
VN0	VN0[5:0]	0 - 63	$((130R-X^R)/130R) * (GVDD-VGS) + VGS$

12. Reset

12.1 Registers

The registers that are initialized are listed below.

Reset Table (Default Value, GM=000, 128RGB x 160)

Item	After Power On	After Hardware Reset	After Software Reset
Frame memory	Random	No Change	No Change
Sleep In/Out	In	In	In
Display In/Out	Off	Off	Off
Display mode(normal/partial)	Normal	Normal	Normal
Display Inversion On/Off	Off	Off	Off
Display Idle Mode On/Off	Off	Off	Off
Column: Start Address(XS)	0000h	0000h	0000h
Column: end Address(XE)	007Fh	007Fh	007Fh(127d) (when MV=0) 009Fh(159d) (when MV=1)
Row: Start Address(YS)	0000h	0000h	0000h
Row: End Address(YE)	009Fh	009Fh	009Fh(159d) (when MV=0) 007Fh(127d) (when MV=1)
Gamma Setting	GC0	GC0	GC0
Color Set	TBD	TBD	No Change
Partial: Start Address(PSL)	0000h	0000h	0000h
Partial: End Address(PEL)	009Fh	009Fh	009Fh
Scroll: Vertical scrolling	Off	Off	Off
Scroll: Top Fixed Area(TFA)	0000h	0000h	0000h
Scroll: Scroll area(VSA)	00A0h	00A0h	00A0h
Scroll: Bottom Fixed Area (BFA)	0000h	0000h	0000h
Scroll Start Address(SSA)	0000h	0000h	0000h
Tearing: On/Off	Off	Off	Off
Tearing Effect Mode*3	0(Mode1)	0(Mode1)	0(Mode1)
Memory Data Access Control (MY/MX/MV/ML/MH/RGB)	0/0/0/0/0/0	0/0/0/0/0/0	No change
Interface Pixel Color Format	6 (18-Bit/Pixel)	6 (18-Bit/Pixel)	No change
RDDPM	08h	08h	08h
RDDMADCTR	00h	00h	No change
RDDCOLMOD	6 (18-Bit/Pixel)	6 (18-Bit/Pixel)	No change
RDDIM	00h	00h	00h
RDDSM	00h	00h	00h
RDDSDR	00h	00h	00h
ID1	54h	54h	54h
ID2	MTP Value	MTP Value	MTP Value
ID3	MTP Value	MTP Value	MTP Value

Notes:

1. There will be no abnormal visible effects on the display when S/W or H/W Reset are applied.
2. After Powered-On Reset finishes within 10μs after both VCI & VDDI are applied.
3. Mode 1 means Tearing Effect Output Line consists of V-Blanking Information only.

Reset Table (Default Value, GM=010, 120RGB x 160)

Item	After Power On	After Hardware Reset	After Software Reset
Frame memory	Random	No Change	No Change
Sleep In/Out	In	In	In
Display In/Out	Off	Off	Off
Display mode(normal/partial)	Normal	Normal	Normal
Display Inversion On/Off	Off	Off	Off
Display Idle Mode On/Off	Off	Off	Off
Column: Start Address(XS)	0000h	0000h	0000h
Column: end Address(XE)	0077h	0077h	0077h(119d) (when MV=0) 0077h(159d) (when MV=1)
Row: Start Address(YS)	0000h	0000h	0000h
Row: End Address(YE)	009Fh	009Fh	009Fh(159d) (when MV=0) 0077h(119d) (when MV=1)
Gamma Setting	GC0	GC0	GC0
Color Set	TBD	TBD	No Change
Partial: Start Address(PSL)	0000h	0000h	0000h
Partial: End Address(PEL)	009Fh	009Fh	009Fh
Scroll: Vertical scrolling	Off	Off	Off
Scroll: Top Fixed Area(TFA)	0000h	0000h	0000h
Scroll: Scroll area(VSA)	00A0h	00A0h	00A0h
Scroll: Bottom Fixed Area (BFA)	0000h	0000h	0000h
Scroll Start Address(SSA)	0000h	0000h	0000h
Tearing: On/Off	Off	Off	Off
Tearing Effect Mode*3	0(Mode1)	0(Mode1)	0(Mode1)
Memory Data Access Control (MY/MX/MV/ML/MH/RBG)	0/0/0/0/0/0	0/0/0/0/0/0	No change
Interface Pixel Color Format	6 (18-Bit/Pixel)	6 (18-Bit/Pixel)	No change
RDDPM	08h	08h	08h
RDDMADCTR	00h	00h	No change
RDDCOLMOD	6 (18-Bit/Pixel)	6 (18-Bit/Pixel)	No change
RDDIM	00h	00h	00h
RDDSM	00h	00h	00h
RDDSDR	00h	00h	00h
ID1	54h	54h	54h
ID2	MTP Value	MTP Value	MTP Value
ID3	MTP Value	MTP Value	MTP Value

Notes:

1. There will be no abnormal visible effects on the display when S/W or H/W Reset are applied.
2. After Powered-On Reset finishes within 10μs after both VCI & VDDI are applied.
3. Mode 1 means Tearing Effect Output Line consists of V-Blanking Information only.

Reset Table (Default Value, GM=010, 128RGB x 128)

Item	After Power On	After Hardware Reset	After Software Reset
Frame memory	Random	No Change	No Change
Sleep In/Out	In	In	In
Display In/Out	Off	Off	Off
Display mode(normal/partial)	Normal	Normal	Normal
Display Inversion On/Off	Off	Off	Off
Display Idle Mode On/Off	Off	Off	Off
Column: Start Address(XS)	0000h	0000h	0000h
Column: end Address(XE)	007Fh	007Fh	007Fh(127d) (when MV=0) 0077h(127d) (when MV=1)
Row: Start Address(YS)	0000h	0000h	0000h
Row: End Address(YE)	007Fh	007Fh	007Fh(127d) (when MV=0) 007Fh(127d) (when MV=1)
Gamma Setting	GC0	GC0	GC0
Color Set	TBD	TBD	No Change
Partial: Start Address(PSL)	0000h	0000h	0000h
Partial: End Address(PEL)	007Fh	007Fh	007Fh
Scroll: Vertical scrolling	Off	Off	Off
Scroll: Top Fixed Area(TFA)	0000h	0000h	0000h
Scroll: Scroll area(VSA)	0080h	0080h	0080h
Scroll: Bottom Fixed Area (BFA)	0000h	0000h	0000h
Scroll Start Address(SSA)	0000h	0000h	0000h
Tearing: On/Off	Off	Off	Off
Tearing Effect Mode*3	0(Mode1)	0(Mode1)	0(Mode1)
Memory Data Access Control (MY/MX/MV/ML/MH/RBG)	0/0/0/0/0/0	0/0/0/0/0/0	No change
Interface Pixel Color Format	6 (18-Bit/Pixel)	6 (18-Bit/Pixel)	No change
RDDPM	08h	08h	08h
RDDMADCTR	00h	00h	No change
RDDCOLMOD	6 (18-Bit/Pixel)	6 (18-Bit/Pixel)	No change
RDDIM	00h	00h	00h
RDDSM	00h	00h	00h
RDDSDR	00h	00h	00h
ID1	54h	54h	54h
ID2	MTP Value	MTP Value	MTP Value
ID3	MTP Value	MTP Value	MTP Value

Notes:

1. There will be no abnormal visible effects on the display when S/W or H/W Reset are applied.
2. After Powered-On Reset finishes within 10μs after both VCI & VDDI are applied.
3. Mode 1 means Tearing Effect Output Line consists of V-Blanking Information only.

Reset Table (Default Value, GM=011, 132RGB x 162)

Item	After Power On	After Hardware Reset	After Software Reset
Frame memory	Random	No Change	No Change
Sleep In/Out	In	In	In
Display In/Out	Off	Off	Off
Display mode(normal/partial)	Normal	Normal	Normal
Display Inversion On/Off	Off	Off	Off
Display Idle Mode On/Off	Off	Off	Off
Column: Start Address(XS)	0000h	0000h	0000h
Column: end Address(XE)	0083h	0083h	0083h(131d) (when MV=0) 00A1h(161d) (when MV=1)
Row: Start Address(YS)	0000h	0000h	0000h
Row: End Address(YE)	00A1h	00A1h	00A1h(161d) (when MV=0) 0083h(131d) (when MV=1)
Gamma Setting	GC0	GC0	GC0
Color Set	TBD	TBD	No Change
Partial: Start Address(PSL)	0000h	0000h	0000h
Partial: End Address(PEL)	00A1h	00A1h	00A1h
Scroll: Vertical scrolling	Off	Off	Off
Scroll: Top Fixed Area(TFA)	0000h	0000h	0000h
Scroll: Scroll area(VSA)	00A2h	00A2h	00A2h
Scroll: Bottom Fixed Area (BFA)	0000h	0000h	0000h
Scroll Start Address(SSA)	0000h	0000h	0000h
Tearing: On/Off	Off	Off	Off
Tearing Effect Mode*3	0(Mode1)	0(Mode1)	0(Mode1)
Memory Data Access Control (MY/MX/MV/ML/MH/RGB)	0/0/0/0/0/0	0/0/0/0/0/0	No change
Interface Pixel Color Format	6 (18-Bit/Pixel)	6 (18-Bit/Pixel)	No change
RDDPM	08h	08h	08h
RDDMADCTR	00h	00h	No change
RDDCOLMOD	6 (18-Bit/Pixel)	6 (18-Bit/Pixel)	No change
RDDIM	00h	00h	00h
RDDSM	00h	00h	00h
RDDSDR	00h	00h	00h
ID1	54h	54h	54h
ID2	MTP Value	MTP Value	MTP Value
ID3	MTP Value	MTP Value	MTP Value

Notes:

1. There will be no abnormal visible effects on the display when S/W or H/W Reset are applied.
2. After Powered-On Reset finishes within 10μs after both VCI & VDDI are applied.
3. Mode 1 means Tearing Effect Output Line consists of V-Blanking Information only.

Reset Table (Default Value, GM=100, 130RGB x 130)

Item	After Power On	After Hardware Reset	After Software Reset
Frame memory	Random	No Change	No Change
Sleep In/Out	In	In	In
Display In/Out	Off	Off	Off
Display mode(normal/partial)	Normal	Normal	Normal
Display Inversion On/Off	Off	Off	Off
Display Idle Mode On/Off	Off	Off	Off
Column: Start Address(XS)	0000h	0000h	0000h
Column: end Address(XE)	0081h	0081h	0081h(when MV=0) 0081h(when MV=1)
Row: Start Address(YS)	0000h	0000h	0000h
Row: End Address(YE)	0081h	0081h	0081h(when MV=0) 0081h(when MV=1)
Gamma Setting	GC0	GC0	GC0
Color Set	TBD	TBD	No Change
Partial: Start Address(PSL)	0000h	0000h	0000h
Partial: End Address(PEL)	0081h	0081h	0081h
Scroll: Vertical scrolling	Off	Off	Off
Scroll: Top Fixed Area(TFA)	0000h	0000h	0000h
Scroll: Scroll area(VSA)	0082h	0082h	0082h
Scroll: Bottom Fixed Area (BFA)	0000h	0000h	0000h
Scroll Start Address(SSA)	0000h	0000h	0000h
Tearing: On/Off	Off	Off	Off
Tearing Effect Mode*3	0(Mode1)	0(Mode1)	0(Mode1)
Memory Data Access Control (MY/MX/MV/ML/MH/RGB)	0/0/0/0/0/0	0/0/0/0/0/0	No change
Interface Pixel Color Format	6 (18-Bit/Pixel)	6 (18-Bit/Pixel)	No change
RDDPM	08h	08h	08h
RDDMADCTR	00h	00h	No change
RDDCOLMOD	6 (18-Bit/Pixel)	6 (18-Bit/Pixel)	No change
RDDIM	00h	00h	00h
RDDSM	00h	00h	00h
RDDSDR	00h	00h	00h
ID1	54h	54h	54h
ID2	MTP Value	MTP Value	MTP Value
ID3	MTP Value	MTP Value	MTP Value

Notes:

1. There will be no abnormal visible effects on the display when S/W or H/W Reset are applied.
2. After Powered-On Reset finishes within 10μs after both VCI & VDDI are applied.
3. Mode 1 means Tearing Effect Output Line consists of V-Blanking Information only.

Reset Table (Default Value, GM=101, 132RGB x 132)

Item	After Power On	After Hardware Reset	After Software Reset
Frame memory	Random	No Change	No Change
Sleep In/Out	In	In	In
Display In/Out	Off	Off	Off
Display mode(normal/partial)	Normal	Normal	Normal
Display Inversion On/Off	Off	Off	Off
Display Idle Mode On/Off	Off	Off	Off
Column: Start Address(XS)	0000h	0000h	0000h
Column: end Address(XE)	0083h	0083h	0083h(when MV=0) 0083h(when MV=1)
Row: Start Address(YS)	0000h	0000h	0000h
Row: End Address(YE)	0083h	0083h	0083h(when MV=0) 0083h(when MV=1)
Gamma Setting	GC0	GC0	GC0
Color Set	TBD	TBD	No Change
Partial: Start Address(PSL)	0000h	0000h	0000h
Partial: End Address(PEL)	0083h	0083h	0083h
Scroll: Vertical scrolling	Off	Off	Off
Scroll: Top Fixed Area(TFA)	0000h	0000h	0000h
Scroll: Scroll area(VSA)	0084h	0084h	0084h
Scroll: Bottom Fixed Area (BFA)	0000h	0000h	0000h
Scroll Start Address(SSA)	0000h	0000h	0000h
Tearing: On/Off	Off	Off	Off
Tearing Effect Mode*3	0(Mode1)	0(Mode1)	0(Mode1)
Memory Data Access Control (MY/MX/MV/ML/MH/RGB)	0/0/0/0/0/0	0/0/0/0/0/0	No change
Interface Pixel Color Format	6 (18-Bit/Pixel)	6 (18-Bit/Pixel)	No change
RDDPM	08h	08h	08h
RDDMADCTR	00h	00h	No change
RDDCOLMOD	6 (18-Bit/Pixel)	6 (18-Bit/Pixel)	No change
RDDIM	00h	00h	00h
RDDSM	00h	00h	00h
RDDSDR	00h	00h	00h
ID1	54h	54h	54h
ID2	MTP Value	MTP Value	MTP Value
ID3	MTP Value	MTP Value	MTP Value

Notes:

1. There will be no abnormal visible effects on the display when S/W or H/W Reset are applied.
2. After Powered-On Reset finishes within 10μs after both VCI & VDDI are applied.
3. Mode 1 means Tearing Effect Output Line consists of V-Blanking Information only.

12.2 Input/Output Pins

12.2.1 Output Pins, I/O Pins

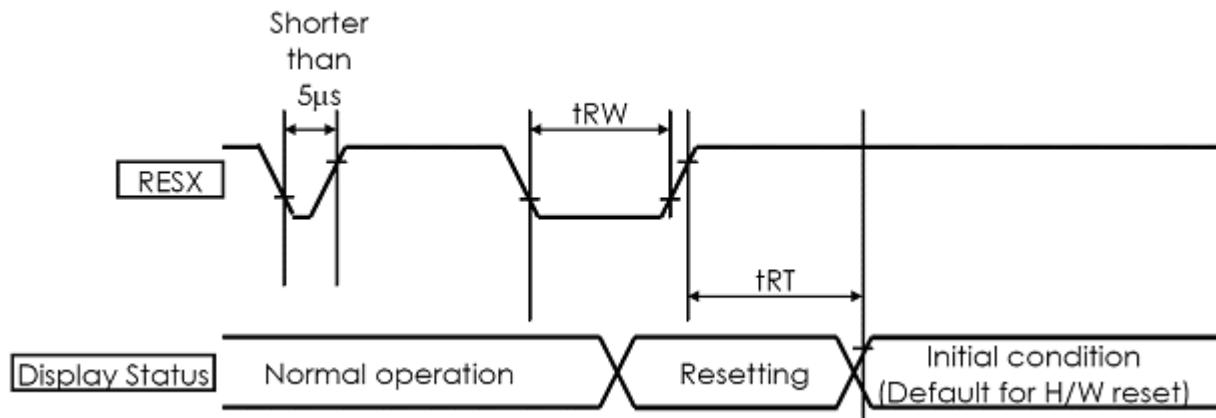
Output or Bi-direction pins	After Power On	After Hardware Reset	After Software Reset
TE	Low	Low	Low
D17to D0(Output driver)	High-Z(Inactive)	High-Z(Inactive)	High-Z(Inactive)

Note: There will be no output from D[7..0] and SDA during Power On/Off sequences, Hardware Reset and Software Reset.

12.2.2 Input Pins

Input pins	During Power On Process	After Power On	After Hardware Reset	After Software Reset	During Power Off Process
RESX	TBD	Input invalid	Input invalid	Input invalid	?
CSX	Input invalid	Input invalid	Input invalid	Input invalid	Input invalid
D/CX	Input invalid	Input invalid	Input invalid	Input invalid	Input invalid
WRX	Input invalid	Input invalid	Input invalid	Input invalid	Input invalid
RDX	Input invalid	Input invalid	Input invalid	Input invalid	Input invalid
D17 to D0	Input invalid	Input invalid	Input invalid	Input invalid	Input invalid
SDA	Input invalid	Input invalid	Input invalid	Input invalid	Input invalid

12.3 Reset Timing



(VSS=0V, VDDI=1.65V to 1.95V, VCI=2.6V to 2.9V, Ta = -30 to 70°C)

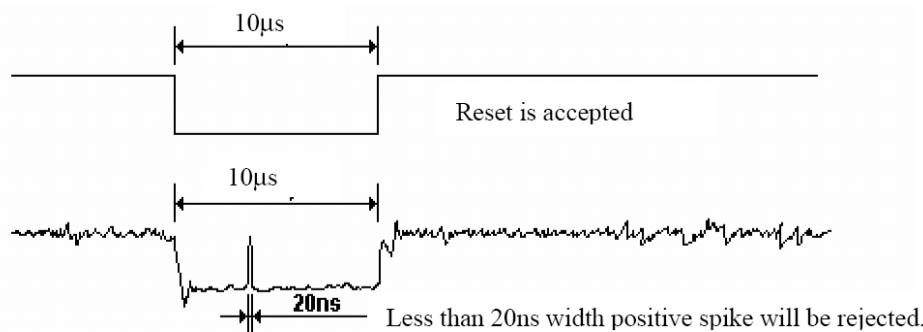
Symbol	Parameter	Related Pins	MIN	TYP	MAX	Note	Unit
tRESW	*1) Reset low pulse width	RESX	10	-	-	-	μs
tREST	*2) Reset complete width	-	-	-	5	When reset applied during Sleep in mode	ms
		-	-	-	120	When reset applied during Sleep out mode	ms

Note

1. Spike due to an electrostatic discharge on RESX line does not cause system reset according to the table below.

RESX Pulse	Action
Shorten than 5μs	Reset Rejected
Longer than 10μs	Reset
Between 5μs and 10μs	Reset starts (It depends on voltage and temperature condition.)

2. During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then return to Default condition for Hardware Reset.
3. During Reset Complete Time, ID2 and VCOMOF value in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of RESX.
4. Spike Rejection also applies during a valid reset pulse as shown below:



5. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

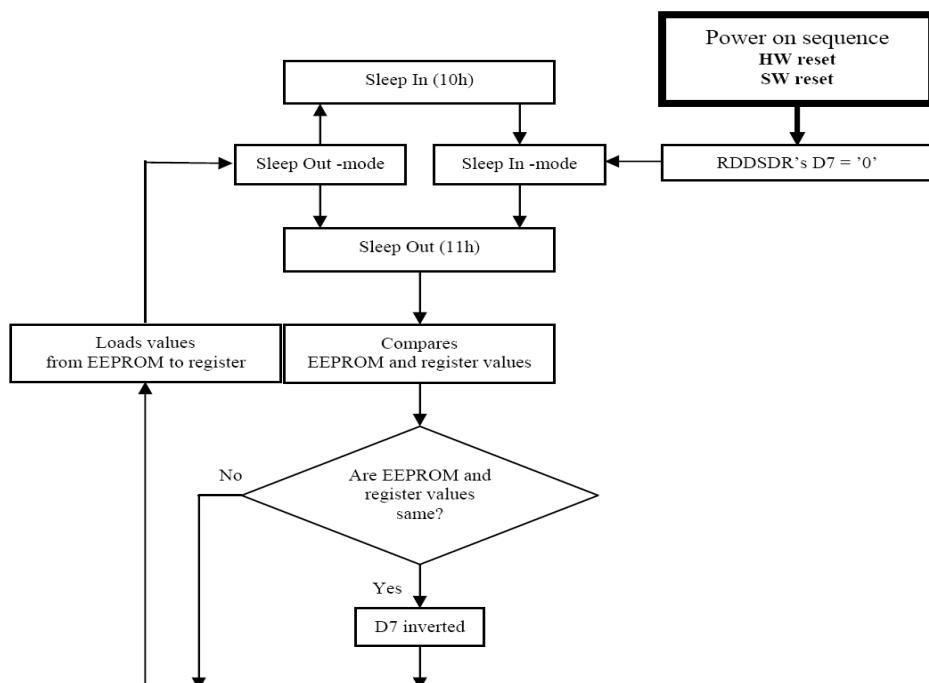
13. SleepOut – Command and Self-Diagnostic Functions of Display

13.1 Register loading Detection

Sleep Out-command (See section 16.1.2.12 Sleep Out (11h)) is a trigger for an internal function of the display module, which indicates, if the display module loading function of factory default values from EEPROM (or similar device) to registers of the display controller is working properly.

There are compared factory values of the EEPROM and register values of the display controller by the display controller. If those both values (EEPROM and register values) are same, there is inverted (= increased by 1) a bit, which is defined in command 16.1.2.10 “Read Display Self-Diagnostic Result (0Fh)” (=RDDSDR) (The used bit of this command is D7). If those both values are not same, the bit(D7) is not inverted (= increased by 1)

The flow chart for this internal function is following:



Note:

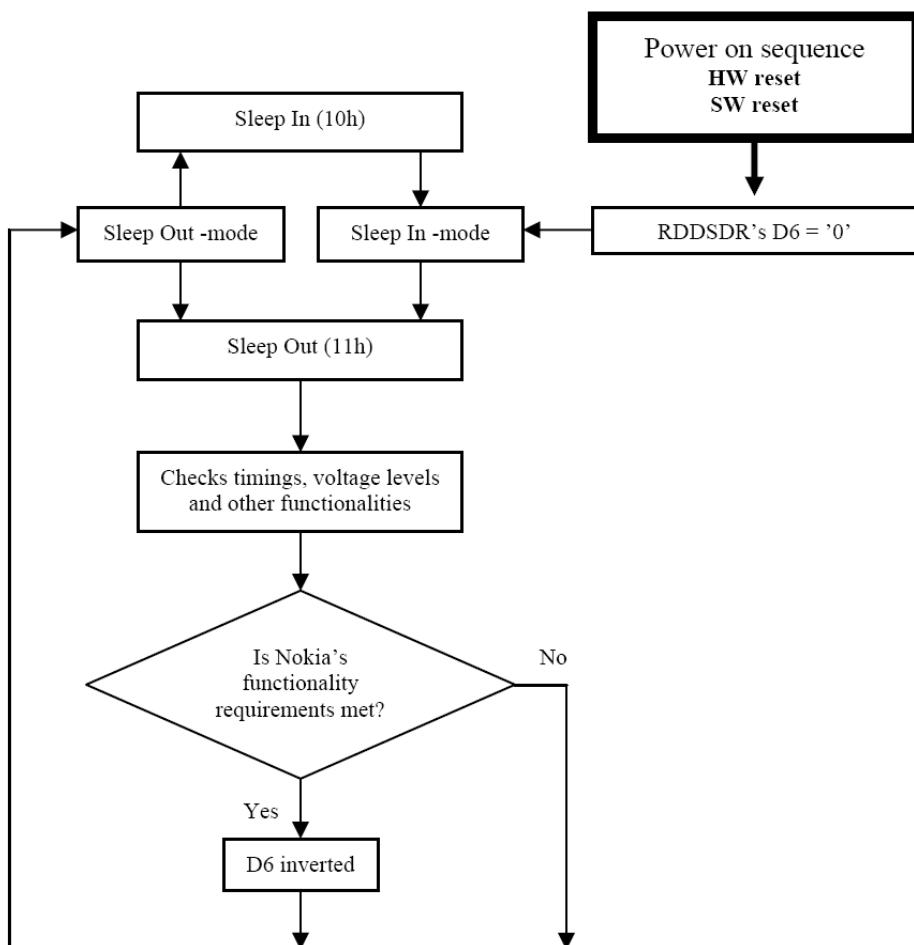
There is not compared and loaded register values, which can be changed by user (00h to AFh and DAh to DDh), by the display module.

13.2 Functionality Detection

Sleep Out-command (See section 16.1.2.12 Sleep Out (11h)) is a trigger for an internal function of the display module, which indicates, if the display module is still running and meets functionality requirements.

The internal function (= the display controller) is comparing, if the display module is still meeting functionality requirements (only Booster voltage level). If functionality requirement is met, there is inverted (= increased by 1) a bit, which defined in command 16.1.2.10 “Read Display Self-Diagnostic Result (0Fh)” (= RDDSDR) (The used bit of this command is D6). If functionality requirement is not same, this bit (D6) is not inverted (=increased by 1).

The flow chart for this internal function is following:



Note: There is needed 120msec after Sleep Out –command, when there is changing from Sleep In –mode to Sleep Out –mode, before there is possible to check if Nokia's functionality requirements are met and a value of RDDSDR's D6 is valid. Otherwise, there is 5msec delay for D6's value, when Sleep Out –command is sent in Sleep Out –mode.

14. Command

14.1 Command List

Code	Command	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Ref.
00H	NOP (No Operation)	X	0	0	0	0	0	0	0	0	00h	14.2.1
01H	Software Reset	X	0	0	0	0	0	0	0	1	01h	14.2.2
04H	Read Display Identification Information	X	0	0	0	0	0	1	0	0	04h	14.2.3
	1 st Parameter	X	X	X	X	X	X	X	X	X	X	
	2 nd Parameter	X	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	54h	
	3 rd Parameter	X	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	80h	
	4 th Parameter	X	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	66h	
09H	Read Display Status	X	0	0	0	0	1	0	0	1	09h	14.2.4
	1 st Parameter	X	X	X	X	X	X	X	X	X	X	
	2 nd Parameter	X	BSTON	MY	MX	MV	ML	RGB	MH	ST24	00h	
	3 rd Parameter	X	ST23	IFPF2	IFPF1	IFPF0	IDMON	PTLON	SLOUT	NORON	61h	
	4 th Parameter	X	VSSON	ST14	INVON	ST12	ST11	DISON	TEON	GCS2	00h	
	5 th Parameter	X	GCS1	GCS0	TELOM	HSON	VSON	PCKON	DEON	ST0	00h	
0AH	Read Display Power Mode	X	0	0	0	0	1	0	1	0	0Ah	12.4.5
	1 st Parameter	X	X	X	X	X	X	X	X	X	X	
	2 nd Parameter	X	BSTON	IDMON	PLTON	SLPOUT	NORON	DISON	D1	D0	08h	
0BH	Read Display MADCTL	X	0	0	0	0	1	0	1	1	0Bh	12.4.6
	1 st Parameter	X	X	X	X	X	X	X	X	X	X	
	2 nd Parameter	X	MY	MX	MV	ML	RGB	MH	D1	D0	00h	
0CH	Read Display Pixel Format	X	0	0	0	0	1	1	0	0	0Ch	12.4.7
	1 st Parameter	X	X	X	X	X	X	X	X	X	X	
	2 nd Parameter	X	VIPF3	VIPF2	VIPF1	VIPF0	D3	IFPF2	IFPF1	IFPF0	06h	
0DH	Read Display Image Mode	X	0	0	0	0	1	1	0	1	0Dh	12.4.8
	1 st Parameter	X	X	X	X	X	X	X	X	X	X	
	2 nd Parameter	X	VSSON	D6	INVON	D4	D3	GCS2	GCS1	GCS0	00h	
0EH	Read Display Signal Mode	x	0	0	0	0	1	1	1	0	0Eh	14.2.9
	1 st Parameter	x	x	x	x	x	x	x	x	x	x	
	2 nd Parameter	x	D7	D6	HSON	VSON	PCKON	DEON	D1	D0	00h	
0FH	Read Display Signal Mode	x	0	0	0	0	1	1	1	1	0Fh	14.2.10
	1 st Parameter	x	X	x	x	x	x	x	x	x	x	
	2 nd Parameter	x	RELD	FUND	D5	D4	D3	D2	D1	D0	00h	

10H	Sleep In	x	0	0	0	1	0	0	0	0	10h	14.2.11
11H	Sleep Out	x	0	0	0	1	0	0	0	1	11h	14.2.12
12H	Partial Mode On	x	0	0	0	1	0	0	1	0	12h	14.2.13
13H	Normal Display Mode On	x	0	0	0	1	0	0	1	1	13h	14.2.14
20H	Display Inversion Off	x	0	0	1	0	0	0	0	0	20h	14.2.15
21H	Display Inversion On	x	0	0	1	0	0	0	0	1	21h	14.2.16
26H	Gamma Set	x	0	0	1	0	0	1	1	0	26h	14.2.17
	1 st Parameter	x	GC7	GC6	GC5	GC4	GC3	GC2	GC1	GC0	01h	
28H	Display Off	x	0	0	1	0	1	0	0	0	28h	14.2.18
29H	Display On	x	0	0	1	0	1	0	0	1	29h	14.2.19
2AH	Column Address Set	x	0	0	1	0	1	0	1	0	2Ah	14.2.20
	1 st Parameter	x	XS15	XS14	XS13	XS12	XS11	XS10	XS9	XS8	-	
	2 nd Parameter	x	XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0	-	
	3 rd Parameter	x	XE15	XE14	XE13	XE12	XE11	XE10	XE9	XE8	-	
	4 th Parameter	x	XE7	XE6	XE5	XE4	XE3	XE2	XE1	XE0	-	
2BH	Page Address Set	x	0	0	1	0	1	0	1	1	2Bh	14.2.21
	1 st Parameter	x	YS15	YS14	YS13	YS12	YS11	YS10	YS9	YS8	-	
	2 nd Parameter	x	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0	-	
	3 rd Parameter	x	YE15	YE14	YE13	YE12	YE11	YE10	YE9	YE8	-	
	4 th Parameter	x	YE7	YE6	YE5	YE4	YE3	YE2	YE1	YE0	-	
2CH	Memory Write	x	0	0	1	0	1	1	0	0	2Ch	14.2.22
	1 st Parameter	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	-	
	:	x	:	:	:	:	:	:	:	:	:	
	N th Parameter	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	-	
2DH	Color Setting for 4K, 65K and 262K	x	0	0	1	0	1	1	0	1	2Dh	14.2.23
	1 st Parameter	x	x	x	R005	R004	R003	R002	R001	R000	-	
	:	x	x	x	Rnn5	Rnn4	Rnn3	Rnn2	Rnn1	Rnn0	-	
	32 nd parameter	x	x	x	R315	R314	R313	R312	R311	R310	-	
	33 rd Parameter	x	x	x	G005	G004	G003	G002	G001	G000	-	
	:	x	x	x	Gnn5	Gnn4	Gnn3	Gnn2	Gnn1	Gnn0	-	
	96 th Parameter	x	x	x	G635	G634	G633	G632	G631	G630	-	
	97 th Parameter	x	x	x	B005	B004	B003	B002	B001	B000	-	
	:	x	x	x	Bnn5	Bnn4	Bnn3	Bnn2	Bnn1	Bnn0	-	
	128 th Parameter	x	x	x	B315	B314	B313	B312	B311	B310	-	

2EH	Memory Read	x	0	0	1	0	1	1	1	0	2Eh	14.2.24
	1 st Parameter	x	x	x	x	x	x	x	x	x	-	
	2 nd Parameter	x	D17	D16	D15	D14	D13	D12	D11	D10	-	
	:	x	:	:	:	:	:	:	:	:	-	
	N th Parameter	x	Dn7	Dn6	Dn5	Dn4	Dn3	Dn2	Dn1	Dn0	-	
30H	Partial Area	x	0	0	1	1	0	0	0	0	30h	14.2.25
	1 st Parameter	x	PSL15	PSL14	PSL13	PSL12	PSL11	PSL10	PSL9	PSL8	-	
	2 nd Parameter	x	PSL7	PSL6	PSL5	PSL4	PSL3	PSL2	PSL1	PSL0	-	
	3 rd Parameter	x	PEL15	PEL14	PEL13	PEL12	PEL11	PEL10	PEL9	PEL8	-	
	4 th Parameter	x	PEL7	PEL6	PEL5	PEL4	PEL3	PEL2	PEL1	PEL0	-	
33H	Vertical Scrolling Definition	x	0	0	1	1	0	0	1	1	33h	14.2.26
	1 st Parameter	x	TFA15	TFA14	TFA13	TFA12	TFA11	TFA10	TFA9	TFA8	-	
	2 nd Parameter	x	TFA7	TFA6	TFA5	TFA4	TFA3	TFA2	TFA1	TFA0	-	
	3 rd Parameter	x	VSA15	VSA14	VSA13	VSA12	VSA11	VSA10	VSA9	VSA8	-	
	4 th Parameter	x	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0	-	
	5 th Parameter	x	BFA15	BFA14	BFA13	BFA12	BFA11	BFA10	BFA9	BFA8	-	
	6 th Parameter	x	BFA7	BFA6	BFA5	BFA4	BFA3	BFA2	BFA1	BFA0	-	
34H	Tearing Effect Line Off	x	0	0	1	1	0	1	0	0	34h	14.2.27
35H	Tearing Effect Line On	x	0	0	1	1	0	1	0	1	35h	14.2.28
	1 st Parameter	x	x	x	x	x	x	x	x	M	00h	
36H	Memory Access Control	x	0	0	1	1	0	1	1	0	36h	14.2.29
	1 st Parameter	x	MY	MX	MV	ML	RGB	MH	x	x	00h	
37H	Vertical Scrolling Start Address	x	0	0	1	1	0	1	1	1	37h	14.2.30
	1 st Parameter	x	SSA 15	SSA 14	SSA 13	SSA 12	SSA 11	SSA 10	SSA 9	SSA 8	00h	
	2 nd Parameter	x	SSA 7	SSA 6	SSA 5	SSA 4	SSA 3	SSA 2	SSA 1	SSA 0	00h	
38H	Idle Mode Off	x	0	0	1	1	1	0	0	0	38h	14.2.31
39H	Idle Mode On	x	0	0	1	1	1	0	0	1	39h	14.2.32
3AH	Interface Pixel Format	x	0	0	1	1	1	0	1	0	3Ah	14.2.33
	1 st Parameter	x	VIPF3	VIPF2	VIPF1	VIPF0	D3	IFPF2	IFPF1	IFPF0	66h	

B1H	Frame Rate Control (In normal mode/Full colors)		1	0	1	1	0	0	0	1	B1h	14.2.37
	1 st Parameter		x	x	x	DIVA4	DIVA3	DIVA2	DIVA1	DIVA0	x	
	2 nd Parameter		x	x	VPA5	VPA4	VPA3	VPA2	VPA1	VPA0	x	
B2H	Frame Rate Control (In Idle mode/8-colors)		1	0	1	1	0	0	1	0	B2h	14.2.38
	1 st Parameter		x	x	x	DIVB4	DIVB3	DIVB2	DIVB1	DIVB0	x	
	2 nd Parameter		x	x	VPB5	VPB4	VPB3	VPB2	VPB1	VPB0	x	
B3H	Frame Rate Control (In Partial mode/full colors)		1	0	1	1	0	0	1	1	B3h	14.2.39
	1 st Parameter		x	x	x	DIVC4	DIVC3	DIVC2	DIVC1	DIVC0	x	
	2 nd Parameter		x	x	VPC5	VPC4	VPC3	VPC2	VPC1	VPC0	x	
B4H	Display Inversion Control	x	1	0	1	1	0	1	0	0	B4h	14.2.40
	1 st Parameter	x	0	0	0	0	0	NLA	NLB	NLC	02H	
B5H	RGB Interface Blanking Porch setting	x	1	0	1	1	0	1	0	1	B5h	14.2.41
	1 st Parameter	x	x	x	HBP5	HBP4	HBP3	HBP2	HBP1	HBP0	08h	
	2 nd Parameter	x	VBP7	VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0	03h	
	3 rd Parameter	x	x	x	x	x	x	x	VBP9	VBP8	00h	
B6H	Display Function Set	x	1	0	1	1	0	1	1	0	B6h	14.2.41
	1 st Parameter		x	x	NO1	NO0	SDT1	SDT0	EQ1	EQ2	06h	
	2 nd Parameter		x	x	x	x	x	PTG0	PT1	PT0	02h	
B7H	Source Driver Direction Control	x	1	0	1	1	0	1	1	1	B7h	14.2.42
	1 st Parameter	x	0	0	0	0	0	0	0	CRL	00h	
B8H	Gate Driver Direction Control	x	1	0	1	1	1	0	0	0	B8h	14.2.43
	1 st Parameter	x	0	0	0	0	0	0	0	CTB	00h	
C0H	Power_Control1	x	1	1	0	0	0	0	0	0	C0h	14.2.44
	1 st Parameter	x	0	0	0	VRH4	VRH3	VRH2	VRH1	VRH0	x	
	2 nd Parameter	x	0	0	0	0	0	VC2	VC1	VC0	02h	
C1H	Power_Control2	x	1	1	0	0	0	0	0	1	C1h	14.2.45
	1 st Parameter	x	0	0	0	0	0	BT2	BT1	BT0	07h	

C2H	Power_Control3	x	1	1	0	0	0	0	1	0	C2h	14.2.46
	1 st Parameter	x	0	0	0	0	0	APA2	APA1	APA0	00h	
C3H	Power_Control4	x	1	1	0	0	0	0	1	1	C3h	14.2.47
	1 st Parameter	x	0	0	0	0	0	APB2	APB1	APB0	00h	
C4H	Power_Control 5	x	1	1	0	0	0	1	0	0	C4h	14.2.48
	1 st Parameter	x	0	0	0	0	0	APC2	APC1	APC1	01h	
C5H	VCOM_Control 1	x	1	1	0	0	0	1	0	1	C5h	14.2.49
	1 st Parameter	x	x	VMH 6	VMH 5	VMH 4	VMH 3	VMH 2	VMH 1	VMH 0	-	
	2 nd Parameter	x	0	VML6	VML5	VML4	VML3	VML2	VML1	VML0	-	
C6H	VCOM_Control 2	x	1	1	0	0	0	1	1	0	C6h	14.2.50
	1 st Parameter	x	0	0	VMA 5	VMA 4	VMA 3	VMA 2	VMA 1	VMA 0	13h /06 h	
C7H	VCOM Offset Control	x	1	1	0	0	0	1	1	1	C7h	14.2.51
	1 st Parameter	0	nVM*	VMF6	VMF5	VMF4	VMF3	VMF2	VMF1	VMF0	40h	
D3H	Write ID4 Value	x	1	1	0	1	0	0	1	1	D3h	14.2.52
	1 st Parameter	x	x	x	x	x	x	x	x	x	x	
	2 nd Parameter	x	ID417	ID416	ID415	ID414	ID413	ID412	ID411	ID410	91h	
	3 rd Parameter	x	ID427	ID426	ID425	ID424	ID423	ID422	ID421	ID420	63h	
	4 th Parameter	x	x	x	x	x	ID433	ID432	ID431	ID430	00h	
	5 th Parameter	x	x	x	x	x	x	x	x	x	x	
D5H	NV Memory Function Controller(1)	x	1	1	0	1	1	0	1	0	D5h	14.2.53
	1 st Parameter	x	ID33	ID32	ID31	ID30	ID23	ID22	ID21	ID20	00h	
	2 nd Parameter	x	OTP_BS	0	0	0	OTP_VMF3	OTP_VMF2	OTP_VMF1	OTP_VMF0	00h	
D6H	NV Memory Function Controller(2)	x	1	1	0	1	1	0	1	0	D6h	14.2.54
	1 st Parameter	x	OTP_D[7]	OTP_D[6]	OTP_D[5]	OTP_D[4]	OTP_D[3]	OTP_D[2]	OTP_D[1]	OTP_D[0]	00h	
	2 nd Parameter	x	0	0	0	0	0	0	OTP_TP[1]	OTP_TP[0]	00h	
D7H	NV Memory Function Controller(3)	x	1	1	0	1	1	0	1	0	D7h	14.2.55
	1 st Parameter	x	0	1	0	1	0	1	0	1	55h	
	2 nd Parameter	x	1	0	1	0	1	0	1	0	AAh	

	3 rd Parameter	x	0	1	1	0	0	1	1	0	66h	
DAH	Read ID1	x	1	1	0	1	1	0	1	0	DAh	14.2.34
	1 st Parameter	x	x	x	x	x	x	x	x	x	x	
	2 nd Parameter	x	1	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	54h
DBH	Read ID2	x	1	1	0	1	1	0	1	1	DBh	14.2.35
	1 st Parameter	x	x	x	x	x	x	x	x	x	x	
	2 nd Parameter	x	1	ID26	ID25	ID24	ID23	ID22	ID21	ID20	80h	
DCH	Read ID3	x	1	1	0	1	1	1	0	0	DCh	14.2.36
	1 st Parameter	x	x	x	x	x	x	x	x	x	x	
	2 nd Parameter	x	1	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	66h
E0H	Positive Gamma Correction Setting		1	1	1	0	0	0	0	0	E0h	14.2.57
	1 st Parameter		x	x							-	
	2 nd Parameter		x	x							-	
	3 rd Parameter		x	x							-	
	4 th Parameter		x	x							-	
	5 th Parameter		x	x							-	
	6 th Parameter		x	x	x						-	
	7 th Parameter		x								-	
	8 th Parameter				VP27[3:0]					VP36[3:0]	-	
	9 th Parameter		x							VP20[6:0]	-	
	10 th Parameter		x	x						VP13[5:0]	-	
	11 st Parameter		x	x						VP6[5:0]	-	
	12 nd Parameter		x	x						VP4[5:0]	-	
	13 rd Parameter		x	x						VP2[5:0]	-	
	14 th Parameter		x	x						VP1[5:0]	-	
	15 th Parameter		x	x						VP0[5:0]	-	
E1H	Negative Gamma Correction Setting		1	1	1	0	0	0	0	1	E1h	14.2.58
	1 st Parameter		x	x							-	
	2 nd Parameter		x	x							-	
	3 rd Parameter		x	x							-	
	4 th Parameter		x	x							-	
	5 th Parameter		x	x							-	
	6 th Parameter		x	x	x					VN13[4:0]	-	

	7 th Parameter	x	VN20[6:0]						-	
	8 th Parameter		VN36[3:0]			VN27[3:0]				-
	9 th Parameter	x	VN43[6:0]						-	
	10 th Parameter	x	X	VN50[5:0]						-
	11 st Parameter	x	x	VN57[5:0]						-
	12 nd Parameter	x	x	VN59[5:0]						-
	13 rd Parameter	x	x	VN61[5:0]						-
	14 th Parameter	x	x	VN62[5:0]						-
	15 th Parameter	x	x	VN63[5:0]						-
F2H	GAM_R_SEL	1	1	1	1	0	0	1	0	F2h
	1 st Parameter	x	x	x	x	x	x	x	GAM_R_SEL	Write

14.2.59

14.2 Command Description

14.2.1 NOP (00h)

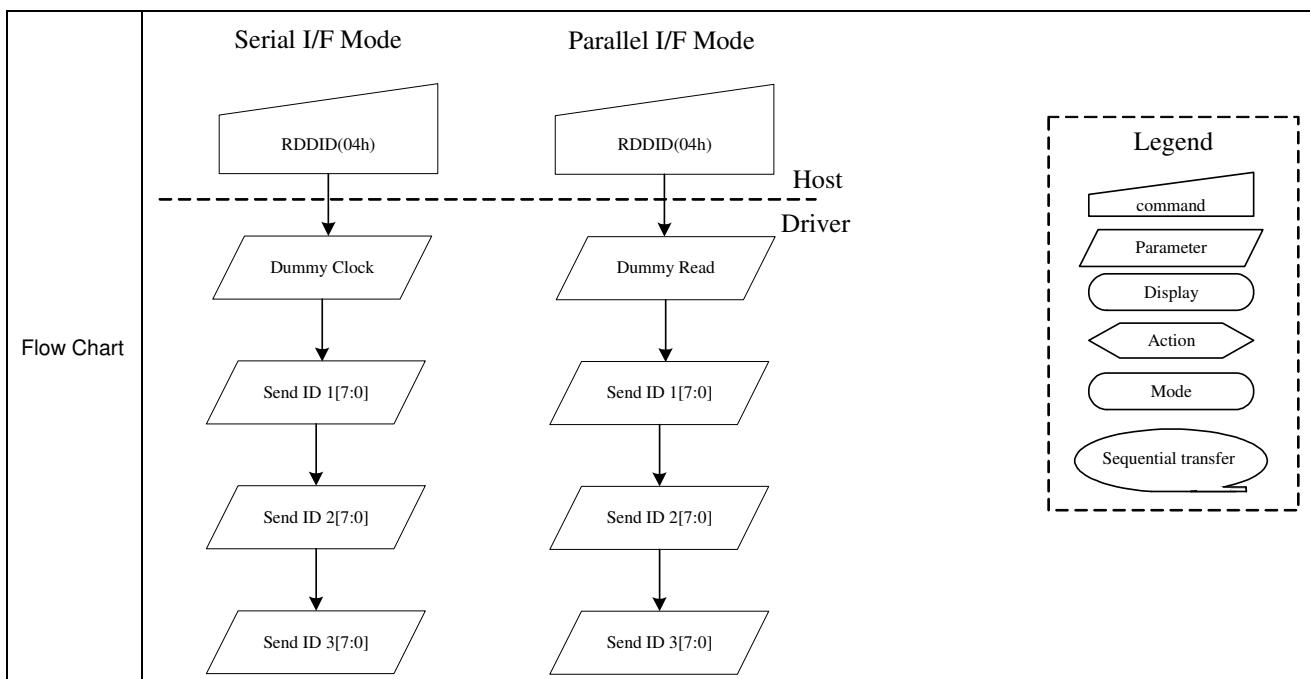
00H	NOP (No Operation)																							
	D/CX	RDX	WRX	D17-D8	D7	D6	D5	D4	D3	D2	D1	D0												
Command	0	1	↑	X	0	0	0	0	0	0	0	00												
Parameter	NO PARAMETER																							
Description	This command is an empty command; it does not have any effect on the display module. However it can be used to terminate Frame Memory Write or Read as described in RAMWR (Memory Write) and RAMRD (Memory Read) Commands. X = Don't care.																							
Restriction	None																							
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>												Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																							
Normal Mode On, Idle Mode Off, Sleep Out	Yes																							
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Sleep In	Yes																							
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>N/A</td> </tr> <tr> <td>SW Reset</td> <td>N/A</td> </tr> <tr> <td>HW Reset</td> <td>N/A</td> </tr> </tbody> </table>												Status	Default Value	Power On Sequence	N/A	SW Reset	N/A	HW Reset	N/A				
Status	Default Value																							
Power On Sequence	N/A																							
SW Reset	N/A																							
HW Reset	N/A																							
Flow Chart	None																							

14.2.2 Software Reset (01h)

01H	SWRESET (Software Reset)																								
	D/CX	RDX	WRX	D17-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	X	0	0	0	0	0	0	0	1	01												
Parameter	NO PARAMETER																								
Description	When the Software Reset command is written, it causes software reset. It resets the commands and parameters to their S/W Reset default values. (See default tables in each command description.) Note: The Frame Memory contents are affected by this command. X = Don't care																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
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Status	Default Value																								
Power On Sequence	N/A																								
SW Reset	N/A																								
HW Reset	N/A																								
Flow Chart	<pre> graph TD SW_RESET[SW RESET] --> DISPLAY[Display whole blank screen] DISPLAY --> SET_COMMANDS{Set Commands to S/W Default Value} SET_COMMANDS --> SLEEP[Sleep in Mode] </pre> <p>Legend</p> <ul style="list-style-type: none"> command Parameter Display Action Mode Sequential transfer 																								

14.2.3 Read Display Identification Information (04h)

04H		RDDIDIF (Read Display Identification Information)																															
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																				
Command	0	1	↑	x	0	0	0	0	0	1	0	0	04																				
1 st Parameter	1	↑	1	x	x	x	x	x	x	x	x	x	x																				
2 nd Parameter	1	↑	1	x	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	54h																				
3 rd Parameter	1	↑	1	x	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	80h																				
4 th Parameter	1	↑	1	x	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	66h																				
Description	This read byte returns 24-bit display identification information. The 1 st Parameter is dummy read. The 2 nd Parameter (ID17 to ID10): LCD module's manufacture ID. The 3 rd Parameter (ID27 to ID20): LCD module/driver version ID The 4 th Parameter (ID37 to ID30): LCD module/driver version ID Note: Commands RDID1/2/3(DAh, DBh, DCh) read data correspond to the parameters 2,3,4 of command 04h, respectively																																
Restriction	-																																
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>														Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes							
Status	Availability																																
Normal Mode On, Idle Mode Off, Sleep Out	Yes																																
Normal Mode On, Idle Mode On, Sleep Out	Yes																																
Partial Mode On, Idle Mode Off, Sleep Out	Yes																																
Partial Mode On, Idle Mode On, Sleep Out	Yes																																
Sleep In	Yes																																
Default	Note: ID1 can be option <table border="1"> <thead> <tr> <th rowspan="2">Status</th><th colspan="3">Default Value</th></tr> <tr> <th>ID1</th><th>ID2</th><th>ID3</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>54h</td><td>80h</td><td>66h</td></tr> <tr> <td>SW Reset</td><td>54h</td><td>80h</td><td>66h</td></tr> <tr> <td>HW Reset</td><td>54h</td><td>80h</td><td>66h</td></tr> </tbody> </table> modified by metal														Status	Default Value			ID1	ID2	ID3	Power On Sequence	54h	80h	66h	SW Reset	54h	80h	66h	HW Reset	54h	80h	66h
Status	Default Value																																
	ID1	ID2	ID3																														
Power On Sequence	54h	80h	66h																														
SW Reset	54h	80h	66h																														
HW Reset	54h	80h	66h																														



14.2.4 Read Display Status (09h)

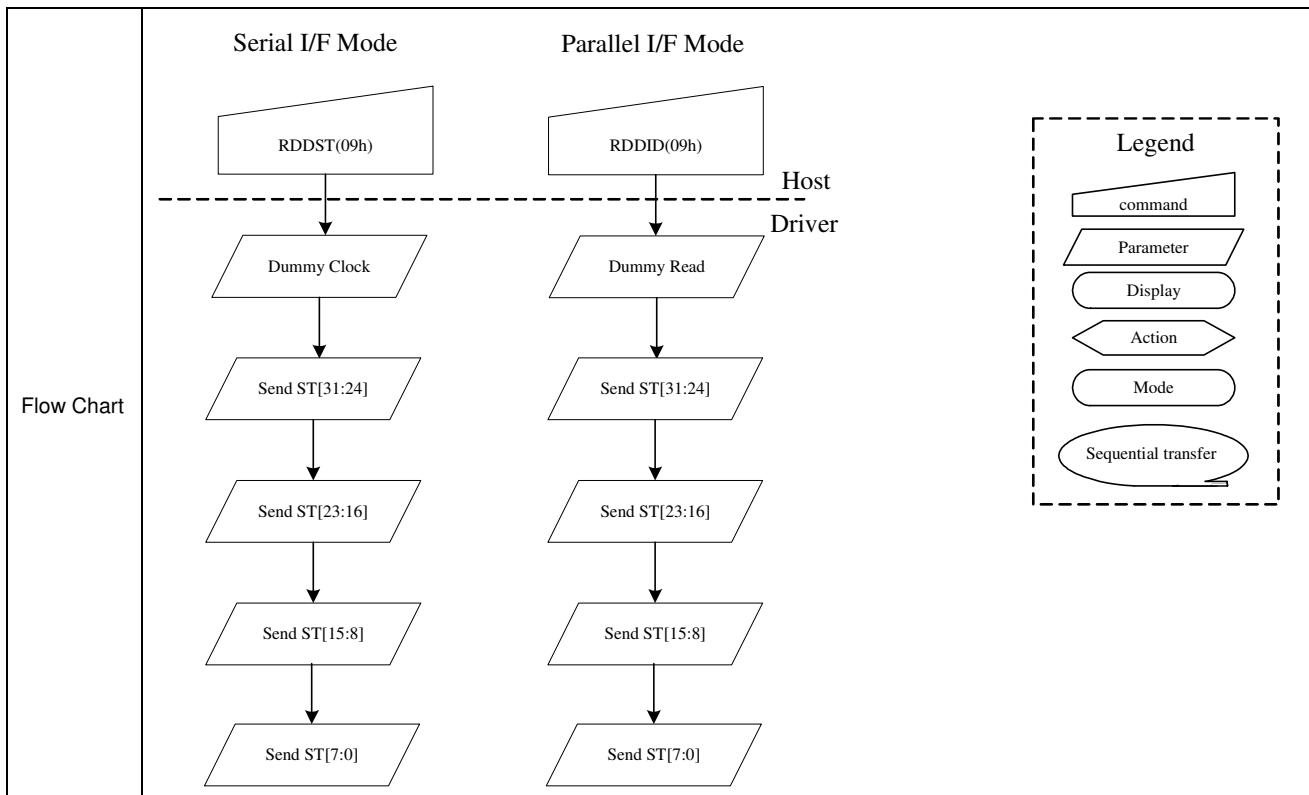
09H		RDDIDIF (Read Display Identification Information)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
Command	0	1	↑	x	0	0	0	0	1	0	0	1	09h	
1 st Parameter	1	↑	1	x	x	x	x	x	x	x	x	x	x	
2 nd Parameter	1	↑	1	x	BOTSON	MY	MX	MV	ML	RGB	MH	ST24	x	
3 rd Parameter	1	↑	1	x	ST23	IFPF2	IFPF1	IFPF0	IDMON	PTLON	SLOUT	NORON	x	
4 th Parameter	1	↑	1	x	VSSON	ST14	INVON	ST12	ST11	DISON	TEON	GCS2	x	
5 th Parameter	1	↑	1	x	GCS1	GCS0	TELOM	HSON	VSON	PCKON	DEON	ST0	x	
Description	This command indicates the current status of the display as described in the table below:													
	Bit	Description			Value									
	BSTON	Booster Voltage Status			“1”=Booster on, “0”=Booster off									
	MY	Row Address Order(MY)			“1”=Decrement, (Bottom to Top, when MADCTL(36h) D7='1') “0”=Increment, (Top to Bottom, when MADCTL(36h) D7='0')									
	MX	Column Address Order(MX)			“1”=Decrement, (Right to Left, when MADCTL(36h) D6='1') “0”=Increment, (Left to Right, when MADCTL(36h) D6='0')									
	MV	Row/Column Exchange(MV)			“1”=Row/column exchange, (when MADCTL (36h) D5='1') “0”=Normal (MV=0), (when MADCTL(36h)D5='0')									
	ML	Vertical refresh Order(ML)			“1”=Decrement, (LCD refresh Bottom to Top, when MADCTL(36h)D4='1') “0”=Increment, (LCD refresh Top to Bottom, when MADCTL(36h)D4='0')									
	RGB	RGB/BGR Order(RGB)			“1”=BGR,(When MADCTL(36h)D3='1') “0”=RGB,(When MADCTL(36h)D3='0')									
	MH	Horizontal refresh Order(MH)			“1”=Decrement, (LCD refresh Right to Left, when MADCTL(36h) D2='1') “0”=Increment, (LCD refresh Left to Right, when MADCTL(36h) D2='0')									
	ST24	Not Used												
	ST23	Not Used												
	IFPF2	Interface Color Pixel Format Definition			“011”=12-bit/pixel									
	IFPF1				“101”=16-bit/pixel									
	IFPF0				“110”=18-bit/pixel									
	IDMON	Idle Mode On/Off			“1”=On, “0”=Off									

	PTLON	Partial Mode On/Off	"1"=On,"0"=Off
	SLOUT	Sleep In/Out	"1"=On,"0"=Off
	NORON	Display Normal Mode On/Off	"1"=Normal Display, "0"=Normal Display Off
	VSSON	Vertical Scrolling Status	"1"=Scroll on,"0"=Scroll off
	ST14	Horizontal Scroll Status	"0"
	INVON	Inversion Status	"1"=On, "0"=Off
	ST12	All Pixels On(Not Used)	"0"
	ST11	All Pixels On(Not Used)	"0"
	DISON	Display On/Off	"1"=On, "0"=Off
	TEON	Tearing effect line on/off	"1"=On, "0"=Off
	GCS2	Gamma Curve Selection	"000"=GC0 "001"=GC1 "010"=GC2 "011"=GC3 "100" to "111" = Not defined
	GCS1		
	GCS		
	TELOM	Tearing effect line mode	"0"=mode1,"1"=mode2
	STO	For Future Use	"0"

Note: For Bits ST30 to ST28, also refer to Section 8-11

Register Availability	Status		Availability
	Normal Mode On, Idle Mode Off, Sleep Out		Yes
	Normal Mode On, Idle Mode On, Sleep Out		Yes
	Partial Mode On, Idle Mode Off, Sleep Out		Yes
	Partial Mode On, Idle Mode On, Sleep Out		Yes
	Sleep In		Yes

Default	Status	Default Value(ST31 to ST0)			
		ST[31-24]	ST[23-16]	ST[15-8]	ST[7-0]
	Power On Sequence	0000-0000	0110-0001	0000-0000	0000-0000
	SW Reset	0xxx-xxx0	0xxx-0001	0000-0000	0000-0000
	HW Reset	0000-0000	0110-0001	0000-0000	0000-0000



14.2.5 Read Display Power Mode (0Ah)

0AH		RDDPM (Read Display Power Mode)																																							
Inst / Para	D/C X	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																												
Command	0	1	↑	x	0	0	0	0	1	0	1	0	0Ah																												
1 st Parameter	1	↑	1	x	x	x	x	x	x	x	x	x	X																												
2 nd Parameter	1	↑	1	x	D7	D6	D5	D4	D3	D2	D1	D0	08h																												
Description	This command indicates the current status of the display as described in the table below: <table border="1"> <thead> <tr> <th>Bit</th><th>Description</th><th>Value</th></tr> </thead> <tbody> <tr> <td>D7</td><td>Booster Voltage Status</td><td>"1"=Booster on, "0"=Booster off</td></tr> <tr> <td>D6</td><td>Idle Mode On/Off</td><td>"1"=Idle Mode On, "0"=Idle Mode Off</td></tr> <tr> <td>D5</td><td>Partial Mode On/Off</td><td>"1"=Partial Mode on, "0"=Partial Mode Off</td></tr> <tr> <td>D4</td><td>Sleep In/Out</td><td>"1"=Sleep Out, "0"=Sleep In</td></tr> <tr> <td>D3</td><td>Display Normal Mode On/Off</td><td>"1"=Normal Display, "0"=Partial Display</td></tr> <tr> <td>D2</td><td>Display On/Off</td><td>"1"=Display On, "0"=Display Off</td></tr> <tr> <td>D1</td><td>Not Defined</td><td>Set to '0'</td></tr> <tr> <td>D0</td><td>Not Defined</td><td>Set to '0'</td></tr> </tbody> </table>														Bit	Description	Value	D7	Booster Voltage Status	"1"=Booster on, "0"=Booster off	D6	Idle Mode On/Off	"1"=Idle Mode On, "0"=Idle Mode Off	D5	Partial Mode On/Off	"1"=Partial Mode on, "0"=Partial Mode Off	D4	Sleep In/Out	"1"=Sleep Out, "0"=Sleep In	D3	Display Normal Mode On/Off	"1"=Normal Display, "0"=Partial Display	D2	Display On/Off	"1"=Display On, "0"=Display Off	D1	Not Defined	Set to '0'	D0	Not Defined	Set to '0'
Bit	Description	Value																																							
D7	Booster Voltage Status	"1"=Booster on, "0"=Booster off																																							
D6	Idle Mode On/Off	"1"=Idle Mode On, "0"=Idle Mode Off																																							
D5	Partial Mode On/Off	"1"=Partial Mode on, "0"=Partial Mode Off																																							
D4	Sleep In/Out	"1"=Sleep Out, "0"=Sleep In																																							
D3	Display Normal Mode On/Off	"1"=Normal Display, "0"=Partial Display																																							
D2	Display On/Off	"1"=Display On, "0"=Display Off																																							
D1	Not Defined	Set to '0'																																							
D0	Not Defined	Set to '0'																																							
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>														Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes															
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SW Reset	0000_1000(08h)																																								
HW Reset	0000_1000(08h)																																								
Flow Chart	<p>The flowchart illustrates the sequence of operations for RDDPM(0Ah) in both Serial I/F Mode and Parallel I/F Mode.</p> <ul style="list-style-type: none"> Serial I/F Mode: The process starts with the RDDPM(0Ah) command being sent from the host to the driver. This is followed by sending the data register value D[7:0]. Parallel I/F Mode: The process starts with the RDDPM(0Ah) command being sent from the host to the driver. This is followed by performing a dummy read operation, which then triggers the driver to send the data register value D [7:0]. <p>A legend on the right side defines the symbols used in the flowchart: <ul style="list-style-type: none"> command: A rectangle. Parameter: A rounded rectangle. Display: An oval. Action: A parallelogram. Mode: A rounded rectangle. Sequential transfer: A rounded rectangle with a diagonal line. </p>																																								

14.2.6 Read Display MADCTL (0Bh)

0BH	RDDMADCTL (Read Display MADCTL)																																								
	D/CX	RDX	WRX	D17-0	D7	D6	D5	D4	D3	D2	D1	D0	HEX																												
Command	0	1	↑	x	0	0	0	0	1	0	1	1	0Bh																												
1 st Parameter	1	↑	1	x	x	x	x	x	x	x	x	x	x																												
2 nd Parameter	1	↑	1	x	D7	D6	D5	D4	D3	D2	D1	D0	00h																												
Description	This command indicates the current status of the display as described in the table below:																																								
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Bit	Description	Value																																							
D7	Page Address Order	"1"=Decrement, "0"=Increment																																							
D6	Column Address Order	"1"=Decrement, "0"=Increment																																							
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D1	Switching between Segment outputs and RAM	Set to '0'																																							
D0	Switching between Common outputs and RAM	Set to '0'																																							
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>														Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes															
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Power On Sequence	0000_0000(00h)																																								
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Flow Chart	<pre> graph TD subgraph "Serial I/F Mode" S1[RDDMADCTR(0Bh)] --> S2[/Send D[7:0]/] end subgraph "Parallel I/F Mode" P1[RDDMADCTR(0Bh)] --> P2[/Dummy Read/] P2 --> P3[/Send D [7:0]/] end subgraph Legend direction TB L1[command] --- L2[Parameter] --- L3[Display] --- L4[Action] --- L5[Mode] --- L6[Sequential transfer] end </pre> <p>The flowchart illustrates two modes of operation for the RDDMADCTR(0Bh) command. In Serial I/F Mode, the command is sent directly to the driver, followed by the data (D[7:0]). In Parallel I/F Mode, the command is sent to the driver, which then performs a dummy read before sending the data (D [7:0]). A legend on the right defines the symbols: a rectangle for command, a parallelogram for parameter, an oval for display, a rounded rectangle for action, a horizontal bar for mode, and an ellipse for sequential transfer.</p>																																								

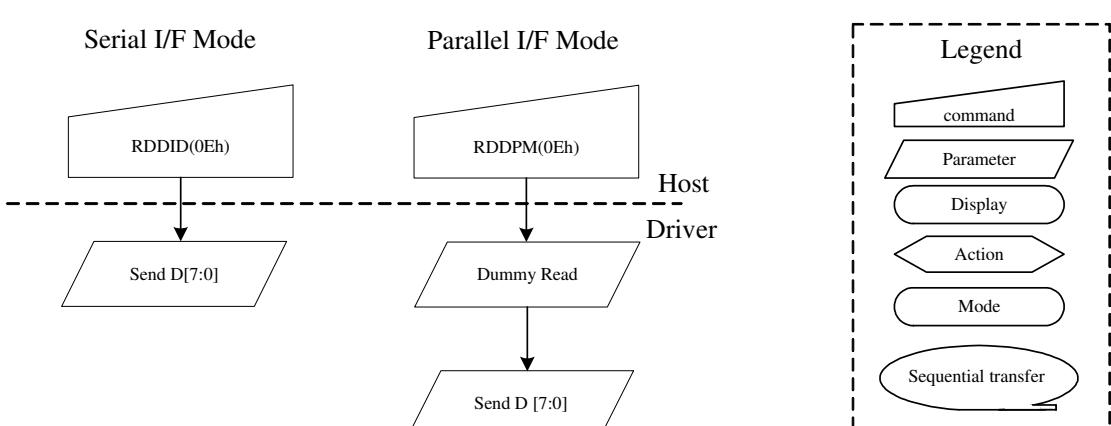
14.2.7 Read Display Pixel Format (0Ch)

0CH		RDDCOLMOD (Read Display COLMOD)																																																				
	D/C X	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																									
Command	0	1	↑	x	0	0	0	0	1	1	0	0	0Ch																																									
1 st Parameter	1	↑	1	x	x	x	x	x	x	x	x	x	x																																									
2 nd Parameter	1	↑	1	x	VIPF3	VIPF2	VIPF1	VIPF0	D3	IFPF2	IFPF1	IFPF0	66h																																									
Description	This command indicates the current status of the display as described in the table below: <table border="1"> <thead> <tr> <th>Bit</th> <th colspan="3">Description</th> <th>Value</th> </tr> </thead> <tbody> <tr> <td>D7</td> <td>VIPF3</td> <td rowspan="4">RGB Interface Color Format</td> <td rowspan="5"></td> <td>0101 = 16 bit/pixel (1 time data transfer)</td> </tr> <tr> <td>D6</td> <td>VIPF2</td> <td>0110 = 18 bit/pixel (1 time data transfer)</td> </tr> <tr> <td>D5</td> <td>VIPF1</td> <td>1110 = 18 bit/pixel (3 times data transfer)</td> </tr> <tr> <td>D4</td> <td>VIPF0</td> <td>The other = not defined</td> </tr> <tr> <td>D3</td> <td>D3</td> <td colspan="2"></td> <td>"0" (Not used)</td> </tr> <tr> <td>D2</td> <td>IFPF2</td> <td rowspan="3">Control Interface Color Format</td> <td rowspan="5"></td> <td>"011"=12 bit/pixel</td> </tr> <tr> <td>D1</td> <td>IFPF 1</td> <td>"101"=16 bit/pixel</td> </tr> <tr> <td>D0</td> <td>IFPF 0</td> <td>"110"=18 bit/pixel</td> </tr> <tr> <td></td> <td></td> <td colspan="2" rowspan="2"></td> <td>The others = not defined</td> </tr> </tbody> </table>														Bit	Description			Value	D7	VIPF3	RGB Interface Color Format		0101 = 16 bit/pixel (1 time data transfer)	D6	VIPF2	0110 = 18 bit/pixel (1 time data transfer)	D5	VIPF1	1110 = 18 bit/pixel (3 times data transfer)	D4	VIPF0	The other = not defined	D3	D3			"0" (Not used)	D2	IFPF2	Control Interface Color Format		"011"=12 bit/pixel	D1	IFPF 1	"101"=16 bit/pixel	D0	IFPF 0	"110"=18 bit/pixel					The others = not defined
Bit	Description			Value																																																		
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D4	VIPF0			The other = not defined																																																		
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D0	IFPF 0			"110"=18 bit/pixel																																																		
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Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>														Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes																												
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Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>0110_0110(18bit/pixel)</td> </tr> <tr> <td>SW Reset</td> <td>No Change</td> </tr> <tr> <td>HW Reset</td> <td>0110_0110(18bit/pixel)</td> </tr> </tbody> </table>														Status	Default Value	Power On Sequence	0110_0110(18bit/pixel)	SW Reset	No Change	HW Reset	0110_0110(18bit/pixel)																																
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Power On Sequence	0110_0110(18bit/pixel)																																																					
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Flow Chart	<p>Serial I/F Mode: RDDCOLMOD(0Eh) → Send D[7:0]</p> <p>Parallel I/F Mode: RDDCOLMOD(0Eh) → Dummy Read → Send D [7:0]</p> <p>Legend:</p> <ul style="list-style-type: none"> command Parameter Display Action Mode Sequential transfer 																																																					

14.2.8 Read Display Image Mode (0Dh)

0DH		RDDIM (Read Display Image Mode)																									
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX														
Command	0	1	↑	x	0	0	0	0	1	1	0	1	0Dh														
1 st Parameter	1	↑	1	x	x	x	x	x	x	x	x	x	x														
2 nd Parameter	1	↑	1	x	D7	D6	D5	D4	D3	D2	D1	D0	00h														
Description	Bit	Description			Value																						
	D7	Vertical Scrolling On/Off			“1”=Vertical scrolling is On, “0”=Vertical scrolling is Off																						
	D6	Horizontal Scrolling On/Off			“0”(Not used)																						
	D5	Inversion On/Off			“1”=Inversion is On, “0”=Inversion is Off																						
	D4	All Pixels On			“0” (Not used)																						
	D3	All Pixel Off			“0” (Not used)																						
	D2	Gamma Curve Selection			“000”=GC0; “001”=GC1; “010”=GC2; “011”=GC3																						
	D1				“100” to “111” = Not defined																						
Register Availability																											
Default																											
Flow Chart	Serial I/F Mode							Parallel I/F Mode																			
Legend																											

14.2.9 Read Display Signal Mode (0Eh)

0EH		RDDSM (Read Display Signal Mode)																																							
Command		D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																											
1 st Parameter	0	1	↑	x	0	0	0	0	1	1	1	1	0	0Eh																											
2 nd Parameter	1	↑	1	x	x	x	x	x	x	x	x	x	x	x																											
Description	This command indicates the current status of the display as described in the table below:																																								
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Partial Mode On, Idle Mode On, Sleep Out	0000_0000(00h)																																								
Sleep In	0000_0000(00h)																																								
Flow Chart	 <pre> graph TD RDDID[RDDID(0Eh)] --> SD[Send D[7:0]] RDDPM[RDDPM(0Eh)] --> DR[Dummy Read] DR --> SD subgraph Legend [Legend] direction TB L1[command] L2[Parameter] L3[Display] L4[Action] L5[Mode] L6[Sequential transfer] end </pre>																																								

14.2.10 Read Display Signal Mode (0Fh)

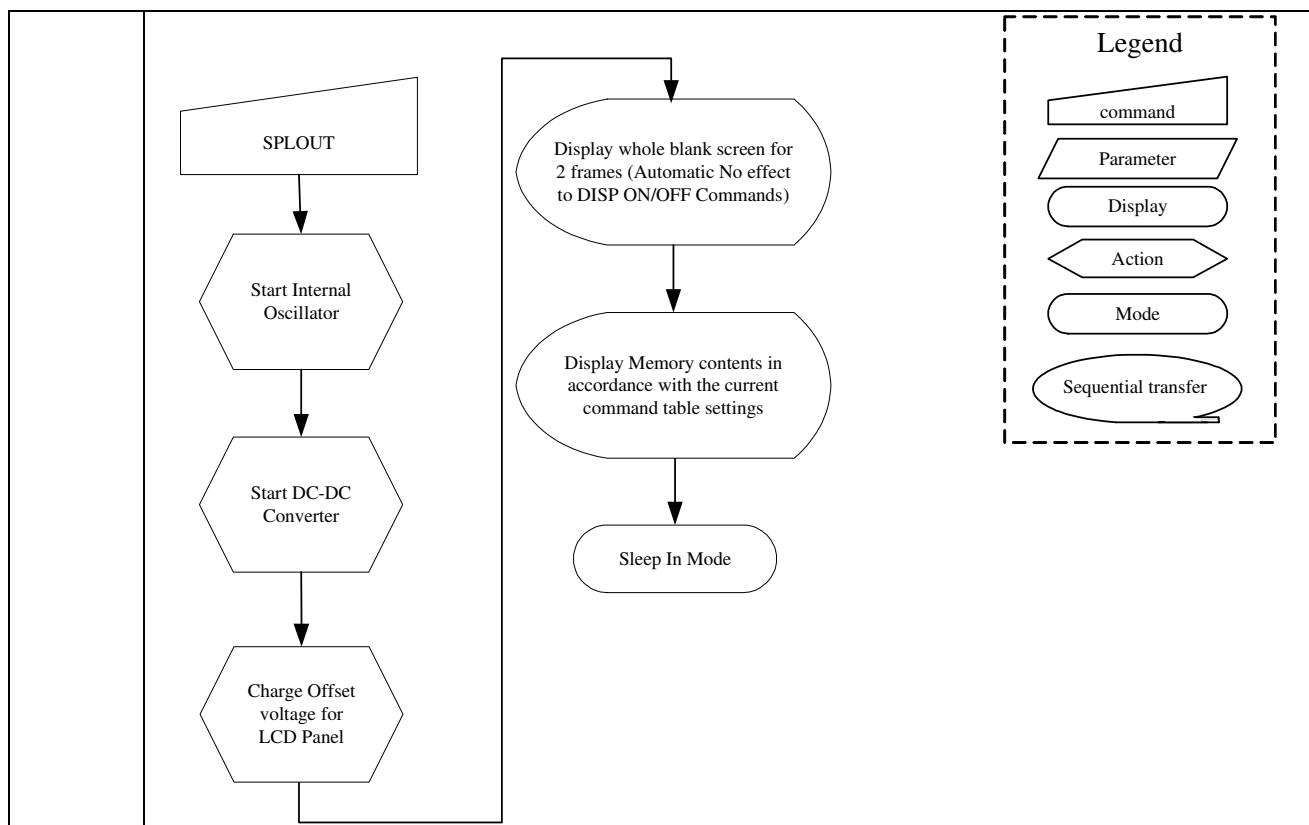
0EH		RDDSM (Read Display Signal Mode)																																							
	D/C X	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																												
Command	0	1	↑	x	0	0	0	0	1	1	1	1	0Fh																												
1 st Parameter	1	↑	1	x	x	x	x	x	x	x	x	x	x																												
2 nd Parameter	1	↑	1	x	D7	D6	D5	D4	D3	D2	D1	D0	00h																												
Description	This command indicates the current status of the display as described in the table below: <table border="1"> <thead> <tr> <th>Bit</th><th>Description</th><th>Value</th></tr> </thead> <tbody> <tr> <td>D7</td><td>Register Loading Detection</td><td></td></tr> <tr> <td>D6</td><td>Functionality Detection</td><td></td></tr> <tr> <td>D5</td><td>Not Used</td><td>"0"</td></tr> <tr> <td>D4</td><td>Not Used</td><td>"0"</td></tr> <tr> <td>D3</td><td>Not Used</td><td>"0"</td></tr> <tr> <td>D2</td><td>Not Used</td><td>"0"</td></tr> <tr> <td>D1</td><td>Not Used</td><td>"0"</td></tr> <tr> <td>D0</td><td>Not Used</td><td>"0"</td></tr> </tbody> </table>														Bit	Description	Value	D7	Register Loading Detection		D6	Functionality Detection		D5	Not Used	"0"	D4	Not Used	"0"	D3	Not Used	"0"	D2	Not Used	"0"	D1	Not Used	"0"	D0	Not Used	"0"
Bit	Description	Value																																							
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Power On Sequence	0000_0000(00h)																																								
SW Reset	0000_0000(00h)																																								
Flow Chart	<p>Legend:</p> <ul style="list-style-type: none"> command Parameter Display Action Mode Sequential transfer 																																								

14.2.11 Sleep In (10h)

SLPIN (Sleep In)																										
10H	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX													
Command	0	1	↑	x	0	0	0	1	0	0	0	0	10h													
Parameter	No Parameter																									
Description	<p>This command causes the LCD module to enter the minimum power consumption mode.</p> <p>In this mode e.g. the DC/DC converter is stopped, Internal oscillator is stopped, and panel scanning is stopped.</p> <p>MCU interface and memory are still working and the memory keeps its contents.</p>																									
Restriction	<p>This command has no effect when module is already in sleep in mode. Sleep In Mode can only be left by the Sleep Out Command (11h). It will be necessary to wait 5msec before sending next command; this is to allow time for the supply voltages and clock circuits to stabilize. It will be necessary to wait 120msec after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.</p>																									
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>														Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																									
Normal Mode On, Idle Mode Off, Sleep Out	Yes																									
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Status	Default Value																									
Power On Sequence	Sleep In Mode																									
SW Reset	Sleep In Mode																									
Flow Chart	<p>It takes 120msec to get into Sleep In mode after SLPIN command issued.</p> <pre> graph TD SLPIN[SLPIN] --> Display[Display whole blank screen automatic NO effect to DISP ON/OFF command] Display --> Drain[Drain charge from LCD panel] Drain --> StopDC[Stop DC/DC Converter] StopDC --> StopIO[Stop Internal Oscillator] StopIO --> SleepInMode[Sleep In Mode] </pre> <p>Legend:</p> <ul style="list-style-type: none"> command Parameter Display Action Mode Sequential transfer 																									

14.2.12 Sleep Out (11h)

SLPOUT (Sleep Out)																										
11H	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX													
Command	0	1	↑	x	0	0	0	1	0	0	0	1	11h													
Parameter	No Parameter																									
Description	This command turns off sleep mode. In this mode e.g. the DC/DC converter is enabled, Internal oscillator is started, and panel scanning is started.																									
Restriction	This command has no effect when module is already in sleep out mode. Sleep Out Mode can only be left by the Sleep In Command (10h). It will be necessary to wait 5 msec before sending next command; this is to allow time for the clock circuits to stabilize. The display module loads all display supplier's factory default values to the registers during this 120 msec and there cannot be any abnormal visual effect on the display image if factory default and register values are same when this load is done and when the display module is already Sleep Out –mode. The display module is doing self-diagnostic functions during this 5msec. It will be necessary to wait 120msec after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent. This command has no effect when module is already in sleep out mode. Sleep Out Mode can only be left by HW Reset, Software Reset (01h), Sleep In (10h), or a NMI event trigger.																									
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>														Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Sleep In	Yes																									
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Sleep In Mode</td> </tr> <tr> <td>SW Reset</td> <td>Sleep In Mode</td> </tr> <tr> <td>HW Reset</td> <td>Sleep In Mode</td> </tr> </tbody> </table>														Status	Default Value	Power On Sequence	Sleep In Mode	SW Reset	Sleep In Mode	HW Reset	Sleep In Mode				
Status	Default Value																									
Power On Sequence	Sleep In Mode																									
SW Reset	Sleep In Mode																									
HW Reset	Sleep In Mode																									
Flow Chart	It takes 120msec to become Sleep Out mode after SLPOUT command issued.																									



14.2.13 Partial Mode On (12h)

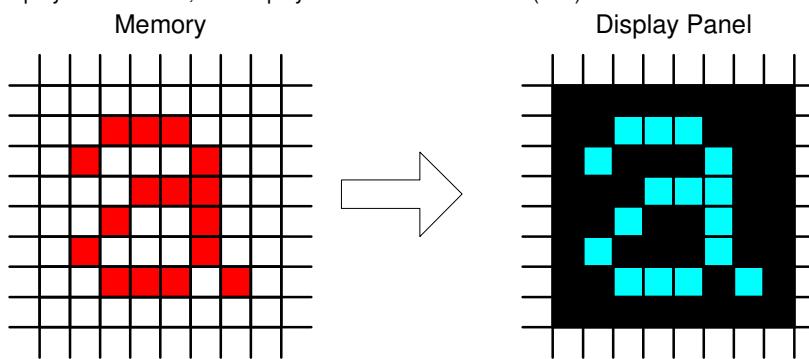
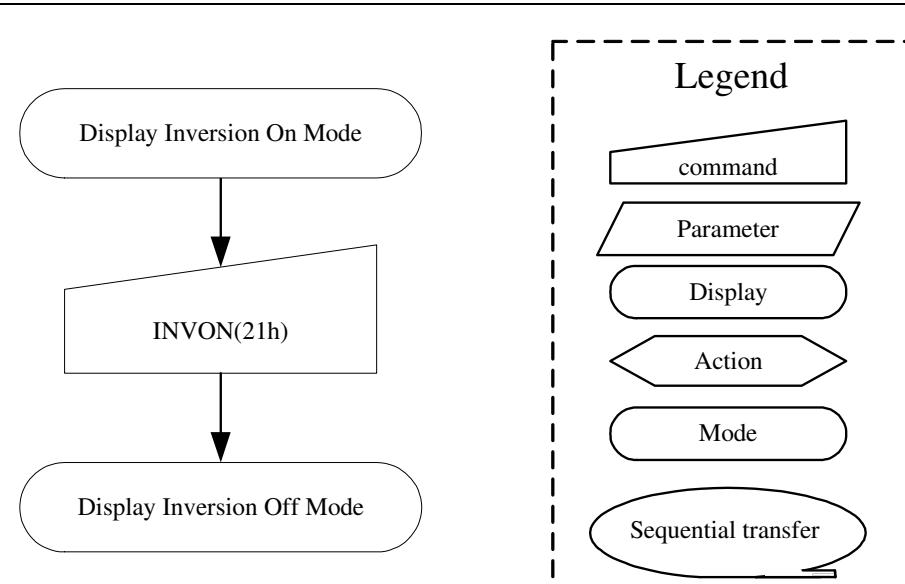
12H	PTLON (Partial Mode On)																								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	x	0	0	0	1	0	0	1	0	12h												
Parameter	No Parameter																								
Description	This command turns on partial mode. The partial mode is described by the Partial Area command (30h). To leave Partial mode, the Normal Display On command (13h) should be written. X = Don't care Note: If a command is written in a frame cycle, the command becomes effective from the next frame.																								
Restriction	This command has no effect during Partial mode is active.																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
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Status	Default Value																								
Power On Sequence	Normal Display Mode On																								
SW Reset	Normal Display Mode On																								
HW Reset	Normal Display Mode On																								
Flow Chart	See Partial Area (30h)																								

14.2.14 Normal Display Mode On (13h)

13H		PTLON (Partial Mode On)																							
		D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX											
Command		0	1	↑	x	0	0	0	1	0	0	1	1	13h											
Parameter	No Parameter																								
Description	<p>This command returns the display to normal mode.</p> <p>Normal display mode on means Partial mode off and Scroll mode Off.</p> <p>Exit from NORON by the Partial mode On command(12h)</p> <p>X = Don't care</p> <p>Note: If a command is written in a frame cycle, the command becomes effective from the next frame.</p>																								
Restriction	This command has no effect when Normal Display mode is active.																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Status	Default Value																								
Power On Sequence	Normal Display Mode On																								
SW Reset	Normal Display Mode On																								
HW Reset	Normal Display Mode On																								
Flow Chart	See Partial Area and Vertical Scrolling Definition Descriptions for details of when to use this command.																								

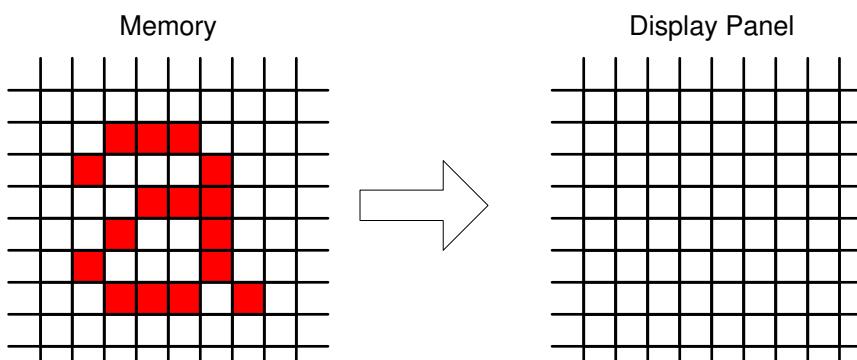
14.2.15 Display Inversion Off (20h)

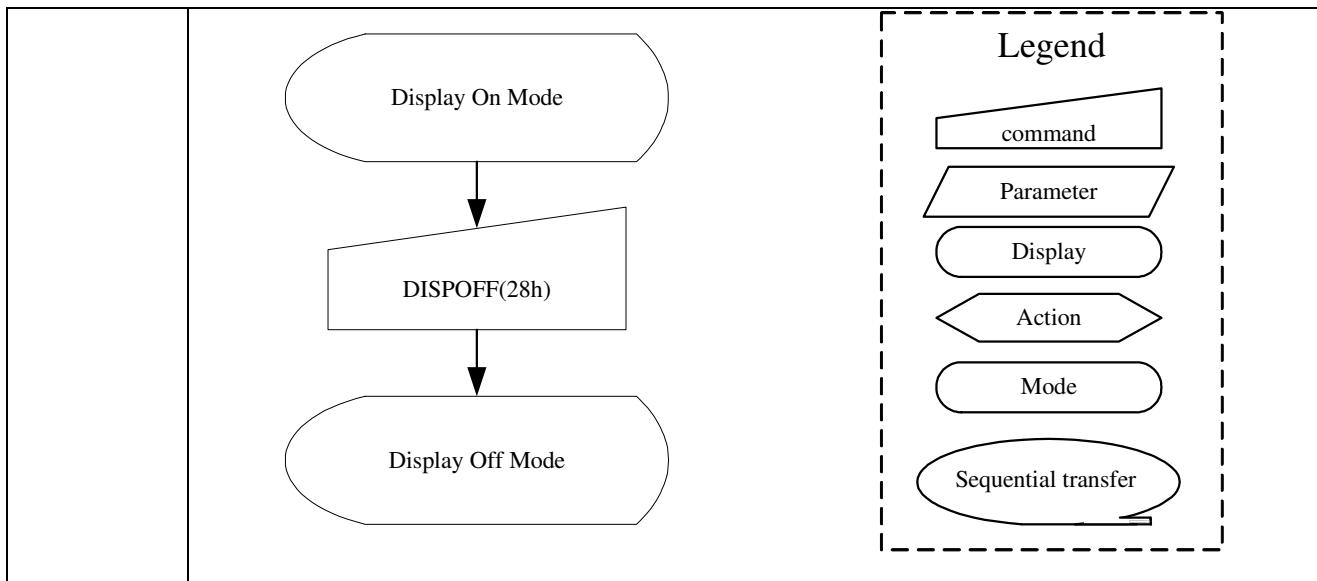
14.2.16 Display Inversion On (21h)

21H		PTLON (Partial Mode On)																							
Command	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Parameter	No Parameter																								
Description	<p>This command is used to enter into display inversion mode. This command makes no change of contents of frame memory. Every bit is inverted from the frame memory to the display. This command does not change any other status. To exit from Display inversion On, the Display Inversion Off command(20h) should be written.</p>  <p>Memory</p> <p>Display Panel</p> <p>X = don't care</p>																								
Restriction	This command has no effect when module is already in inversion on mode.																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Normal Display Mode Off</td> </tr> <tr> <td>SW Reset</td> <td>Normal Display Mode Off</td> </tr> <tr> <td>HW Reset</td> <td>Normal Display Mode Off</td> </tr> </tbody> </table>													Status	Default Value	Power On Sequence	Normal Display Mode Off	SW Reset	Normal Display Mode Off	HW Reset	Normal Display Mode Off				
Status	Default Value																								
Power On Sequence	Normal Display Mode Off																								
SW Reset	Normal Display Mode Off																								
HW Reset	Normal Display Mode Off																								
Flow Chart	 <p>Display Inversion On Mode</p> <p>INVON(21h)</p> <p>Display Inversion Off Mode</p> <p>Legend</p> <ul style="list-style-type: none"> command Parameter Display Action Mode Sequential transfer 																								

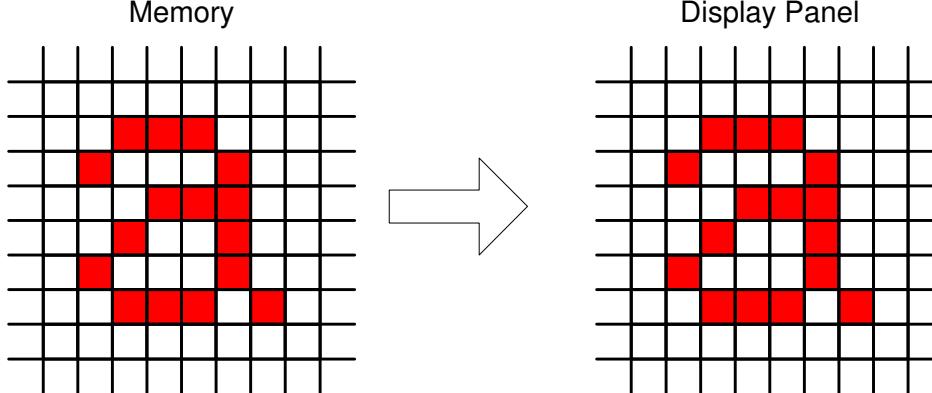
14.2.17 Gamma Set (26h)

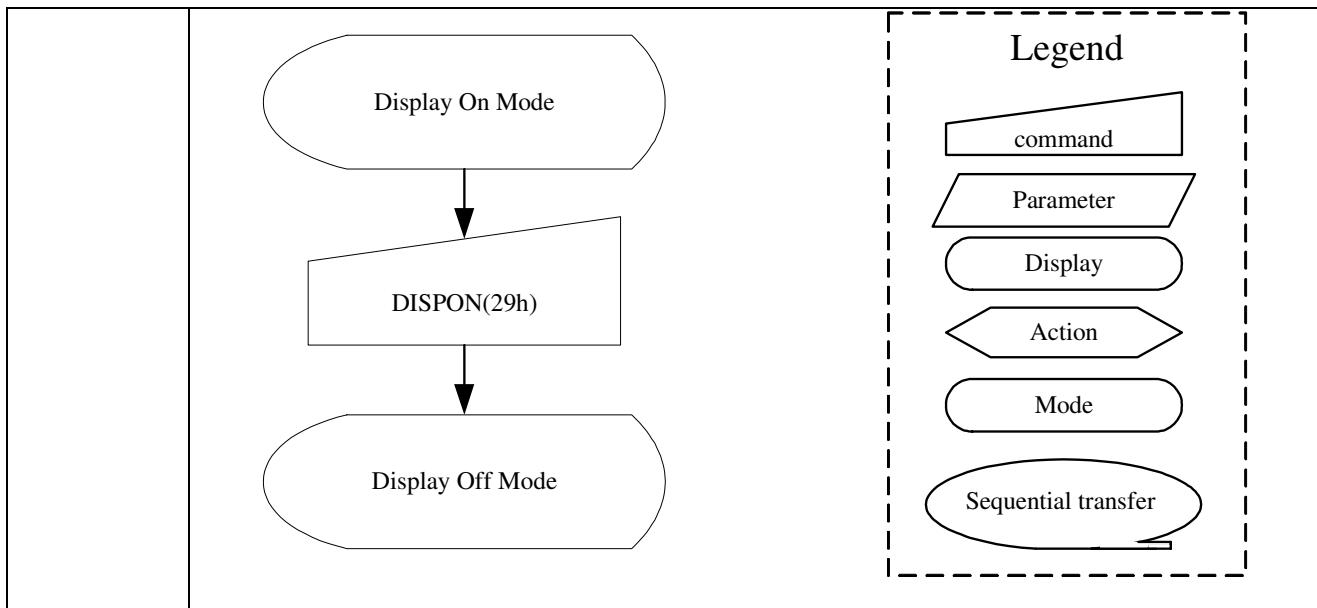
14.2.18 Display Off (28h)

28H		DISPOFF (Display Off)																										
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX															
Command	0	1	↑	x	0	0	1	0	1	0	0	0	28h															
Parameter	No Parameter																											
Description	This command is used to enter into DISPLAY OFF mode. In this mode, the output from Frame Memory is disabled and blank page inserted. This command makes no change of contents of frame memory. This command does not change any other status. There will be no abnormal visible effect on the display. Exit from this command by Display On(29h)																											
Memory  Display Panel																												
X = don't care																												
Restriction	This command has no effect when module is already in display off mode.																											
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse; text-align: center;"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>														Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes		
Status	Availability																											
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Normal Mode On, Idle Mode On, Sleep Out	Yes																											
Partial Mode On, Idle Mode Off, Sleep Out	Yes																											
Partial Mode On, Idle Mode On, Sleep Out	Yes																											
Sleep In	Yes																											
Default	<table border="1" style="width: 100%; border-collapse: collapse; text-align: center;"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Display Off</td> </tr> <tr> <td>SW Reset</td> <td>Display Off</td> </tr> <tr> <td>HW Reset</td> <td>Display Off</td> </tr> </tbody> </table>														Status	Default Value	Power On Sequence	Display Off	SW Reset	Display Off	HW Reset	Display Off						
Status	Default Value																											
Power On Sequence	Display Off																											
SW Reset	Display Off																											
HW Reset	Display Off																											
Flow Chart																												

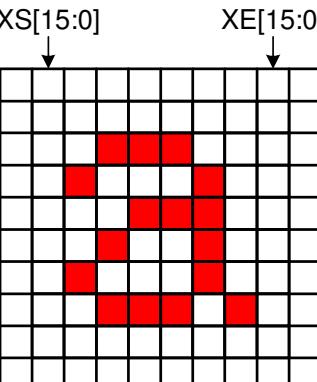


14.2.19 Display On (29h)

29H		DISPON (Display On)																									
		D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX													
Command		0	1	↑	x	0	0	1	0	1	0	0	1	29h													
Parameter	No Parameter																										
Description	<p>This command is used to recover from DISPLAY OFF mode. Output from the Frame Memory is enabled.</p> <p>This command makes no change of contents of frame memory.</p> <p>This command does not change any other status.</p>  <p>X = don't care</p>																										
Restriction	This command has no effect when module is already in display on mode.																										
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>														Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes	
Status	Availability																										
Normal Mode On, Idle Mode Off, Sleep Out	Yes																										
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Status	Default Value																										
Power On Sequence	Display Off																										
SW Reset	Display Off																										
HW Reset	Display Off																										
Flow Chart																											



14.2.20 Column Address Set (2Ah)

2AH		CASET (Column Address Set)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
Command	0	1	↑	x	0	0	1	0	1	0	1	0	2Ah	
1 st Parameter	1	1	↑	x	XS15	XS14	XS13	XS12	XS11	XS10	XS9	XS8	-	
2 nd Parameter	1	1	↑	x	XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0	-	
3 rd Parameter	1	1	↑	x	XE15	XE14	XE13	XE12	XE11	XE10	XE9	XE8	-	
4 th Parameter	1	1	↑	x	XE7	XE6	XE5	XE4	XE3	XE2	XE1	XE0	-	
Description	This command is used to define area of frame memory where MCU can access. This command makes no change on the other driver status. The values of XS[15:0] and XE[15:0] are referred when RAMWR command comes. Each value represents one column line in the Frame Memory.													
	 X = don't care													
Restriction	XS [15:0] always must be equal to or less than XE[15:0]. When XS[15:0] or XE[15:0] is greater than maximum address like below, data of out of range will be ignored. <ol style="list-style-type: none"> 132X132 memory base (GM='101') <p>(Parameter range: $0 \leq XS[15:0] \leq XE[15:0] \leq 131(0083h):MV="0"$) (Parameter range: $0 \leq XS[15:0] \leq XE[15:0] \leq 131(0083h):MV="1"$)</p> 130X130 memory base (GM='100') <p>(Parameter range: $0 \leq XS[15:0] \leq XE[15:0] \leq 129(0081h):MV="0"$) (Parameter range: $0 \leq XS[15:0] \leq XE[15:0] \leq 129(0081h):MV="1"$)</p> 128X160 memory base (GM='011') <p>(Parameter range: $0 \leq XS[15:0] \leq XE[15:0] \leq 127(007Fh):MV="0"$) (Parameter range: $0 \leq XS[15:0] \leq XE[15:0] \leq 159(009Fh):MV="1"$)</p> 120X160 memory base (GM='010') <p>(Parameter range: $0 \leq XS[15:0] \leq XE[15:0] \leq 119(0077h):MV="0"$) (Parameter range: $0 \leq XS[15:0] \leq XE[15:0] \leq 159(009Fh):MV="1"$)</p> 128X128 memory base (GM='001') <p>(Parameter range: $0 \leq XS[15:0] \leq XE[15:0] \leq 127(007Fh):MV="0"$) (Parameter range: $0 \leq XS[15:0] \leq XE[15:0] \leq 127(007Fh):MV="1"$)</p> 132X162 memory base (GM='000') <p>(Parameter range: $0 \leq XS[15:0] \leq XE[15:0] \leq 131(0083h):MV="0"$)</p> 													

	(Parameter range: $0 \leq XS[15:0] \leq XE[15:0] \leq 127(00A1h)$:MV="1") X = Don't care												
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												

1. 132 x 132 memory base(GM='101')

Status	Default Value		
	XS[15:0]	XE[15:0]	EX[15:0] (MV=1)
Power On Sequence	0000h	0083h(131)	
S/W Reset	0000h	0083h(131)	0083h(131)
HW Reset	0000h	0083h(131)	

Status	Default Value		
	XS[15:0]	XE[15:0]	EX[15:0] (MV=1)
Power On Sequence	0000h	0081h(129)	
S/W Reset	0000h	0081h(129)	0081h(129)
HW Reset	0000h	0081h(129)	

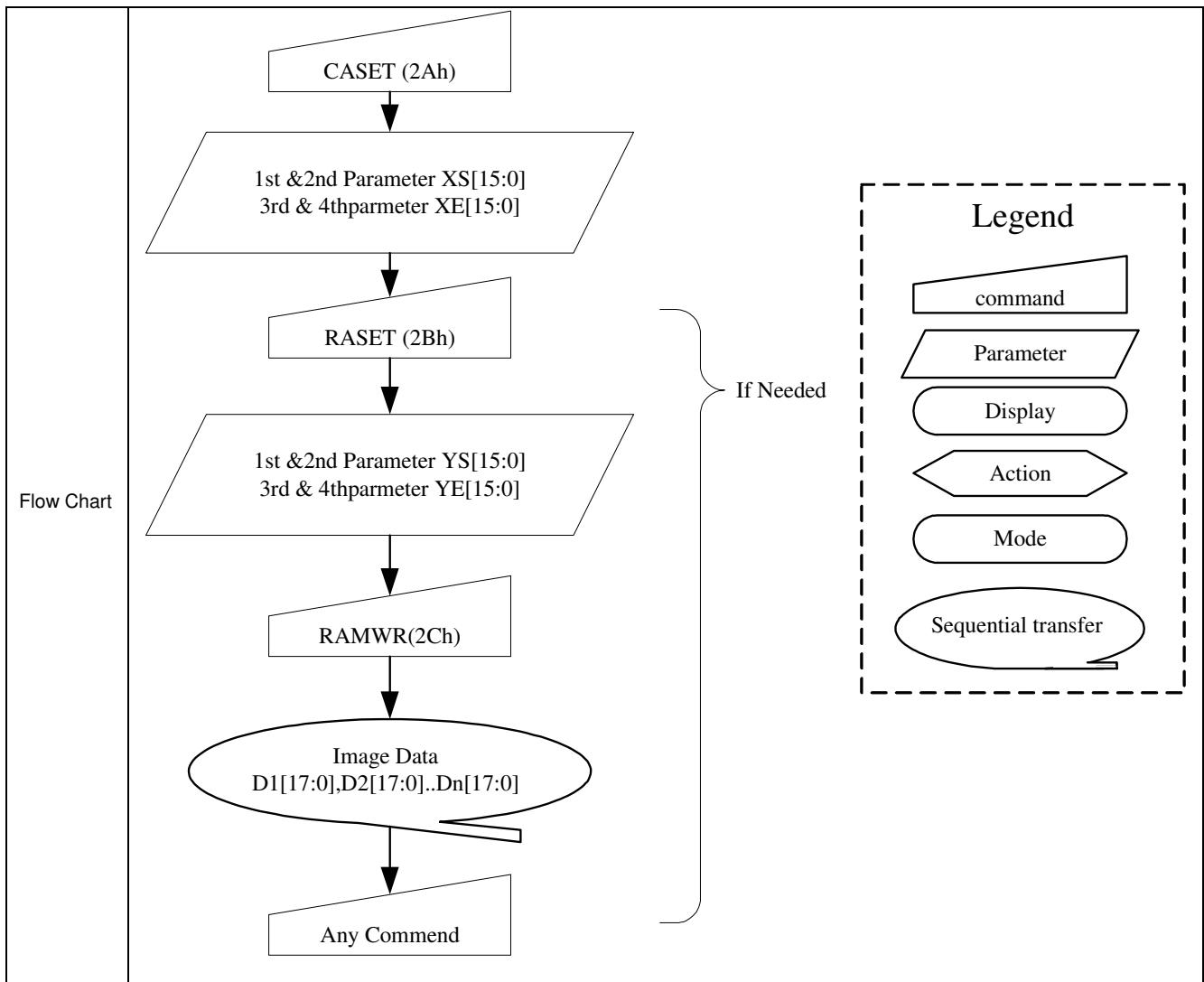
Status	Default Value		
	XS[15:0]	XE[15:0]	EX[15:0] (MV=1)
Power On Sequence	0000h	007Fh(127)	
S/W Reset	0000h	007Fh(127)	009Fh(159)
HW Reset	0000h	007Fh(127)	

Status	Default Value		
	XS[15:0]	XE[15:0]	EX[15:0] (MV=1)
Power On Sequence	0000h	0077h(119)	
S/W Reset	0000h	0077h(119)	009Fh(159)
HW Reset	0000h	0077h(119)	

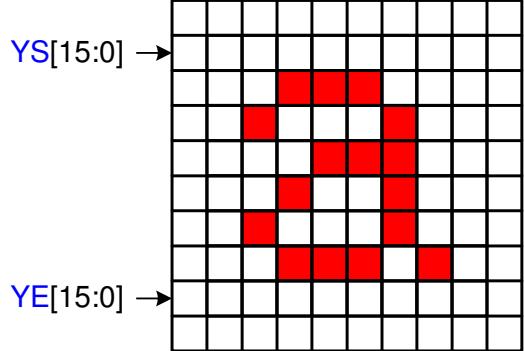
Status	Default Value		
	XS[15:0]	XE[15:0]	EX[15:0] (MV=1)
Power On Sequence	0000h	007Fh(127)	
S/W Reset	0000h	007Fh(127)	009Fh(127)
HW Reset	0000h	0077h(119)	

Status	Default Value		
	XS[15:0]	XE[15:0]	EX[15:0] (MV=1)
Power On Sequence	0000h	0083h(131)	
S/W Reset	0000h	0083h(131)	00A1h(161)
HW Reset	0000h	0083h(131)	

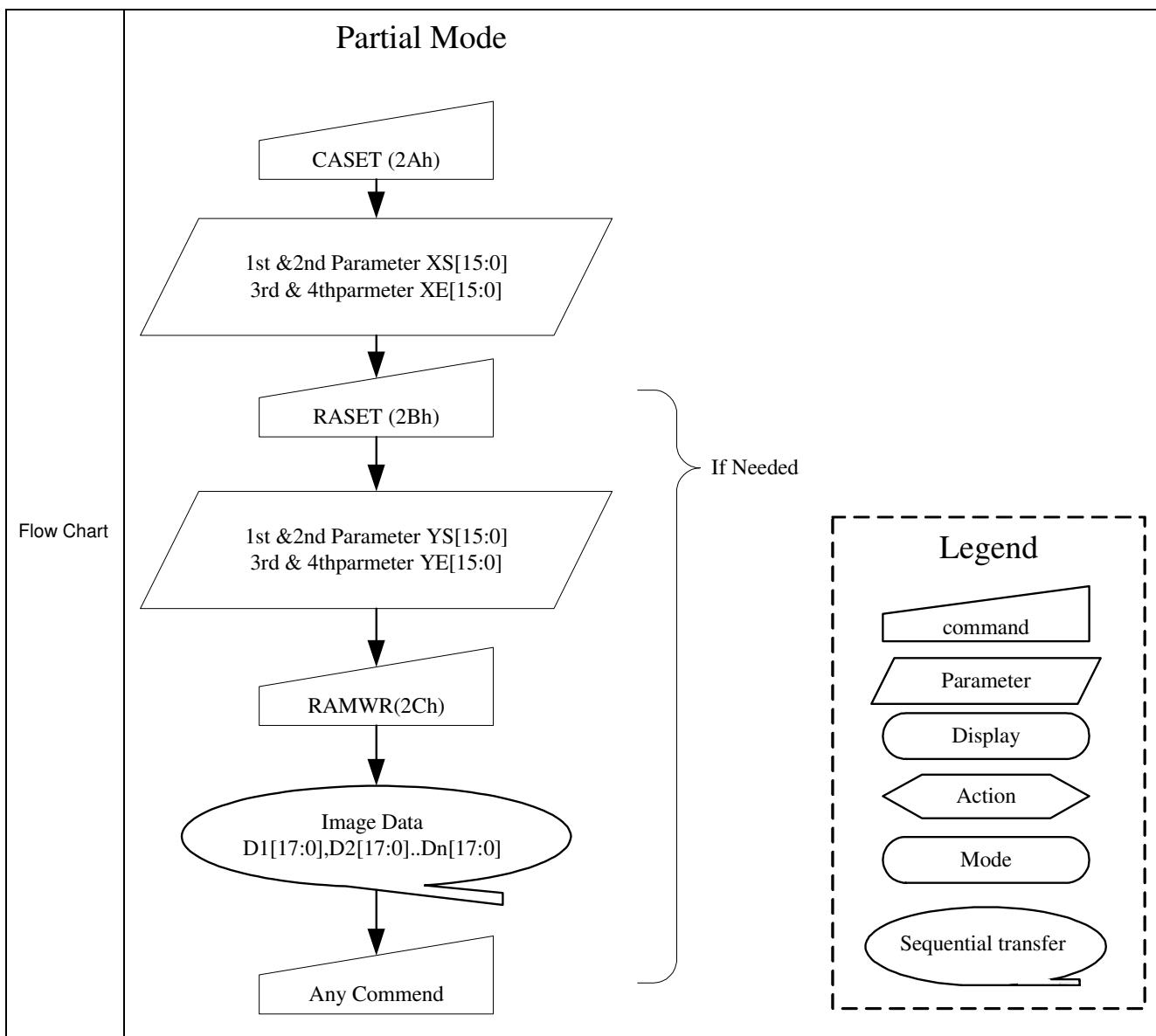
- 2. 130 x 130 memory base(GM='100')
- 3. 128 x 160 memory base(GM='011')
- 4. 120 x 160 memory base(GM='010')
- 5. 128 x 128 memory base(GM='001')
- 6. 132 x 162 memory base(GM='000')



14.2.21 Page Address Set (2Bh)

2BH		PASET (Page Address Set)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
Command	0	1	↑	x	0	0	1	0	1	0	1	1	1	2Bh
1 st Parameter	1	1	↑	x	YS15	YS14	YS13	YS12	YS11	YS10	YS9	YS8	-	
2 nd Parameter	1	1	↑	x	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0	-	
3 rd Parameter	1	1	↑	x	YE15	YE14	YE13	YE12	YE11	YE10	YE9	YE8	-	
4 th Parameter	1	1	↑	x	YE7	YE6	YE5	YE4	YE3	YE2	YE1	YE0	-	
Description	This command is used to define area of frame memory where MCU can access. This command makes no change on the other driver status. The value of YS [15:0] and YE [15:0] are referred when RAMWR command comes. Each value represents one Page line in the Frame Memory.													
														
Restriction	YS [15:0] always must be equal to or less than EP [15:0]. When YS[15:0] or YE[15:0] is greater than maximum row address like below, data of out of range will be ignored. <ol style="list-style-type: none"> 132X132 memory base (GM='101') <ul style="list-style-type: none"> (Parameter range: $0 \leq YS[15:0] \leq YE[15:0] \leq 131(0083h)$):MV="0" (Parameter range: $0 \leq YS[15:0] \leq YE[15:0] \leq 131(0083h)$):MV="1" 130X130 memory base (GM='100') <ul style="list-style-type: none"> (Parameter range: $0 \leq YS[15:0] \leq YE[15:0] \leq 129(0081h)$):MV="0" (Parameter range: $0 \leq YS[15:0] \leq YE[15:0] \leq 129(0081h)$):MV="1" 128X160 memory base (GM='011') <ul style="list-style-type: none"> (Parameter range: $0 \leq YS[15:0] \leq YE[15:0] \leq 159(009Fh)$):MV="0" (Parameter range: $0 \leq YS[15:0] \leq YE[15:0] \leq 127(007Fh)$):MV="1" 120X160 memory base (GM='010') <ul style="list-style-type: none"> (Parameter range: $0 \leq YS[15:0] \leq YE[15:0] \leq 159(009Fh)$):MV="0" (Parameter range: $0 \leq YS[15:0] \leq YE[15:0] \leq 119(0077h)$):MV="1" 128X128 memory base (GM='001') <ul style="list-style-type: none"> (Parameter range: $0 \leq YS[15:0] \leq YE[15:0] \leq 127(007Fh)$):MV="0" (Parameter range: $0 \leq YS[15:0] \leq YE[15:0] \leq 127(007Fh)$):MV="1" 132X162 memory base (GM='000') 													

	(Parameter range: $0 \leq YS[15:0] \leq YE[15:0] \leq 161(00A1h)$):MV="0" (Parameter range: $0 \leq YS[15:0] \leq YE[15:0] \leq 131(0083h)$):MV="1" X = Don't care																																																																																																														
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	<p>1. 132 x 132 memory base(GM='101')</p> <table border="1"> <thead> <tr> <th rowspan="2">Status</th><th colspan="3">Default Value</th></tr> <tr> <th>YS[15:0]</th><th>YE[15:0]</th><th>YX[15:0] (MV=1)</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>0000h</td><td colspan="2">0083h(131)</td></tr> <tr> <td>S/W Reset</td><td>0000h</td><td>0083h(131)</td><td>0083h(131)</td></tr> <tr> <td>HW Reset</td><td>0000h</td><td colspan="2">0083h(131)</td></tr> <tr> <th rowspan="2">Status</th><th colspan="3">Default Value</th></tr> <tr> <th>YS[15:0]</th><th>YE[15:0]</th><th>YX[15:0] (MV=1)</th></tr> <tr> <td>Power On Sequence</td><td>0000h</td><td colspan="2">0081h(129)</td></tr> <tr> <td>S/W Reset</td><td>0000h</td><td>0081h(129)</td><td>0081h(129)</td></tr> <tr> <td>HW Reset</td><td>0000h</td><td colspan="2">0081h(129)</td></tr> <tr> <th rowspan="2">Status</th><th colspan="3">Default Value</th></tr> <tr> <th>YS[15:0]</th><th>YE[15:0] (MV=0)</th><th>YE[15:0] (MV=1)</th></tr> <tr> <td>Power On Sequence</td><td>0000h</td><td colspan="2">009Fh(159)</td></tr> <tr> <td>SW Reset</td><td>0000h</td><td>009Fh(159)</td><td>007Fh(127)</td></tr> <tr> <td>HW Reset</td><td>0000h</td><td colspan="2">009Fh(159)</td></tr> <tr> <th rowspan="2">Status</th><th colspan="3">Default Value</th></tr> <tr> <th>YS[15:0]</th><th>YE[15:0] (MV=0)</th><th>YE[15:0] (MV=1)</th></tr> <tr> <td>Power On Sequence</td><td>0000h</td><td colspan="2">009Fh(159)</td></tr> <tr> <td>SW Reset</td><td>0000h</td><td>009Fh(159)</td><td>0077h(119)</td></tr> <tr> <td>HW Reset</td><td>0000h</td><td colspan="2">009Fh(159)</td></tr> <tr> <th rowspan="2">Status</th><th colspan="3">Default Value</th></tr> <tr> <th>YS[15:0]</th><th>YE[15:0] (MV=0)</th><th>YE[15:0] (MV=1)</th></tr> <tr> <td>Power On Sequence</td><td>0000h</td><td colspan="2">007Fh(127)</td></tr> <tr> <td>SW Reset</td><td>0000h</td><td>007Fh(127)</td><td>007Fh(127)</td></tr> <tr> <td>HW Reset</td><td>0000h</td><td colspan="2">007Fh(127)</td></tr> <tr> <th rowspan="2">Status</th><th colspan="3">Default Value</th></tr> <tr> <th>YS[15:0]</th><th>YE[15:0] (MV=0)</th><th>YE[15:0] (MV=1)</th></tr> <tr> <td>Power On Sequence</td><td>0000h</td><td colspan="2">00A1h(161)</td></tr> <tr> <td>SW Reset</td><td>0000h</td><td>00A1h(161)</td><td>0083h(131)</td></tr> </tbody> </table> <p>2. 130 x 130 memory base(GM='100') 3. 128X160 memory base(GM='011') 4. 120X160 memory base(GM='010') 5. 120X160 memory base(GM='001') 6. 132X162 memory base(GM='000')</p>	Status	Default Value			YS[15:0]	YE[15:0]	YX[15:0] (MV=1)	Power On Sequence	0000h	0083h(131)		S/W Reset	0000h	0083h(131)	0083h(131)	HW Reset	0000h	0083h(131)		Status	Default Value			YS[15:0]	YE[15:0]	YX[15:0] (MV=1)	Power On Sequence	0000h	0081h(129)		S/W Reset	0000h	0081h(129)	0081h(129)	HW Reset	0000h	0081h(129)		Status	Default Value			YS[15:0]	YE[15:0] (MV=0)	YE[15:0] (MV=1)	Power On Sequence	0000h	009Fh(159)		SW Reset	0000h	009Fh(159)	007Fh(127)	HW Reset	0000h	009Fh(159)		Status	Default Value			YS[15:0]	YE[15:0] (MV=0)	YE[15:0] (MV=1)	Power On Sequence	0000h	009Fh(159)		SW Reset	0000h	009Fh(159)	0077h(119)	HW Reset	0000h	009Fh(159)		Status	Default Value			YS[15:0]	YE[15:0] (MV=0)	YE[15:0] (MV=1)	Power On Sequence	0000h	007Fh(127)		SW Reset	0000h	007Fh(127)	007Fh(127)	HW Reset	0000h	007Fh(127)		Status	Default Value			YS[15:0]	YE[15:0] (MV=0)	YE[15:0] (MV=1)	Power On Sequence	0000h	00A1h(161)		SW Reset	0000h	00A1h(161)	0083h(131)
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SW Reset	0000h	00A1h(161)	0083h(131)																																																																																																												



14.2.22 Memory Write (2Ch)

2CH	RAMWR (Memory Write)																							
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX											
Command	0	1	↑	x	0	0	1	0	1	1	0	0	2Ch											
1 st Parameter	1	1	↑	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	-											
:	1	1	↑	x	:	:	:	:	:	:	:	:	:											
N TH Parameter	1	1	↑	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	-											
Description	This command is used to transfer data from MCU to frame memory. This command makes no change to the other driver status. When this command is accepted, the column register and the page register are reset to the Start Column/ Start Page positions. The Start Column / Start Page positions are different in accordance with MADCTL setting. Then D[17:0] is stored in frame memory and the column refister and the row register incremented. Sending any other command can stop frame Write. X=Don't care																							
Restriction	In all color modes, there is no restriction on length of parameters. 1. 132X132 memory base (GM='101') 132X132X18-bit memory can be written by this command. Memory range(0000h, 0000h) -> (0083h,083h) 2. 130X130 memory base (GM='100') 130X130X18-bit memory can be written by this command. Memory range(0000h, 0000h) -> (0081h,081h) 3. 128X160 memory base (GM='011') 128X160X18-bit memory can be written by this command. Memory range(0000h, 0000h) -> (007Fh,09Fh) 4. 120X160 memory base (GM='010') 120X160X18-bit memory can be written by this command. Memory range(0000h, 0000h) -> (0077h,09Fh) 5. 128X128 memory base (GM='001') 120X128X18-bit memory can be written by this command. Memory range(0000h, 0000h) -> (007Fh,007Fh) 6. 132X162 memory base (GM='000') 132X162X18-bit memory can be written by this command. Memory range(0000h, 0000h) -> (0083h,00A1h)																							
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Status</th> <th style="text-align: center;">Availability</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">Normal Mode On, Idle Mode Off, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Normal Mode On, Idle Mode On, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Partial Mode On, Idle Mode Off, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Partial Mode On, Idle Mode On, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Sleep In</td> <td style="text-align: center;">Yes</td> </tr> </tbody> </table>												Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																							
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Normal Mode On, Idle Mode On, Sleep Out	Yes																							
Partial Mode On, Idle Mode Off, Sleep Out	Yes																							
Partial Mode On, Idle Mode On, Sleep Out	Yes																							
Sleep In	Yes																							

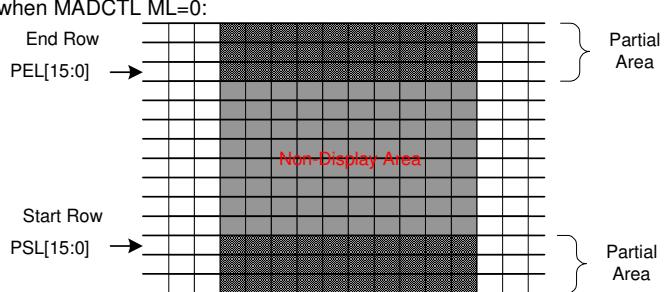
Default	<table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>Contents of memory is set randomly</td></tr> <tr> <td>SW Reset</td><td>Contents of memory is not cleared</td></tr> </tbody> </table>	Status	Default Value	Power On Sequence	Contents of memory is set randomly	SW Reset	Contents of memory is not cleared
Status	Default Value						
Power On Sequence	Contents of memory is set randomly						
SW Reset	Contents of memory is not cleared						
<pre> graph TD CASET["CASET (2Ah)"] --> ImageData("Image Data D1[17:0], D2[17:0]..Dn[17:0]") ImageData --> AnyCommand["Any Command"] </pre>							
<p>Legend</p> <ul style="list-style-type: none"> command Parameter Display Action Mode Sequential transfer 							
Flow Chart							

14.2.23 Color Setting fro 4K, 65K and 262K (2Dh)

2DH	RAMWR (Memory Write)																								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	x	0	0	1	0	1	1	0	1	2Dh												
1 st Parameter	1	1	↑	x	x	x	R005	R004	R003	R002	R001	R000	-												
:	1	1	↑	x	x	x	Rnn5	Rnn4	Rnn3	Rnn2	Rnn1	Rnn0	-												
32 nd Parameter	1	1	↑	x	x	x	R315	R314	R313	R312	R311	R310	-												
33 rd Parameter	1	1	↑	x	x	x	G005	G004	G003	G002	G001	G000	-												
:	1	1	↑	x	x	x	Gnn5	Gnn4	Gnn3	Gnn2	Gnn1	Gnn0	-												
96 th Parameter	1	1	↑	x	x	x	G635	G634	G633	G632	G631	G630	-												
97 th Parameter	1	1	↑	x	x	x	B005	B004	B003	B002	B001	B000													
:	1	1	↑	x	x	x	Bnn5	Bnn4	Bnn3	Bnn2	Bnn1	Bnn0	-												
128 th Parameter	1	1	↑	x	x	x	B315	B314	B313	B312	B311	B310	-												
Description	This command is used to define the LUT for 12bit-to-18-bit color depth conversations 128-Bytes must be written to the LUT regardless of the color mode. In this condition, 4K-color(4-4-4), and 65K-color(5-6-5) data input are transferred 6That-6(G)-6(B) through RGB LUT table. This command has no effect on other commands/parameters and Contents of frame memory. Visible change takes effect next time the Frame Memory is written to.																								
Restriction	Do not send any command before the last data is sent or LUT is not defined correctly.																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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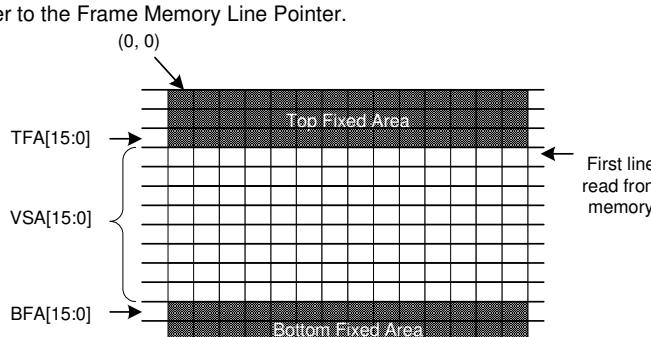
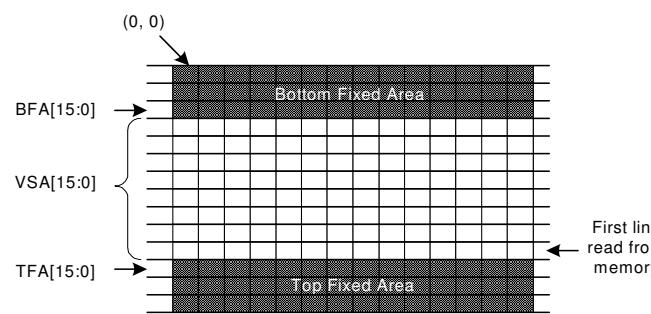
14.2.24 Memory Read (2Eh)

14.2.25 Partial Area (30h)

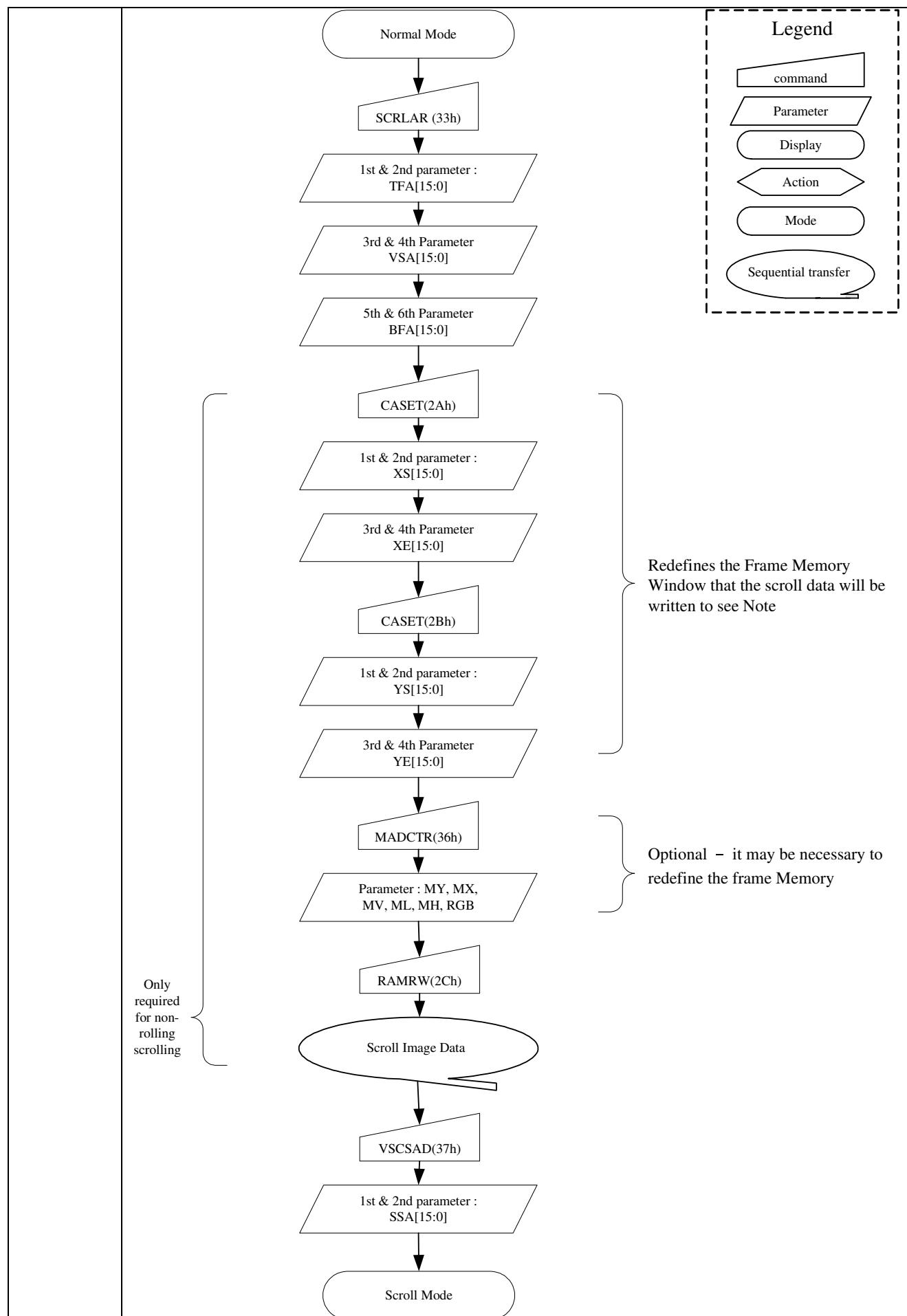
30H		PLTAR (Partial Area)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
Command	0	1	↑	x	0	0	1	1	0	0	0	0	30h	
1 st Parameter	1	1	↑	x	PSL15	PSL14	PSL13	PSL12	PSL11	PSL10	PSL9	PSL8	-	
2 nd Parameter	1	1	↑	x	PSL7	PSL6	PSL5	PSL4	PSL3	PSL2	PSL1	PSL0	-	
3 rd Parameter	1	1	↑	x	PEL15	PEL14	PEL13	PEL12	PEL11	PEL10	PEL9	PEL8	-	
4 th Parameter	1	1	↑	x	PEL7	PEL6	PEL5	PEL4	PEL3	PEL2	PEL1	PEL0	-	
Description	This command defines the partial mode's display area. There are 4 parameters associated with this command, the first defines the Start Row (PSL) and the second the End Row (PEL), as illustrated in the figures below. PSL and PEL refer to the Frame Memory Line Pointer. If End Row>Start Row when MADCTL B4=0:  If End Row > Start Row when MADCTL ML=1:  If End Row < Start Row when MADCTL ML=0:  If End Row < Start Row when MADCTL ML=1: 													

	<p>If End Row = Start Row then the Partial Area will be one row deep.</p>																																															
Restriction	-																																															
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HW Reset	0000h	0083h	0081h	009Fh	009Fh	007Fh	00A1h																																									
Flow Chart	<p>1. To Enter partial Mode</p> <pre> graph TD PTLAR["PTLAR(30h)"] --> PSL["1st & 2nd Parameter PSL[15:0]"] PSL --> PEL["3rd & 4th Parameter PEL[15:0]"] PEL --> PTLon["PTLON(12h)"] PTLon --> PartialMode1("Partial Mode") </pre> <p>2. To Exit Partial Mode</p> <pre> graph TD PartialMode1 --> DISPOFF["DISPOFF(28h)"] DISPOFF --> NORON["NORON(13h)"] NORON --> PartialModeOFF("Partial Mode OFF") PartialModeOFF --> RAMRW["RAMRW(2Ch)"] RAMRW --> ImageData["Image Data D1[17:0], D2[17:0]..Dn[17:0]"] ImageData --> DISPON["DISPON(29h)"] DISPON --> Optional["Optional to prevent Tearing Effect Image Display"] </pre> <p>Legend</p> <ul style="list-style-type: none"> command Parameter Display Action Mode Sequential transfer 																																															

14.2.26 Vertical Scrolling Definition (33h)

33H		VSCRDEF (Vertical Scrolling Definition)												
		D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command		0	1	↑	x	0	0	1	1	0	0	1	1	33h
1 st Parameter	1	1	↑	x	TFA 15	TFA 14	TFA 13	TFA 12	TFA 11	TFA 10	TFA 9	TFA 8	-	
2 nd Parameter	1	1	↑	x	TFA 7	TFA 6	TFA 5	TFA 4	TFA 3	TFA 2	TFA 1	TFA 0	-	
3 rd Parameter	1	1	↑	x	VSA 15	VSA 14	VSA 13	VSA 12	VSA 11	VSA 10	VSA 9	VSA 8	-	
4 th Parameter	1	1	↑	x	VSA 7	VSA 6	VSA 5	VSA 4	VSA 3	VSA 2	VSA 1	VSA 0	-	
5 th Parameter	1	1	↑	x	BFA 15	BFA 14	BFA 13	BFA 12	BFA 11	BFA 10	BFA 9	BFA 8	-	
6 th Parameter	1	1	↑	x	BFA 7	BFA 6	BFA 5	BFA 4	BFA 3	BFA 2	BFA 1	BFA 0	-	
Description	<p>This command defines the Vertical Scrolling Area of the display.</p> <p>When MADCTL ML=0</p> <p>The 1st & 2nd parameter TFA[15...0] describes the Top Fixed Area (in No. of lines from Top of the Frame Memory and Display).</p> <p>The 3rd & 4th parameter VSA[15...0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the bottom most line of the Top Fixed Area.</p> <p>The 5th & 6th parameter BFA[15...0] describes the Bottom Fixed Area (in No. of lines from Bottom of the Frame Memory and Display).</p> <p>TFA, VSA and BFA refer to the Frame Memory Line Pointer.</p> 													
	<p>When MADCTL ML=1</p> <p>The 1st & 2nd parameter TFA[15...0] describes the Top Fixed Area (in No. of lines from Bottom of the Frame Memory and Display).</p> <p>The 3rd & 4th parameter VSA[15...0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the top most line of the Top Fixed Area.</p> <p>The 5th & 6th parameter BFA[15...0] describes the Bottom Fixed Area (in No. of lines from Top of the Frame Memory and Display).</p> 													

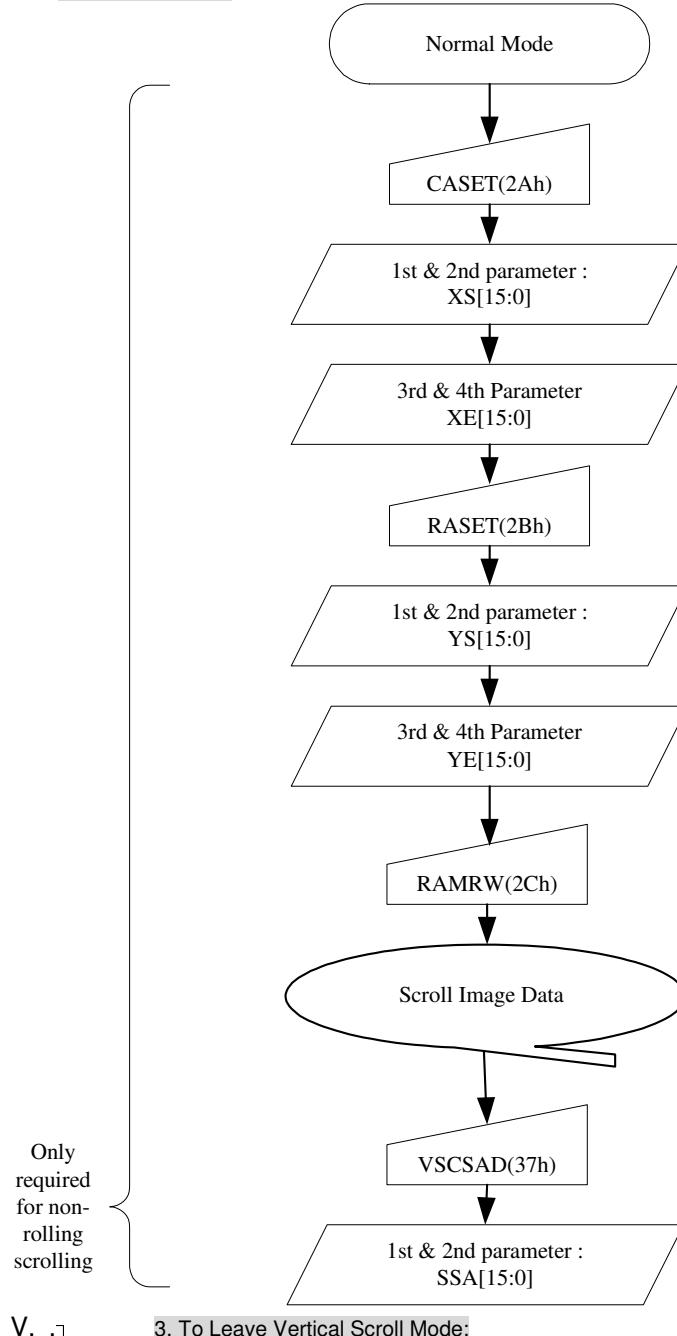
Restriction	<p>The condition is (TFA+VSA+BFA)=128 in 128RGBx128 (GM="001")</p> <p>The condition is (TFA+VSA+BFA)=130 in 130RGBx130 (GM="100")</p> <p>The condition is (TFA+VSA+BFA)=132 in 132RGBx132 (GM="101")</p> <p>The condition is (TFA+VSA+BFA)=160 in 128RGBx160 (GM="011") or 120RGBx160(GM="010")</p> <p>The condition is (TFA+VSA+BFA)=162 in 132RGBx162(GM="000")</p> <p>Otherwise Scrolling mode is undefined.</p> <p>In Vertical Scroll Mode, MADCTL parameter MV should be set to '0' – this affects the Frame memory Write.</p>																																																			
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes																																							
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	TFA[15:0]	VSA[15:0]					BFA[15:0]																																													
GM	"xx"	"101"	"100"	"011"	"010"	"001"	"000"	"xx"																																												
Power On Sequence	0000h	0083h	0081h	00A0h	00A0h	0080h	00A2h	0000h																																												
SW Reset	0000h	0083h	0081h	00A0h	00A0h	0080h	00A2h	0000h																																												
HW Reset	0000h	0083h	0081h	00A0h	00A0h	0080h	00A2h	0000h																																												
Flow Chart	1. To enter Vertical Scroll Mode:																																																			



Note 1

The Frame Memory Window size must be defined correctly otherwise undesirable image will be displayed.

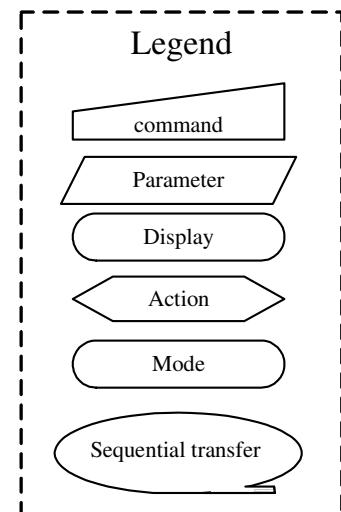
2. Continuous Scroll:

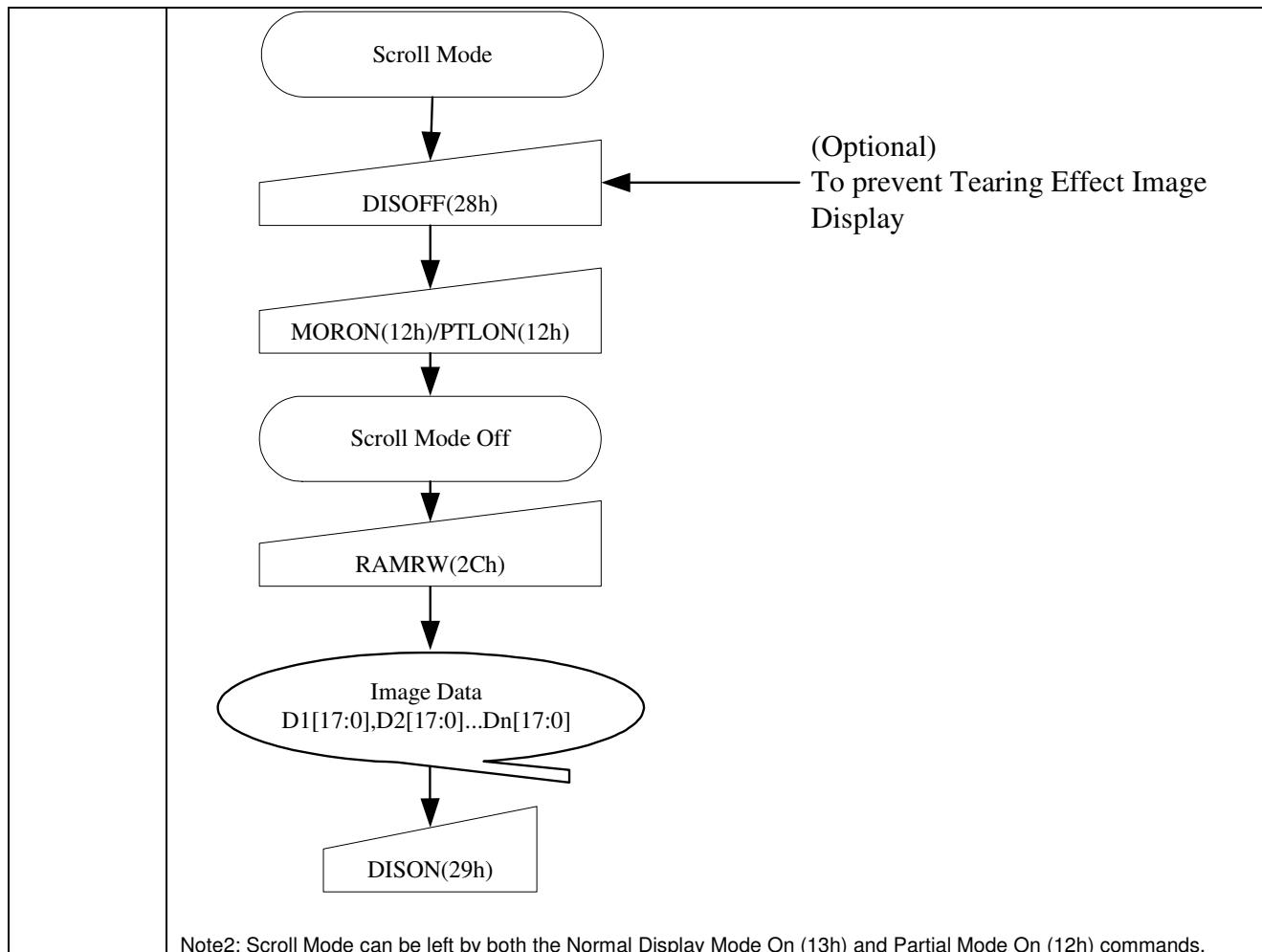


Only required for non-rolling scrolling

V. .

3. To Leave Vertical Scroll Mode:



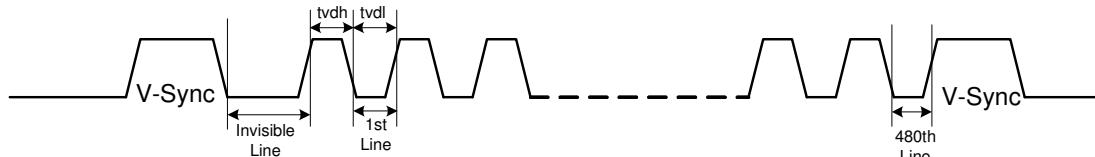


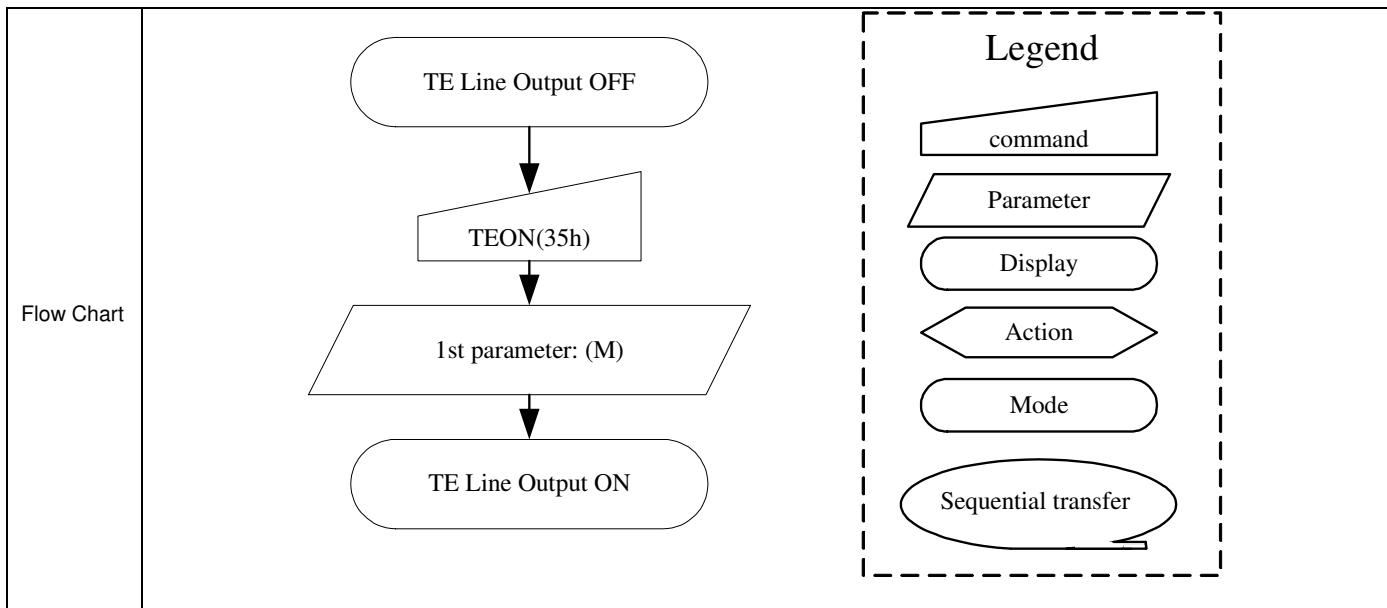
Note2: Scroll Mode can be left by both the Normal Display Mode On (13h) and Partial Mode On (12h) commands.

14.2.27 Tearing Effect Line Off (34h)

34H		TEOFF (Tearing Effect Line OFF)																							
		D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX											
Command		0	1	↑	x	0	0	1	1	0	1	0	0	34h											
Parameter	NO PARAMETER																								
Description	This command is used to turn OFF (Active Low) the Tearing Effect output signal from the TE signal line.																								
Restriction	This command has no effect when Tearing Effect output is already OFF.																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Status	Default Value																								
Power On Sequence	OFF																								
SW Reset	OFF																								
HW Reset	OFF																								
Flow Chart	<pre> graph TD A([TE Line Output ON]) --> B[TEOFF(34h)] B --> C([TE Line Output OFF]) </pre> <p>Legend</p> <ul style="list-style-type: none"> command Parameter Display Action Mode Sequential transfer 																								

14.2.28 Tearing Effect Line On (35h)

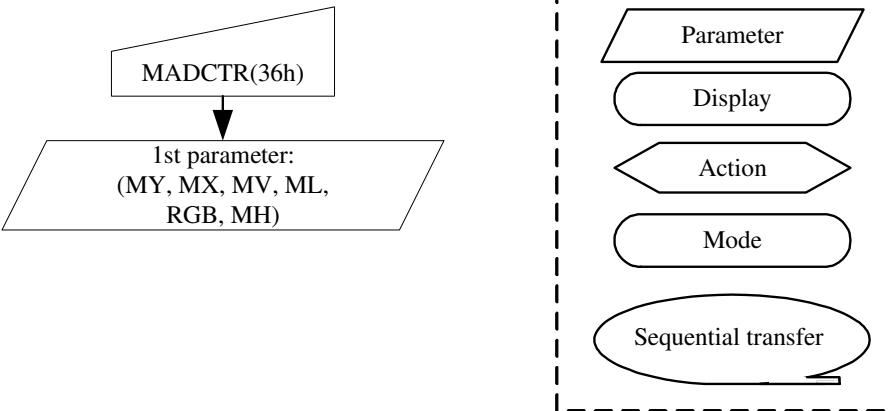
TEON (Tearing Effect Line ON)																									
35H	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	x	0	0	1	1	0	1	0	1	35h												
1 st Parameter	1	1	↑	x	x	x	x	x	x	x	x	M	00h												
Description	This command is used to turn ON the Tearing Effect output signal from the TE signal line. This output is not affected by changing MADCTL bit ML. The Tearing Effect Line On has one parameter which describes the mode of the Tearing Effect Output Line. (X=Don't Care). When M=0: The Tearing Effect Output line consists of V-Blanking information only.:  When M=1: The Tearing Effect Output Line consists of both V-Blanking and H-Blanking information: 																								
	<i>Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.</i>																								
Restriction	This command has no effect when Tearing Effect output is already OFF.																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
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Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>Tearing effect off & M=0</td></tr> <tr> <td>SW Reset</td><td>Tearing effect off & M=0</td></tr> <tr> <td>HW Reset</td><td>Tearing effect off & M=0</td></tr> </tbody> </table>													Status	Default Value	Power On Sequence	Tearing effect off & M=0	SW Reset	Tearing effect off & M=0	HW Reset	Tearing effect off & M=0				
Status	Default Value																								
Power On Sequence	Tearing effect off & M=0																								
SW Reset	Tearing effect off & M=0																								
HW Reset	Tearing effect off & M=0																								



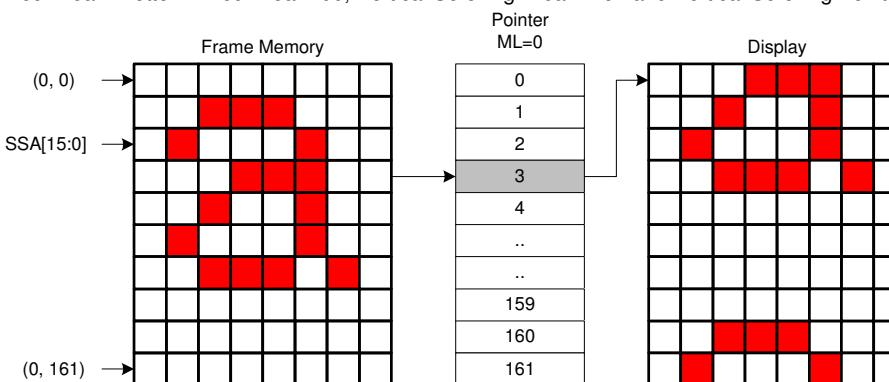
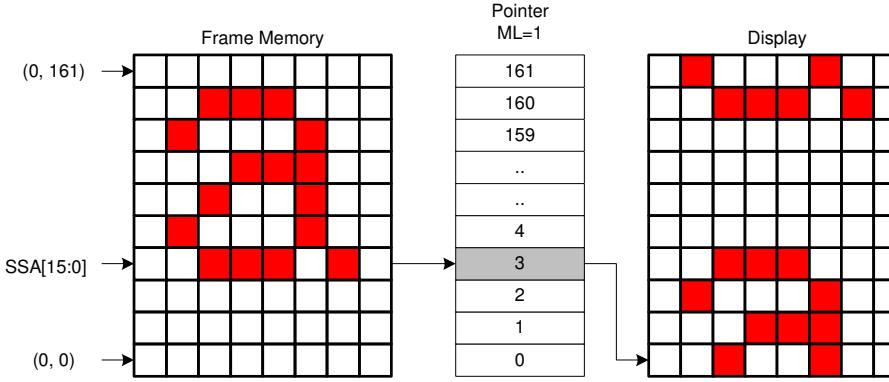
14.2.29 Memory Access Control (36h)

36H		MADCTL (Memory Access Control)																														
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																			
Command	0	1	↑	x	0	0	1	1	0	1	1	0	36h																			
1 st Parameter	1	1	↑	x	MY	MX	MV	ML	RGB	MH	x	x	00h																			
This command defines read/write scanning direction of frame memory. This command makes no change on the other driver status. Bit Assignment																																
	<table border="1"> <thead> <tr> <th>Bit</th> <th>Description</th> <th>Comment</th> </tr> </thead> <tbody> <tr> <td>MY</td> <td>Row Address Order</td> <td rowspan="3">These 3 bits controls MPU to memory write/read direction.</td></tr> <tr> <td>MX</td> <td>Column Address Order</td> </tr> <tr> <td>MV</td> <td>Page/Column Selection</td> </tr> <tr> <td>ML</td> <td>Vertical Order</td> <td>LCD Vertical refresh direction control</td></tr> <tr> <td>RGB</td> <td>RGB/BGR Order</td> <td>Color selector switch control 0=RGB color filter panel 1=BGR color filter panel</td></tr> <tr> <td>MH</td> <td>Display data latch order</td> <td>'1'=LCD Refresh right to left '0'=LCD Refresh left to right</td></tr> </tbody> </table>													Bit	Description	Comment	MY	Row Address Order	These 3 bits controls MPU to memory write/read direction.	MX	Column Address Order	MV	Page/Column Selection	ML	Vertical Order	LCD Vertical refresh direction control	RGB	RGB/BGR Order	Color selector switch control 0=RGB color filter panel 1=BGR color filter panel	MH	Display data latch order	'1'=LCD Refresh right to left '0'=LCD Refresh left to right
Bit	Description	Comment																														
MY	Row Address Order	These 3 bits controls MPU to memory write/read direction.																														
MX	Column Address Order																															
MV	Page/Column Selection																															
ML	Vertical Order	LCD Vertical refresh direction control																														
RGB	RGB/BGR Order	Color selector switch control 0=RGB color filter panel 1=BGR color filter panel																														
MH	Display data latch order	'1'=LCD Refresh right to left '0'=LCD Refresh left to right																														
B5	B6	B7	Image in Frame Memory																													
0	0	0																														
0	0	1																														
0	1	0																														
0	1	1																														
	B5	B6	B7	Image in Frame Memory																												
	1	0	0																													
	1	0	1																													
	1	1	0																													
	1	1	1																													

	<p>B3 = 0</p> <p>Memory</p> <p>R G B</p> <p>Sent RGB</p> <p>Display Panel</p> <p>R G B</p>												
	<p>B3 = 1</p> <p>Memory</p> <p>R G B</p> <p>Sent BGR</p> <p>Display Panel</p> <p>B G R</p>												
Restriction	-D1 and D0 of the 1 st parameter are set to "00" internally.												
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												

Default	<table border="1" data-bbox="572 238 1207 372"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>MY=0,MX=0,MV=0,ML=0,RGB=0,MH=0</td></tr> <tr> <td>SW Reset</td><td>No Change</td></tr> <tr> <td>HW Reset</td><td>MY=0,MX=0,MV=0,ML=0,RGB=0,MH=0</td></tr> </tbody> </table>	Status	Default Value	Power On Sequence	MY=0,MX=0,MV=0,ML=0,RGB=0,MH=0	SW Reset	No Change	HW Reset	MY=0,MX=0,MV=0,ML=0,RGB=0,MH=0
Status	Default Value								
Power On Sequence	MY=0,MX=0,MV=0,ML=0,RGB=0,MH=0								
SW Reset	No Change								
HW Reset	MY=0,MX=0,MV=0,ML=0,RGB=0,MH=0								
Flow Chart	 <pre> graph TD A[MADCTR(36h)] --> B[1st parameter: (MY, MX, MV, ML, RGB, MH)] </pre> <div style="border: 1px dashed black; padding: 5px; margin-top: 10px;"> <p>Legend</p> <ul style="list-style-type: none"> command Parameter Display Action Mode Sequential transfer </div>								

14.2.30 Vertical Scrolling Start Address (37h)

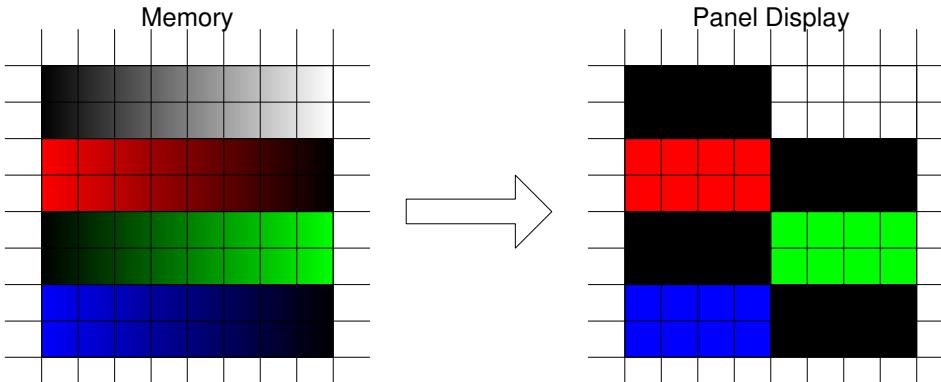
VSCRSADD (Vertical Scrolling Start Address)													
37H	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	1	1	0	1	1	1	37h
1 st Parameter	1	1	↑	x	SSA 15	SSA 14	SSA 13	SSA 12	SSA 11	SSA 10	SSA 9	SSA 8	00h
2 nd Parameter	1	1	↑	x	SSA 7	SSA 6	SSA 5	SSA 4	SSA 3	SSA 2	SSA 1	SSA 0	00h
Description	This command is used together with Vertical Scrolling Definition (33h). These two commands describe the scrolling area and the scrolling mode. The Vertical Scrolling Start Address command has one parameter which describes the address of the line in the Frame Memory that will be written as the first line after the last line of the Top Fixed Area on the display as illustrated below: This command Start the scrolling. When MADCTL ML=0 Example: GM=000, 132RGBx162 When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 162 and Vertical Scrolling Pointer SSA='3'.  When MADCTL ML=1 Example: GM=000, 132RGBx162 When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 162 and SSA='3'.  Note: When new Pointer position and Picture Data are sent, the result on the display will happen at the next Panel Scan to avoid tearing effect. SSA refers to the Frame Memory scan address When new Pointer position and Picture Data, internal system works as 128x128 and maximum scan address becomes 127 internal of 161. X=Don't care												
Restriction	Since the value of the Vertical Scrolling Start Address is absolute (with reference to the Frame Memory), it must not enter the fixed area (defined by Vertical Scrolling Definition (33h) – otherwise undesirable image will be displayed on the Panel). SSA[15:0] is based on 1-line unit. SSA[15:0] =0000h, 0001h, 0002h, 003h, ..., 00A1h												

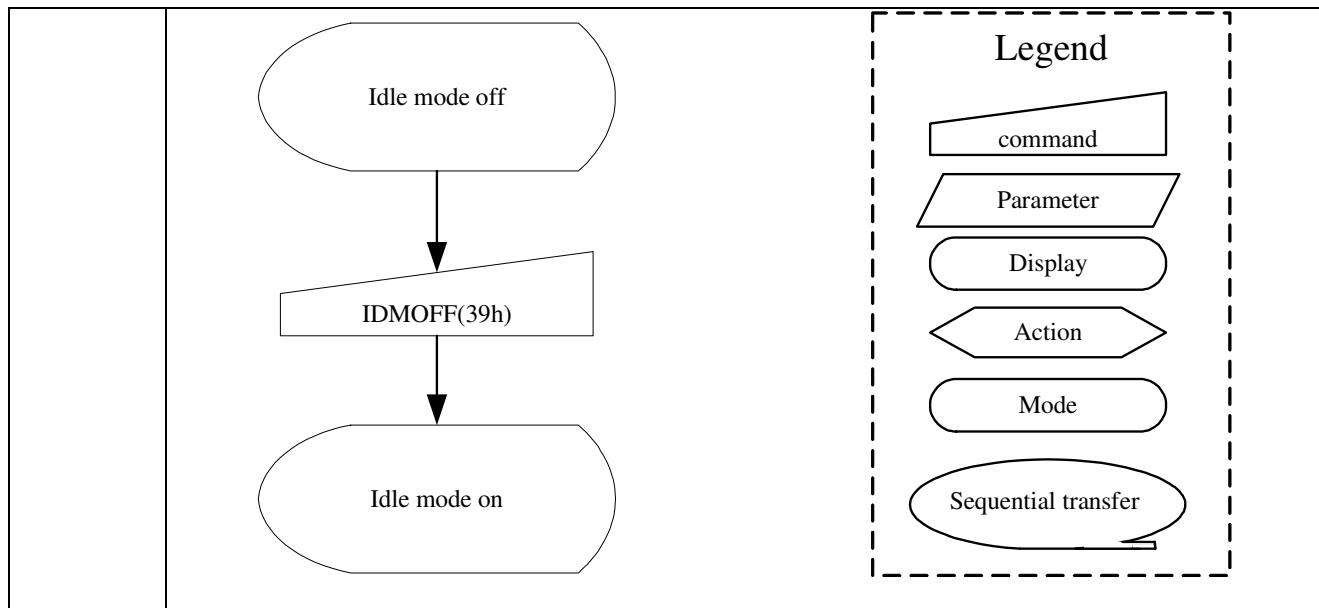
		Status	Availability
Register Availability		Normal Mode On, Idle Mode Off, Sleep Out	Yes
		Normal Mode On, Idle Mode On, Sleep Out	Yes
		Partial Mode On, Idle Mode Off, Sleep Out	Yes
		Partial Mode On, Idle Mode On, Sleep Out	Yes
		Sleep In	Yes
		Status	Default Value
Default		Power On Sequence	0000h
		SW Reset	0000h
		HW Reset	0000h
Flow Chart	See Vertical Scrolling Definition (33h) description.		

14.2.31 Idle Mode Off (38h)

38H		IDMOFF (Idle Mode Off)																							
		D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX											
Command		0	1	↑	x	0	0	1	1	1	0	0	0	38h											
Parameter	NO PARAMETER																								
Description	This command is used to recover from Idle mode on. There will be no abnormal visible effect on the display mode change transition. In the Idle off mode <ol style="list-style-type: none"> 1. LCD can display maximum 4096, 65K, 262K colors. 2. Normal frame frequency is applied. X = don't care																								
Restriction	This command has no effect when module is already in idle off mode.																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Status	Default Value																								
Power On Sequence	Idle Mode Off																								
SW Reset	Idle Mode Off																								
HW Reset	Idle Mode Off																								
Flow Chart	<pre> graph TD A([Idle mode on]) --> B[IDMOFF(38h)] B --> C([Idle mode off]) </pre> <p>Legend:</p> <ul style="list-style-type: none"> command Parameter Display Action Mode Sequential transfer 																								

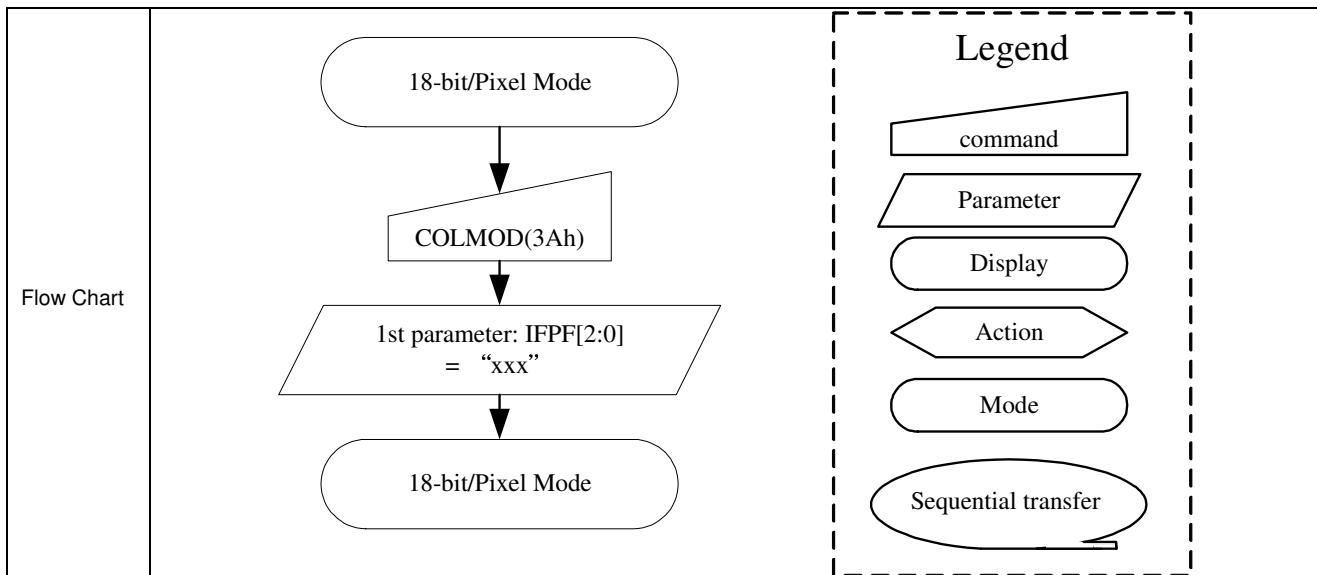
14.2.32 Idle Mode On (39h)

39H		IDMON (Idle Mode On)																																																																		
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																							
Command	0	1	↑	x	0	0	1	1	1	0	0	1	39h																																																							
Parameter	NO PARAMETER																																																																			
Description	<p>This command is used to enter into Idle mode on.</p> <p>There will be no abnormal visible effect on the display mode change transition.</p> <p>In the Idle mode,</p> <ol style="list-style-type: none"> 1. Color expression is reduced. The primary and the secondary colors using MSB of each R,G and B in the Frame Memory, 8 color depth data is displayed. 2. 8-Color mode frame frequency is applied. 3. Exit from IDMON by Idle Mode Off(38h) command.  <table border="1" data-bbox="477 1185 1255 1522"> <thead> <tr> <th></th><th>R5 R4 R3 R2 R1 R0</th><th>G5 G4 G3 G2 G1 G0</th><th>B5 B4 B3 B2 B1 B0</th></tr> </thead> <tbody> <tr> <td>Black</td><td>0XXXXX</td><td>0XXXXX</td><td>0XXXXX</td></tr> <tr> <td>Blue</td><td>0XXXXX</td><td>0XXXXX</td><td>1XXXXX</td></tr> <tr> <td>Red</td><td>1XXXXX</td><td>0XXXXX</td><td>0XXXXX</td></tr> <tr> <td>Magenta</td><td>1XXXXX</td><td>0XXXXX</td><td>1XXXXX</td></tr> <tr> <td>Green</td><td>0XXXXX</td><td>1XXXXX</td><td>0XXXXX</td></tr> <tr> <td>Cyan</td><td>0XXXXX</td><td>1XXXXX</td><td>1XXXXX</td></tr> <tr> <td>Yellow</td><td>1XXXXX</td><td>1XXXXX</td><td>0XXXXX</td></tr> <tr> <td>White</td><td>1XXXXX</td><td>1XXXXX</td><td>1XXXXX</td></tr> </tbody> </table> <p>This command has no effect when module is already in idle on mode.</p> <table border="1" data-bbox="572 1596 1155 1799"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table> <table border="1" data-bbox="631 1866 1096 1978"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>Idle Mode Off</td></tr> <tr> <td>SW Reset</td><td>Idle Mode Off</td></tr> </tbody> </table>		R5 R4 R3 R2 R1 R0	G5 G4 G3 G2 G1 G0	B5 B4 B3 B2 B1 B0	Black	0XXXXX	0XXXXX	0XXXXX	Blue	0XXXXX	0XXXXX	1XXXXX	Red	1XXXXX	0XXXXX	0XXXXX	Magenta	1XXXXX	0XXXXX	1XXXXX	Green	0XXXXX	1XXXXX	0XXXXX	Cyan	0XXXXX	1XXXXX	1XXXXX	Yellow	1XXXXX	1XXXXX	0XXXXX	White	1XXXXX	1XXXXX	1XXXXX	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes	Status	Default Value	Power On Sequence	Idle Mode Off	SW Reset	Idle Mode Off													
	R5 R4 R3 R2 R1 R0	G5 G4 G3 G2 G1 G0	B5 B4 B3 B2 B1 B0																																																																	
Black	0XXXXX	0XXXXX	0XXXXX																																																																	
Blue	0XXXXX	0XXXXX	1XXXXX																																																																	
Red	1XXXXX	0XXXXX	0XXXXX																																																																	
Magenta	1XXXXX	0XXXXX	1XXXXX																																																																	
Green	0XXXXX	1XXXXX	0XXXXX																																																																	
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Status	Default Value																																																																			
Power On Sequence	Idle Mode Off																																																																			
SW Reset	Idle Mode Off																																																																			
Flow Chart																																																																				



14.2.33 Interface Pixel Format (3Ah)

IDMON (Idle Mode On)																									
39H	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	x	0	0	1	1	1	0	1	0	3Ah												
1 st Parameter	1	1	↑	x	VIPF3	VIPF2	VIPF1	VIPF0	D3	IFPF2	IFPF1	IFPF0	66h												
This command is used to define the format of RGB picture data, which is to be transferred via the MCU interface. The formats are shown in the table:																									
Description	Bit	Description				Value																			
	VIPF3	RGB Interface Color Format				“0101”=16 bit/pixel (1 times data transfer)																			
	VIPF2					“0110”=18 bit/pixel (1 times data transfer)																			
	VIPF1					“1110”=18 bit/pixel (3 times data transfer)																			
	VIPF0					The others = not defined																			
	D3					“0” (Not Used)																			
	IFPF2	Control Interface Color Format				“011”=12 bit/pixel																			
	IFPF1					“101”=16 bit/pixel																			
	IFPF0					“110”=18 bit/pixel																			
Note																									
1.In 12-bits/Pixel, 16-bits/Pixel mode, the LUT is applied to transfer data into the Frame Memory.																									
2. When VIPF[3:0]=1110, 6-bits data width of 3-times transfer is used to transmit 1 pixel data with the 18-bits color depth information.																									
X = don't care																									
Restriction	There is no visible effect until the Frame Memory is written to.																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Sleep In	Yes																								
<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>18bit/pixel</td> </tr> <tr> <td>SW Reset</td> <td>No change</td> </tr> </tbody> </table>													Status	Default Value	Power On Sequence	18bit/pixel	SW Reset	No change							
Status	Default Value																								
Power On Sequence	18bit/pixel																								
SW Reset	No change																								



14.2.37 Frame Rate Control (In normal mode/Full colors) (B1h)

B1h	Frame Rate Control(In normal mode/Full colors)																							
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	1	0	1	1	0	0	0	1	B1h												
1 st Parameter	1	1	↑	x	x	x	DIVA4	DIVA3	DIVA2	DIVA1	DIVA0	x												
2 nd Parameter	1	1	↑	x	x	VPA5	VPA4	VPA3	VPA2	VPA1	VPA0	x												
Description	Sets the division ratio for internal clocks of Normal mode at CPU interface mode. DIVA[4:0]: division ratio for internal clocks when Normal mode. VPA[5:0]: VS porch for internal clocks when Normal mode $Frame_rate = \frac{200kHz}{(Line + VPA[5 : 0])(DIVA[4 : 0] + 4)}$ (1) When GM=101(132*132) In Normal mode, line=132, Default value DIVA[4:0]=17, VPA[5:0]=20, Frame rate=62.7Hz (2) When GM=100(130*130) In Normal mode, line=130, Default value DIVA[4:0]=17, VPA[5:0]=20, Frame rate=63.5Hz (3) When GM=011(128*160) In Normal mode, line=160, Default value DIVA[4:0]=14, VPA[5:0]=20, Frame rate=61.7Hz (4) When GM=010(120*160) In Normal mode, line=160, Default value DIVA[4:0]=14, VPA[5:0]=20, Frame rate=61.7Hz (5) When GM=001(128*128) In Normal mode, line=128, Default value DIVA[4:0]=17, VPA[5:0]=20, Frame rate=64.4Hz (6) When GM=000(132*162) In Normal mode, line=162, Default value DIVA[4:0]=14, VPA[5:0]=20, Frame rate=61Hz																							
Restriction	-																							
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>												Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																							
Normal Mode On, Idle Mode Off, Sleep Out	Yes																							
Normal Mode On, Idle Mode On, Sleep Out	Yes																							
Partial Mode On, Idle Mode Off, Sleep Out	Yes																							
Partial Mode On, Idle Mode On, Sleep Out	Yes																							
Sleep In	Yes																							

Default	(1) When GM=000(132*162), GM=011(128*160) or GM=010(120*160)	<table border="1"> <thead> <tr> <th>Status</th><th colspan="2">Default Value</th></tr> <tr> <th></th><th>DIVA[4:0]</th><th>VPA[5:0]</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>0Eh/14d</td><td>14h/20d</td></tr> <tr> <td>S/W Reset</td><td>0Eh/14d</td><td>14h/20d</td></tr> <tr> <td>H/W Reset</td><td>0Eh/14d</td><td>14h/20d</td></tr> </tbody> </table>	Status	Default Value			DIVA[4:0]	VPA[5:0]	Power On Sequence	0Eh/14d	14h/20d	S/W Reset	0Eh/14d	14h/20d	H/W Reset	0Eh/14d	14h/20d
Status	Default Value																
	DIVA[4:0]	VPA[5:0]															
Power On Sequence	0Eh/14d	14h/20d															
S/W Reset	0Eh/14d	14h/20d															
H/W Reset	0Eh/14d	14h/20d															
(2) When GM=001(128*128), GM=100(130*130), GM=101(132*132)	<table border="1"> <thead> <tr> <th>Status</th><th colspan="2">Default Value</th></tr> <tr> <th></th><th>DIVA[4:0]</th><th>VPA[5:0]</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>11h/17d</td><td>11h/17d</td></tr> <tr> <td>S/W Reset</td><td>11h/17d</td><td>11h/17d</td></tr> <tr> <td>H/W Reset</td><td>11h/17d</td><td>11h/17d</td></tr> </tbody> </table>	Status	Default Value			DIVA[4:0]	VPA[5:0]	Power On Sequence	11h/17d	11h/17d	S/W Reset	11h/17d	11h/17d	H/W Reset	11h/17d	11h/17d	
Status	Default Value																
	DIVA[4:0]	VPA[5:0]															
Power On Sequence	11h/17d	11h/17d															
S/W Reset	11h/17d	11h/17d															
H/W Reset	11h/17d	11h/17d															
Flow Chart	<pre> graph TD A[RGBCTR1(B1h)] --> B[/] B --> C[1st parameter: DIVA[4:0] 2nd parameter: VPA[4:0]] </pre>	<p>Legend</p> <ul style="list-style-type: none"> command Parameter Display Action Mode Sequential transfer 															

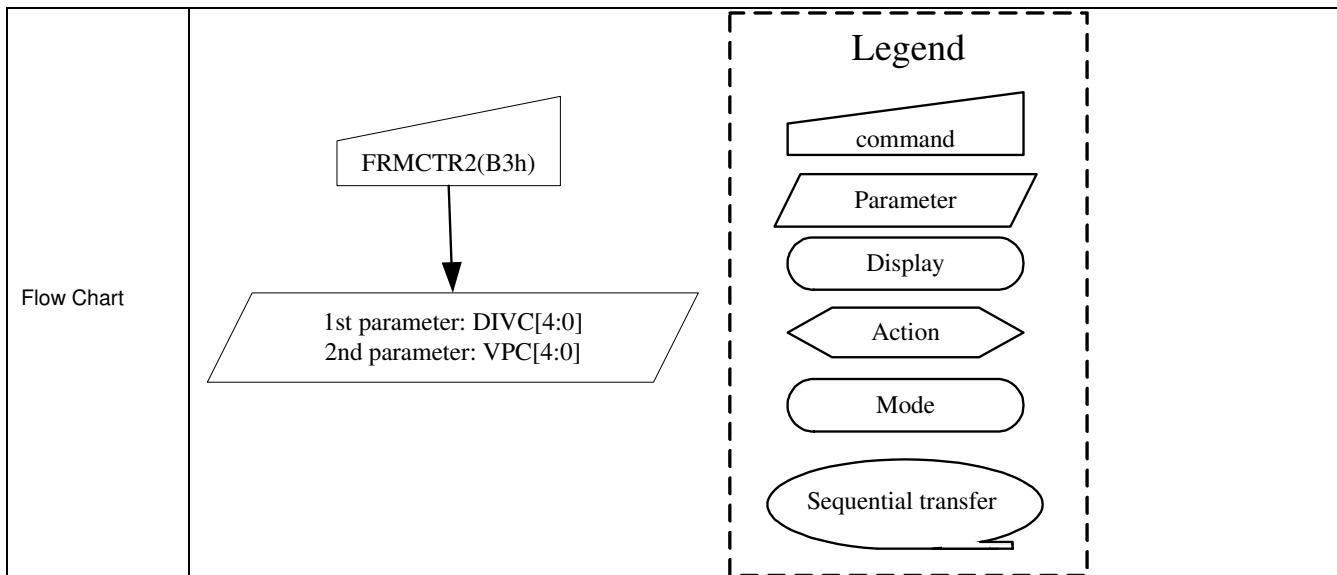
14.2.38 Frame Rate Control(In Idle mode/8-colors) (B2h)

B2h	Frame Rate Control(In Idle mode/Full colors)																							
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	1	0	1	1	0	0	1	0	B2h												
1 st Parameter	1	1	↑	x	x	x	DIVB4	DIVB3	DIVB2	DIVB1	DIVB0	x												
2 nd Parameter	1	1	↑	x	x	VPB5	VPB4	VPB3	VPB2	VPB1	VPB0	x												
Description	Sets the division ratio for internal clocks of Idle mode at CPU interface mode. DIVB[4:0]: division ratio for internal clocks when Idle mode. VPB[5:0]: VS porch for internal clocks when Idle mode $Frame_rate = \frac{200kHz}{(Line + VPB[5 : 0])(DIVB[4 : 0] + 4)}$ <ul style="list-style-type: none"> (1) When GM=101(132*132) In Normal mode, line=132, Default value DIVA[4:0]=17, VPA[5:0]=20, Frame rate=62.7Hz (2) When GM=100(130*130) In Normal mode, line=130, Default value DIVA[4:0]=17, VPA[5:0]=20, Frame rate=63.5Hz (3) When GM=011(128*160) In 8-color mode, line=160, Default value DIVB[4:0]=14, VPB[5:0]=20, Frame rate=61.7Hz (4) When GM=010(120*160) In 8-color I mode, line=160, Default value DIVB[4:0]=14, VPB[5:0]=20, Frame rate=61.7Hz (5) When GM=001(128*128) In 8-color mode, line=128, Default value DIVB[4:0]=17, VPB[5:0]=20, Frame rate=64.4Hz (6) When GM=000(132*162) In 8-color mode, line=162, Default value DIVB[4:0]=14, VPB[5:0]=20, Frame rate=61Hz 																							
Restriction	-																							
Register Availability	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>												Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																							
Normal Mode On, Idle Mode Off, Sleep Out	Yes																							
Normal Mode On, Idle Mode On, Sleep Out	Yes																							
Partial Mode On, Idle Mode Off, Sleep Out	Yes																							
Partial Mode On, Idle Mode On, Sleep Out	Yes																							
Sleep In	Yes																							

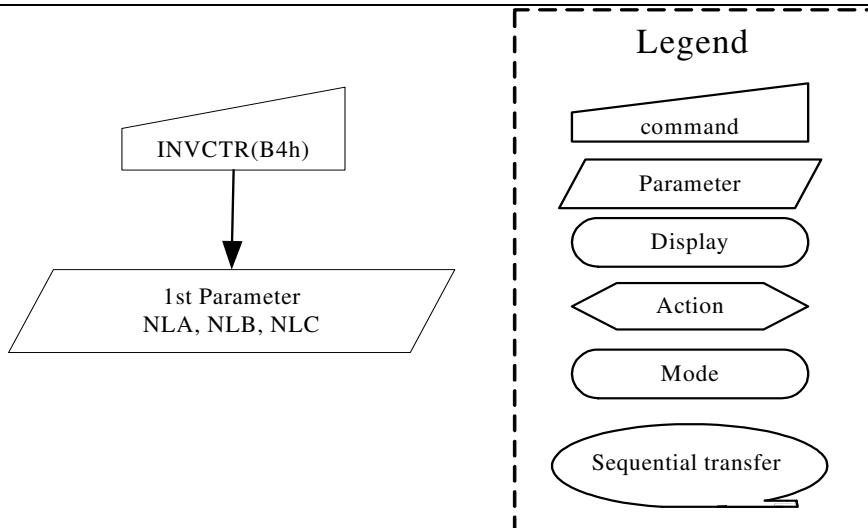
Default	(1) When GM=000(132*162), GM=011(128*160) or GM=010(120*160)	<table border="1"> <thead> <tr> <th>Status</th><th colspan="2">Default Value</th></tr> </thead> <tbody> <tr> <td>DIVB[4:0]</td><td>VPB[5:0]</td><td></td></tr> <tr> <td>Power On Sequence</td><td>0Eh/14d</td><td>14h/20d</td></tr> <tr> <td>S/W Reset</td><td>0Eh/14d</td><td>14h/20d</td></tr> <tr> <td>H/W Reset</td><td>0Eh/14d</td><td>14h/20d</td></tr> </tbody> </table>	Status	Default Value		DIVB[4:0]	VPB[5:0]		Power On Sequence	0Eh/14d	14h/20d	S/W Reset	0Eh/14d	14h/20d	H/W Reset	0Eh/14d	14h/20d
Status	Default Value																
DIVB[4:0]	VPB[5:0]																
Power On Sequence	0Eh/14d	14h/20d															
S/W Reset	0Eh/14d	14h/20d															
H/W Reset	0Eh/14d	14h/20d															
(2) When GM=001(128*128), GM=100(130*130), GM=101(132*132)	<table border="1"> <thead> <tr> <th>Status</th><th colspan="2">Default Value</th></tr> </thead> <tbody> <tr> <td>DIVB[4:0]</td><td>VPB[5:0]</td><td></td></tr> <tr> <td>Power On Sequence</td><td>11h/17d</td><td>11h/17d</td></tr> <tr> <td>S/W Reset</td><td>11h/17d</td><td>11h/17d</td></tr> <tr> <td>H/W Reset</td><td>11h/17d</td><td>11h/17d</td></tr> </tbody> </table>	Status	Default Value		DIVB[4:0]	VPB[5:0]		Power On Sequence	11h/17d	11h/17d	S/W Reset	11h/17d	11h/17d	H/W Reset	11h/17d	11h/17d	
Status	Default Value																
DIVB[4:0]	VPB[5:0]																
Power On Sequence	11h/17d	11h/17d															
S/W Reset	11h/17d	11h/17d															
H/W Reset	11h/17d	11h/17d															
Flow Chart	<pre> graph TD A[FRMCTR2(B2h)] --> B{1st parameter: DIVB[4:0] 2nd parameter: VPB[4:0]} </pre>	<p>Legend</p> <ul style="list-style-type: none"> command Parameter Display Action Mode Sequential transfer 															

14.2.39 Frame Rate Control(In Partial mode/full colors) (B3h)

B3h		Frame Rate Control(In Partial mode/Full colors)																																						
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX																												
Command	0	1	↑	1	0	1	1	0	0	1	1	B3h																												
1 st Parameter	1	1	↑	x	x	x	DIVC4	DIVC3	DIVC2	DIVC1	DIVC0	x																												
2 nd Parameter	1	1	↑	x	x	VPC5	VPC4	VPC3	VPC2	VPC1	VPC0	x																												
Description	Sets the division ratio for internal clocks of Partial mode at CPU interface mode. DIVB[4:0]: division ratio for internal clocks when Partial mode. VPB[5:0]: VS porch for internal clocks when Partial mode $Frame_rate = \frac{200kHz}{(Line + VPC[5:0])(DIVC[4:0] + 4)}$ <ul style="list-style-type: none"> (1) When GM=101(132*132) In Normal mode, line=132, Default value DIVA[4:0]=17, VPA[5:0]=20, Frame rate=62.7Hz (2) When GM=100(130*130) In Normal mode, line=130, Default value DIVA[4:0]=17, VPA[5:0]=20, Frame rate=63.5Hz (3) When GM=011(128*160) In Partial mode, line=160, Default value DIVC[4:0]=14, VPC[5:0]=20, Frame rate=61.7Hz (4) When GM=010(120*160) In Partial mode, line=160, Default value DIVC[4:0]=14, VPC[5:0]=20, Frame rate=61.7Hz (5) When GM=001(128*128) In Partial mode, line=128, Default value DIVC[4:0]=17, VPC[5:0]=20, Frame rate=64.4Hz (6) When GM=000(132*162) In Partial mode, line=162, Default value DIVC[4:0]=14, VPC[5:0]=20, Frame rate=61Hz 																																							
Restriction	-																																							
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>												Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes																
Status	Availability																																							
Normal Mode On, Idle Mode Off, Sleep Out	Yes																																							
Normal Mode On, Idle Mode On, Sleep Out	Yes																																							
Partial Mode On, Idle Mode Off, Sleep Out	Yes																																							
Partial Mode On, Idle Mode On, Sleep Out	Yes																																							
Sleep In	Yes																																							
Default	<ul style="list-style-type: none"> (1) When GM=000(132*162), GM=011(128*160) or GM=010(120*160) <table border="1"> <thead> <tr> <th rowspan="2">Status</th><th colspan="2">Default Value</th></tr> <tr> <th>DIVC4:0]</th><th>VPC[5:0]</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>0Eh/14d</td><td>14h/20d</td></tr> <tr> <td>S/W Reset</td><td>0Eh/14d</td><td>14h/20d</td></tr> <tr> <td>H/W Reset</td><td>0Eh/14d</td><td>14h/20d</td></tr> </tbody> </table> (3) When GM=001(128*128), GM=100(130*130), GM=101(132*132) <table border="1"> <thead> <tr> <th rowspan="2">Status</th><th colspan="2">Default Value</th></tr> <tr> <th>DIVB[4:0]</th><th>VPB[5:0]</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>11h/17d</td><td>11h/17d</td></tr> <tr> <td>S/W Reset</td><td>11h/17d</td><td>11h/17d</td></tr> <tr> <td>H/W Reset</td><td>11h/17d</td><td>11h/17d</td></tr> </tbody> </table> 												Status	Default Value		DIVC4:0]	VPC[5:0]	Power On Sequence	0Eh/14d	14h/20d	S/W Reset	0Eh/14d	14h/20d	H/W Reset	0Eh/14d	14h/20d	Status	Default Value		DIVB[4:0]	VPB[5:0]	Power On Sequence	11h/17d	11h/17d	S/W Reset	11h/17d	11h/17d	H/W Reset	11h/17d	11h/17d
Status	Default Value																																							
	DIVC4:0]	VPC[5:0]																																						
Power On Sequence	0Eh/14d	14h/20d																																						
S/W Reset	0Eh/14d	14h/20d																																						
H/W Reset	0Eh/14d	14h/20d																																						
Status	Default Value																																							
	DIVB[4:0]	VPB[5:0]																																						
Power On Sequence	11h/17d	11h/17d																																						
S/W Reset	11h/17d	11h/17d																																						
H/W Reset	11h/17d	11h/17d																																						



14.2.40 Display Inversion Control (B4h)

B4h		Display Inversion Control																																				
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																									
Command	0	1	↑	x	1	0	1	1	0	1	0	0	B4h																									
1 st Parameter	1	1	↑	x	0	0	0	0	0	NLA	NLB	NLC	02H																									
		-Display Inversion mode control -NLA: Inversion setting in full colors normal mode(Normal mode on) <table border="1" style="margin-left: 20px;"> <tr><td>NLA</td><td>Inversion setting in full colors normal mode</td></tr> <tr><td>0</td><td>Line Inversion</td></tr> <tr><td>1</td><td>Frame Inversion</td></tr> </table> -NLB: Inversion setting in Idle mode(Idle mode on) <table border="1" style="margin-left: 20px;"> <tr><td>NLB</td><td>Inversion setting in Idle mode</td></tr> <tr><td>0</td><td>Line Inversion</td></tr> <tr><td>1</td><td>Frame Inversion</td></tr> </table> -NLC: Inversion setting in full colors partial mode(Partial mode on/Idle mode off) <table border="1" style="margin-left: 20px;"> <tr><td>NLC</td><td>Inversion setting in full colors partial mode</td></tr> <tr><td>0</td><td>Line Inversion</td></tr> <tr><td>1</td><td>Frame Inversion</td></tr> </table>													NLA	Inversion setting in full colors normal mode	0	Line Inversion	1	Frame Inversion	NLB	Inversion setting in Idle mode	0	Line Inversion	1	Frame Inversion	NLC	Inversion setting in full colors partial mode	0	Line Inversion	1	Frame Inversion						
NLA	Inversion setting in full colors normal mode																																					
0	Line Inversion																																					
1	Frame Inversion																																					
NLB	Inversion setting in Idle mode																																					
0	Line Inversion																																					
1	Frame Inversion																																					
NLC	Inversion setting in full colors partial mode																																					
0	Line Inversion																																					
1	Frame Inversion																																					
Restriction	If this register not using the register need be reserved.																																					
Register Availability	<table border="1" style="width: 100%;"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr><td>Sleep In</td><td>Yes</td></tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes													
Status	Availability																																					
Normal Mode On, Idle Mode Off, Sleep Out	Yes																																					
Normal Mode On, Idle Mode On, Sleep Out	Yes																																					
Partial Mode On, Idle Mode Off, Sleep Out	Yes																																					
Partial Mode On, Idle Mode On, Sleep Out	Yes																																					
Sleep In	Yes																																					
Default	<table border="1" style="width: 100%;"> <thead> <tr> <th>Status</th> <th colspan="4">Default Value</th></tr> <tr> <th></th> <th>NLA</th> <th>NLB</th> <th>NLC</th> <th>D7-0</th> </tr> </thead> <tbody> <tr><td>Power On Sequence</td><td>0d</td><td>1d</td><td>0d</td><td>02h</td></tr> <tr><td>S/W Reset</td><td>0d</td><td>1d</td><td>0d</td><td>02h</td></tr> <tr><td>H/W Reset</td><td>0d</td><td>1d</td><td>0d</td><td>02h</td></tr> </tbody> </table>													Status	Default Value					NLA	NLB	NLC	D7-0	Power On Sequence	0d	1d	0d	02h	S/W Reset	0d	1d	0d	02h	H/W Reset	0d	1d	0d	02h
Status	Default Value																																					
	NLA	NLB	NLC	D7-0																																		
Power On Sequence	0d	1d	0d	02h																																		
S/W Reset	0d	1d	0d	02h																																		
H/W Reset	0d	1d	0d	02h																																		
Flow Chart	 <p>Legend</p> <ul style="list-style-type: none"> command Parameter Display Action Mode Sequential transfer 																																					

14.2.41 RGB Interface Blanking Porch setting (B5h)

B5h	RGB Interface Blanking Porch setting																																																			
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																							
Command	0	1	↑	x	1	0	1	1	0	1	0	1	1	B5h																																						
1 st Parameter	1	1	↑	x	x	x	HBP5	HBP4	HBP3	HBP2	HBP1	HBP0	08h																																							
2 nd Parameter	1	1	↑	x	VBP7	VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0	03h																																							
3 rd Parameter	1	1	↑	x	x	x	x	x	x	x	VBP9	VBP8	00h																																							
Description	Vertical and Horizontal back porch control when RGB I/F mode2(RCM[1:0]=11) HBP[5:0]: Set the delay period from falling edge of HSYNC signal to first valid data. <table border="1" style="margin-left: auto; margin-right: auto;"> <tr><td>HBP[5:0]</td><td>No.of clock cycle of DOTCLK</td></tr> <tr><td>00d</td><td>2</td></tr> <tr><td>01d</td><td>3</td></tr> <tr><td>02d</td><td>4</td></tr> <tr><td>03d</td><td>5</td></tr> <tr><td>:</td><td>:</td></tr> <tr><td>:</td><td>(STEP1)</td></tr> <tr><td>:</td><td>:</td></tr> <tr><td>62d</td><td>64</td></tr> <tr><td>63d</td><td>65</td></tr> </table> VBP[9:0]: Set the delay period from falling edge of VSYNC signal to first valid line. <table border="1" style="margin-left: auto; margin-right: auto;"> <tr><td>VBP[9:0]</td><td>No. of clock cycle of HSYNC</td></tr> <tr><td>00d</td><td>(invalid)</td></tr> <tr><td>01d</td><td>1</td></tr> <tr><td>02d</td><td>2</td></tr> <tr><td>03d</td><td>3</td></tr> <tr><td>:</td><td>:</td></tr> <tr><td>:</td><td>(STEP1):</td></tr> <tr><td>:</td><td>:</td></tr> <tr><td>1022d</td><td>1022</td></tr> </table>														HBP[5:0]	No.of clock cycle of DOTCLK	00d	2	01d	3	02d	4	03d	5	:	:	:	(STEP1)	:	:	62d	64	63d	65	VBP[9:0]	No. of clock cycle of HSYNC	00d	(invalid)	01d	1	02d	2	03d	3	:	:	:	(STEP1):	:	:	1022d	1022
HBP[5:0]	No.of clock cycle of DOTCLK																																																			
00d	2																																																			
01d	3																																																			
02d	4																																																			
03d	5																																																			
:	:																																																			
:	(STEP1)																																																			
:	:																																																			
62d	64																																																			
63d	65																																																			
VBP[9:0]	No. of clock cycle of HSYNC																																																			
00d	(invalid)																																																			
01d	1																																																			
02d	2																																																			
03d	3																																																			
:	:																																																			
:	(STEP1):																																																			
:	:																																																			
1022d	1022																																																			
Restriction	-																																																			
Register Availability		Status				Availability																																														
		Normal Mode On, Idle Mode Off, Sleep Out						Yes																																												
		Normal Mode On, Idle Mode On, Sleep Out						Yes																																												
		Partial Mode On, Idle Mode Off, Sleep Out						Yes																																												
		Partial Mode On, Idle Mode On, Sleep Out						Yes																																												
		Sleep In						Yes																																												

	Status	Default Value	
		HBP[5:0]	VBP[9:0]
Default	Power On Sequence	08h	03h
	S/W Reset	08h	03h
	H/W Reset	08h	03h

Flow Chart	BPCTR(B5h)	Legend					
		command	Parameter	Display	Action	Mode	Sequential transfer

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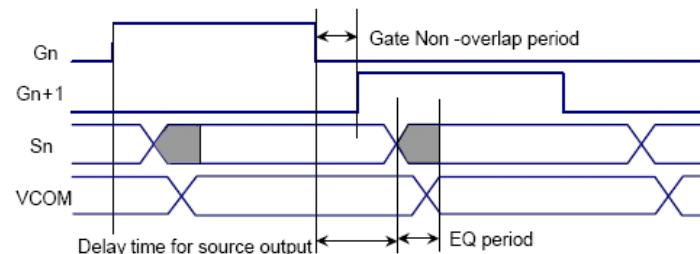
graph TD
    A[BPCTR(B5h)] --> B{ }
    B --> C["1st parameter: HBP[5:0]"]
    B --> D["2nd parameter: VBP[5:0]"]
    B --> E["3rd parameter: VBP[9:8]"]

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1st parameter: HBP[5:0]
2nd parameter: VBP[5:0]
3rd parameter: VBP[9:8]

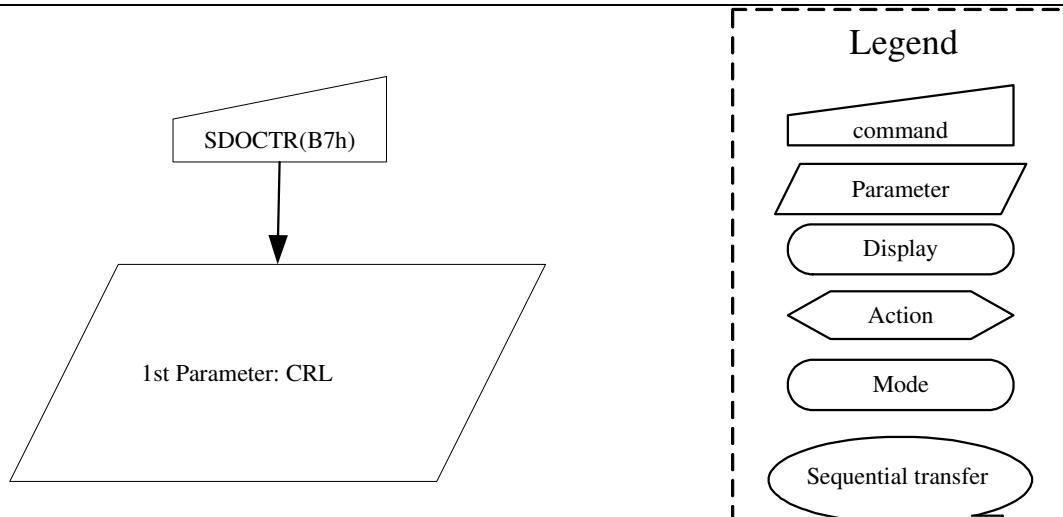
14.2.43 Display Function set 5 (B6h)

RGB Interface Blanking Porch setting																																																																							
B6h	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																										
Command	0	1	↑	x	1	0	1	1	0	1	1	0	B6h																																																										
1 st	1	1	↑	x	0	0	NO1	NO0	SDT1	SDT0	EQ1	EQ2	07h																																																										
2 nd	1	1	↑	x	0	0	0	0	0	PTG0	PT1	PT0	02h																																																										
Description	<p>-1st parameter: Set output waveform relation.</p> <p>-NO[1:0]: Set the amount for non-overlap of the gate output</p> <table border="1"> <thead> <tr> <th colspan="2" rowspan="2">NO[1:0]</th> <th>Amount of non-overlap of the gate output</th> </tr> <tr> <th>Refer the Internal oscillator</th> </tr> </thead> <tbody> <tr> <td>00</td><td>0</td><td>4 clock cycle</td></tr> <tr> <td>01</td><td>1</td><td>5 clock cycle</td></tr> <tr> <td>10</td><td>2</td><td>6 clock cycle</td></tr> <tr> <td>11</td><td>3</td><td>7 clock cycle</td></tr> </tbody> </table> <p>-SDT[1:0]: Set delay amount from gate signal falling edge to the source output.</p> <table border="1"> <thead> <tr> <th colspan="2" rowspan="2">SDT[1:0]</th> <th>Amount of non-overlap of the source output</th> </tr> <tr> <th>Refer the Internal oscillator</th> </tr> </thead> <tbody> <tr> <td>00</td><td>0</td><td>4 clock cycle</td></tr> <tr> <td>01</td><td>1</td><td>4 clock cycle</td></tr> <tr> <td>10</td><td>2</td><td>4.5 clock cycle</td></tr> <tr> <td>11</td><td>3</td><td>5.5 clock cycle</td></tr> </tbody> </table> <p>-EQ[1:0]: Set the Equalizing period.</p> <table border="1"> <thead> <tr> <th colspan="2" rowspan="2">EQ[1:0]</th> <th>EQ period</th> </tr> <tr> <th>Refer the Internal oscillator</th> </tr> </thead> <tbody> <tr> <td>00</td><td>0</td><td>No EQ</td></tr> <tr> <td>01</td><td>1</td><td>0.5 clock cycle</td></tr> <tr> <td>10</td><td>2</td><td>1 clock cycle</td></tr> <tr> <td>11</td><td>3</td><td>1.5 clock cycle</td></tr> </tbody> </table> <p>-2nd parameter: Set the output waveform in non-display area.</p> <p>-PTG[0]: Determine gate output in a non-display area in the partial mode.</p> <table border="1"> <thead> <tr> <th colspan="2">PTG[0]</th> <th>Gate output in a non-display area</th> </tr> </thead> <tbody> <tr> <td>0</td><td>0</td><td>Normal scan</td></tr> <tr> <td>1</td><td>1</td><td>Fix on VGL</td></tr> </tbody> </table>														NO[1:0]		Amount of non-overlap of the gate output	Refer the Internal oscillator	00	0	4 clock cycle	01	1	5 clock cycle	10	2	6 clock cycle	11	3	7 clock cycle	SDT[1:0]		Amount of non-overlap of the source output	Refer the Internal oscillator	00	0	4 clock cycle	01	1	4 clock cycle	10	2	4.5 clock cycle	11	3	5.5 clock cycle	EQ[1:0]		EQ period	Refer the Internal oscillator	00	0	No EQ	01	1	0.5 clock cycle	10	2	1 clock cycle	11	3	1.5 clock cycle	PTG[0]		Gate output in a non-display area	0	0	Normal scan	1	1	Fix on VGL
NO[1:0]		Amount of non-overlap of the gate output																																																																					
		Refer the Internal oscillator																																																																					
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EQ[1:0]		EQ period																																																																					
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00	0	No EQ																																																																					
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0	0	Normal scan																																																																					
1	1	Fix on VGL																																																																					

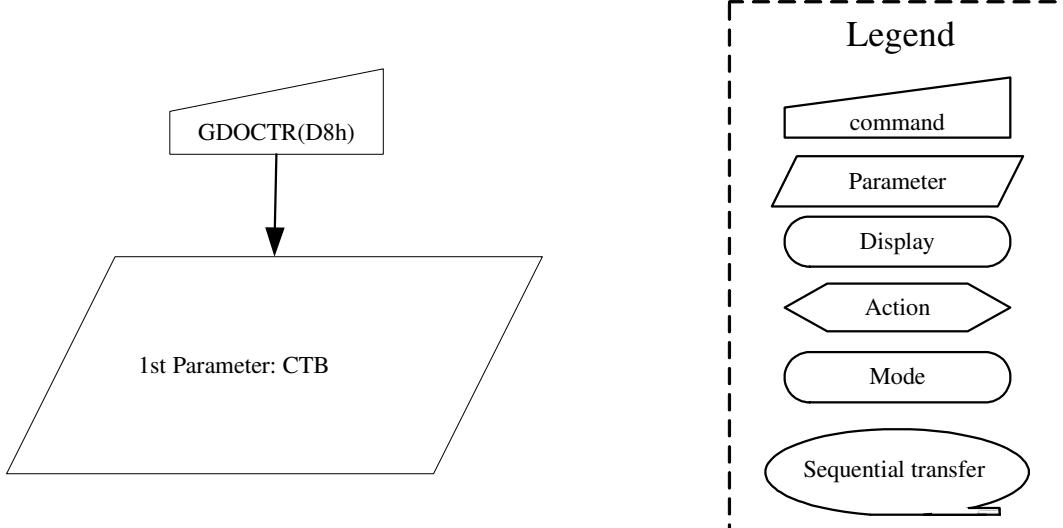


	<p>-PT[1:0]: Determine Source/VCOM output in a non-display area in the partial mode</p> <table border="1"> <thead> <tr> <th colspan="2" rowspan="2">PT[1:0]</th><th colspan="2">Source output on non-display area</th><th colspan="2">VCOM output on non-display area</th></tr> <tr> <th>Positive</th><th>Negative</th><th>Positive</th><th>Negative</th></tr> </thead> <tbody> <tr> <td>00</td><td>0</td><td>V63</td><td>V0</td><td>VCOMH</td><td>VCOML</td></tr> <tr> <td>01</td><td>1</td><td>V0</td><td>V63</td><td>VCOMH</td><td>VCOML</td></tr> <tr> <td>10</td><td>2</td><td>AGND</td><td>AGND</td><td>AGND</td><td>AGND</td></tr> <tr> <td>11</td><td>3</td><td>Hi-z</td><td>Hi-z</td><td>AGND</td><td>AGND</td></tr> </tbody> </table>						PT[1:0]		Source output on non-display area		VCOM output on non-display area		Positive	Negative	Positive	Negative	00	0	V63	V0	VCOMH	VCOML	01	1	V0	V63	VCOMH	VCOML	10	2	AGND	AGND	AGND	AGND	11	3	Hi-z	Hi-z	AGND	AGND
PT[1:0]		Source output on non-display area		VCOM output on non-display area																																				
		Positive	Negative	Positive	Negative																																			
00	0	V63	V0	VCOMH	VCOML																																			
01	1	V0	V63	VCOMH	VCOML																																			
10	2	AGND	AGND	AGND	AGND																																			
11	3	Hi-z	Hi-z	AGND	AGND																																			
Restriction	If this register not using the register need be reserved.																																							
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>						Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes																						
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Status	Default Value																																							
	NO[1:0]	STD[1:0]	EQ[1:0]	PTG[1:0]	PT[1:0]																																			
Power On Sequence	0d	1d	2d	0d	2d																																			
S/W Reset	0d	1d	2d	0d	2d																																			
H/W Reset	0d	1d	2d	0d	2d																																			
Flow Chart	<p>Legend</p> <ul style="list-style-type: none"> command Parameter Display Action Mode Sequential transfer 																																							

14.2.42 Source Driver Direction Control (B7h)

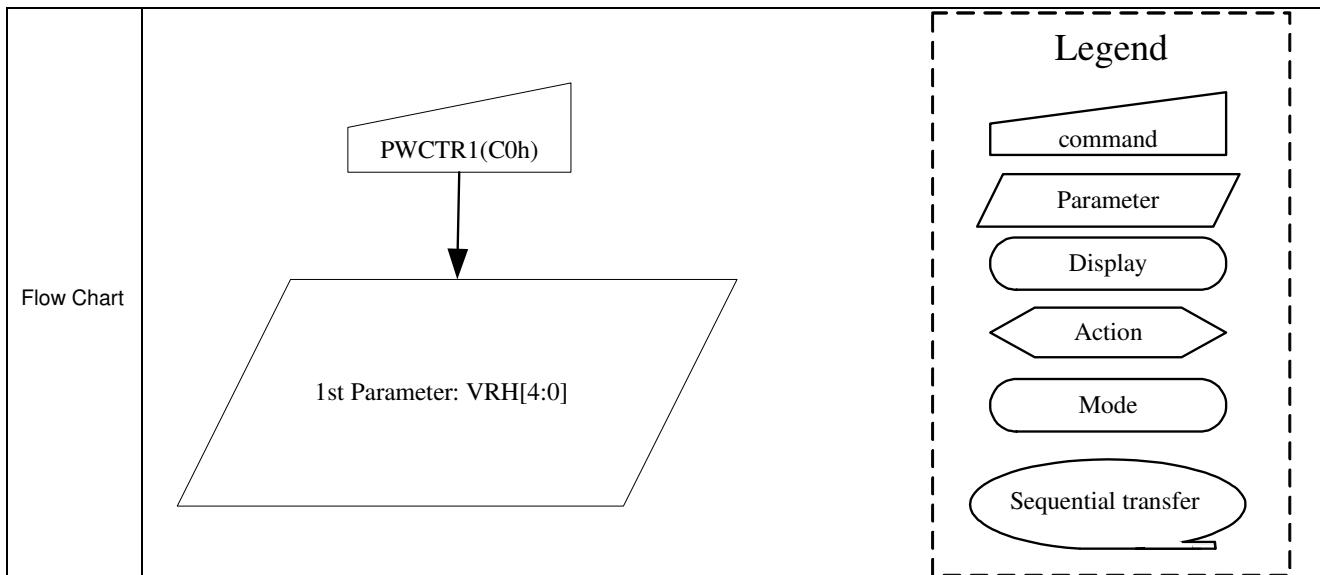
B7h	Display Inversion Control																																						
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																										
Command	0	1	↑	x	1	0	1	1	0	1	1	1	B7h																										
1 st Parameter	1	1	↑	x	0	0	0	0	0	0	0	CRL	00h																										
Description	-CRL: Source output direction select register <table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <th rowspan="2">CRL</th> <th colspan="6">Module source output direction</th> </tr> <tr> <th>GM='101'</th> <th>GM='100'</th> <th>GM='011'</th> <th>GM='010'</th> <th>GM='001'</th> <th>GM='000'</th> </tr> <tr> <td>0</td> <td>S1 -> S396</td> <td>S7 -> S396</td> <td>S7 -> S390</td> <td>S7 -> S366</td> <td>S7 -> S390</td> <td>S1 -> S396</td> </tr> <tr> <td>1</td> <td>S1 -> S396</td> <td>S396 -> S7</td> <td>S390 ->S7</td> <td>S366 -> S7</td> <td>S390 -> S7</td> <td>S396 -> S1</td> </tr> </table>												CRL	Module source output direction						GM='101'	GM='100'	GM='011'	GM='010'	GM='001'	GM='000'	0	S1 -> S396	S7 -> S396	S7 -> S390	S7 -> S366	S7 -> S390	S1 -> S396	1	S1 -> S396	S396 -> S7	S390 ->S7	S366 -> S7	S390 -> S7	S396 -> S1
CRL	Module source output direction																																						
	GM='101'	GM='100'	GM='011'	GM='010'	GM='001'	GM='000'																																	
0	S1 -> S396	S7 -> S396	S7 -> S390	S7 -> S366	S7 -> S390	S1 -> S396																																	
1	S1 -> S396	S396 -> S7	S390 ->S7	S366 -> S7	S390 -> S7	S396 -> S1																																	
Restriction	If this register not using the register need be reserved.																																						
Register Availability	<table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <th>Status</th> <th>Availability</th> </tr> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </table>												Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes															
Status	Availability																																						
Normal Mode On, Idle Mode Off, Sleep Out	Yes																																						
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Sleep In	Yes																																						
Default	<table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <th rowspan="2">Status</th> <th>Default Value</th> </tr> <tr> <th>CRL</th> </tr> <tr> <td>Power On Sequence</td> <td>0d</td> </tr> <tr> <td>S/W Reset</td> <td>0d</td> </tr> <tr> <td>H/W Reset</td> <td>0d</td> </tr> </table>												Status	Default Value	CRL	Power On Sequence	0d	S/W Reset	0d	H/W Reset	0d																		
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	CRL																																						
Power On Sequence	0d																																						
S/W Reset	0d																																						
H/W Reset	0d																																						
Flow Chart	 <p>The flowchart starts with a rectangle labeled "SDOCTR(B7h)" with an arrow pointing down to a trapezoid labeled "1st Parameter: CRL". To the right of the trapezoid is a legend enclosed in a dashed box. The legend contains six items: "command" (rectangle), "Parameter" (trapezoid), "Display" (oval), "Action" (diamond), "Mode" (trapezoid), and "Sequential transfer" (oval).</p>																																						

14.2.43 Gate Driver Direction Control (B8h)

Display Inversion Control																																					
B8h	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																								
Command	0	1	↑	x	1	0	1	1	1	0	0	0	B8h																								
1 st Parameter	1	1	↑	x	0	0	0	0	0	0	0	CTB	00h																								
Description	-CTB: Gate output direction select register																																				
	<table border="1"> <thead> <tr> <th colspan="6">Module gate output direction</th> </tr> <tr> <th>CTB</th> <th>GM='101'</th> <th>GM='100'</th> <th>GM='011','010'</th> <th>GM='011'</th> <th>GM='000'</th> </tr> </thead> <tbody> <tr> <td>0</td><td>G2 -> G133</td><td>G2 -> G131</td><td>G2 -> G161</td><td>G2 -> G129</td><td>G1 -> G162</td></tr> <tr> <td>1</td><td>G133 -> G2</td><td>G131 -> G2</td><td>G161 ->G2</td><td>G129 -> G2</td><td>G162 -> G1</td></tr> </tbody> </table>													Module gate output direction						CTB	GM='101'	GM='100'	GM='011','010'	GM='011'	GM='000'	0	G2 -> G133	G2 -> G131	G2 -> G161	G2 -> G129	G1 -> G162	1	G133 -> G2	G131 -> G2	G161 ->G2	G129 -> G2	G162 -> G1
Module gate output direction																																					
CTB	GM='101'	GM='100'	GM='011','010'	GM='011'	GM='000'																																
0	G2 -> G133	G2 -> G131	G2 -> G161	G2 -> G129	G1 -> G162																																
1	G133 -> G2	G131 -> G2	G161 ->G2	G129 -> G2	G162 -> G1																																
Restriction	If this register not using the register need be reserved.																																				
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes												
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Sleep In	Yes																																				
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> <tr> <th colspan="2">CRL</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>0d</td></tr> <tr> <td>S/W Reset</td><td>0d</td></tr> <tr> <td>H/W Reset</td><td>0d</td></tr> </tbody> </table>													Status	Default Value	CRL		Power On Sequence	0d	S/W Reset	0d	H/W Reset	0d														
Status	Default Value																																				
CRL																																					
Power On Sequence	0d																																				
S/W Reset	0d																																				
H/W Reset	0d																																				
Flow Chart	 <p>Legend</p> <ul style="list-style-type: none"> command Parameter Display Action Mode Sequential transfer 																																				

14.2.44 Power_Control1 (C0h)

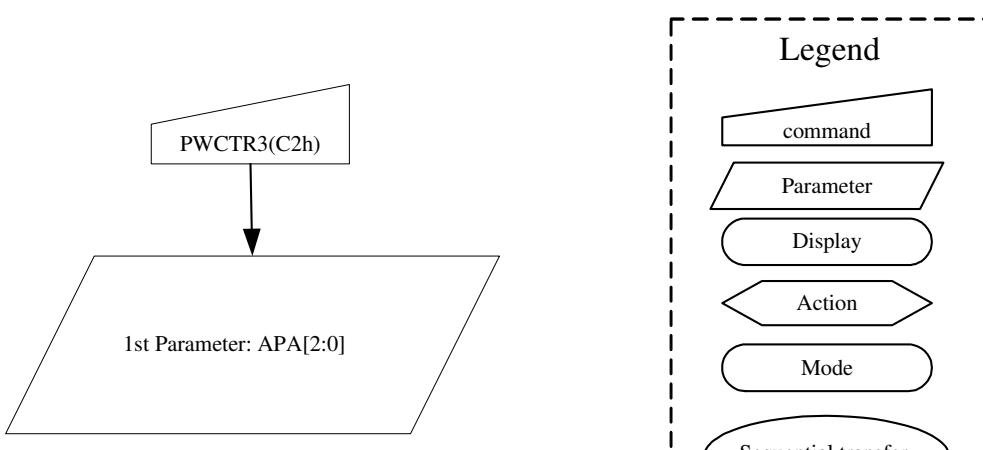
Power_Control1																											
C0H	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX														
Command	0	1	↑	x	1	1	0	0	0	0	0	0	C0h														
1 st Parameter	1	1	↑	x	0	0	0	VRH4	VRH3	VRH2	VRH1	VRH0	x														
2 nd Parameter	1	1	↑	x	0	0	0	0	0	VC2	VC1	VC0	02h														
Description	Set the GVDD and voltage																										
Description	VRH[4:0]		GVDD		VC[2:0]		VCI1		VC[2:0]		VCI1																
	00000	0	5.00	000	0	2.75	000	0	2.75	000	0	2.75															
	00001	1	4.75	001	1	2.70	001	1	2.70	001	1	2.70															
	00010	2	4.70	010	2	2.65	010	2	2.65	010	2	2.65															
	00011	3	4.65	011	3	2.60	011	3	2.60	011	3	2.60															
	00100	4	4.60	100	4	2.55	100	4	2.55	100	4	2.55															
	00101	5	4.55	101	5	2.50	101	5	2.50	101	5	2.50															
	00110	6	4.50	110	6	2.45	110	6	2.45	110	6	2.45															
	00111	7	4.45	111	7	2.40	111	7	2.40	111	7	2.40															
	01000	8	4.40																								
	01001	9	4.35																								
	01010	10	4.30																								
	01011	11	4.25																								
	01100	12	4.20																								
	01101	13	4.15																								
	01110	14	4.10																								
	01111	15	4.05																								
	10000	16	4.00																								
	10001	17	3.95																								
	10010	18	3.90																								
	10011	19	3.85																								
	10100	20	3.80																								
	10101	21	3.75																								
	10110	22	3.70																								
	10111	23	3.65																								
	11000	24	3.60																								
	11001	25	3.55																								
	11010	26	3.50																								
	11011	27	3.45																								
	11100	28	3.40																								
	11101	29	3.35																								
	11110	30	3.25																								
	11111	31	3.00																								
Restriction																											
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes		
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Partial Mode On, Idle Mode Off, Sleep Out	Yes																										
Partial Mode On, Idle Mode On, Sleep Out	Yes																										
Sleep In	Yes																										
Default	<table border="1"> <thead> <tr> <th rowspan="2">Status</th> <th colspan="2">Default Value</th> </tr> <tr> <th>VRH[4:0]</th> <th>VC[2:0]</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>10d</td> <td>5d</td> </tr> <tr> <td>SW Reset</td> <td>10d</td> <td>5d</td> </tr> <tr> <td>HW Reset</td> <td>10d</td> <td>5d</td> </tr> </tbody> </table>													Status	Default Value		VRH[4:0]	VC[2:0]	Power On Sequence	10d	5d	SW Reset	10d	5d	HW Reset	10d	5d
Status	Default Value																										
	VRH[4:0]	VC[2:0]																									
Power On Sequence	10d	5d																									
SW Reset	10d	5d																									
HW Reset	10d	5d																									



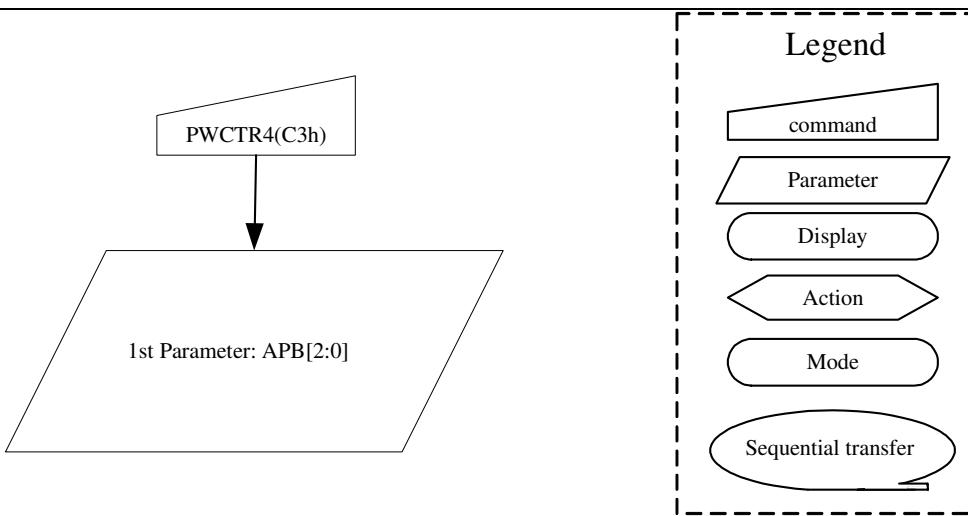
14.2.45 Power_Control2 (C1h)

C1H		Power_Control 2																																																																												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																																	
Command	0	1	↑	x	1	1	0	0	0	0	0	1	C1h																																																																	
1 st Parameter	1	1	↑	x	0	0	0	0	0	BT2	BT1	BT0	05h																																																																	
Description	Set the AVDD, VCL, VGH and VGL supply power level.																																																																													
	<table border="1"> <thead> <tr> <th colspan="3">BT[2:0]</th><th>AVDD</th><th>VCL</th><th>VGH</th><th>VGL</th><th colspan="6"></th></tr> </thead> <tbody> <tr> <td>010</td><td>2</td><td>2xVCI</td><td>-1xVCI1</td><td>2.5xAVDD</td><td>-2.5xAVDD</td><td></td><td colspan="6"></td></tr> <tr> <td>011</td><td>3</td><td>2xVCI</td><td>-1xVCI1</td><td>3xAVDD</td><td>-2.5xAVDD</td><td></td><td colspan="6"></td></tr> <tr> <td>100</td><td>4</td><td>2xVCI</td><td>-1xVCI1</td><td>2.5xAVDD</td><td>-3xAVDD</td><td></td><td colspan="6"></td></tr> <tr> <td>101</td><td>5</td><td>2xVCI</td><td>-1xVCI1</td><td>3xAVDD</td><td>-3xAVDD</td><td></td><td colspan="6" rowspan="3"></td></tr> </tbody> </table>													BT[2:0]			AVDD	VCL	VGH	VGL							010	2	2xVCI	-1xVCI1	2.5xAVDD	-2.5xAVDD								011	3	2xVCI	-1xVCI1	3xAVDD	-2.5xAVDD								100	4	2xVCI	-1xVCI1	2.5xAVDD	-3xAVDD								101	5	2xVCI	-1xVCI1	3xAVDD	-3xAVDD							
BT[2:0]			AVDD	VCL	VGH	VGL																																																																								
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011	3	2xVCI	-1xVCI1	3xAVDD	-2.5xAVDD																																																																									
100	4	2xVCI	-1xVCI1	2.5xAVDD	-3xAVDD																																																																									
101	5	2xVCI	-1xVCI1	3xAVDD	-3xAVDD																																																																									
Restriction	If this register not using the register need be reserved. The deviation value of VGH/VGL between with Measurement and Specification VGH-VGL <= 32V																																																																													
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Flow Chart	<pre> graph TD PWCTR2["PWCTR2(C1h)"] --> BT[2:0] subgraph Legend [Legend] direction TB C[command] P[Parameter] D[Display] A[Action] M[Mode] ST[Sequential transfer] end </pre> <p>The flowchart starts with a rectangle labeled "PWCTR2(C1h)". An arrow points down to a parallelogram labeled "1st Parameter: BT[2:0]". To the right of the flowchart is a legend enclosed in a dashed box. The legend contains six items: "command" (a triangle pointing down), "Parameter" (an elongated oval), "Display" (an oval), "Action" (a diamond), "Mode" (an oval), and "Sequential transfer" (an oval with a curved arrow).</p>																																																																													

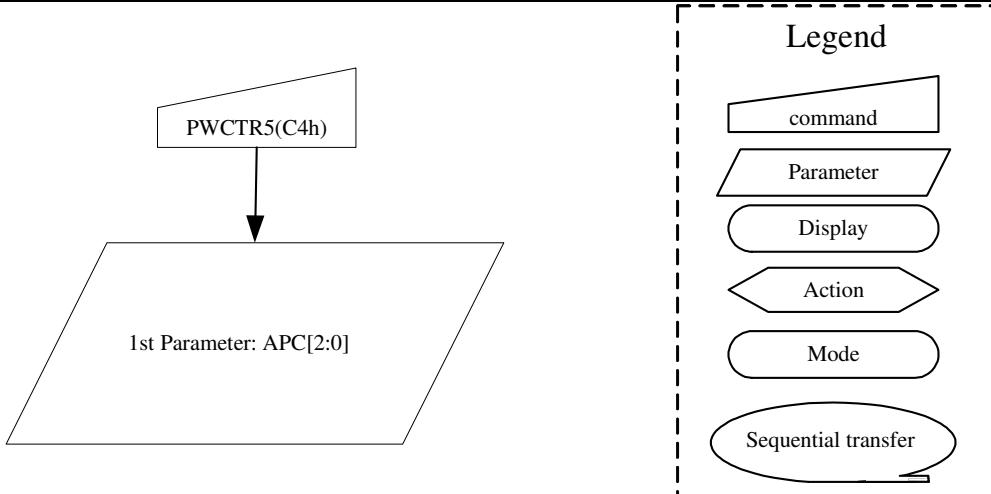
14.2.46 Power_Control 3 (C2h)

C2H	Power_Control 3																																							
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																											
Command	0	1	↑	x	1	1	0	0	0	0	1	0	C2h																											
1 st Parameter	1	1	↑	x	0	0	0	0	0	APA2	APA1	APA0	00h																											
	Set the amount of current in Operation amplifier in normal mode/full colors. Adjust the amount of fixed current from the fixed current sources in the operational amplifier for the source driver.																																							
Description	<table border="1"> <thead> <tr> <th colspan="2">APA[2:0]</th> <th>Amount of Current in Operational Amplifier</th> </tr> </thead> <tbody> <tr> <td>000</td><td>0</td><td>Least</td></tr> <tr> <td>001</td><td>1</td><td>Small</td></tr> <tr> <td>010</td><td>2</td><td>Medium Low</td></tr> <tr> <td>011</td><td>3</td><td>Medium</td></tr> <tr> <td>100</td><td>4</td><td>Medium High</td></tr> <tr> <td>101</td><td>5</td><td>Large</td></tr> <tr> <td>110</td><td>6</td><td>Reserved</td></tr> <tr> <td>111</td><td>7</td><td>Reserved</td></tr> </tbody> </table>													APA[2:0]		Amount of Current in Operational Amplifier	000	0	Least	001	1	Small	010	2	Medium Low	011	3	Medium	100	4	Medium High	101	5	Large	110	6	Reserved	111	7	Reserved
APA[2:0]		Amount of Current in Operational Amplifier																																						
000	0	Least																																						
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Restriction	If some parameter of the register is not use the register need to be reserved.																																							
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Power On Sequence	0d																																							
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Flow Chart	 <p>Legend</p> <ul style="list-style-type: none"> command Parameter Display Action Mode Sequential transfer 																																							

14.2.47 Power_Control 4 (C3h)

C3H	Power_Control 4(in Idle mode / 8 colors)																																							
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																											
Command	0	1	↑	x	1	1	0	0	0	0	1	1	C3h																											
1 st Parameter	1	1	↑	x	0	0	0	0	0	APB2	APB1	APB0	00h																											
Description	Set the amount of current in Operational amplifier in Idle mode/8-colors Adjust the amount of fixed current from the fixed current source in the operational amplifier for the source driver. <table border="1"> <thead> <tr> <th colspan="2">APB[2:0]</th> <th>Amount of Current in Operational Amplifier</th> </tr> </thead> <tbody> <tr> <td>000</td> <td>0</td> <td>Least</td> </tr> <tr> <td>001</td> <td>1</td> <td>Small</td> </tr> <tr> <td>010</td> <td>2</td> <td>Medium Low</td> </tr> <tr> <td>011</td> <td>3</td> <td>Medium</td> </tr> <tr> <td>100</td> <td>4</td> <td>Medium High</td> </tr> <tr> <td>101</td> <td>5</td> <td>Large</td> </tr> <tr> <td>110</td> <td>6</td> <td>Reserved</td> </tr> <tr> <td>111</td> <td>7</td> <td>Reserved</td> </tr> </tbody> </table>													APB[2:0]		Amount of Current in Operational Amplifier	000	0	Least	001	1	Small	010	2	Medium Low	011	3	Medium	100	4	Medium High	101	5	Large	110	6	Reserved	111	7	Reserved
APB[2:0]		Amount of Current in Operational Amplifier																																						
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Flow Chart	 <p>Legend</p> <ul style="list-style-type: none"> command Parameter Display Action Mode Sequential transfer 																																							

14.2.48 Power_Control 5 (C4h)

Power_Control_5(in Partial mode/full mode)																															
C4H	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																		
Command	0	1	↑	x	1	1	0	0	0	1	0	0	C4h																		
1 st Parameter	1	1	↑	x	0	0	0	0	0	APC2	APC1	APC1	01h																		
Set the amount of current in Operational amplifier in Partial mode/full-colors Adjust the amount of fixed current from the fixed current source in the operational amplifier for the source driver.																															
Description	<table border="1"> <thead> <tr> <th>APC[2:0]</th> <th>Amount of Current in Operational Amplifier</th> </tr> </thead> <tbody> <tr> <td>000</td> <td>Least</td> </tr> <tr> <td>001</td> <td>Small</td> </tr> <tr> <td>010</td> <td>Medium Low</td> </tr> <tr> <td>011</td> <td>Medium</td> </tr> <tr> <td>100</td> <td>Medium High</td> </tr> <tr> <td>101</td> <td>Large</td> </tr> <tr> <td>110</td> <td>Reserved</td> </tr> <tr> <td>111</td> <td>Reserved</td> </tr> </tbody> </table>													APC[2:0]	Amount of Current in Operational Amplifier	000	Least	001	Small	010	Medium Low	011	Medium	100	Medium High	101	Large	110	Reserved	111	Reserved
APC[2:0]	Amount of Current in Operational Amplifier																														
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Status	Availability																														
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Flow Chart	 <p>Legend</p> <ul style="list-style-type: none"> command Parameter Display Action Mode Sequential transfer 																														

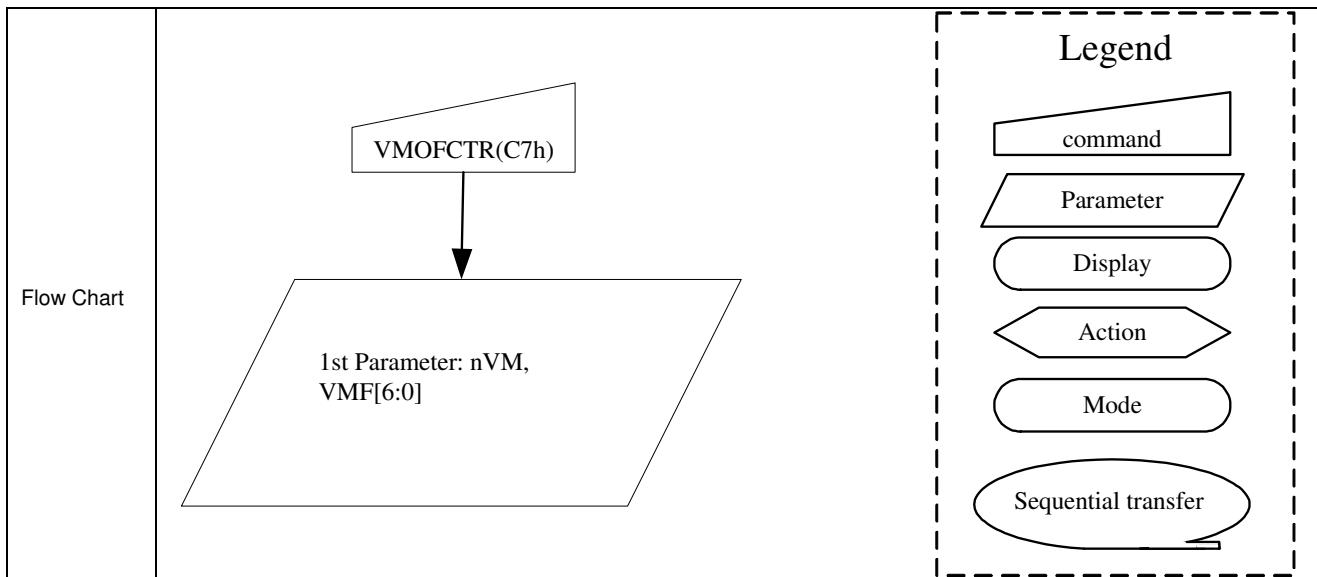
14.2.49 VCOM_Control 1 (C5h)

C5H	VCOM_Control1												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	1	1	0	0	0	1	0	1	C5h
1 st Parameter	1	1	↑	x	x	VMH6	VMH5	VMH4	VMH3	VMH2	VMH1	VMH0	-
2 nd Parameter	1	1	↑	x	0	VML6	VML5	VML4	VML3	VML2	VML1	VML0	-
Set VCOMH Voltage	VMH[6:0] VCOMH VMH[6:0] VCOMH VMH[6:0] VCOMH VMH[6:0] VCOMH												
	0000000 0	2.500	0011011 27	3.175	0110110 54	3.850	1010001 81	4.525					
	0000001 1	2.525	0011100 28	3.200	0110111 55	3.875	1010010 82	4.550					
	0000010 2	2.550	0011101 29	3.225	0110000 56	3.900	1010011 83	4.575					
	0000011 3	2.575	0011110 30	3.250	0110001 57	3.925	1010100 84	4.600					
	00000100 4	2.600	0011111 31	3.275	0110110 58	3.950	1010101 85	4.625					
	00000101 5	2.625	0100000 32	3.300	0110111 59	3.975	1010110 86	4.650					
	00000110 6	2.650	0100001 33	3.325	0111000 60	4.000	1010111 87	4.675					
	00000111 7	2.675	0100010 34	3.350	0111001 61	4.025	1011000 88	4.700					
	0001000 8	2.700	0100011 35	3.375	0111110 62	4.050	1011001 89	4.725					
	0001001 9	2.725	0100100 36	3.400	0111111 63	4.075	1011010 90	4.750					
	0001010 10	2.750	0100101 37	3.425	1000000 64	4.100	1011011 91	4.775					
	0001011 11	2.775	0100110 38	3.450	1000001 65	4.125	1011100 92	4.800					
	0001100 12	2.800	0100111 39	3.475	1000010 66	4.150	1011101 93	4.825					
	0001101 13	2.825	0101000 40	3.500	1000011 67	4.175	1011110 94	4.850					
	0001110 14	2.850	0101001 41	3.525	1000100 68	4.200	1011111 95	4.875					
	0001111 15	2.875	0101010 42	3.550	1000101 69	4.225	1100000 96	4.900					
	0010000 16	2.900	0101011 43	3.575	1000110 70	4.250	1100001 97	4.925					
	0010001 17	2.925	0101100 44	3.600	1000111 71	4.275	1100010 98	4.950					
	0010010 18	2.950	0101101 45	3.625	1001000 72	4.300	1100011 99	4.975					
	0010011 19	2.975	0101110 46	3.650	1001001 73	4.325	1100100 100	5.000					
	0010100 20	3.000	0101111 47	3.675	1001010 74	4.350	1100101 101						
	0010101 21	3.025	0110000 48	3.700	1001011 75	4.375							Not Permitted
	0010110 22	3.050	0110001 49	3.725	1001100 76	4.400	0111111 127						
	0010111 23	3.075	0110010 50	3.750	1001101 77	4.425							
	0011000 24	3.100	0110011 51	3.775	1001110 78	4.450							
	0011001 25	3.125	0110100 52	3.800	1001111 79	4.475							
	0011010 26	3.150	0110101 53	3.825	1010000 80	4.500							
Description	-Set VCOML Voltage												
	VML[6:0] VCOML VML[6:0] VCOML VML[6:0] VCOML VML[6:0] VCOML												
	0000000 0	-2.500	0011011 27	-1.825	0110110 54	-1.150	1010001 81	-0.475					
	0000001 1	-2.475	0011100 28	-1.800	0110111 55	-1.125	1010010 82	-0.450					
	0000010 2	-2.450	0011101 29	-1.775	0111000 56	-1.100	1010011 83	-0.425					
	0000011 3	-2.425	0011110 30	-1.750	0111001 57	-1.075	1010100 84	-0.400					
	00000100 4	-2.400	0011111 31	-1.725	0111010 58	-1.050	1010101 85	-0.375					
	00000101 5	-2.375	0100000 32	-1.700	0111011 59	-1.025	1010110 86	-0.350					
	00000110 6	-2.350	0100001 33	-1.675	0111100 60	-1.000	1010111 87	-0.325					
	00000111 7	-2.325	0100010 34	-1.650	0111101 61	-0.975	1011000 88	-0.300					
	00000100 8	-2.300	0100011 35	-1.625	0111110 62	-0.950	1011001 89	-0.275					
	00000101 9	-2.275	0100100 36	-1.600	0111111 63	-0.925	1011010 90	-0.250					
	00000102 10	-2.250	0100101 37	-1.575	1000000 64	-0.900	1011011 91	-0.225					
	00000103 11	-2.225	0100110 38	-1.550	1000001 65	-0.875	1011100 92	-0.200					
	00000104 12	-2.200	0100111 39	-1.525	1000010 66	-0.850	1011101 93	-0.175					
	00000105 13	-2.175	0101000 40	-1.500	1000011 67	-0.825	1011110 94	-0.150					
	00000106 14	-2.150	0101001 41	-1.475	1000100 68	-0.800	1011111 95	-0.125					
	00000107 15	-2.125	0101010 42	-1.450	1000101 69	-0.775	1100000 96	-0.100					
	00000108 16	-2.100	0101011 43	-1.425	1000110 70	-0.750	1100001 97	-0.075					
	00000109 17	-2.075	0101100 44	-1.400	1000111 71	-0.725	1100010 98	-0.050					
	00000110 18	-2.050	0101101 45	-1.375	1001000 72	-0.700	1100011 99	-0.025					
	00000111 19	-2.025	0101110 46	-1.350	1001001 73	-0.675	1100100 100	0.000					
	00000112 20	-2.000	0101111 47	-1.325	1001010 74	-0.650	1100101 101						
	00000113 21	-1.975	0110000 48	-1.300	1001011 75	-0.625							Not Permitted
	00000114 22	-1.950	0110001 49	-1.275	1001100 76	-0.600	1111111 127						
	00000115 23	-1.925	0110010 50	-1.250	1001101 77	-0.575							
	00000116 24	-1.900	0110011 51	-1.225	1001110 78	-0.550							
	00000117 25	-1.875	0110100 52	-1.200	1001111 79	-0.525							
	00000118 26	-1.850	0110101 53	-1.175	1010000 80	-0.500							
Restriction	-If this register not using the register need be reserved. -The VCOM amplitude: VCOMH-VCOML <=5.5V -The deviation value of VCOMH/VCOML between with Measurement and Specification: Max <=25mV -The deviation value of VCOMAC between with Measurement and Specification: Max <= 50mV												

Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th colspan="2">Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td colspan="2">Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td colspan="2">Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td colspan="2">Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td colspan="2">Yes</td></tr> <tr> <td>Sleep In</td><td colspan="2" rowspan="6">Yes</td></tr> </tbody> </table>		Status	Availability		Normal Mode On, Idle Mode Off, Sleep Out	Yes		Normal Mode On, Idle Mode On, Sleep Out	Yes		Partial Mode On, Idle Mode Off, Sleep Out	Yes		Partial Mode On, Idle Mode On, Sleep Out	Yes		Sleep In	Yes		
Status	Availability																				
Normal Mode On, Idle Mode Off, Sleep Out	Yes																				
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Default	<table border="1"> <thead> <tr> <th rowspan="2">Status</th> <th colspan="3">Default Value</th> </tr> <tr> <th>nVM</th> <th>VMH[6:0]</th> <th>VML[6:0]</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>0d</td> <td>67d</td> <td>77d</td> </tr> <tr> <td>SW Reset</td> <td>0d</td> <td>67d</td> <td>77d</td> </tr> <tr> <td>HW Reset</td> <td>0d</td> <td>67d</td> <td>77d</td> </tr> </tbody> </table>		Status	Default Value			nVM	VMH[6:0]	VML[6:0]	Power On Sequence	0d	67d	77d	SW Reset	0d	67d	77d	HW Reset	0d	67d	77d
Status	Default Value																				
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Power On Sequence	0d	67d	77d																		
SW Reset	0d	67d	77d																		
HW Reset	0d	67d	77d																		
Flow Chart	<pre> graph TD A[VMCTR(C5h)] --> B{ } B --> C["1st Parameter: VMH[6:0]"] B --> D["2nd Parameter: VML[6:0]"] </pre>	Legend <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 																			

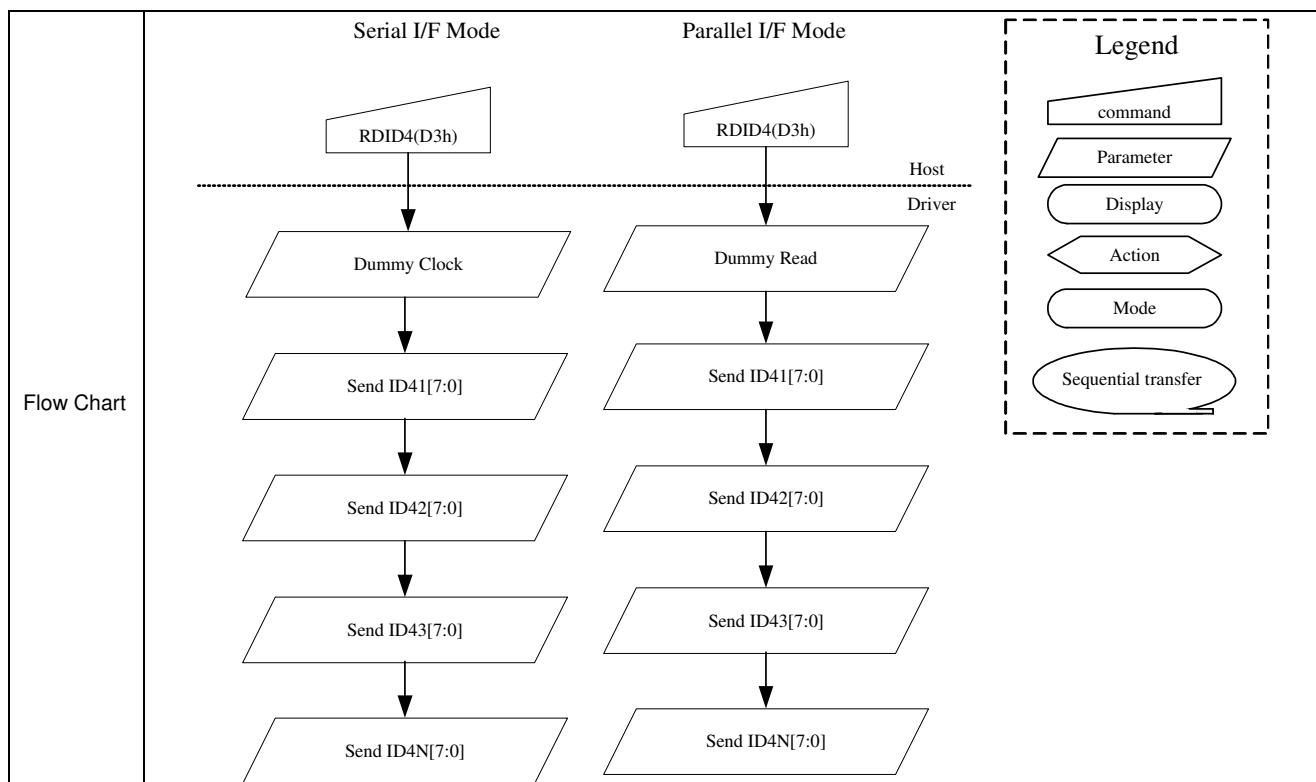
14.2.51 VCOM Offset Control (C7h)

VCOM Offset Control																																																										
C7H	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																													
Command	0	1	↑	x	1	1	0	0	0	1	1	1	C7h																																													
1 st Parameter	1	1	↑	0	nVM*	VMF6	VMF5	VMF4	VMF3	VMF2	VMF1	VMF0	40h																																													
Description	-Set VCOMH Voltage <table border="1"> <thead> <tr> <th>VMF[6:0]</th> <th>VCOMH Output</th> <th>VCOML Output Level</th> </tr> </thead> <tbody> <tr><td>0</td><td>"VMH"</td><td>"VML"</td></tr> <tr><td>1</td><td>"VMH"-63d</td><td>"VML"-63d</td></tr> <tr><td>2</td><td>"VMH"-62d</td><td>"VML"-62d</td></tr> <tr><td>:</td><td>:</td><td>:</td></tr> <tr><td>62</td><td>"VMH"-2d</td><td>"VML"-2d</td></tr> <tr><td>63</td><td>"VMH"-1d</td><td>"VML"-1d</td></tr> <tr><td>64</td><td>"VMH"</td><td>"VML"</td></tr> <tr><td>65</td><td>"VMH"+1d</td><td>"VML"+1d</td></tr> <tr><td>66</td><td>"VMH"+2d</td><td>"VML"+2d</td></tr> <tr><td>:</td><td>:</td><td>:</td></tr> <tr><td>126</td><td>"VMH"+62d</td><td>"VML"+62d</td></tr> <tr><td>127</td><td>"VMH"+63d</td><td>"VML"+63d</td></tr> </tbody> </table> If "VMH"+xd or "VML"+xd is less than 0d, it becomes 0d If "VMH"+xd or "VML"+xd is large than 100d, it becomes 100d VMF[5:0] are stored in NV memoy to contrast -Select the VMF[6:0]value <table border="1"> <thead> <tr> <th>nVM</th> <th>VMF[6:0] value</th> </tr> </thead> <tbody> <tr><td>0</td><td>VCOM offset value from NV memory</td></tr> <tr><td>1</td><td>VCOM offset value in the VMF[6:0] registers</td></tr> </tbody> </table>													VMF[6:0]	VCOMH Output	VCOML Output Level	0	"VMH"	"VML"	1	"VMH"-63d	"VML"-63d	2	"VMH"-62d	"VML"-62d	:	:	:	62	"VMH"-2d	"VML"-2d	63	"VMH"-1d	"VML"-1d	64	"VMH"	"VML"	65	"VMH"+1d	"VML"+1d	66	"VMH"+2d	"VML"+2d	:	:	:	126	"VMH"+62d	"VML"+62d	127	"VMH"+63d	"VML"+63d	nVM	VMF[6:0] value	0	VCOM offset value from NV memory	1	VCOM offset value in the VMF[6:0] registers
VMF[6:0]	VCOMH Output	VCOML Output Level																																																								
0	"VMH"	"VML"																																																								
1	"VMH"-63d	"VML"-63d																																																								
2	"VMH"-62d	"VML"-62d																																																								
:	:	:																																																								
62	"VMH"-2d	"VML"-2d																																																								
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1	VCOM offset value in the VMF[6:0] registers																																																									
Restriction	-If this register not use the register need be reserved. -To control the VCOM output voltage with VMF[5::0] command, nVM parameter should be set '1'																																																									
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr><td>Sleep In</td><td>Yes</td></tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes																																	
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Power On Sequence	40h																																																									
SW Reset	40h																																																									
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14.2.52 Write ID4 Value (D3h)

D3H		Read the ID4 value																															
		D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																			
Command	0	1	↑	x	1	1	0	1	0	0	0	1	1	D3h																			
1 st Parameter	1	↑	1	x	x	x	x	x	x	x	x	x	x	x																			
2 nd Parameter	1	↑	1	x	ID417	ID416	ID415	ID414	ID413	ID412	ID411	ID410	91h																				
3 rd Parameter	1	↑	1	x	ID427	ID426	ID425	ID424	ID423	ID422	ID421	ID420	63h																				
4 th Parameter	1	↑	1	x	x	x	x	x	ID433	ID432	ID431	ID430	00h																				
5 th Parameter	1	↑	1	x	x	x	x	x	x	x	x	x	x	x																			
Description	-Read the Driver IC information from mask value. -Ignored the EXTC pin. -The 1 st parameter is dummy data -The 2 nd parameter ID41[7:0] is Driver IC ID code. (Default value=91h) -The value be defined later -Currently, "01h", "02h", "03h", "05h" can't be used. -The 3 rd parameter ID42[7:0] is Driver IC Part number ID. (The code be define by Driver IC Vendor, and default value=63h) -The 4 th parameter ID43[7:0] is Driver IC version ID -When the Driver maker modifies any function it should be modify the parameters at this ID code before sample out also. -If Driver Maker don't need 2 parameter if can't reduce to one parameter. -If the parameters are not enough Driver makers can add or reduce yourself																																
Restriction	-																																
Register Availability	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>														Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes							
Status	Availability																																
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Status	Default Value																																
	ID41[7:0]	ID42[7:0]	ID43[7:0]																														
Power On Sequence	01h	21h	TBD																														
SW Reset	01h	21h	TBD																														
HW Reset	01h	21h	TBD																														



14.2.53 NV Memory Function Controller(1) (D5h)

NV Memory Function Controller1																																																																																																																							
D5H	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																																																																										
Command	0	1	↑	x	1	1	0	1	1	0	1	0	D5h																																																																																																										
1 st Parameter	1	1	↑	x	ID33	ID32	ID31	ID30	ID23	ID22	ID21	ID20	00h																																																																																																										
2 nd Parameter	1	1	↑	x	OTP_BS	0	0	0	OTP_VMF3	OTP_VMF2	OTP_VMF1	OTP_VMF0	00h																																																																																																										
Description	<ul style="list-style-type: none"> -ID2, ID3, and VMF can be written four times. -Read status(written times) of the NV memory. -Written times for ID2 <table border="1" style="margin-top: 10px;"> <tr> <td rowspan="2" style="text-align: center; vertical-align: middle;">ID2 Times</td> <th colspan="8" style="text-align: center;">1st Parameter</th> </tr> <tr> <td>ID33</td><td>ID32</td><td>ID31</td><td>ID30</td><td>ID23</td><td>ID22</td><td>ID21</td><td>ID20</td> </tr> <tr> <td>1st</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td></tr> <tr> <td>2nd</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td></tr> <tr> <td>3rd</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td></tr> <tr> <td>4th</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td></tr> </table> <ul style="list-style-type: none"> -Written times for ID3 <table border="1" style="margin-top: 10px;"> <tr> <td rowspan="2" style="text-align: center; vertical-align: middle;">ID3 Times</td> <th colspan="8" style="text-align: center;">1st Parameter</th> </tr> <tr> <td>ID33</td><td>ID32</td><td>ID31</td><td>ID30</td><td>ID23</td><td>ID22</td><td>ID21</td><td>ID20</td> </tr> <tr> <td>1st</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td></tr> <tr> <td>2nd</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td></tr> <tr> <td>3rd</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td></tr> <tr> <td>4th</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td></tr> </table> <ul style="list-style-type: none"> -Written times for OTP_VMF 													ID2 Times	1 st Parameter								ID33	ID32	ID31	ID30	ID23	ID22	ID21	ID20	1 st	0	0	0	0	0	0	0	1	2 nd	0	0	0	0	0	0	1	1	3 rd	0	0	0	0	0	1	1	1	4 th	0	0	0	0	1	1	1	1	ID3 Times	1 st Parameter								ID33	ID32	ID31	ID30	ID23	ID22	ID21	ID20	1 st	0	0	0	1	0	0	0	0	2 nd	0	0	1	1	0	0	0	0	3 rd	0	1	1	1	0	0	0	0	4 th	1	1	1	1	0	0	0	0
ID2 Times	1 st Parameter																																																																																																																						
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1 st	0	0	0	0	0	0	0	1																																																																																																															
2 nd	0	0	0	0	0	0	1	1																																																																																																															
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1 st	0	0	0	1	0	0	0	0																																																																																																															
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Times	OTP_VMF			2 nd Parameter																															
		VMF3	VMF2	VMF1	VMF0																														
1 st		0	0	0	1																														
2 nd		0	0	1	1																														
3 rd		0	1	1	1																														
4 th		1	1	1	1																														
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Status	Default Value																																		
Power On Sequence	N/A																																		
SW Reset	N/A																																		
HW Reset	N/A																																		
Flow Chart																																			

14.2.54 NV Memory Function Controller(2) (D6h)

NV Memory Function Controller1																									
D6H	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	x	1	1	0	1	1	0	1	0	D6h												
1 st Parameter	1	1	↑	x	OTP_D[7]	OTP_D[6]	OTP_D[5]	OTP_D[4]	OTP_D[3]	OTP_D[2]	OTP_D[1]	OTP_D[0]	00h												
2 nd Parameter	1	1	↑	x	0	0	0	0	0	0	OTP_TP[1]	OTP_TP[0]	00h												
Description	-Parameter 1 bit[7:0] : OTP Write Data OTP_D[7:0] ID2[7:0] ID3[7:0] {1'b0, VMF[6:0]} Ctrl[4:0] -> {3'd0, BG_AD[1:0], OSC_CT[2:0]} -Parameter 2 OTP type selection: bit[1:0] : OTP Address OTP[1:0] 00: ID2, 01:ID3, 10:VMF, 11:Ctrl MTP write EPWRITE command Please see MTP Access sequence for program(Data write) for more detail																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Flow Chart																									

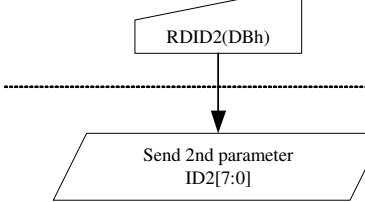
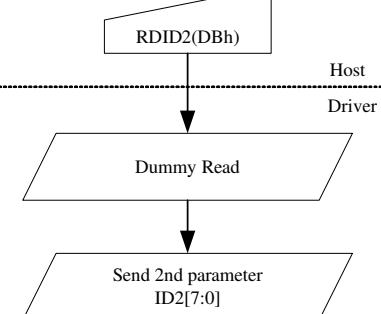
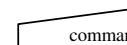
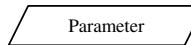
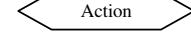
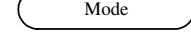
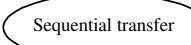
14.2.55 NV Memory Function Controller(3) (D7h)

D7H		NV Memory Function Controller1																							
		D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX											
Command		0	1	↑	x	1	1	0	1	1	0	1	0	D7h											
1 st Parameter		1	1	↑	x	0	1	0	1	0	1	0	1	55h											
2 nd Parameter		1	1	↑	x	1	0	1	0	1	0	1	0	AAh											
3 rd Parameter		1	1	↑	x	0	1	1	0	0	1	1	0	66h											
Description	MTP write EPWRITE command Please see MTP Access sequence for program(Data write) for more detail																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
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Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>N/A</td> </tr> <tr> <td>SW Reset</td> <td>N/A</td> </tr> <tr> <td>HW Reset</td> <td>N/A</td> </tr> </tbody> </table>													Status	Default Value	Power On Sequence	N/A	SW Reset	N/A	HW Reset	N/A				
Status	Default Value																								
Power On Sequence	N/A																								
SW Reset	N/A																								
HW Reset	N/A																								
Flow Chart																									

14.2.34 Read ID1 (DAh)

DAH		RDID1 (Read ID1)																								
	DAH	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	x	1	1	0	1	1	0	1	0	0	DAh												
1 st Parameter	1	↑	1	x	x	x	x	x	x	x	x	x	x	x												
2 nd Parameter	1	↑	1	x	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	54h													
Description	This read byte return 8-bit LCD module's ID. The 1 st parameter is dummy data The 2 nd parameter (ID17to ID10): LCD module manufacturer ID X = Don't care																									
Restriction																										
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>														Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																									
Normal Mode On, Idle Mode Off, Sleep Out	Yes																									
Normal Mode On, Idle Mode On, Sleep Out	Yes																									
Partial Mode On, Idle Mode Off, Sleep Out	Yes																									
Partial Mode On, Idle Mode On, Sleep Out	Yes																									
Sleep In	Yes																									
Default	<table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>54h</td></tr> <tr> <td>SW Reset</td><td>54h</td></tr> <tr> <td>HW Reset</td><td>54h</td></tr> </tbody> </table> <p>Note : ID1 can be modified by metal option</p>														Status	Default Value	Power On Sequence	54h	SW Reset	54h	HW Reset	54h				
Status	Default Value																									
Power On Sequence	54h																									
SW Reset	54h																									
HW Reset	54h																									
Flow Chart	<pre> graph TD RDID1[RDID1(DAh)] --> S1[/Send 2nd parameter ID1[7:0]/] RDID1 --> P1[/Dummy Read/] S1 --> S2[/Send 2nd parameter ID1[7:0]/] P1 --> S2 style RDID1 fill:none,stroke:none style S1 fill:none,stroke:none style P1 fill:none,stroke:none style S2 fill:none,stroke:none style Host fill:none,stroke:none style Driver fill:none,stroke:none </pre> <p>Legend:</p> <ul style="list-style-type: none"> command Parameter Display Action Mode Sequential transfer 																									

14.2.35 Read ID2 (DBh)

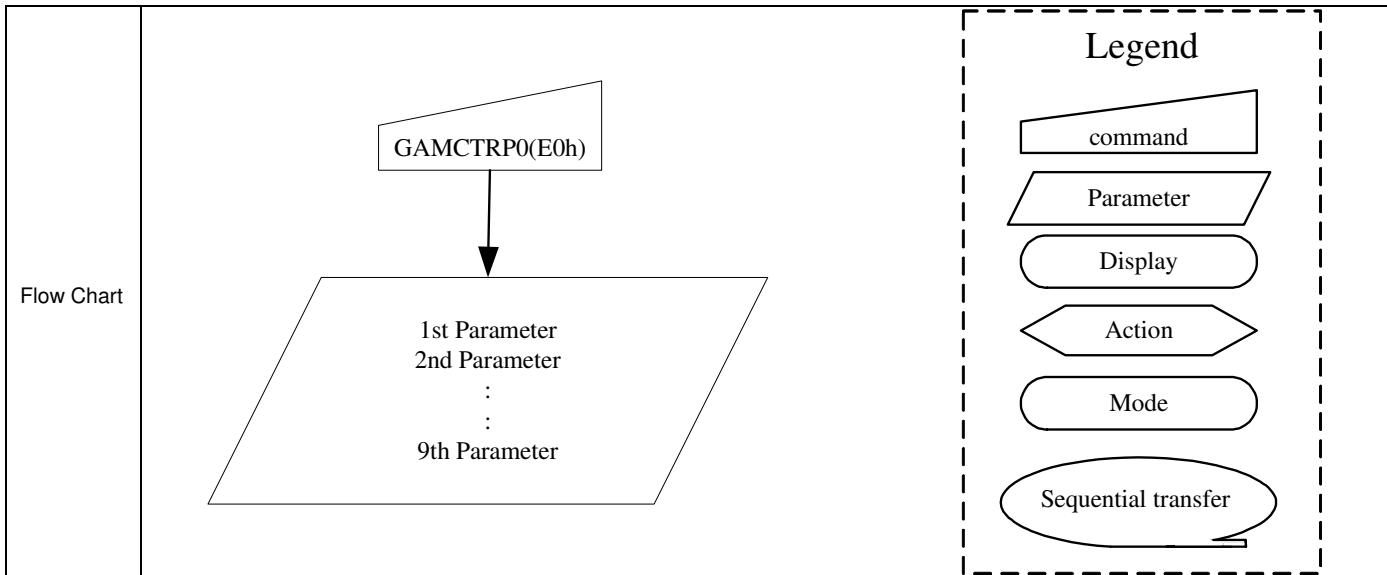
DBH	RDID2 (Read ID2)																								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	x	1	1	0	1	1	0	1	1	DBh												
1 st Parameter	1	↑	1	x	x	x	x	x	x	x	x	x	x												
2 nd Parameter	1	↑	1	x	1	ID26	ID25	ID24	ID23	ID22	ID21	ID20	80h												
Description	This read byte returns 8-bit LCD module/driver version ID Th ^e 1st parameter is dummy data Th ^e 2nd parameter (ID26 to ID20): LCD module/driver version ID Parameter Range: ID=80h to FFh Note : See command RDDID(04h) 3rd parameter																								
Restriction																									
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>See Description</td> </tr> <tr> <td>SW Reset</td> <td>See Description</td> </tr> <tr> <td>HW Reset</td> <td>See Description</td> </tr> </tbody> </table>													Status	Default Value	Power On Sequence	See Description	SW Reset	See Description	HW Reset	See Description				
Status	Default Value																								
Power On Sequence	See Description																								
SW Reset	See Description																								
HW Reset	See Description																								
Flow Chart	<div style="display: flex; justify-content: space-around;"> <div style="text-align: center;"> Serial I/F Mode  </div> <div style="text-align: center;"> Parallel I/F Mode  </div> </div> <div style="border: 1px dashed black; padding: 5px; margin-top: 10px;"> Legend <ul style="list-style-type: none">  Command  Parameter  Display  Action  Mode  Sequential transfer </div>																								

14.2.36 Read ID3 (DCh)

DCH		RDID3 (Read ID3)																							
Command	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
1 st Parameter	0	1	↑	x	1	1	0	1	1	1	0	0	DCh												
2 nd Parameter	1	↑	1	x	x	x	x	x	x	x	x	x	x												
Description	-This read byte return 8-bit LCD module/driver ID -The 1 st parameter is dummy data -The 2 nd parameter (ID37 to ID30): LCD module/driver ID -Parameter range: ID=00h to FFh Note : See command RDDID(04h) 4th parameter																								
Restriction																									
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>66h</td></tr> <tr> <td>SW Reset</td><td>66h</td></tr> <tr> <td>HW Reset</td><td>66h</td></tr> </tbody> </table>													Status	Default Value	Power On Sequence	66h	SW Reset	66h	HW Reset	66h				
Status	Default Value																								
Power On Sequence	66h																								
SW Reset	66h																								
HW Reset	66h																								
Flow Chart	<p>Serial I/F Mode</p> <p>Parallel I/F Mode</p> <p>Legend</p> <ul style="list-style-type: none"> command Parameter Display Action Mode Sequential transfer 																								

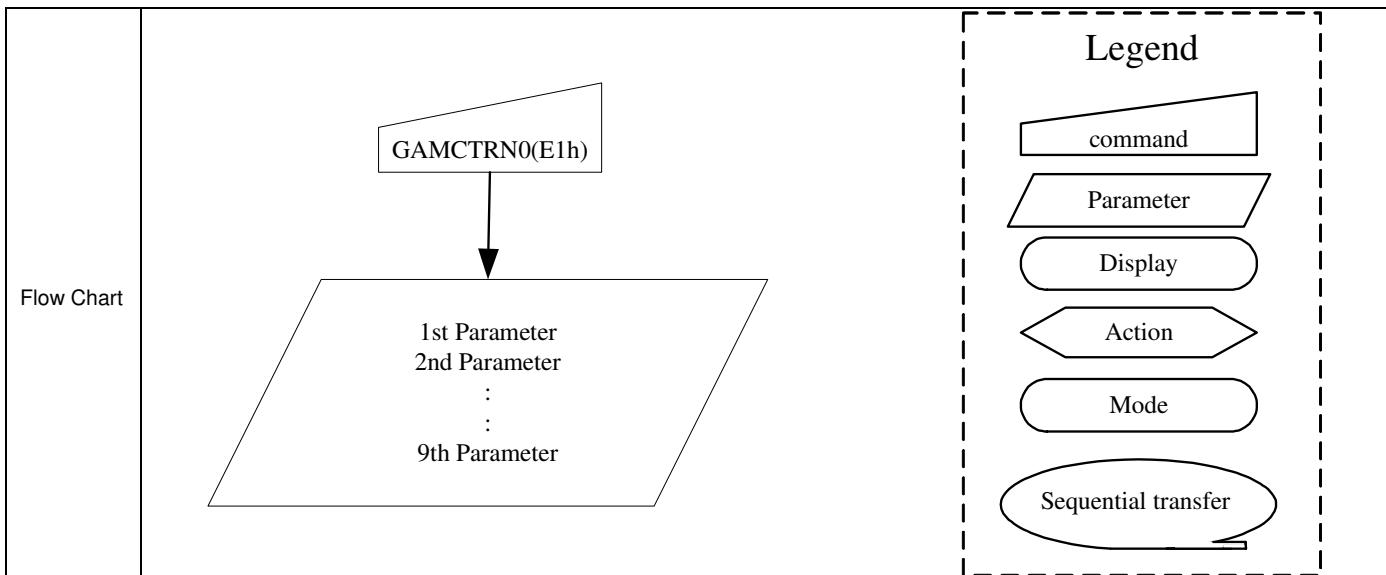
14.2.56 Positive Gamma Correction Setting (E0h)

E1H		Positive Gamma Correction Setting																						
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	1	1	1	0	0	0	0	1	E0h												
1 st Parameter	1	1	↑	x	x	VP63[5:0]						x												
2 nd Parameter	1	1	↑	x	x	VP62[5:0]						x												
3 rd Parameter	1	1	↑	x	x	VP61[5:0]						x												
4 th Parameter	1	1	↑	x	x	VP59[5:0]						x												
5 th Parameter	1	1	↑	x	x	VP57[5:0]						x												
6 th Parameter	1	1	↑	x	x	x	VP50[4:0]					x												
7 th Parameter	1	1	↑	x	VP43[6:0]							x												
8 th Parameter	1	1	↑	VP27[3:0]					VP36[3:0]															
9 th Parameter	1	1	↑	x	VP20[6:0]																			
10 th Parameter	1	1	↑	x	x	x	VP13[4:0]					x												
11 th Parameter	1	1	↑	x	x	VP6[5:0]																		
12 th Parameter	1	1	↑	x	x	VP4[5:0]																		
13 th Parameter	1	1	↑	x	x	VP2[5:0]																		
14 th Parameter	1	1	↑	x	x	VP1[5:0]																		
15 th Parameter	1	1	↑	x	x	VP0[5:0]																		
Description	Set the gray scale voltage to adjust the gamma characteristics of the TFT panel. It apply to gamma curve selection for only activate when EXTC=1 and GAM_R_SEL=1 VP0 is the maximum gamma output voltage in positive polarity. VP63 is the minimum gamma output voltage in positive polarity.																							
Restriction	-																							
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>												Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																							
Normal Mode On, Idle Mode Off, Sleep Out	Yes																							
Normal Mode On, Idle Mode On, Sleep Out	Yes																							
Partial Mode On, Idle Mode Off, Sleep Out	Yes																							
Partial Mode On, Idle Mode On, Sleep Out	Yes																							
Sleep In	Yes																							
Default	<table border="1"> <thead> <tr> <th rowspan="2">Status</th> <th>Default Value</th> </tr> <tr> <th>1st ~ 9th Parameter</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>All "00"</td> </tr> <tr> <td>SW Reset</td> <td>All "00"</td> </tr> <tr> <td>HW Reset</td> <td>All "00"</td> </tr> </tbody> </table>												Status	Default Value	1 st ~ 9 th Parameter	Power On Sequence	All "00"	SW Reset	All "00"	HW Reset	All "00"			
Status	Default Value																							
	1 st ~ 9 th Parameter																							
Power On Sequence	All "00"																							
SW Reset	All "00"																							
HW Reset	All "00"																							



14.2.57 Negative Gamma Correction Setting (E1h)

Negative Gamma Correction Setting																																	
E1H	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX																					
Command	0	1	↑	1	1	1	0	0	0	0	1	E1h																					
1 st Parameter	1	1	↑	x	x	VN0[5:0]											x																
2 nd Parameter	1	1	↑	x	x	VN1[5:0]											x																
3 rd Parameter	1	1	↑	x	x	VN2[5:0]											x																
4 th Parameter	1	1	↑	x	x	VN4[5:0]											x																
5 th Parameter	1	1	↑	x	x	VN6[5:0]											x																
6 th Parameter	1	1	↑	x	x	x	VN13[4:0]						VN13[4:0]		VN13[4:0]		x																
7 th Parameter	1	1	↑	x	VN20[6:0]											VN20[6:0]		x															
8 th Parameter	1	1	↑	VN36[3:0]					VN27[3:0]				VN27[3:0]		VN27[3:0]		VN27[3:0]		x														
9 th Parameter	1	1	↑	x	VN43[6:0]											VN43[6:0]		x															
10 th Parameter	1	1	↑	x	x	x	VN50[4:0]						VN50[4:0]		VN50[4:0]		VN50[4:0]		x														
11 th Parameter	1	1	↑	x	x	VN57[5:0]											VN57[5:0]		x														
12 th Parameter	1	1	↑	x	x	VN59[5:0]											VN59[5:0]		x														
13 th Parameter	1	1	↑	x	x	VN61[5:0]											VN61[5:0]		x														
14 th Parameter	1	1	↑	x	x	VN62[5:0]											VN62[5:0]		x														
15 th Parameter	1	1	↑	x	x	VN63[5:0]											VN63[5:0]		x														
Description	Set the gray scale voltage to adjust the gamma characteristics of the TFT panel. It apply to gamma curve selection for only activate when EXTC=1 and GAM_R_SEL=1 VN0 is the minimum gamma output voltage in negative polarity. VN63 is the maximum gamma output voltage in negative polarity.																																
Restriction	-																																
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>												Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes									
Status	Availability																																
Normal Mode On, Idle Mode Off, Sleep Out	Yes																																
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Status	Default Value																																
	1 st ~ 9 th Parameter																																
Power On Sequence	All "00"																																
SW Reset	All "00"																																
HW Reset	All "00"																																



14.2.58 GAM_R_SEL (F2h)

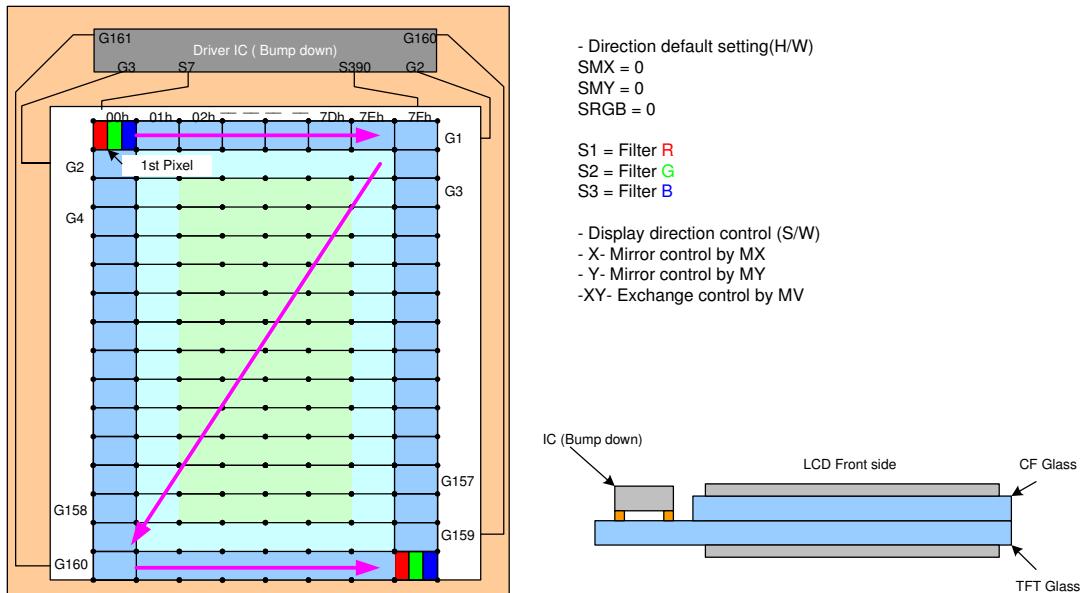
Gamma Setting (Green)																								
F2h	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	1	1	1	1	0	0	1	0	F2h												
1 st Parameter	1	1	↑	x	x	x	x	x	x	x	GAM_R_SEL	x												
Description	GAM_R_SEL: Gamma adjustment E0h and E1h enable control 0: Disable (Default) 1: Enable																							
Restriction	-																							
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>												Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																							
Normal Mode On, Idle Mode Off, Sleep Out	Yes																							
Normal Mode On, Idle Mode On, Sleep Out	Yes																							
Partial Mode On, Idle Mode Off, Sleep Out	Yes																							
Partial Mode On, Idle Mode On, Sleep Out	Yes																							
Sleep In	Yes																							
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Status	Default Value																							
Power On Sequence	0h																							
SW Reset	0h																							
HW Reset	0h																							

15. Example Connection with Panel direction and Different Resolution

15.1 Application of connect with panel direction (when GM='011')

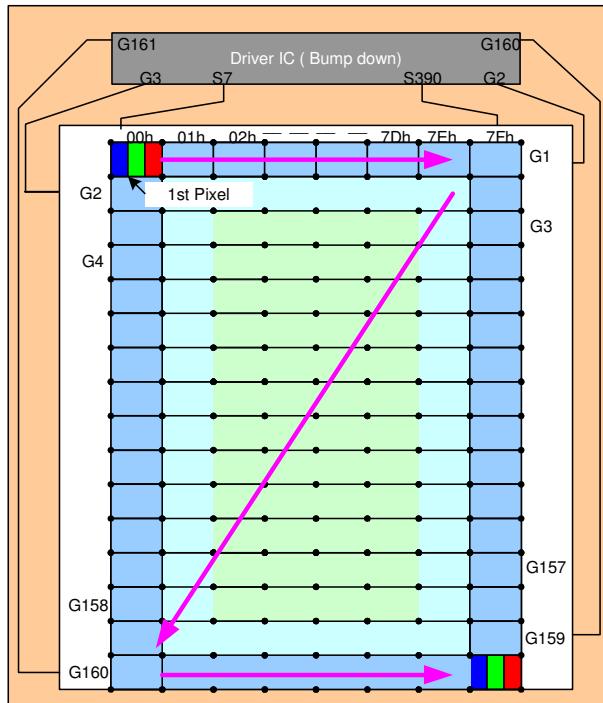
Case 1: (This is default case)

- 1st Pixel is at Left Top of the pane
- RGB filter order = RGB



Case 2:

- 1st Pixel is at Left Top of the panel
- RGB filter order = BGR



- Direction default setting(H/W)

SMX = 0

SMY = 0

SRGB = 1

S1 = Filter B

S2 = Filter G

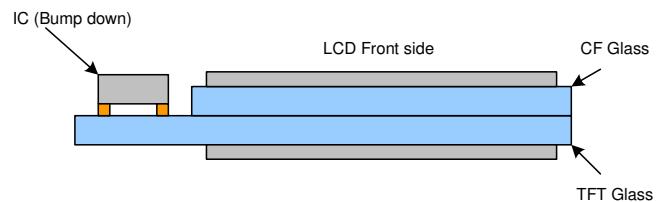
S3 = Filter R

- Display direction control (S/W)

- X- Mirror control by MX

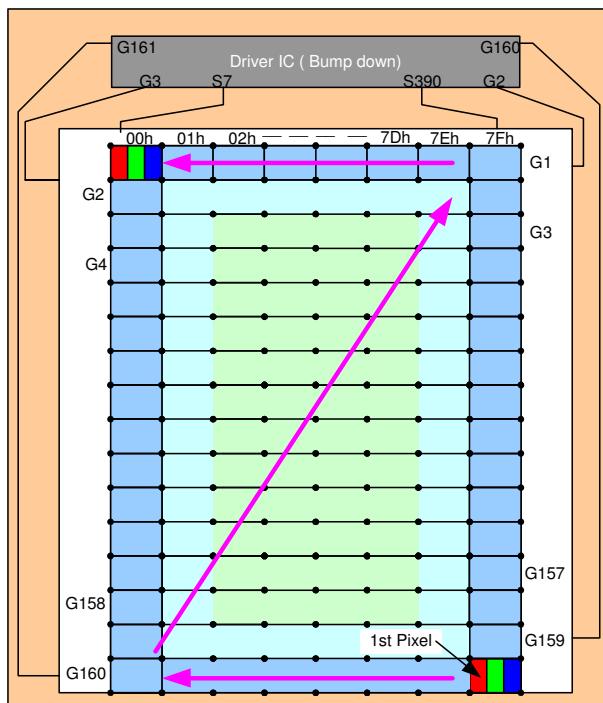
- Y- Mirror control by MY

-XY- Exchange control by MV



Case3:

- 1st Pixel is at Right Bottom of the panel
- RGB filter order = "RGB"



- Direction default setting(H/W)

SMX = 0

SMY = 0

SRGB = 0

S1 = Filter R

S2 = Filter G

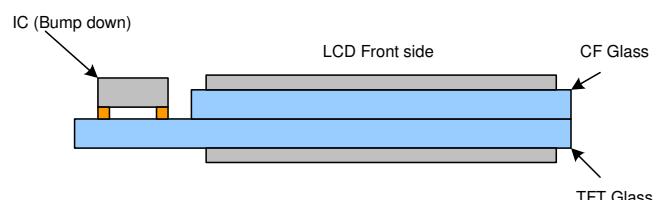
S3 = Filter B

- Display direction control (S/W)

- X- Mirror control by MX

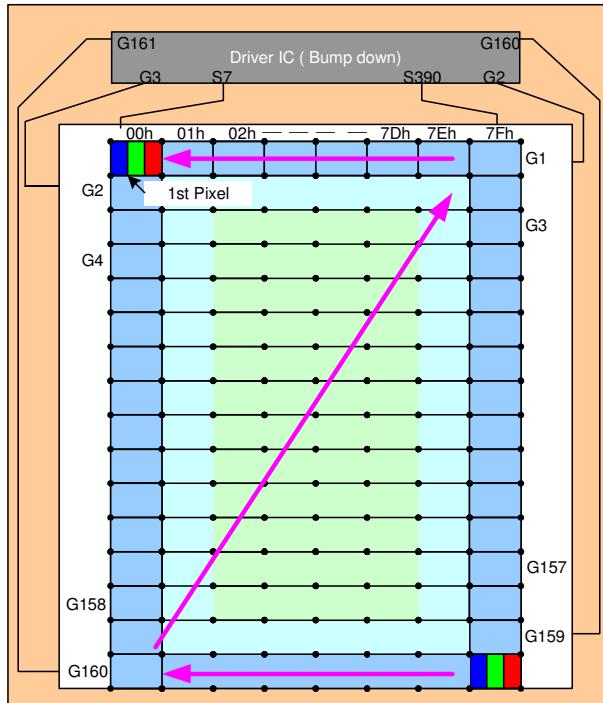
- Y- Mirror control by MY

-XY- Exchange control by MV



Case 4:

- 1st Pixel is at Right-Bottom of the panel
- RGB filter order = "BGR"



- Direction default setting(H/W)

SMX = 0

SMY = 0

SRGB = 1

S1 = Filter B

S2 = Filter G

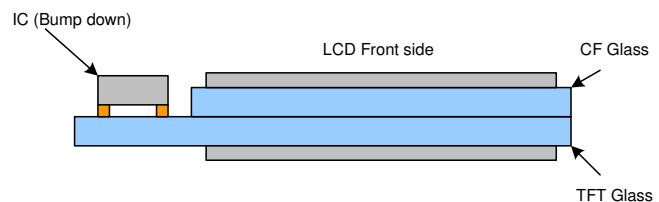
S3 = Filter R

- Display direction control (S/W)

- X- Mirror control by MX

- Y- Mirror control by MY

-XY- Exchange control by MV

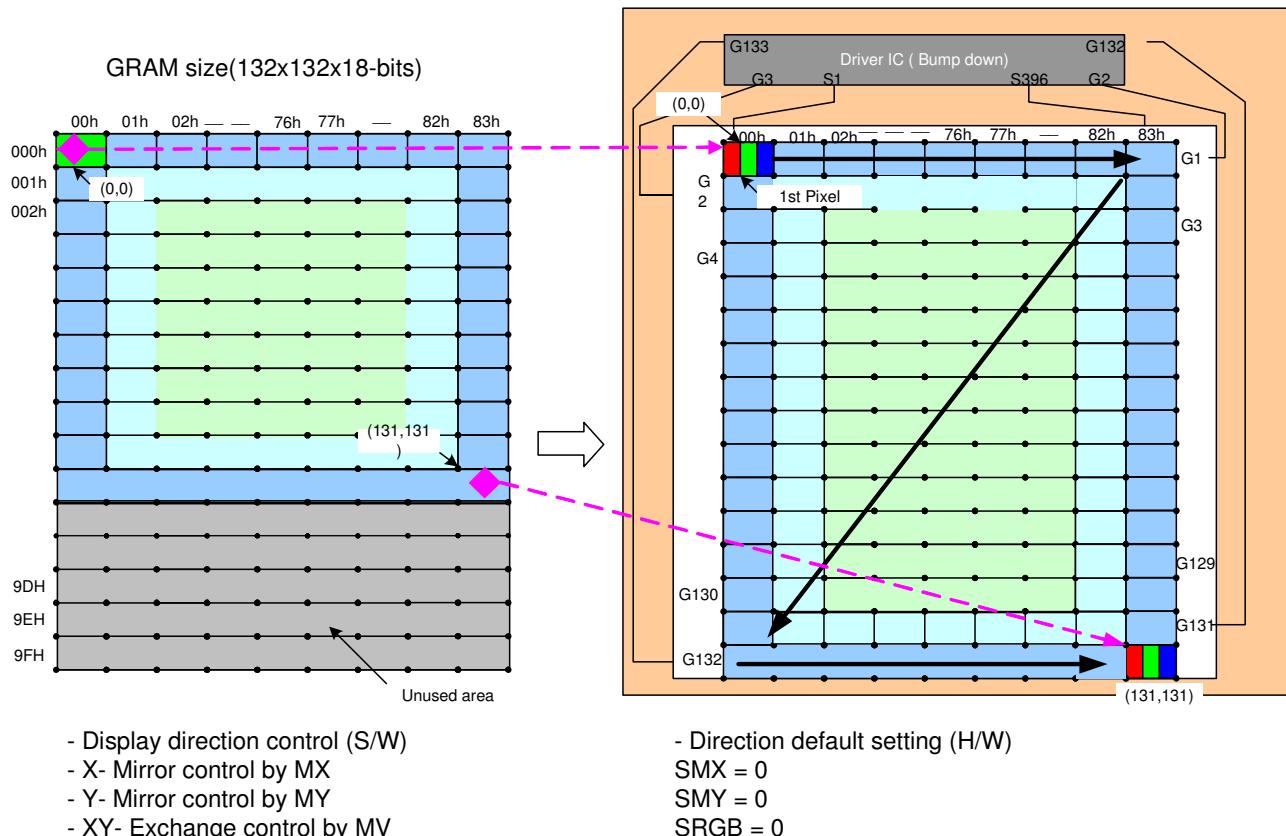


15.2 Application of connection with Different resolution

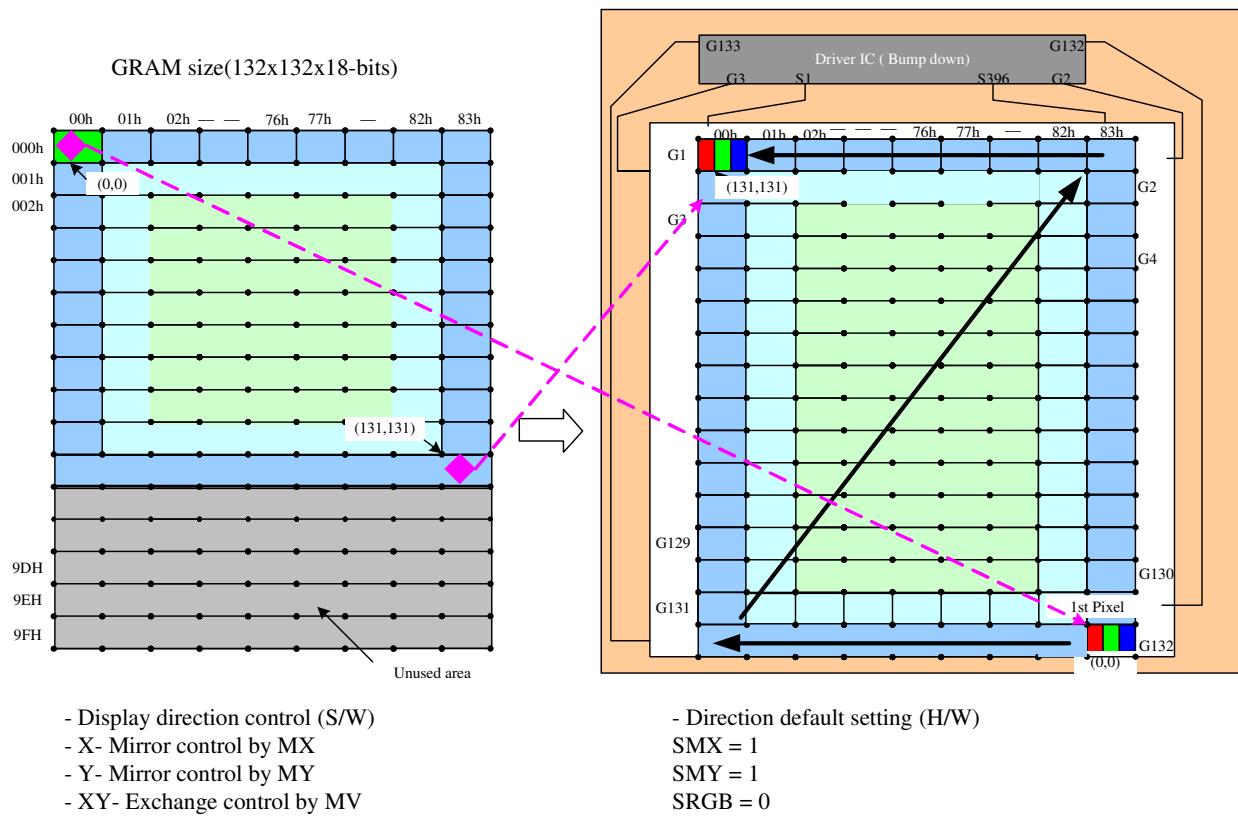
Case 1 of Resolution (132RGB x 132)(GM[2:0] = "101") RAM size=132 x 132 x 18-bits(Used)

Display size = 132RGB x 132

1) Example for SMX=SMY='0'



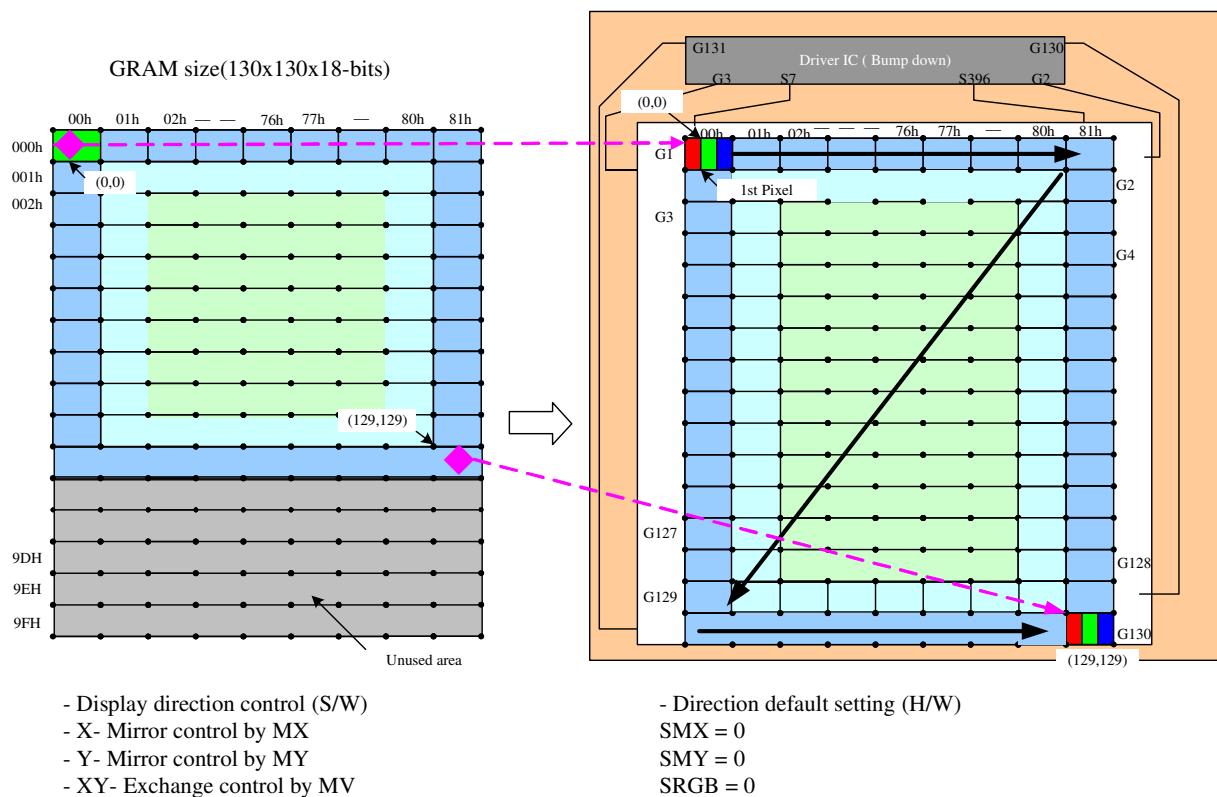
2) Example for SMX=SMY='1'



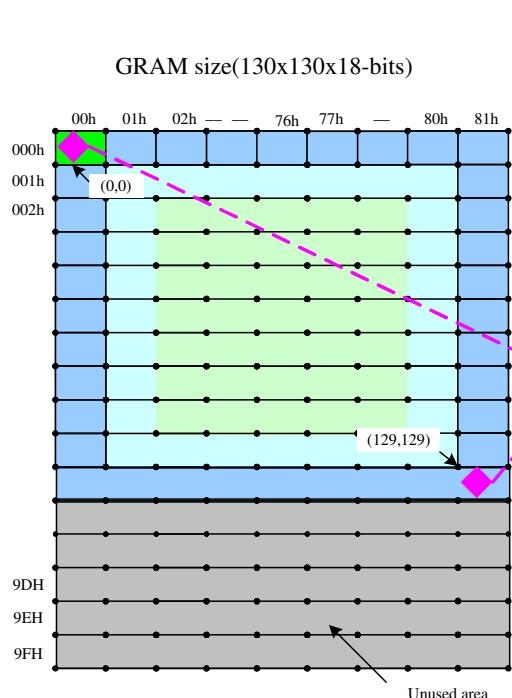
Case 2 of Resolution (130RGB x 130)(GM[2:0] = "100") RAM size=130 x 130 x 18-bits(Used)

Display size = 130RGB x 130

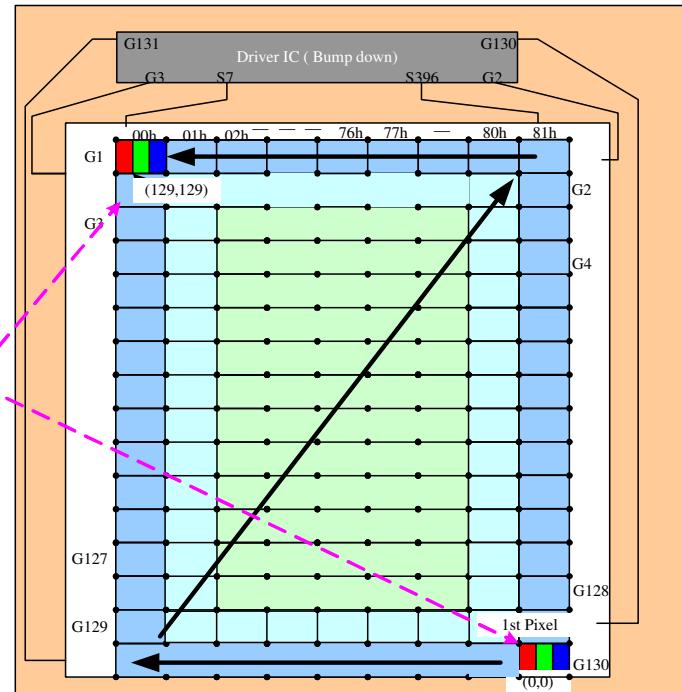
1) Example for SMX=SMY='0'



2) Example for SMX=SMY='1'



- Display direction control (S/W)
- X- Mirror control by MX
- Y- Mirror control by MY
- XY- Exchange control by MV

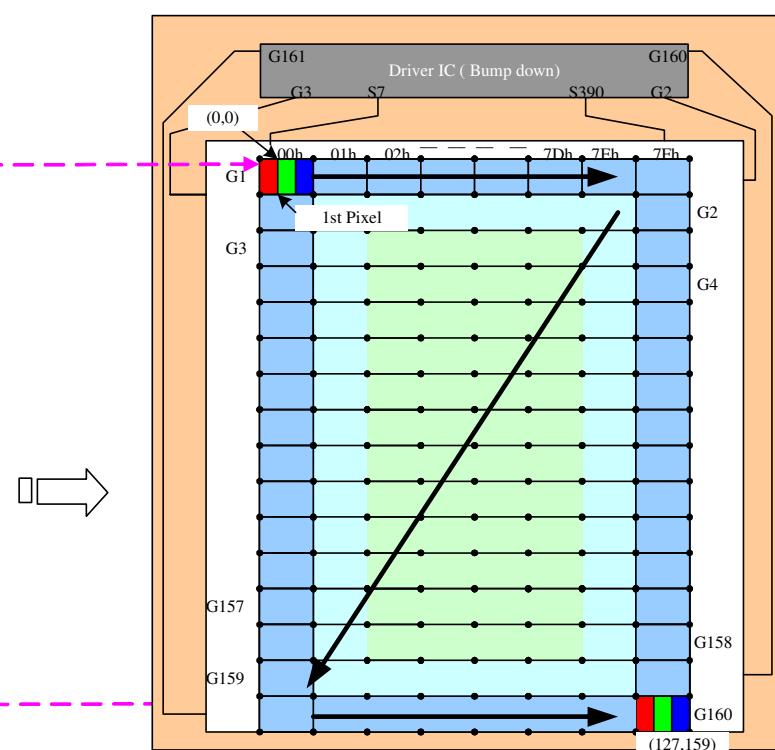
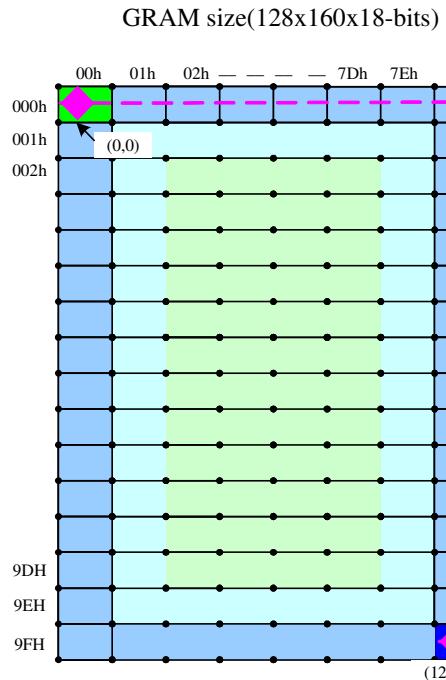


- Direction default setting (H/W)
- SMX = 1
- SMY = 1
- SRGB = 0

Case 3 of Resolution (128RGB x 160)(GM[2:0]=""011") RAM size=128 x 160 x 18-bits(Used)

Display size = 128RGB x 160

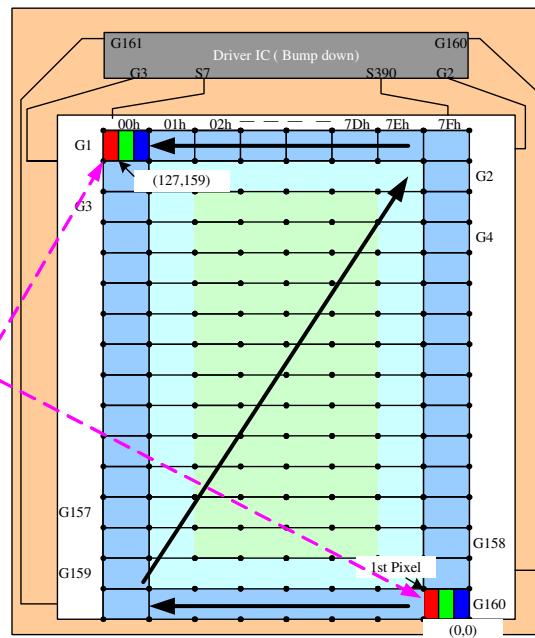
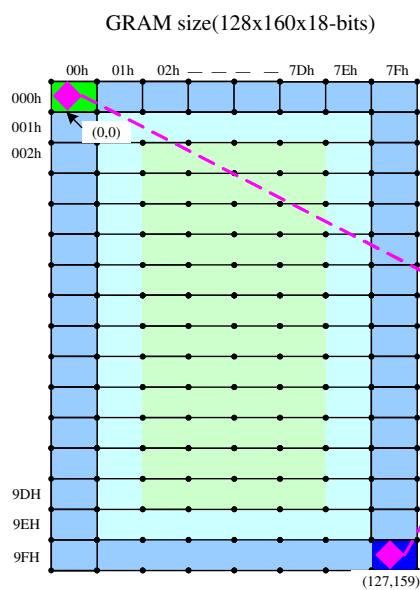
1) Example for SMX=SMY='0'



- Display direction control (S/W)
- X- Mirror control by MX
- Y- Mirror control by MY
- XY- Exchange control by MV

- Direction default setting (H/W)
- SMX = 0
- SMY = 0
- SRGB = 0

2) Example for SMX=SMY='1'



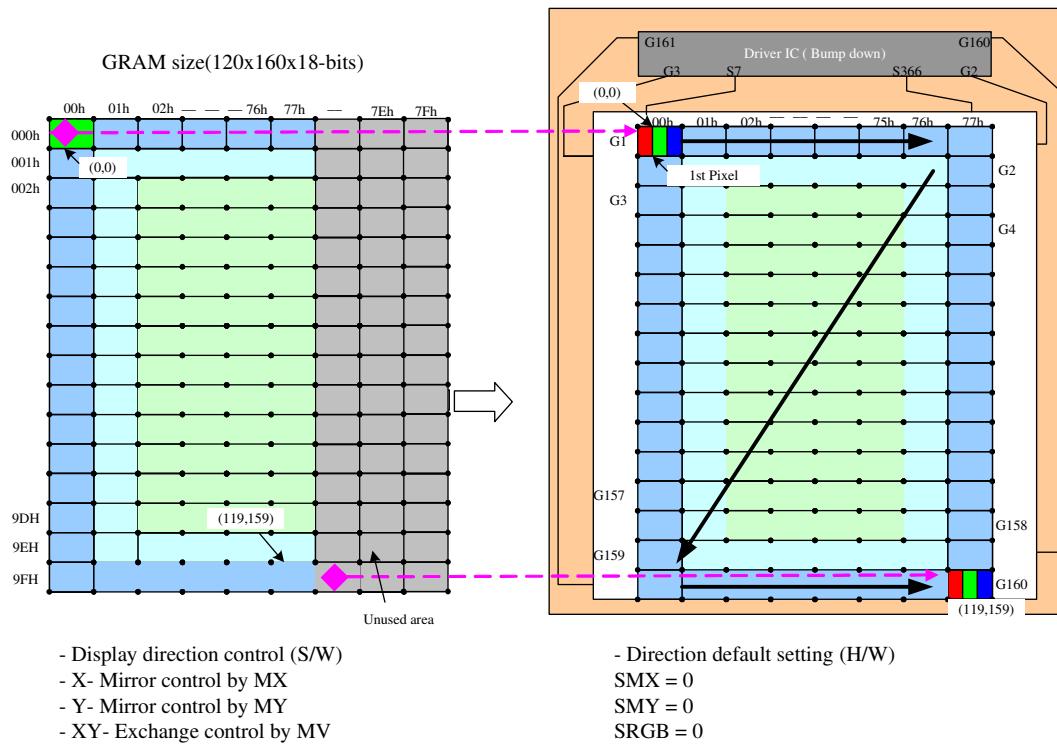
- Display direction control (S/W)
- X- Mirror control by MX
- Y- Mirror control by MY
- XY- Exchange control by MV

- Direction default setting (H/W)
- SMX = 1
- SMY = 1
- SRGB = 0

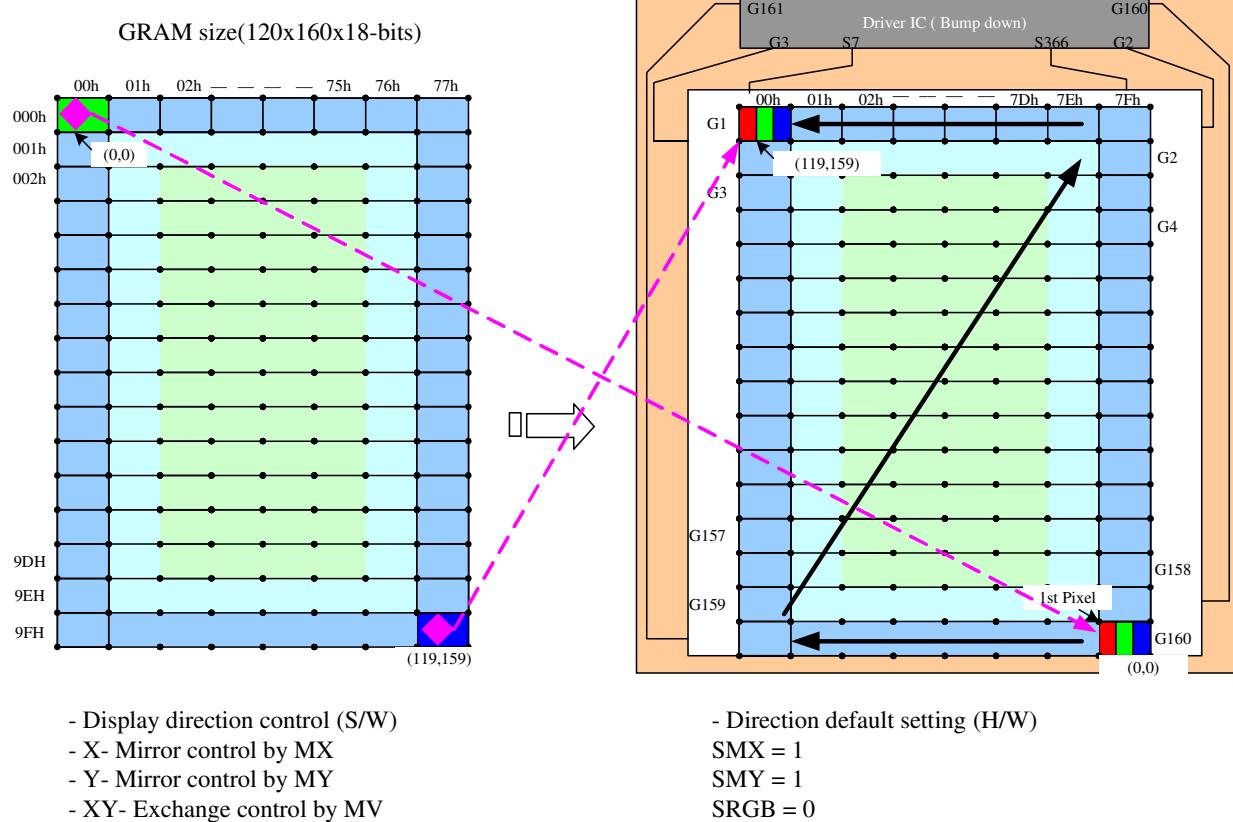
Case4 of Resolution (120RGB x 160)(GM[2:0] = "010") RAM size=120 x 160 x 18-bits(Used)

Display size = 120RGB x 160

1) Example for SMX=SMY='0'

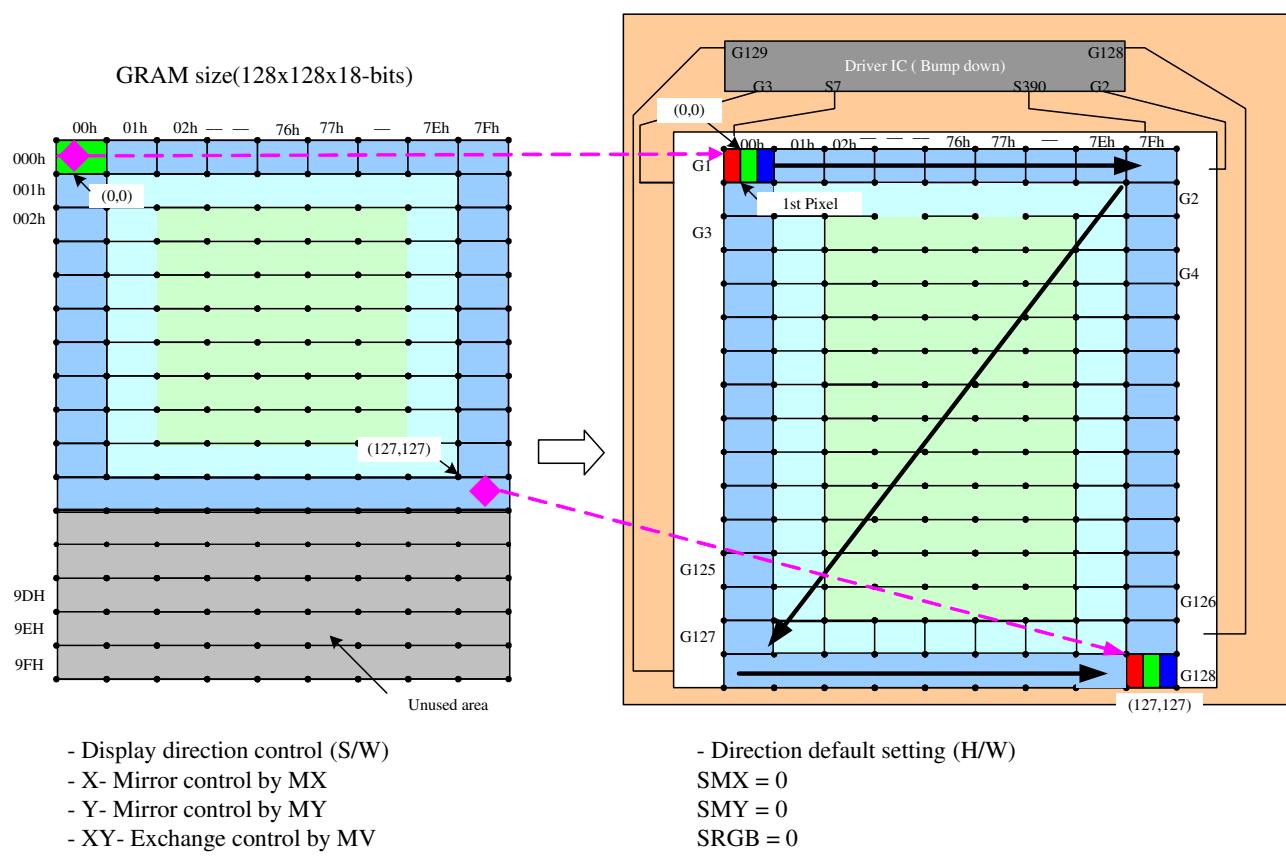


2) Example for SMX=SMY='1'

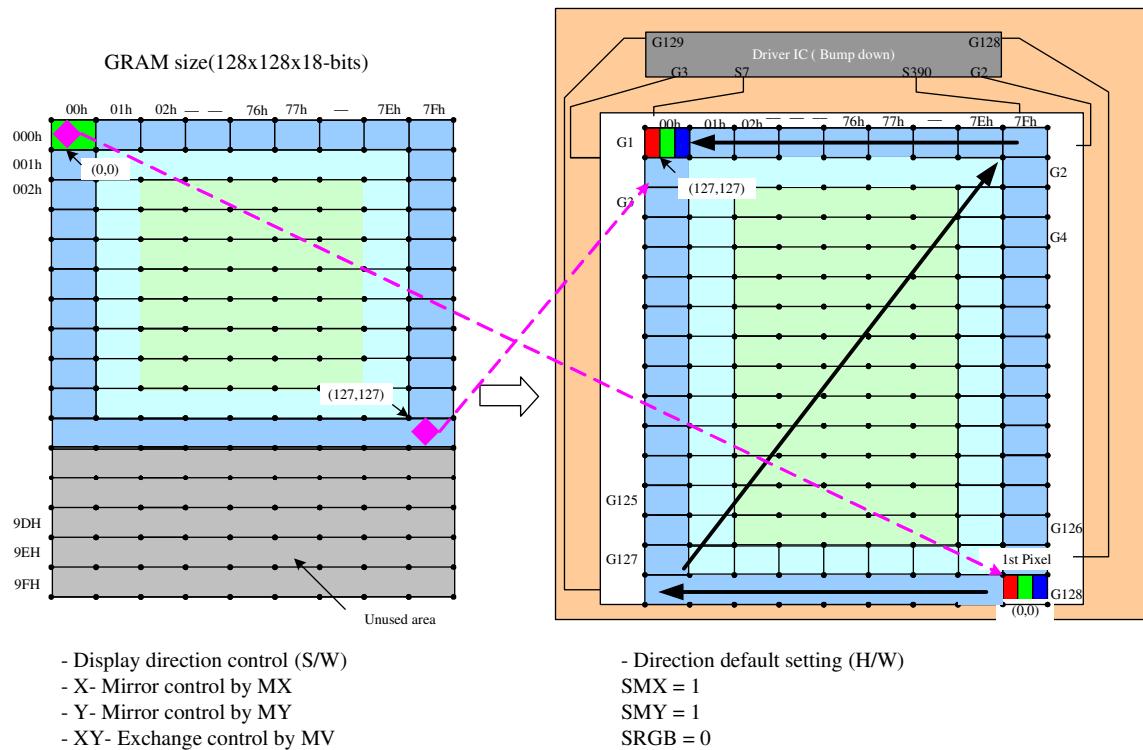


Case 5 of Resolution (128RGBx128)(GM[2:0]=""001") RAM size=128 x 128 x 18-bits(Used)

1) Example for SMX=SMY='0'



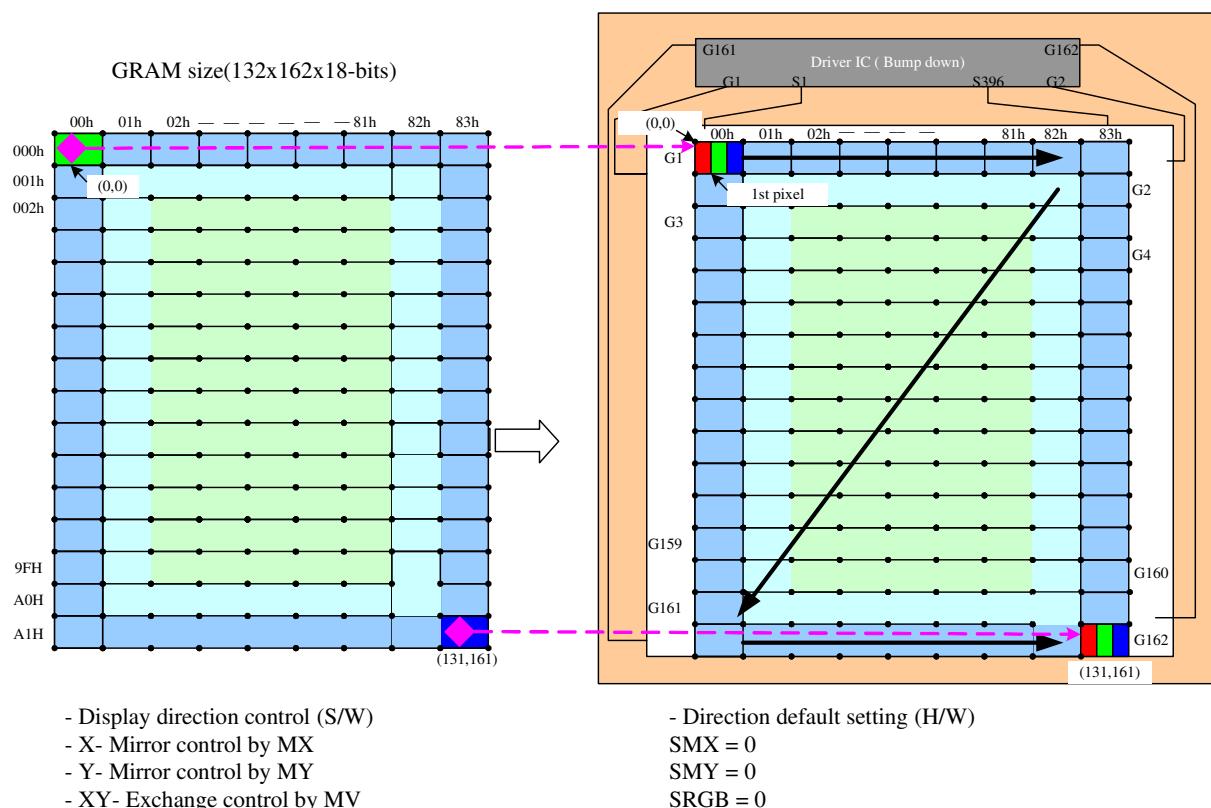
2) Example for SMX=SMY='1'



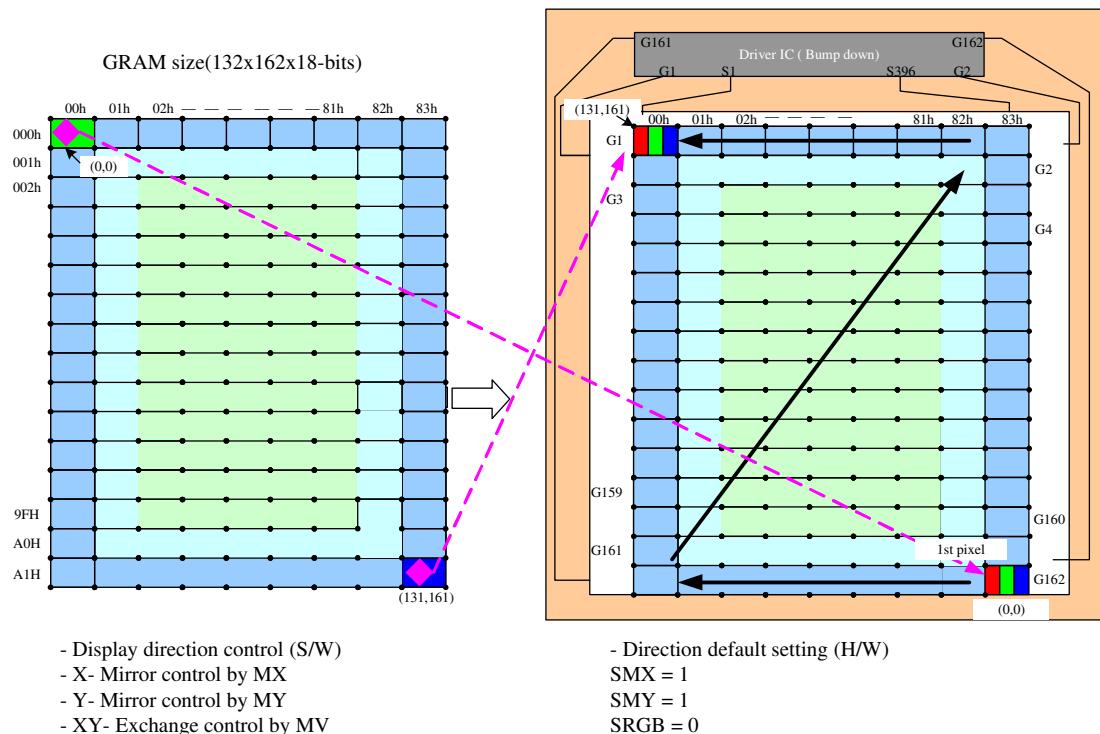
Case 6 of Resolution (132RGB x 162)(GM[2:0] = "000") RAM size = 132 x 162 x 18-bits(Used)

Display size = 132RGB x 162

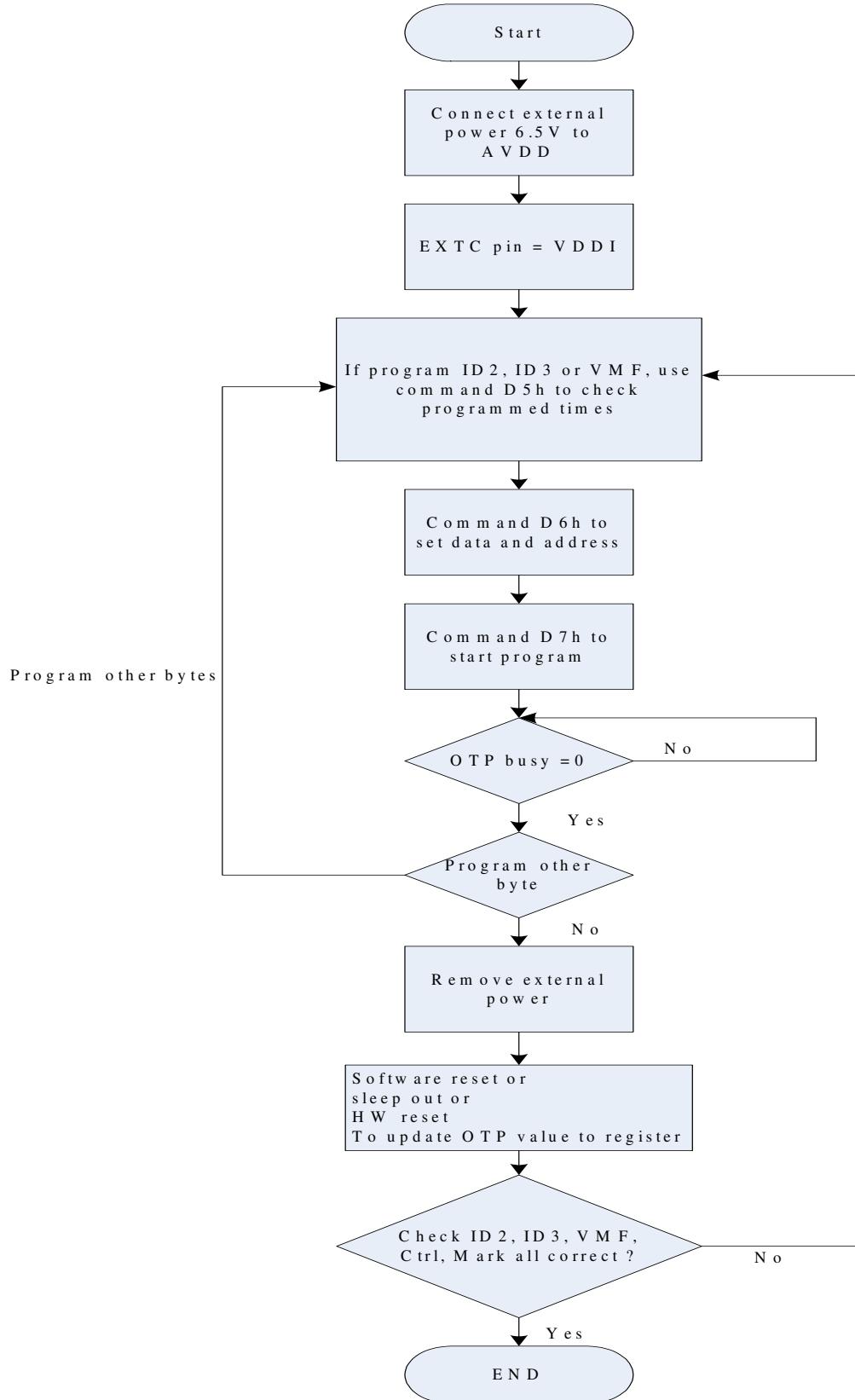
1) Example for $SMX=SMY='0'$



2) Example for $SMX=SMY='1'$



16. OTP Programming Flow



Note. Please remove external power 6.5V after programming.

17. Electrical Characteristics

17.1 Absolute Maximum Ratings

The absolute maximum rating is listed on following table. When ILI9163C is used out of the absolute maximum ratings, the ILI9163C may be permanently damaged. To use the ILI9163C within the following electrical characteristics limit is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded during normal operation, the ILI9163C will malfunction and cause poor reliability.

Item	Symbol	Unit	Value Note
Supply voltage	VCI	V	-0.3 ~ + 4.8
Supply voltage (Logic)	VDDI	V	-0.3 ~ + 4.6
Supply voltage (Digital)	VCC	V	-0.3 ~ + 2.4
Driver supply voltage	VGH-VGL	V	-0.3 ~ + 33.0
Logic input voltage range	VIN	V	-0.3 ~ VDDI + 0.3
Logic output voltage range	VO	V	-0.3 ~ VDDI + 0.3
Operating temperature	Topr	°C	-40 ~ + 85
Storage temperature	Tstg	°C	-55 ~ + 110

Notes: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

17.2 DC Characteristics

Item	Symbol	Unit	Condition	Min.	Typ.	Max.	Note
Power & Operation Voltage							
Analog Operating voltage	VCI	V	Operating voltage	2.5	2.78	4.8	Note2
Logic Operating voltage	VDDI	V	I/O supply voltage	1.65	1.8/2.78	3.3	Note2
Digital Operating voltage	VCC	V	Digital supply voltage		1.8		Note2
Gate Driver High voltage	VGH	V		10.0		16.0	Note3
Gate Driver Low voltage	VGL	V		-16.0		-7.5	Note3
Driver Supply voltage		V	VGH-VGL	19		32	Note3
Input/Output							
Logic High level input voltage	VIH	V		0.7VDDI		VDDI	Note1,2,3
Logic Low level input voltage	VIL	V		VSS		0.3VDDI	Note1,2,3
Logic High level output voltage	VOH	V	IOH = -1.0mA	0.8VDDI		VDDI	Note1,2,3
Logic High level output voltage	VOL	V	IOL = 1.0mA	VSS		0.2VDDI	Note1,2,3
Logic input leakage current	IIL	µA	VIN = VDDI or VSS	-0.1		+0.1	Note1,2,3
Sleep in current consumption	ISLP	µA	VCI=VDDI=2.8V Ta=25 °C			70	Note1,2,3
VCOM Operation							

VCOM High voltage	VCOMH	V	Ccom=12nF	2.5		5.0	Note 3
VCOM Low voltage	VCOML	V	Ccom=12nF	-2.5		0.0	Note 3
VCOM Amplitude voltage	VOMA	V	VCOMH-VCOML	4.0		5.5	Note 3
Source Driver							
Source output range	Vsout	V		0.1		AVDD-0.1	Note4
Gamma reference voltage	GVDD	V		3.0		5.0	Note3

Note 1: VDDI=1.65 to 3.3V, VCI=2.5 to 4.8V, AGND=GND=0V, Ta=-30 to 70°C (to +85°C no damage)

Note2: Please supply digital VDDI voltage equal or less than analog VCI voltage. ($VDDI \leq VCI$)

Note2,3,4: When the measurements are performed with LCD module. Measurement Points are like below.

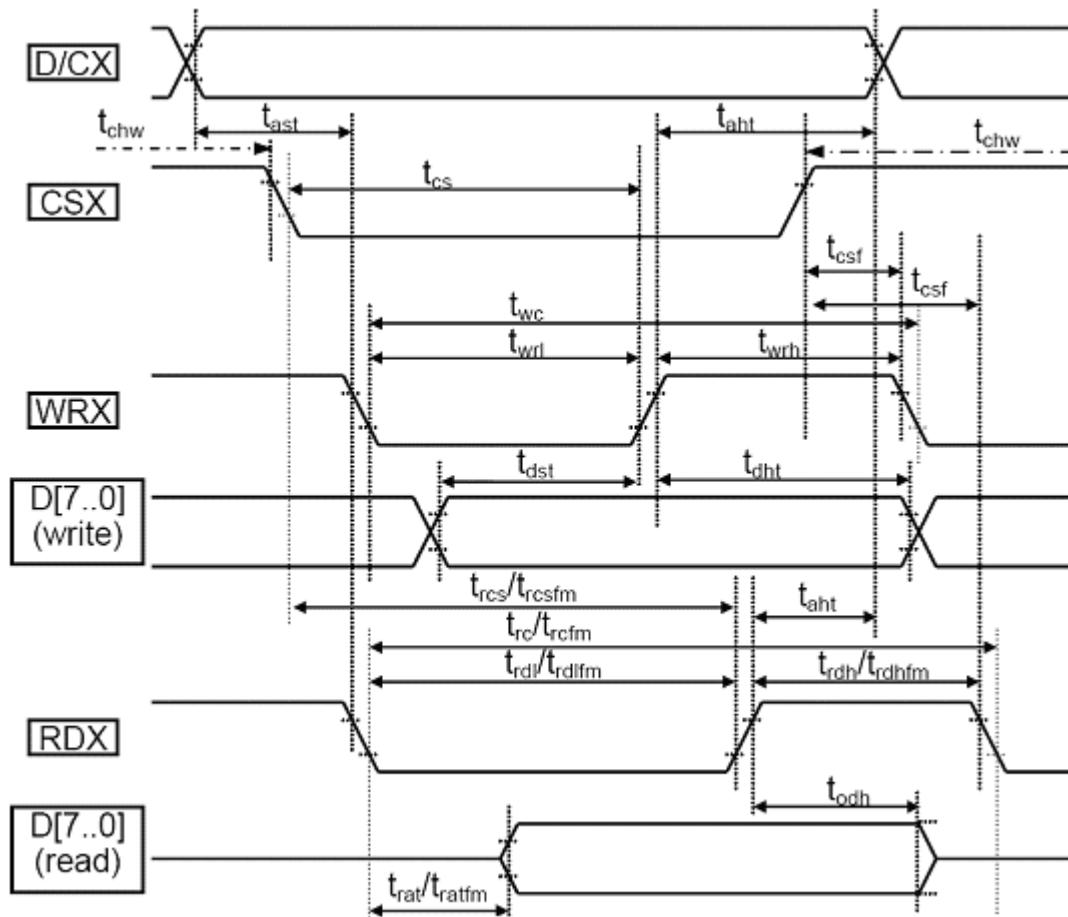
Note3: CSX, RDX, WRX, D[23:0], D/CX, RESX, TE, PCLK, VS, HS, DE, SDA, SCL, GM2, GM1, GM0, RCM1, RCM0, P68, IM2, IM1, IM0,

SRGB, REV, SMX, SMY, RL, TB, IDM, SHUT, PREG, GS and Test pins.

Note5: Source channel loading = 10pF/channel, Gate channel loading = 50pF/channel

17.3 AC Characteristics

17.3.1. Parallel CPU 18/16/9/8-bit Bus



Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

Table 17.3.1 AC characteristics of parallel CPU I/F in asynchronous mode

Signal	Symbol	Parameter	min	max	unit	description
D/CX	tast	Address setup time	0		ns	
	taht	Address hold time(Write/Read)	10		ns	
CSX	tchw	"S""H" Pulse Width	0		ns	
	tcs	Chip Select setup time (Write)	10		ns	
	trcs	Chip Select setup time (Read ID)	45		ns	
	trcsfm	Chip Select setup time (Read FM)	355		ns	
	tcsf	Chip Select Wait time(Write/read)	10		ns	
WRX	twc	Write cycle	66		ns	
	twrh	Controlpulse H duration	15		ns	
	twrl	Control pulse L duration	15		ns	
RDX	trc	Read cycle (ID)	160		ns	When read ID

	trdh	Control pulse H duration(ID)	90		ns	data
	trdl	Control pulse L duration(ID)	45		ns	
RDX	trcfm	Read cycle (FM)	450		ns	When read from frame memory
	trdhfm	Control pulse H duration (FM)	90		ns	
	trdlfm	Control pulse L duration (FM)	355		ns	
D[17..0]	tdst	Data setup time	10		ns	For maximum CL = 30pF
	tdht	Data hold time	10		ns	
	trat	Read access time (ID)		40	ns	For minimum CL = 8pF
	tratfm	Read access time (FM)		340	ns	
	todh	Output disable time	20	80	ns	

Note 1: VDDI 1.65 to 3.3V, VCI=2.6 to 3.3V, AGND=GND=0V, Ta=-30 to 70 °C (to +85°C no damage)

Note 2: This input signal rise time and fall time (tr, tf) is specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for input signals

17.3.2. Display Serial Interface (SPI)

17.3.2.1 3-pin Serial Interface

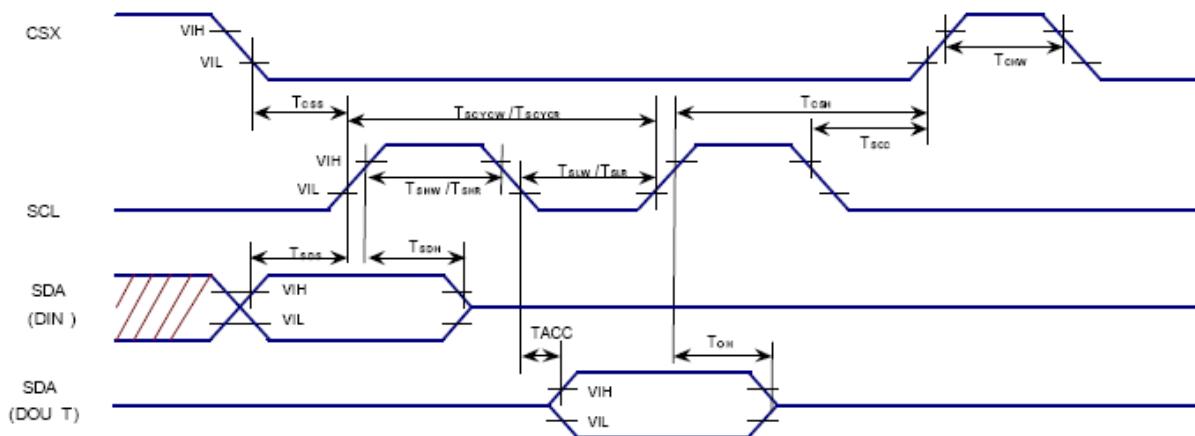


Table 17.3.2.1: 3-pin Serial Interface Characteristics

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
CSX	TCSS	Chip select setup time	10		ns	
	TCSH	Chip select hold time	30		ns	
	TCHW	Chip select "H" pulse width	30		ns	
SCL	TSCYCW	Serial clock cycle(Write)	66		ns	
	TSHW	S“L”"H" pulse width(Write)	15		ns	
	TSLW	S“L”"L" pulse width(Write)	15		ns	
	TSCYCR	Serial clock cycle(Read)	150		ns	
	TSHR	S“L”"H" pulse width(Read)	60		ns	
	TSLR	S“L”"L" pulse width(Read)	60		ns	
SDA(DIN) (DOUT)	TSDS	Data setup time	5		ns	
	TSDH	Data hold time	5		ns	
	TACC	Access time	5	50	ns	For maximum CL = 30pF
	TOH	Output disable time	10		ns	For minimum CL = 8pF

Note 1: VDDI=1.65 to 3.3V, VCI=2.6 to 3.3V, AGND=GND=0V. Ta=-30 to 70°C (to +85°C no damage)

Note 2 : The input signal rise time and fall time(t_r , t_f) is specified at 15 ns or less.

Logic high and low levels are specified as 10% and 90% of VDDI for Input signals.

17.3.2.2 4-pin Serial Interface

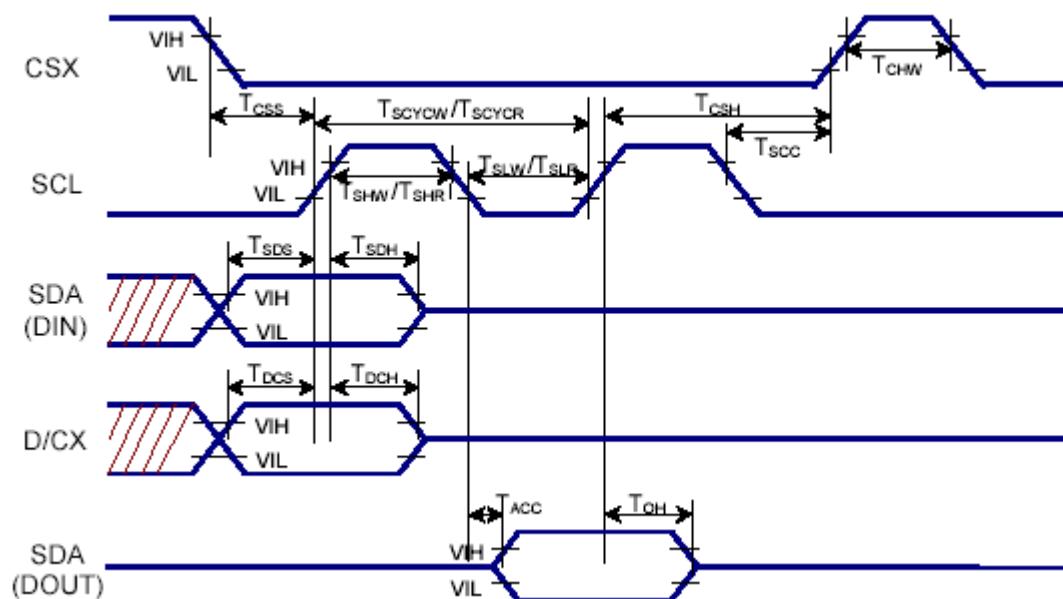


Table 17.3.2.2: 4 pin Serial Interface Characteristics

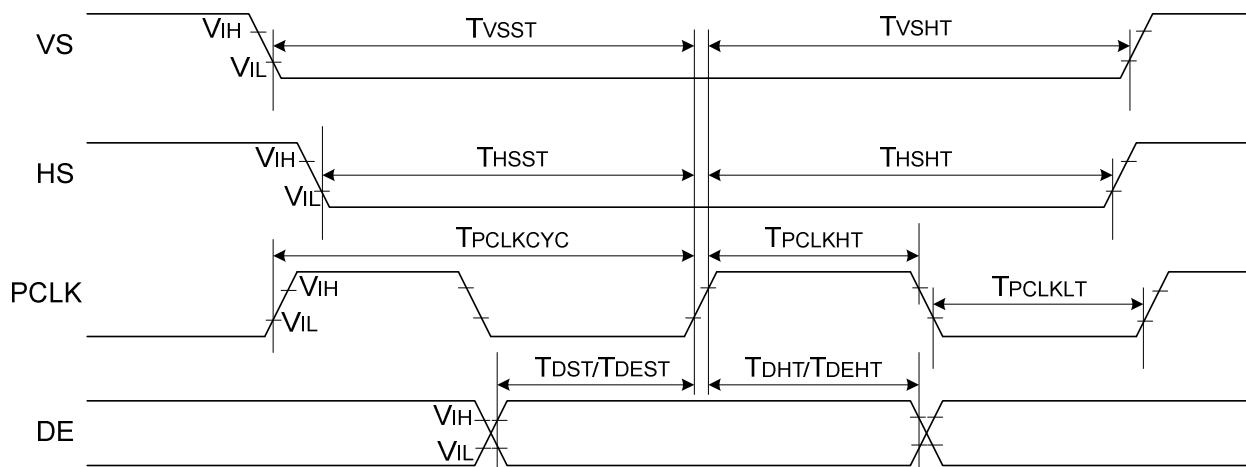
Signal	Symbol	Parameter	MIN	MAX	Unit	Description
CSX	TCSS	Chip select setup time	10		ns	
	TCSH	Chip select hold time	30		ns	
	TCHW	Chip select "H" pulse width	30		ns	
SCL	TSCYCW	Serial clock cycle(Write)	66		ns	
	TSHW	S“L”“H” pulse width(Write)	15		ns	
	TSLW	S“L”“L” pulse width(Write)	15		ns	
	TSCYCR	Serial clock cycle(Read)	150		ns	
	TSHR	S“L”“H” pulse width(Read)	60		ns	
	TSLR	S“L”“L” pulse width(Read)	60		ns	
D/CX	TDCS	D/CX setup time	5		ns	
	TDCH	D/CX hold time	5		ns	
SDA(DIN) (DOUT)	TSDS	Data setup time	5		ns	
	TSDH	Data hold time	5		ns	
	TACC	Access time	5	50	ns	For maximum CL = 30pF
	TOH	Output disable time	10		ns	For minimum CL = 8pF

Note 1: VDDI=1.65 to 3.3V, VCI=2.6 to 3.3V, AGND=GND=0V. Ta=-30 to 70°C (to +85°C no damage)

Note 2 : The input signal rise time and fall time(t_r , t_f) is specified at 15 ns or less.

Logic high and low levels are specified as 10% and 90% of VDDI for Input signals.

17.3.3. Parallel RGB 18/16/6-bit Bus



Signal	Symbol	Parameter	MIN	MAX	Unit	Description
PCLK	TPCLKCYC	TPCLK Cycle time	66	-	ns	
	TPCLKLT	Pixel low pulse width	15	-	ns	
	TPCLKHT	Pixel high pulse width	15	-	ns	
VS	TVSST	Vertical Sync. setup time	15	-	ns	
	TVSHT	Vertical Sync. hold time	15	-	ns	
HS	THSST	Horizontal Sync. setup time	15	-	ns	
	THSHT	Horizontal Sync. hold time	15	-	ns	
DE	TDEST	Data Enable setup time	15	-	ns	
	TDEHT	Data Enable hold time	15	-	ns	
D[17:0]	TDST	Data setup time	15	-	ns	
	TDHT	Data hold time	15	-	ns	

18. Revision History

Version No.	Date	Page	Description
V0.01	2009/12/28		New Created
V0.02	2010/2/2	130	Tearing effect description
V0.03	2010/2/26	179	
V0.04	2010/3/24	191~197	AC/DC timing revise
		43	modify type error in Figure 31
V0.05	2010/3/31	101	Sleep out description
		10	Modify SMX/SMY decription
		157	Modify C1h default vaule
		14	Modify Au bump hight and remove 400um chip thickness
V0.06	2010/5/10	10	Modify SDA description
V0.07	2010/5/26	11	LCM[0:1]
V0.08	2010/7/30	12 69~71	Modify TESEL description Add Gamma structure
V0.09	2010/9/01	13 14 22	To modify VCL description Add 300um chip thickness SPI 3-wire/4-wire write
V0.10	2011/01/18	193	Add sleep in current