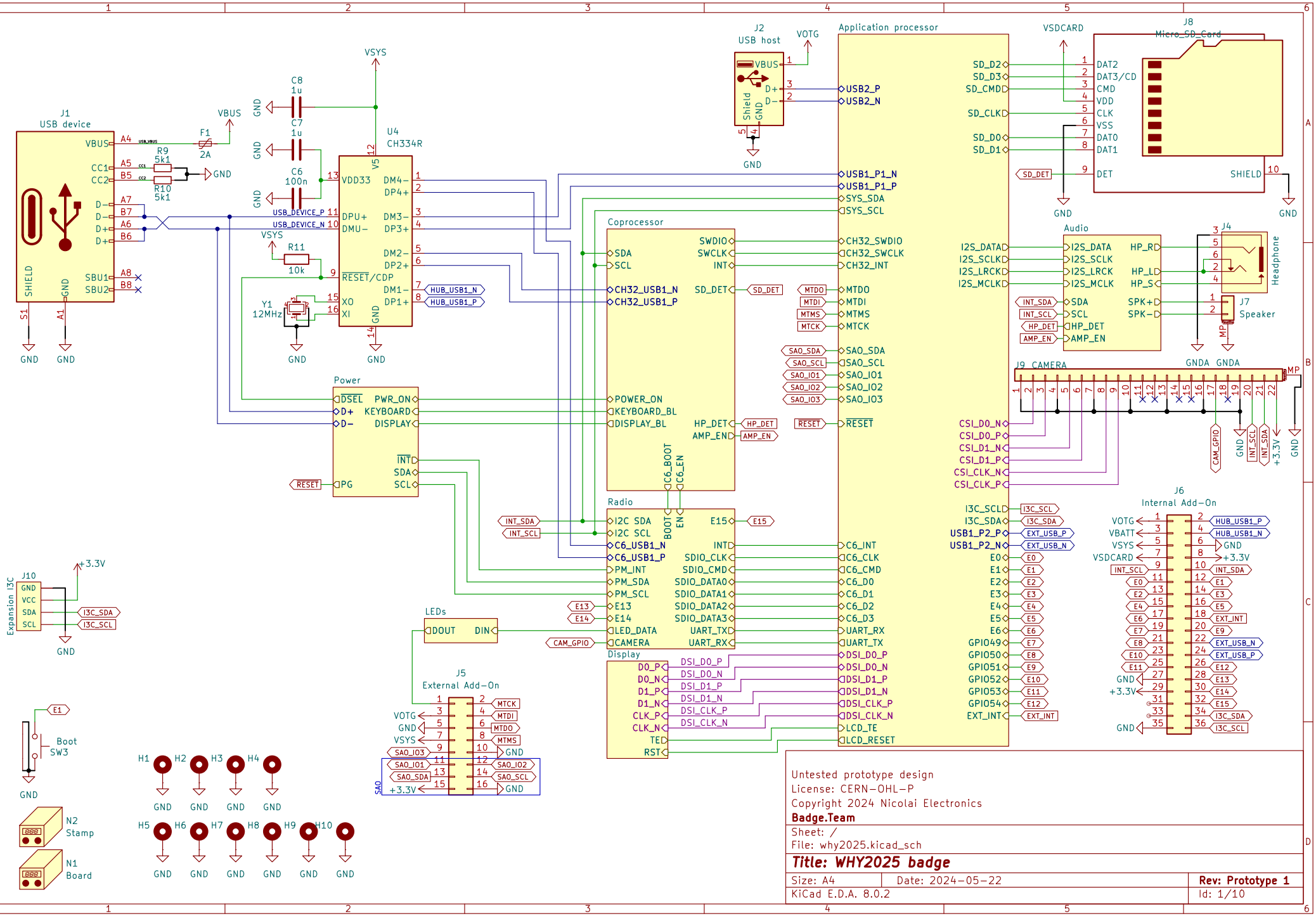
J1
USB device
VBUS
CC1
CC2
D−
D+
SHIELD
GND
SBU1
SBU2
F1
2A
R9
5k1
R10
5k1
C8
1u
C7
1u
C6
100n
U4
CH334R
VDD33
DPU+
DMU−
RESET/CDP
XO
XI
DM4−
DP4+
DM3−
DP3+
DM2−
DP2+
DM1−
DP1+
R11
10k
Y1
12MHz
USB_DEVICE_P
USB_DEVICE_N
HUB_USB1_N
HUB_USB1_P
Power
DSEL
PWR_ON
KEYBOARD
DISPLAY
PG
INT
SDA
SCL
J2
USB host
VOTG
Shield
Application processor
USB2_P
USB2_N
USB1_P1_N
USB1_P1_P
SYS_SDA
SYS_SCL
Coprocessor
SWDIO
SWCLK
INT
SDA
SCL
CH32_USB1_N
CH32_USB1_P
SD_DET
MTDO
MTDI
MTMS
MTCK
SAO_SDA
SAO_SCL
SAO_IO1
SAO_IO2
SAO_IO3
POWER_ON
KEYBOARD_BL
DISPLAY_BL
HP_DET
AMP_EN
RESET
C6_BOOT
C6_EN
Radio
I2C SDA
I2C SCL
C6_USB1_N
C6_USB1_P
PM_INT
PM_SDA
PM_SCL
E13
E14
LED_DATA
CAMERA
E15
BOOT
EN
INT
SDIO_CLK
SDIO_CMD
SDIO_DATA0
SDIO_DATA1
SDIO_DATA2
SDIO_DATA3
UART_TX
UART_RX
Display
D0_P
D0_N
D1_P
D1_N
CLK_P
CLK_N
TE
RST
DSI_D0_P
DSI_D0_N
DSI_D1_P
DSI_D1_N
DSI_CLK_P
DSI_CLK_N
LCD_TE
LCD_RESET
C6_INT
C6_CLK
C6_CMD
C6_D0
C6_D1
C6_D2
C6_D3
UART_RX
UART_TX
CAM_GPIO
LEDs
DOUT
DIN
J5
External Add−On
SAO
J10
Expansion I3C
I3C_SDA
I3C_SCL
VSDCARD
J8
Micro_SD_Card
SD_D2
SD_D3
SD_CMD
SD_CLK
SD_D0
SD_D1
DAT2
DAT3/CD
CMD
VDD
CLK
VSS
DAT0
DAT1
DET
SHIELD
Audio
I2S_DATA
I2S_SCLK
I2S_LRCK
I2S_MCLK
HP_R
HP_L
HP_S
SPK+
SPK−
HP_DET
AMP_EN
J4
Headphone
J7
Speaker
J9 CAMERA
CSI_D0_N
CSI_D0_P
CSI_D1_N
CSI_D1_P
CSI_CLK_N
CSI_CLK_P
J6
Internal Add−On
GPIO49
GPIO50
GPIO51
GPIO52
GPIO53
GPIO54
EXT_INT
EXT_USB_P
EXT_USB_N
Boot
SW3
N2
Stamp
N1
Board
H1
H2
H3
H4
H5
H6
H7
H8
H9
H10
Untested prototype design
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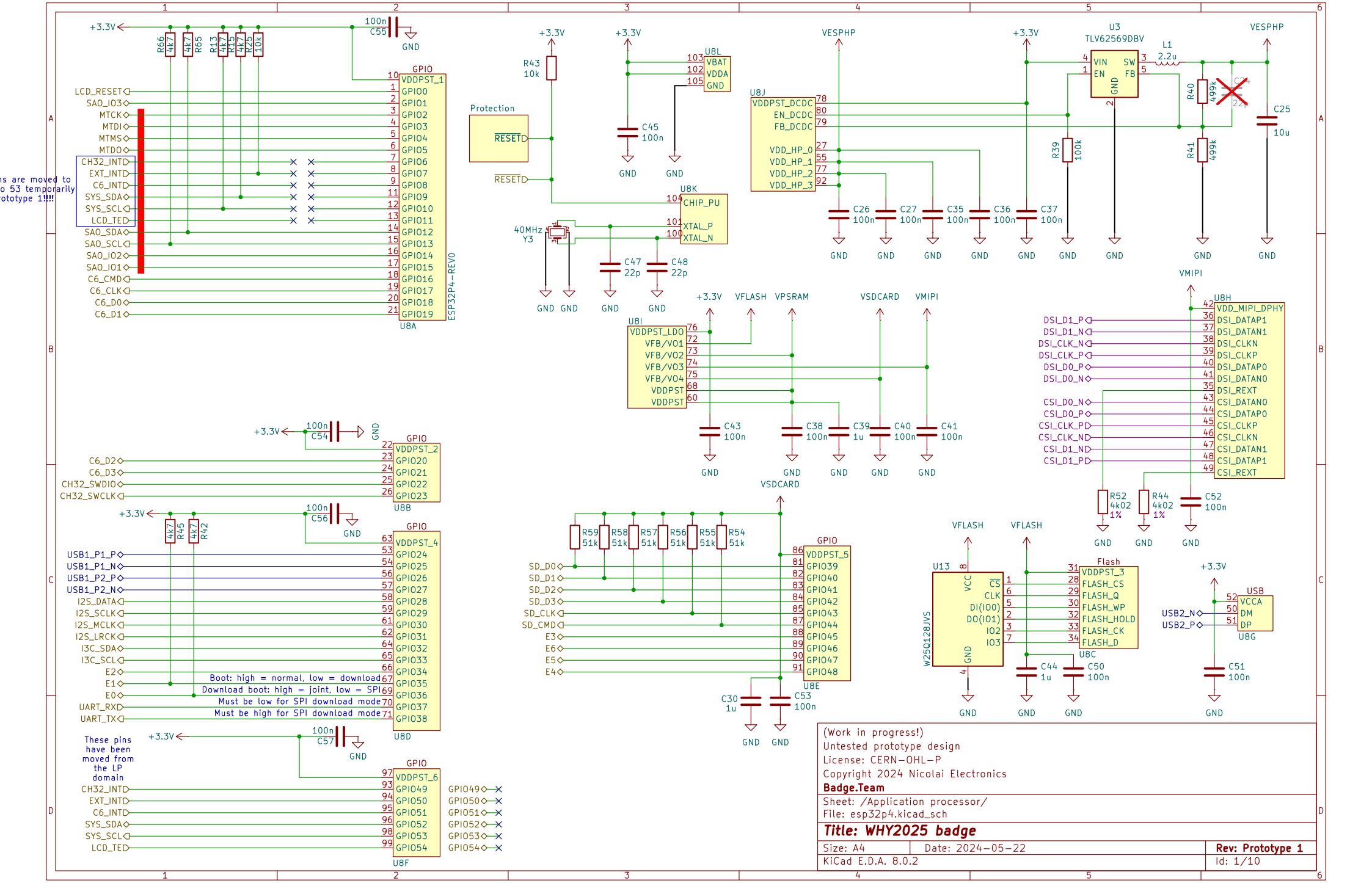
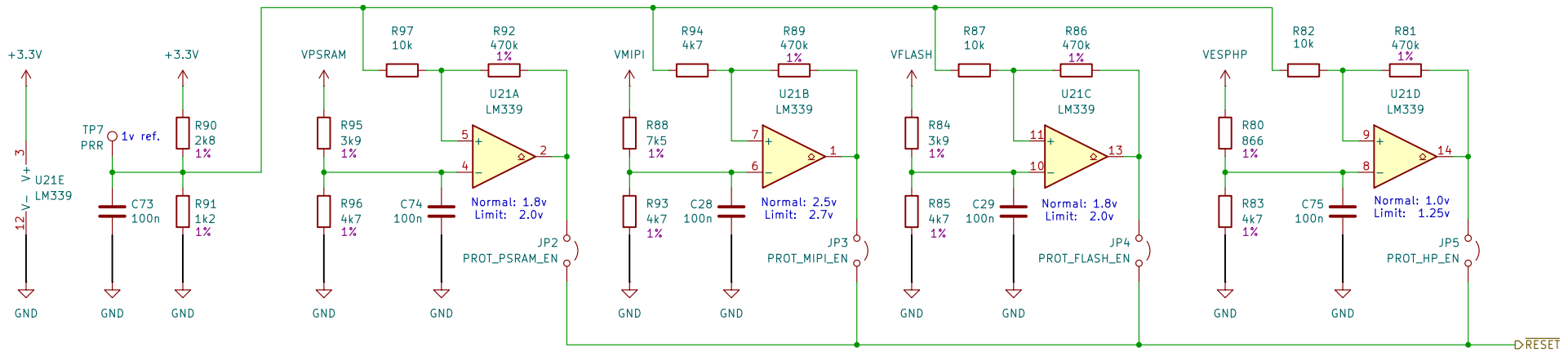
Copyright 2024 Nicolai Electronics
Badge.Team
Sheet: /
File: why2025.kicad_sch
Title: WHY2025 badge
Size: A4
Date: 2024−05−22
Rev: Prototype 1
KiCad E.D.A. 8.0.2
Id: 1/10


+3.3V
R66 4k7
R65 4k7
R13 4k7
R15 4k7
R25 4k7
10k
100n C55
GND
GPIO
VDDPST_1
GPIO0
GPIO1
GPIO2
GPIO3
GPIO4
GPIO5
GPIO6
GPIO7
GPIO8
GPIO9
GPIO10
GPIO11
GPIO12
GPIO13
GPIO14
GPIO15
GPIO16
GPIO17
GPIO18
GPIO19
ESP32P4-REV0
U8A
LCD_RESET
SAO_IO3
MTCK
MTDI
MTMS
MTDO
CH32_INTD
EXT_INTD
C6_INTD
SYS_SDA
SYS_SCL
LCD_TED
SAO_SDA
SAO_SCL
SAO_IO2
SAO_IO1
C6_CMD
C6_CLK
C6_D0
C6_D1
ns are moved to
o 53 temporarily
rototype 1!!!!
Protection
RESET
R43 10k
U8L
VBAT
VDDA
GND
C45 100n
U8K
CHIP_PU
XTAL_P
XTAL_N
40MHz
Y3
C47 22p
C48 22p
U8J
VDDPST_DCDC
EN_DCDC
FB_DCDC
VDD_HP_0
VDD_HP_1
VDD_HP_2
VDD_HP_3
C26 100n
C27 100n
C35 100n
C36 100n
C37 100n
U3
TLV62569DBV
VIN
SW
EN
FB
L1 2.2u
R40 499k
C24 22p
R39 100k
R41 499k
C25 10u
VESPHP
U8I
VDDPST_LDO
VFB/VO1
VFB/VO2
VFB/VO3
VFB/VO4
VDDPST
C43 100n
C38 100n
C39 1u
C40 100n
C41 100n
VFLASH
VPSRAM
VSDCARD
VMIPI
U8H
VDD_MIPI_DPHY
DSI_D1_P
DSI_D1_N
DSI_CLK_N
DSI_CLK_P
DSI_D0_P
DSI_D0_N
DSI_DATAP1
DSI_DATAN1
DSI_CLKN
DSI_CLKP
DSI_DATAP0
DSI_DATAN0
DSI_REXT
CSI_D0_N
CSI_D0_P
CSI_CLK_P
CSI_CLK_N
CSI_D1_N
CSI_D1_P
CSI_DATAN0
CSI_DATAP0
CSI_CLKP
CSI_CLKN
CSI_DATAN1
CSI_DATAP1
CSI_REXT
R52 4k02 1%
R44 4k02 1%
C52 100n
C54 100n
U8B
C6_D2
C6_D3
CH32_SWDIO
CH32_SWCLK
C56 100n
R45 4k7
R42 4k7
U8D
USB1_P1_P
USB1_P1_N
USB1_P2_P
USB1_P2_N
I2S_DATA
I2S_SCLK
I2S_MCLK
I2S_LRCK
I3C_SDA
I3C_SCL
E2
E1
E0
UART_RX
UART_TX
Boot: high = normal, low = download
Download boot: high = joint, low = SPI
Must be low for SPI download mode
Must be high for SPI download mode
These pins
have been
moved from
the LP
domain
C57 100n
U8F
CH32_INTD
EXT_INTD
C6_INTD
SYS_SDA
SYS_SCL
LCD_TED
GPIO49
GPIO50
GPIO51
GPIO52
GPIO53
GPIO54
R59 51k
R58 51k
R57 51k
R56 51k
R55 51k
R54 51k
U8E
SD_D0
SD_D1
SD_D2
SD_D3
SD_CLK
SD_CMD
E3
E6
E5
E4
C30 1u
C53 100n
U13
W25Q128JVS
CS
CLK
DI(IO0)
DO(IO1)
IO2
IO3
C44 1u
C50 100n
U8C
Flash
FLASH_CS
FLASH_Q
FLASH_WP
FLASH_HOLD
FLASH_CK
FLASH_D
USB
VCCA
DM
DP
U8G
USB2_N
USB2_P
C51 100n
(Work in progress!)
Untested prototype design
License: CERN-OHL-P
Copyright 2024 Nicolai Electronics
Badge.Team
Sheet: /Application processor/
File: esp32p4.kicad_sch
Title: WHY2025 badge
Size: A4
Date: 2024-05-22
Rev: Prototype 1
KiCad E.D.A. 8.0.2
Id: 1/10



The protection for the software programmable LDO outputs of the ESP32P4.
We want to limit the LDO voltages to U_nom +0.3V. If that occurs, the ESP32P4 $\overline{\text{RESET}}$ signal will become low.

This circuit uses a LM339 quad comparator with a reference voltage of 1.0 V. The circuit uses a threshold at +0.2V above nominal. They are configured as an inverting comparator with hysteresis. The LM339 has open collector outputs, so we can combine them.

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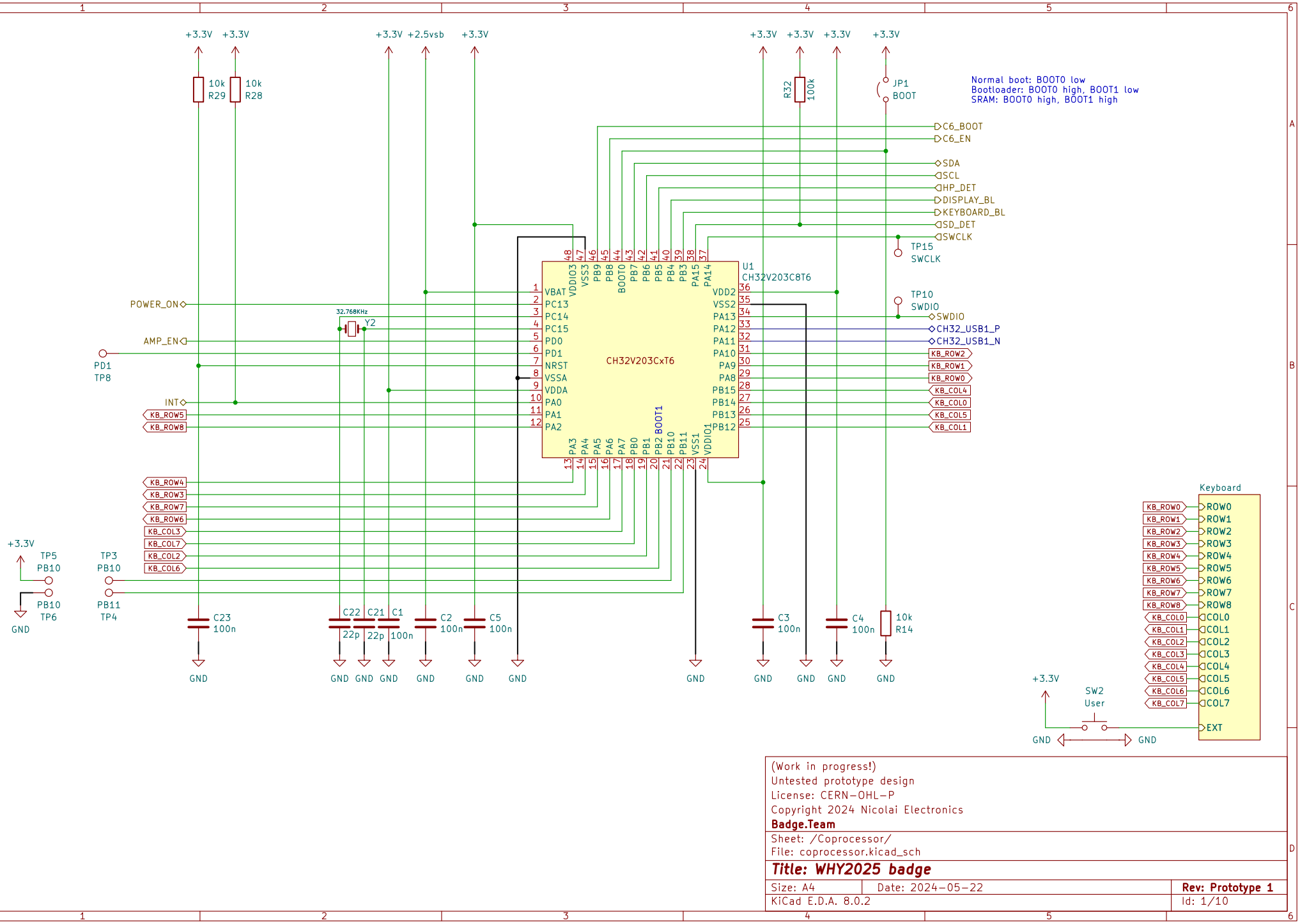
Sheet: /Application processor/Protection/
File: protection.kicad_sch

Title: WHY2025 badge

Size: A4	Date: 2024-05-22	**Rev: Prototype 1**
KiCad E.D.A. 8.0.2		Id: 1/10



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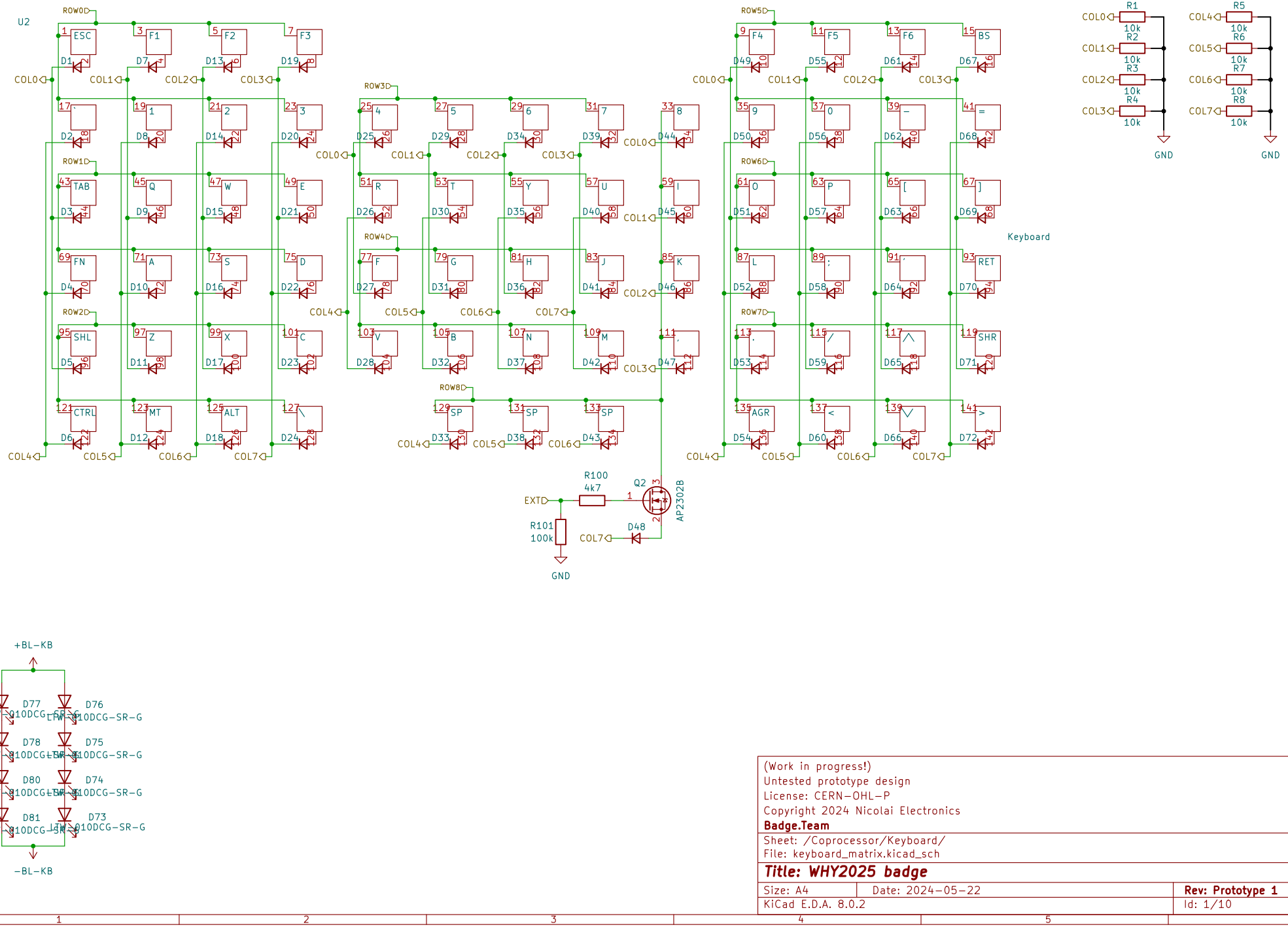
Sheet: /Coprocessor/
File: coprocessor.kicad_sch

Title: WHY2025 badge

Size: A4	Date: 2024-05-22	**Rev: Prototype 1**
KiCad E.D.A. 8.0.2		Id: 1/10



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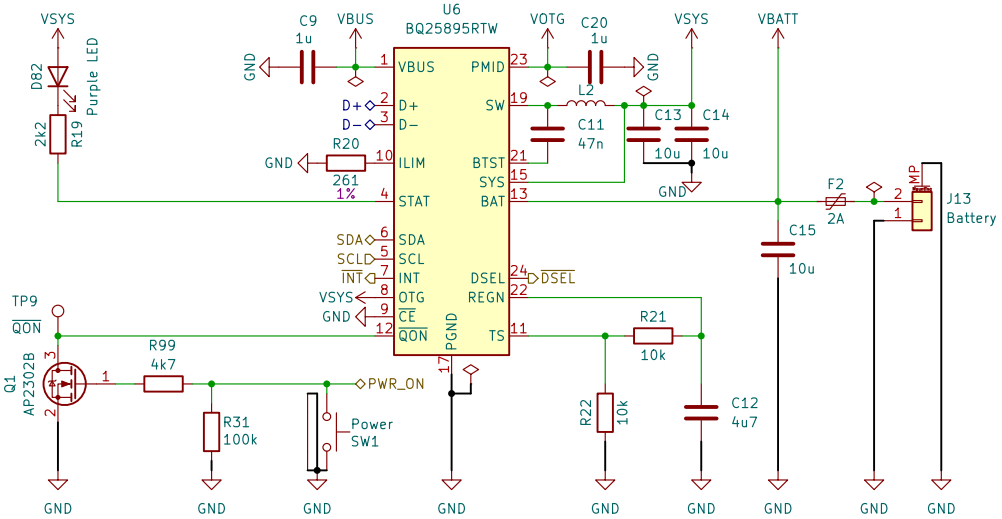
Sheet: /Coprocessor/Keyboard/
File: keyboard_matrix.kicad_sch

Title: WHY2025 badge

Size: A4	Date: 2024-05-22	**Rev: Prototype 1**
KiCad E.D.A. 8.0.2		Id: 1/10

PMIC

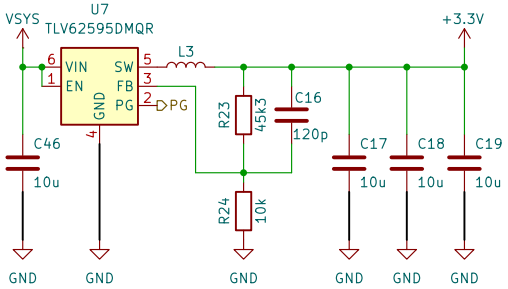


DSEL is an open−drain output, pulled low when the D+/D− pins are in use for charger detection.
D+/D− float otherwise.

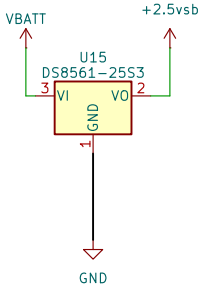
Watch out with the I2C bus of this device, wrong configuration can be dangerous.

VBUS is the voltage coming from the input USB−C port. This voltage can be 5 up to 14 volts.
VOTG is 5V generated from VBATT or VBUS depending on the power source of the system.
VBATT is connected to the rechargeable battery.
VSYS is an unregulated 3.5 to 4.5v output used to power the DC−DC converters for the rest of the components.

3.3v DC/DC

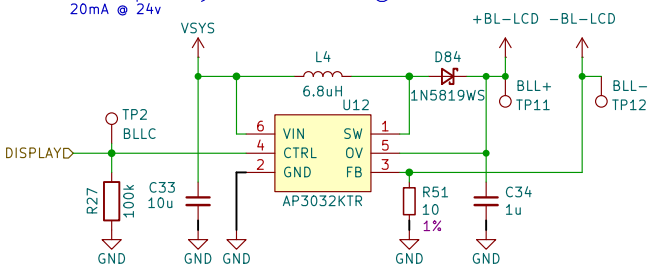


Standby



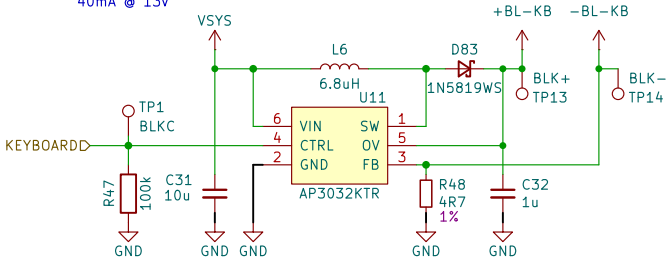
Display backlight DC/DC

20mA @ 24v



Keyboard backlight DC/DC

40mA @ 13v



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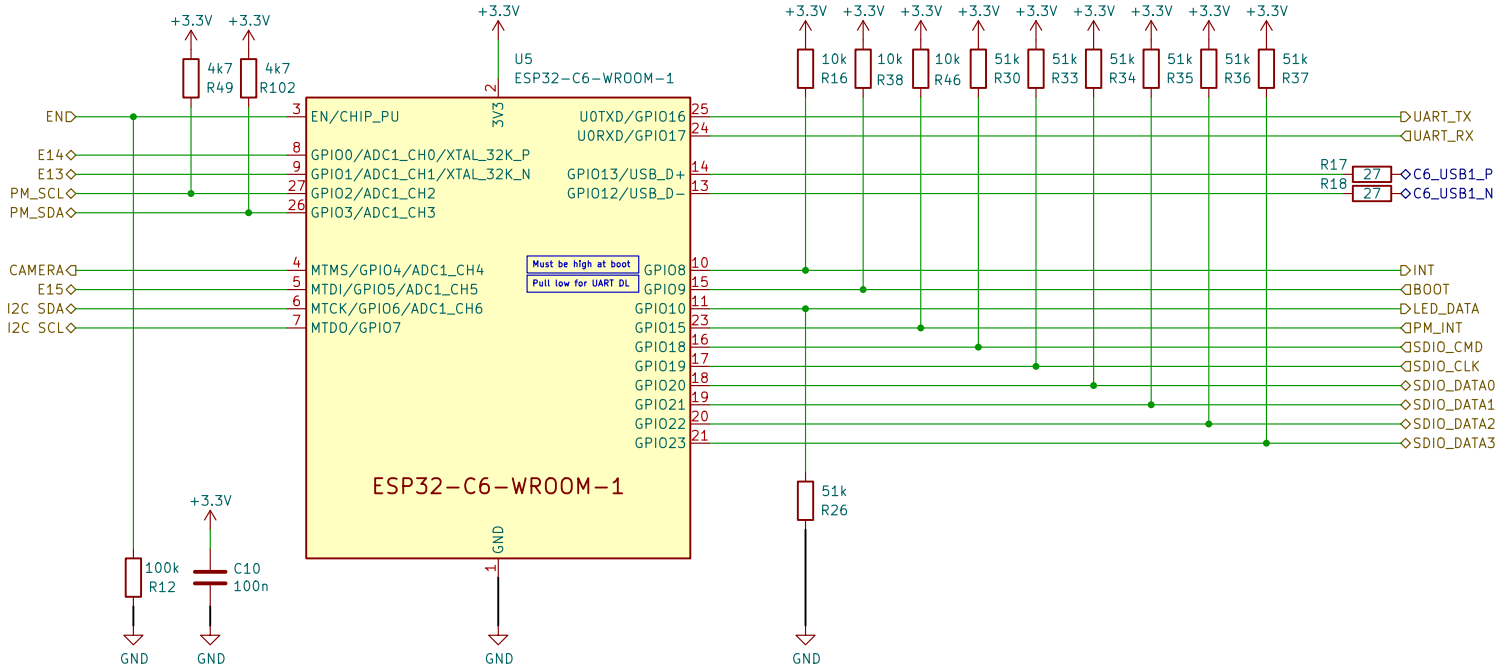
Sheet: /Power/
File: power.kicad_sch

Title: WHY2025 badge

Size: A4	Date: 2024−05−22	**Rev: Prototype 1**
KiCad E.D.A. 8.0.2		Id: 1/10



Bootstrapping pins:
- GPIO8: Has to be high at power on
- GPIO9: Connect to pull-up resistor, pull to GND to start download mode

Low power peripherals:
- UART: RX on GPIO4, TX on GPIO5
- I2C: SDA on GPIO6, SCL on GPIO7

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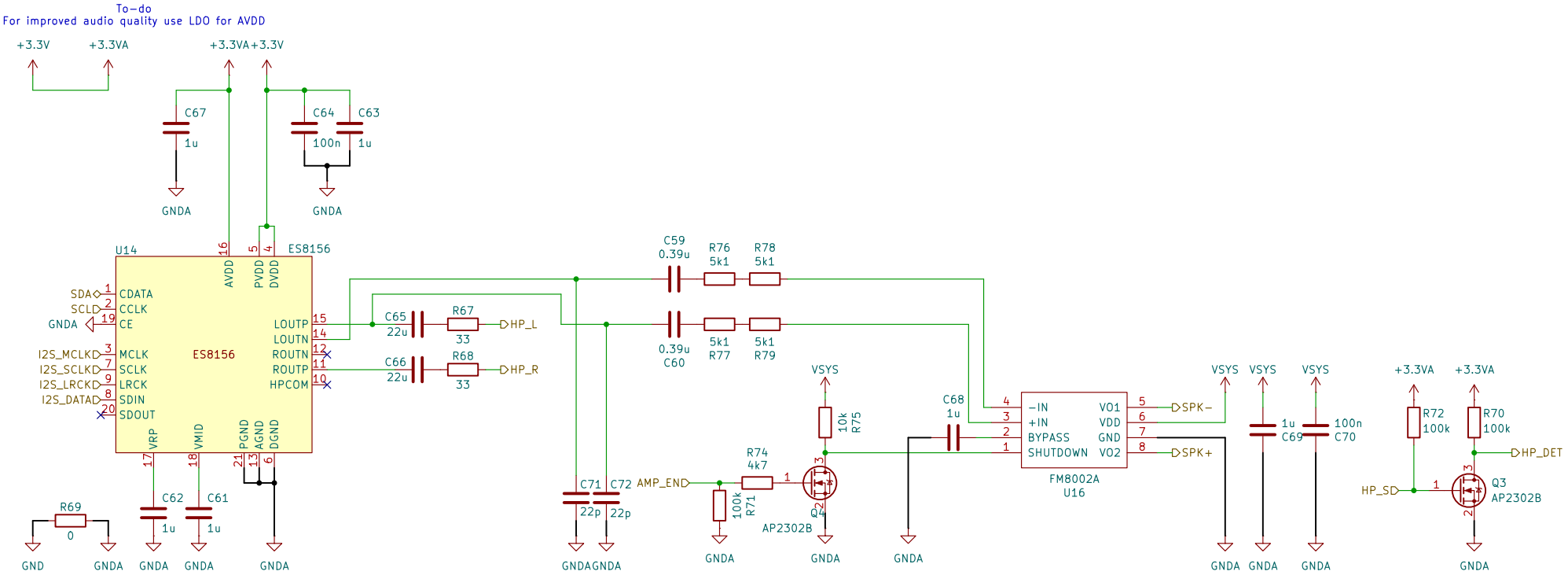
Sheet: /Radio/
File: radio.kicad_sch

Title: WHY2025 badge

Size: A4	Date: 2024-05-22	**Rev: Prototype 1**
KiCad E.D.A. 8.0.2		Id: 1/10



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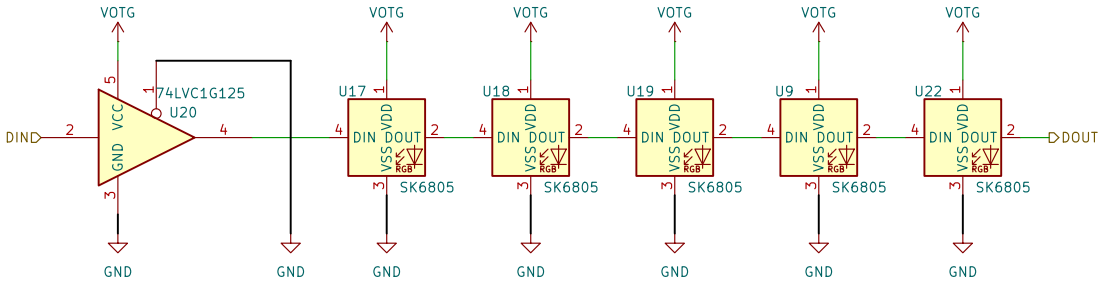
Sheet: /Audio/
File: audio.kicad_sch

Title: WHY2025 badge

Size: A4	Date: 2024-05-22	**Rev: Prototype 1**
KiCad E.D.A. 8.0.2		Id: 1/10



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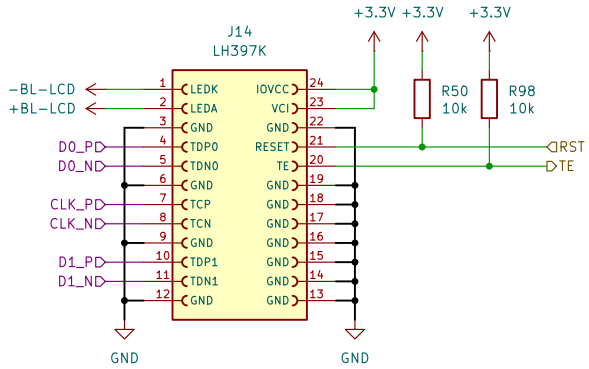
Sheet: /LEDs/
File: leds.kicad_sch

Title: WHY2025 badge

Size: A4	Date: 2024-05-22	**Rev: Prototype 1**
KiCad E.D.A. 8.0.2		Id: 1/10



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Sheet: /Display/
File: display.kicad_sch

Title: WHY2025 badge

Size: A4	Date: 2024-05-22	**Rev: Prototype 1**
KiCad E.D.A. 8.0.2		Id: 1/10