

DC-DC Converter for PV Module Integration

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Master's Project



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This report has been written with \LaTeX using TeXstudio. During the project PLECS, MATLAB and LTspice have been used for simulations, while the RT-box from Plexim has been used for implementation of the control system. The creation of flow charts have been done using www.draw.io. Hardware schematic and PCB layout have been created using Altium Designer.



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Abstract:

PV modules must work at their Maximum Power Point (MPP) to achieve the highest efficiency. Several environmental conditions like partial shading and temperature change can reduce the output power of the PV modules. The goal of this project is to design a Module Integrated Converter (MIC) for a PV module. It should be able to drive the PV at its MPP when the weather conditions change. A MIC consist of a DC-DC converter and a Maximum Power Point Tracking (MPPT) algorithm. It is decided to implement a non-inverting buck-boost converter with a Perturb and Observe (P&O) MPPT algorithm. The objective of the project is to be able to drive a PV module at its MPP constantly regardless of the environmental conditions.

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Preface

This paper describes the report of the group project "DC-DC converter for PV module integration." It has been developed from the 10th of September to the 19th of December of 2018, at Aalborg University, Institute of Energy, by the group INTRO-760.

This document discusses the procedure and results of a DC to DC converter design to maximize the energy obtained from photovoltaic generation.

The literature references are shown in square brackets, with a number referring to a specific document which can be found in the bibliography. If the reference is after the dot, it means that it refers to the whole previous paragraph. Pictures and tables will be denoted in the X,Y format, with X representing the chapter and Y the figure or table number. The process and development has been based on the Problem Based Learning (PBL) method.

Aalborg University, December 14, 2018

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Nomenclature

Abbreviations:

AC	Alternating Current
ADC	Analog to Digital Converter
BW	Bandwidth
DC	Direct Current
FET	Field-Effect Transistor
FSM	Finite State Machine
IC	Integrated Circuit
LPF	Low Pass Filter
MIC	Module Integrated Converter
MOSFET	Metal Oxide Semiconductor Field-Effect Transistor
MPP	Maximum Power Point
MPPT	Maximum Power Point Tracking
PBL	Problem Based Learning
PCB	Printed Circuit Board
PLECS	Piecewise Linear Electrical Circuit Simulation
PV	Photovoltaic
PWM	Pulse Width Modulation
P&O	Perturb and Observe
RT Box	Response Time Box
SPICE	Simulation Program with Integrated Circuits Emphasis
STC	Standard Test Conditions

Symbols:

ΔI_L	Inductor current ripple
ΔV_{in}	Input voltage ripple
ΔV_{out}	Output voltage ripple
η	Efficiency
η_{mpp}	MPP efficiency
a	Diode's quality factor
C	Capacitance
C_{in}	Input capacitor
C_{out}	Output capacitor
D	Duty cycle
D_{boost}	Boost mode duty cycle
D_{buck}	Buck mode duty cycle
E	Energy
f	Frequency
f_c	Corner frequency
I	Current
I_{DS}	Drain-to-source current
I_{in}	Input current
I_{mpp}	MPP current
I_{out}	Output current
I_o	Diode's saturation current
I_{ph}	Photogenerated current
I_{pv}	PV panel's current
I_{sc}	Short-circuit current
k	Constant
K	Boltzmann constant
L	Inductance
N	Number of solar panels
N_s	Number of series connected solar cells
P	Power
P_{cond}	Conduction losses
P_{max}	Maximum power
P_{mpp}	MPP power
q	Electrical charge
R	Resistance
$R_{driverout}$	Output resistance of the driver
R_{DS}	Drain-to-source resistance
R_L	Load resistance
$R_{limiting}$	External gate resistor
R_{MOSFET}	Internal gate resistor

R_p	Parallel resistance
R_s	Series resistance
$R_{thermal}$	Thermal resistance
t	Time
T	Temperature
$T_{housing}$	Ambient temperature
T_J	Junction temperature
T_{sw}	Switching period
V	Voltage
V_{DD}	Supply voltage
V_{DS}	Drain-to-source voltage
V_{GS}	Gate-to-source voltage
V_{in}	Input voltage
V_{mpp}	MPP voltage
V_{oc}	Open-circuit voltage
V_{out}	Output voltage
V_{pv}	PV panel's voltage
V_t	Thermal voltage
V_{th}	Threshold voltage

Introduction

To this date, sustainable energy sources have become an area of worldwide focus in an attempt to reduce the environmental impact due to emissions of CO₂ and other greenhouse gasses. The development of competitive systems to exploit renewable energy sources is the best alternative to reduce the use of fossil fuels for the production of electricity. Over the last years, there has been a considerable increase in electricity production from renewable energy sources being the fastest growing sectors wind and solar energy. In 2017, photovoltaic generation was the renewable energy source which experienced the highest increase in newly installed capacity. The total installed capacity reached approximately 402 GW[1].

Photovoltaic (PV) is referred to the production of electricity in the form of direct current (DC) directly from sunlight shining on solar cells. Solar cells are semiconductor devices which typically can produce around 0.5 V DC so they are connected to form a PV panel. These panels can also be connected to other PV panels resulting in a PV array [2]. This way, according to the system's requirements, the PV panels can be interconnected in series or parallel in order to get at the output a higher voltage or current, respectively.

Nevertheless, it is important to keep into consideration the mismatches that may appear on the power generated by the different PV panels. Mismatches can be caused by partial shading, manufacturing tolerances, defects in the PV modules due to weather conditions and ageing among others. Even a small mismatch can result in a high reduction of the power production from the entire PV array [3]. This results in losses in the PV system which can be reduced by forcing every PV module to work at its Maximum Power Point (MPP) by using a Maximum Power Point Tracking (MPPT) unit. This can be reached by using electronic devices called Module Integrated Converters (MICs). MICs consist on DC-AC micro inverters or DC-DC converters that incorporate a MPPT controller. The MPPT is used to ensure that the power generated is the one corresponding to the MPP of the panel [3].

1.1 Photovoltaic generation

The generation of direct current electricity from solar energy is a phenomenon known as *Photovoltaic effect* which was first discovered by a French physicist named

Edmond Becquerel in 1839 [4]. This phenomenon allows the generation of electrical energy in a solar cell, when it is exposed to the sunlight [4]. The greater the intensity of the light (irradiance) that is absorbed by the PV panel, the higher the amount of electric power generated. On the other hand, the efficiency of the panel decreases with increasing temperature [2]. When the solar cell's temperature increases it results in a slightly increase of the generated current, however, the voltage decreases considerably [2]. This results in a reduction of the power generated by the solar panel.

Some of the most important parameters associated to a PV panel's data sheet are the following: maximum power (P_{max}), open-circuit voltage (V_{oc}), short-circuit current (I_{sc}), MPP voltage (V_{mpp}), MPP current (I_{mpp}) and efficiency (η) [2]. These features are important to define the characteristic curves of the PV panel. PV panel's I-V curves are a graphical representation of the relationship between the voltage and current of the solar panel. Different I-V curves are obtained for different temperatures and levels of irradiance [5]. Figure 1.1 shows the characteristic curves of a generic PV panel.

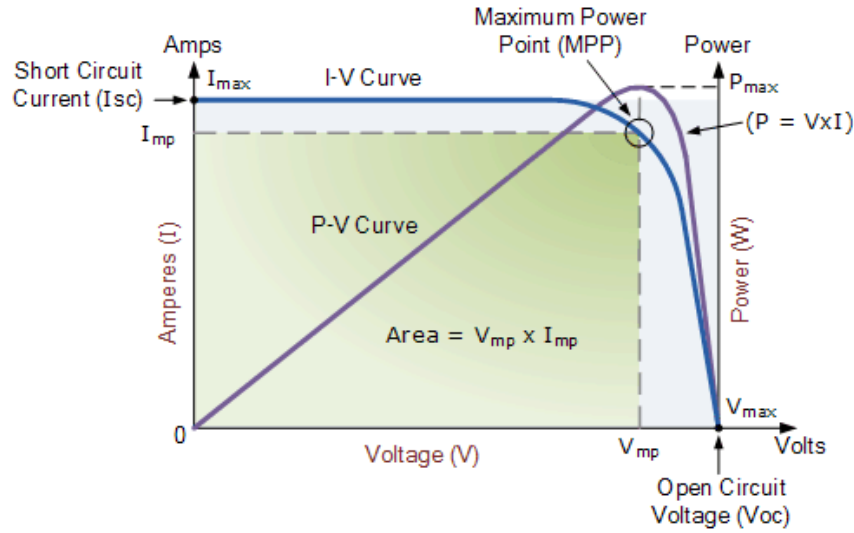


Figure 1.1: I-V and P-V curves of a generic solar panel [5].

The PV panel's I-V curve is shown in blue in Figure 1.1 for a given PV cell's temperature and solar irradiance. As it is well known, the power generated by a PV cell is the product of current and voltage at each point. Hence, the P-V curve of the solar panel can be obtained and it is displayed in purple. From the P-V curve, the maximum power generated by the solar panel (P_{max}) is obtained. This maximum power corresponds to the so called MPP and takes place for a specific combination of voltage (V_{mpp}) and current (I_{mpp}). Therefore, the ideal operating point of a PV panel corresponds to the MPP which varies according to the level of solar radiation and the temperature [2].

There are different types of photovoltaic systems, however, the most common PV systems implemented nowadays are grid-connected [2]. This type of PV system is mainly composed of a solar array, a DC-DC converter with an MPPT controller

unit and an inverter, as shown in Figure 1.2.

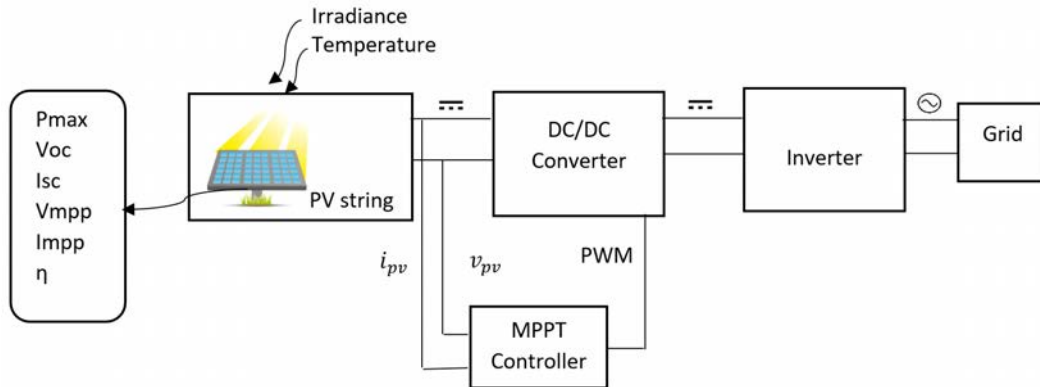


Figure 1.2: Basic block diagram of a PV system.

As mentioned at the beginning of the chapter, PV modules can be connected to each other resulting in a PV array which generates electrical energy in the form of direct current. The MPPT controller unit takes the PV array's output voltage and current as input variables in order to calculate the corresponding duty cycle for tracking the MPP. The duty cycle is the input of a Pulse Width Modulation (PWM) block. The PWM is used to generate the pulses for the switching components of the DC-DC converter in order to get the PV array to work continuously at its MPP. The output of the DC-DC converter is connected to an inverter to convert the DC electric energy in an AC electrical signal compatible with the grid.[2]

1.2 Module Integrated Converter

Usually, one MPPT is commonly used for many PV modules as shown in figure 1.2. This approach may lead to suboptimal efficiency of the system since the uneven power generated by the PV modules might lead to a system with a local MPP in addition to a global MPP [6]. In figure 1.3 a system exhibiting two MPP, due to partial shading of one of the system's PV panels, is shown. In order to ensure that the system is working in the global MPP and not in the local MPP, the inverter's controller will have to perform a voltage sweep in order to find the global MPP. This voltage sweep is a higher level of complexity in the MPPT control system [6]. In any case, the system will not be able to get the maximum power generation, as one panel is bypassed by a diode: Whenever a panel in a string is not able to supply enough current, its protection parallel diode might become biased [7].

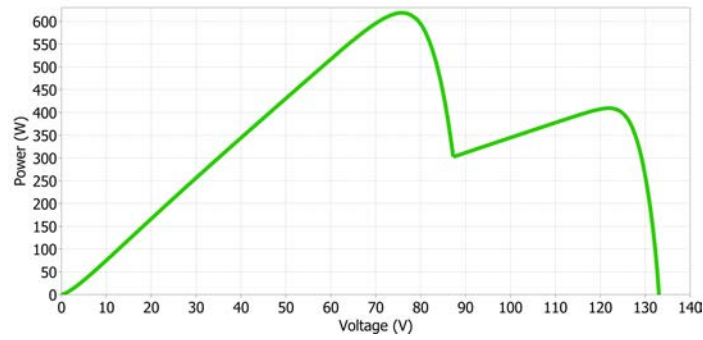


Figure 1.3: P-V curve of a system with more than one MPP. Three panels string. Two at full irradiance, one panel at 40% irradiance.

Another approach is using a MIC, which is a DC to DC converter featuring a MPPT controller included in each PV module which will result in higher overall efficiencies [7]. With this configuration, events like partial shading, uneven dirt, wear distribution or manufacturing imperfections are properly handled and do not affect the rest of the PV modules in the array. Also, a more detailed control of the plant is achieved since separate data from each individual panel is obtained [7]. Each PV module will then be connected directly to a MIC allowing the output voltage and current to be defined by the load. This way the system is able to operate at different voltage and current levels whilst maintaining the MPP [7].

MICs can be either microinverters or DC-DC converters. In figure 1.4 a PV system using MICs is shown. Notice that N panels might be used. Series or parallel connections can be used to link MICs' outputs and then connect this output to the inverter input.

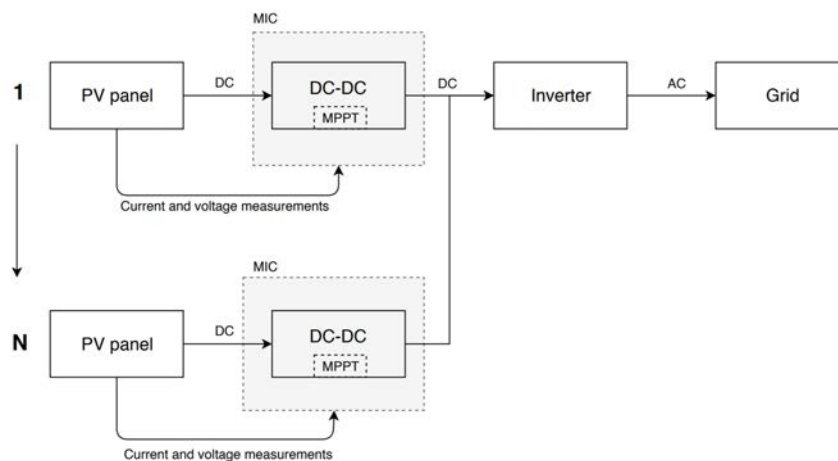


Figure 1.4: PV generation with DC-DC MIC system structure.

The panels with a MIC consisting on a microinverter, include a DC-DC converter with MPPT together with an inverter and are directly tied to grid. In figure 1.5 a microinverter system structure can be seen. For the user, this system is simpler, as only the PV must be purchase, the user does not have to worry about

selecting and installing an inverter.

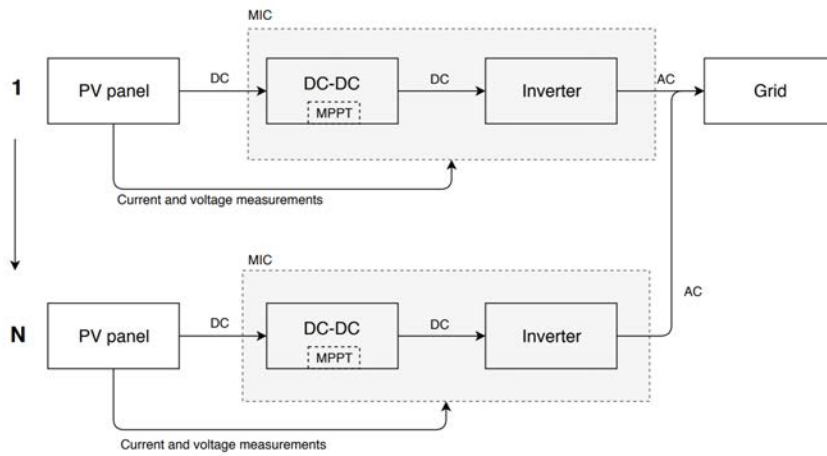


Figure 1.5: PV generation with microinverter MIC system structure.

The main advantage of the microinverter system is that it is simpler for the user, however, it implies an increase in costs and is usually less efficient than a DC-DC system with a single higher power inverter [7]. Therefore, for the development of this project a DC-DC MIC will be implemented.

1.3 Problem statement

The problem statement for this project can be formulated as the following question:

How can a module integrated converter be designed to maximize the PV power generation under real conditions?

The problem statement will be answered by fulfilling the following objectives:

- Design a DC-DC converter for integration with a PV panel.
- Analyze different implementations of MPPT techniques and implement the selected control system.
- Hardware implementation of the MIC components including the Printed Circuit Board (PCB) layout.
- Test of the system using a PV simulator and validation of the results.



Existing solutions for Module Integrated Converter

The main topic for this project consist on designing a MIC which basically is a DC-DC converter and a MPPT controller. Therefore, this chapter first analyzes different topologies for DC-DC converter commonly used in MICs. This chapter also gives some background information of the most common MPPT techniques.

2.1 Topologies of DC-DC converters

There are different types of DC-DC converters used for PV module integration. However, the main topologies of power converters used in MICs are buck, boost and non-inverting buck-boost DC-DC converters. The functionality and the advantages and disadvantages of these three topologies will be analyzed in this section.

2.1.1 Buck converter

A buck converter is one of the simplest DC-DC converters with the task of decreasing the input voltage. The required components are a DC source for the input voltage, two switches (a diode and a transistor), an inductor, a capacitor and a load. The equivalent diagram in figure 2.1 illustrates a buck converter.

A buck converter performs in two operating states. During the first state, the MOSFET is conducting and the diode is reversed bias thus working as an open-circuit. The voltage drop then is divided between the inductor and the load. Since the voltage is split, the voltage drop on the load is lower than the input voltage. In addition, both the capacitor and the inductor are being charged. In the second state, the MOSFET is switched off and the current flows through the diode as it is forward-biased. During this state, the inductor works as a current source and the capacitor stabilizes the voltage [8].

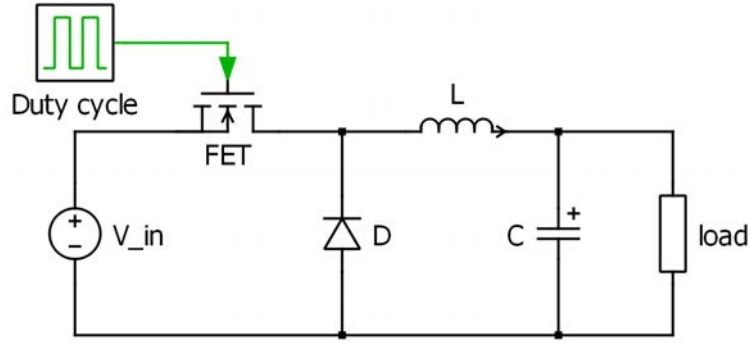


Figure 2.1: Equivalent circuit for the DC-DC buck converter.

The main advantage of using a buck converter is that the structure is very simple and only one controlled switch is needed. Also, the component count and thus cost of implementation is low. Furthermore, the buck converter can reach efficiencies up to 99% [9]. However, this topology is not very versatile since it does not allow the increase of output voltage with respect to the input.

2.1.2 Boost converter

A boost converter is another type of DC-DC converter similar to the buck converter but instead of lowering the output voltage, it produces a higher electrical potential at the output with respect to that at the input. The circuit consists of two switches (a transistor and a diode), an inductor, a capacitor, a load and a DC source for the input voltage. Figure 2.2 shows the equivalent circuit diagram for the boost converter with the aforementioned components.

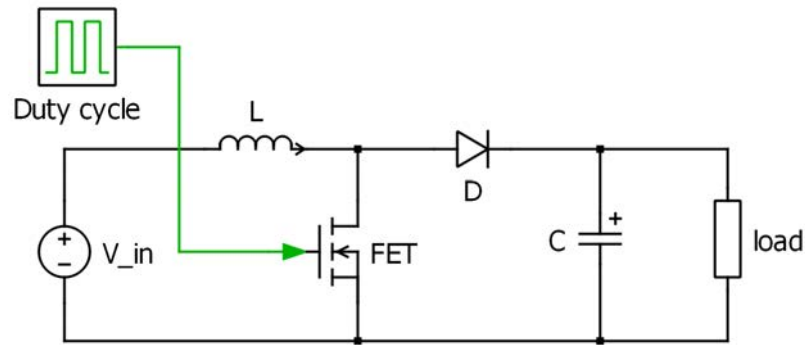


Figure 2.2: Equivalent circuit for the DC-DC boost converter.

Similarly to the buck converter, this topology has two states. When the MOSFET is on, the current flows only through the inductor because the diode is reverse biased. Energy is then stored in the inductor, which voltage is equal to the input voltage, and current increases. Meanwhile, the capacitor releases the previously stored energy to the load. During the second state, when the MOSFET is turned

off, the current loops through the inductor, diode, capacitor and the load. Since the inductor had been previously charged, it now works as a current source in series with the voltage source of the circuit. The voltage across the load is then risen with respect to that at the input. Furthermore, the capacitor is being charged [8]. It is also a cheap converter and it is easy to control [10]. However, as it happened with the buck, the boost converter is also limited to rising the voltage and lowering it cannot be achieved. The boost converter voltage gain has a non-linear transfer function that can produce cause damage to the system's components if the duty cycle is not properly limited to a maximum values.

2.1.3 Non-inverting buck-boost converter

The non-inverting buck-boost converter is a DC-DC converter that allows the voltage at its output to be higher or lower than the voltage at its input. The equivalent circuit diagram can be seen in figure 2.3. It uses a DC source, 4 switches, of which 2 are controlled devices, two capacitors, an inductor and a load.

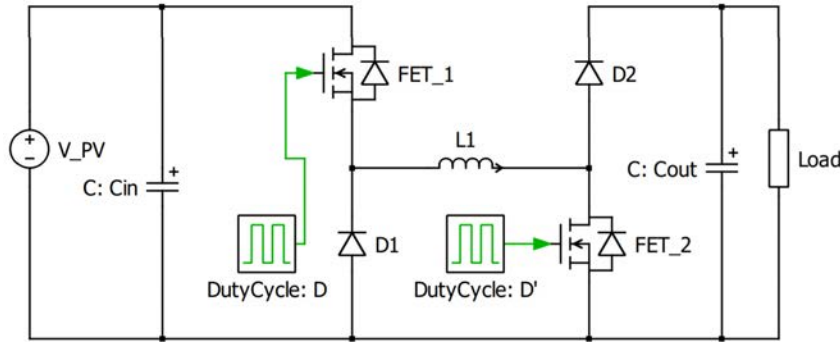


Figure 2.3: Equivalent circuit for the non-inverting buck-boost converter.

The controller can force the system to work in any of the following modes:

1. Buck $\rightarrow D \in [0, 1]; D' = 0$
2. Boost $\rightarrow D = 1; D' \in [0, 1]$
3. Buck-Boost $\rightarrow D \in [0, 1]; D' \in [0, 1]$

Usually, the inverter's input voltage (DC-link voltage) is fixed to some value higher than the peak grid's voltage. The possibility of higher and lower voltages at the converter's output allows different ways of associating photovoltaic modules. Then, the user is able to arbitrarily decide how many PV modules to link in series. Differently of what would happen in the case of buck or boost converters where the constraints regarding the number of panels are a bigger concern. In the case of the boost, the number of panels N is limited by the maximum duty cycle that is allowed, following equation 2.1, where V_{DC} is the voltage at the input of the inverter and V_{MPP} is PV panels' maximum power voltage. In the case of the buck, the number of panels is limited by the minimum allowed duty cycle, as described in equation 2.2. Then the boost has a more requiring constraint when considering

the maximum number of panels and the buck has a more requiring constraint when considering the minimum number of panels.

$$N = \frac{V_{DC} \cdot (1 - \delta_{MAX})}{V_{MPP}} \quad (2.1)$$

$$N = \frac{V_{DC}}{V_{MPP} \cdot \delta} \quad (2.2)$$

Compared with other topologies that can have both higher and lower voltages at the output, this DC-DC converter features a single inductor and no intermediate capacitor. With such reduction in passive components the price, efficiency and power density improves significantly [11]. One of the drawbacks of the non-inverting buck-boost topology is the control's complexity, which must calculate the appropriate duty cycle D and D' in any of the modes and also the transition between these modes. The buck-boost mode is specially complicated as there are two duty cycles to calculate. This problem might be addressed by setting a constant duty cycle in one of the bridge's legs and then the control will calculate the other leg's duty cycle [12].

Although this topology exhibits appropriate features, it can be further improved by replacing the diodes by MOSFETs. The circuit may be seen in figure 2.4 and it is called Bidirectional Non-Inverting Buck-Boost converter.

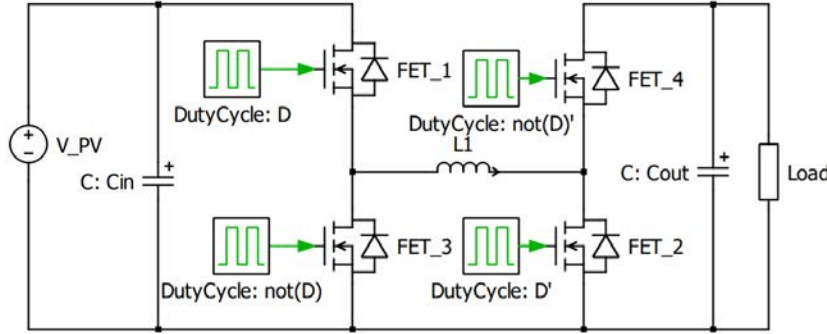


Figure 2.4: Bidirectional Non-inverting buck-boost converter.

With this variation, the following changes occur:

1. The system becomes bidirectional.
2. The conduction losses are smaller.

The conduction losses are smaller due to the fact that the losses in a diode evolve with a slope equal to the diode forward voltage: around 0.7V for silicon while the losses in a MOSFET evolve quadratically with current with R_{DSon} , as seen in equation 2.3. For a R_{DSon} , the conduction losses will be lower in the MOSFET while the current is below 35A.

$$P_{diode} = V_d \cdot i \quad P_{MOSFET} = i^2 \cdot R_{DSon} \quad (2.3)$$

If the system is bidirectional it can be used for different purposes, as the topology seen in figure 2.5, which features an isolated DC-link. This topology has a bidirectional MIC, as energy flows in both directions is needed. The goal of this system is to have a single MPP. This is achieved by:

1. Set the working conditions to have as many PV panels performing under the MPP as possible. In this case there are two panels which generate more than the third one.
2. Now evaluate the power generation difference between those panels working in the MPP and those with a lower power generation. The average power generation is computed.
3. The control system must lower the power difference to 0. This target is met by getting power from those panels which are generating more than average (in the picture seen as P3 and P2) and supplying this power back to the panels below the average power generation (in the picture seen as P1).

This strategy's advantage is that the power processed by the converters is lower than in a system where all the energy is flowing through the converter. Achieving lower losses, in absolute value.

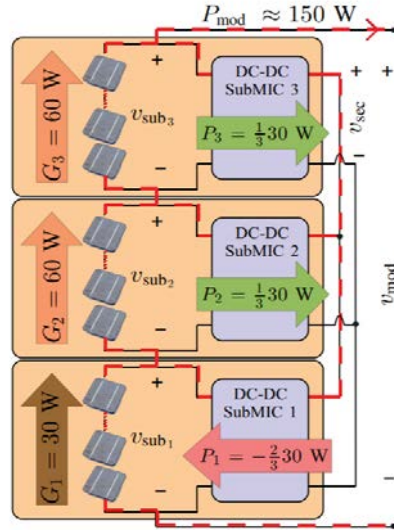


Figure 2.5: Bidirectional MIC use [7].

As seen in figure 2.4, the duty cycles of the switches that replace the diodes are \overline{D} and $\overline{D'}$. This line over the variables means that it is the complementary value of the original variable. The duty cycle is the boolean variable that indicates the conduction state of a switch.

A drawback of the bidirectional system is the increased difficulty of the driver circuitry and the requirement of a dead time in order to avoid the short circuit of FET_1 and FET_3 or FET_2 and FET_4 , which could damage the system. When using diodes, the system is intrinsically protected against a shoot-through event.

2.2 Maximum Power Point Tracking techniques

There is a variety of different techniques for finding the maximum power point. Therefore, three different MPPT algorithms will be described in this project, otherwise it would go beyond the scope of this work. These three methods are the Perturb and Observe (P&O), constant voltage and incremental conductance. P&O and incremental conductance are the most used algorithms in commercial PV panels. On the other hand, constant voltage has been selected as an idea for other less used methods. Each MPPT algorithm will be described based on a flow chart.

2.2.1 Constant voltage

Empirical experiments have shown that the voltage of the MPP has a linear dependence on the open circuit voltage at different ambient conditions[13].

$$V_{mpp} = k \cdot V_{oc} \quad (2.4)$$

In equation 2.4, k represents a constant that depends on the characteristics of the respective PV panel. To determine the value of k , the optimal voltage (V_{mpp}) and the open-circuit voltage (V_{oc}) must be recorded for each temperature and solar irradiation. According to different papers, this value lies between 70 and 80 percent of V_{OC} [14]. The algorithm starts with the recording of V_{oc} and a predetermined k -value. In each iteration step V_{mpp} is calculated first. After this, the operating voltage is compared with the calculated V_{mpp} . If the voltage is not equal, the constant k is changed for the next iteration step to track the MPP. When the algorithm has reached the MPP, the algorithm is stopped, as it is showed in the flow chart in the figure 2.6. [13]

The advantage of using constant voltage is that only the voltage is measured and the system is controlled by a simple control loop. Therefore, implementation costs are low compared to the other two methods. The use of PV modules with the constant voltage as MPPT algorithm is only possible in regions with low temperature fluctuations. The reason for this disadvantage is that the point of the MPP varies greatly with strong temperature fluctuations and the assumption of linear dependence is no longer valid. In addition, it is not possible to find the MPP with the algorithm if the PV module is partially shaded. Another disadvantage is the effort of calculating the optimal k for different levels of irradiance and temperature is very high and, therefore, the complexity of the algorithm increases.[13]

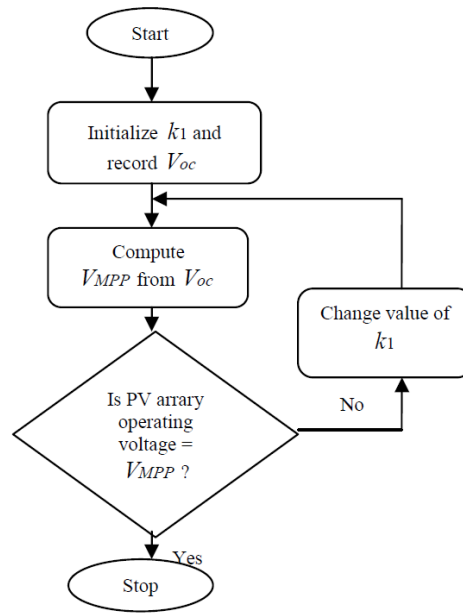


Figure 2.6: Flow chart for the constant voltage algorithm [13].

2.2.2 Perturb and observe

With the P&O method, the currently measured power is periodically compared with the previous power. If the measured power is greater than the power from the previous measurement, the algorithm is moving in the right direction to the MPP. If a power reduction is detected after the comparison, the algorithm is moving away from the MPP. The next step is the identification of a voltage increase or reduction to regulate the voltage for getting the MPP voltage. This depends on which side of the MPP the algorithm is working. If the algorithm detects less voltage than the MPP, the voltage for the next step should increase. If more voltage than the MPP is detected, the algorithm decreases the voltage for the next step to reach the MPP. The flowchart in figure 2.7 illustrates this method. The classical algorithm uses a fixed step to change the voltage. When the MPP is reached, the algorithm oscillates around the this point. [13]

One of the advantages of the P&O algorithm is that the required computing power of the P&O algorithm is low, in its simplest implementation. The algorithm contains the calculation of the power and the comparison with the previous power for each step. There is a disadvantage when the algorithm is near to the MPP since, at this point, the algorithm oscillates around it, so that the MPP cannot be reached exactly. The oscillation depends on the value of the perturb step. If the fixed step value is high, the MPP will be tracked quickly. However, the oscillation around the MPP is higher, which reduces the efficiency of the PV panel. The advantage of a small step value is that the oscillations are reduced, but it takes more time to reach the MPP. [6]

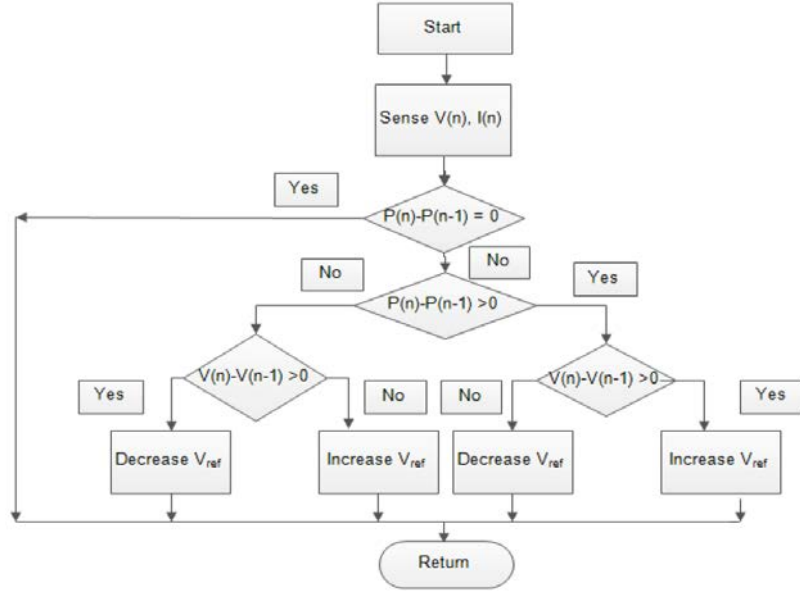


Figure 2.7: Flow chart for the conventional P&O algorithm [15].

2.2.3 Incremental conductance

The approach of incremental conductance is that the MPP is at the position where the derivative of the power with respect to the voltage is 0, see figure 1.1. On the left side of the MPP the derivative is greater than 0 while on the right side it is less than 0, this behavior is described by the following equations. [6]

$$\frac{dP}{dV} = 0, \text{ at MPP} \quad (2.5)$$

$$\frac{dP}{dV} > 0, \text{ left side from MPP} \quad (2.6)$$

$$\frac{dP}{dV} < 0, \text{ right side from MPP} \quad (2.7)$$

The algorithm compares the incremental conductance with the previous one to increase (left side of MPP) or decrease (right side of MPP) the voltage. After the MPP has been reached, the algorithm is stopped. Thus, there will be no oscillation around the MPP. If a change in the current is detected, the algorithm starts to find the MPP again, as you can see in the flow chart in figure 2.8. [6]

An advantage of this MPPT algorithm is that it can reach exactly the MPP. This increases the efficiency of the PV panel. As with the P&O algorithm, a fixed value is used to change the voltage. If the value is high, the probability is higher that the algorithm oscillates around the MPP. Two sensors, for the voltage and the current, are used for the implementation of this method. In addition, the microcontroller requires a higher computing power than with the P&O algorithm. This is because more commands are called up during an iteration step. The costs for the algorithm development and microcontroller are higher compared to the other two algorithms. [6]

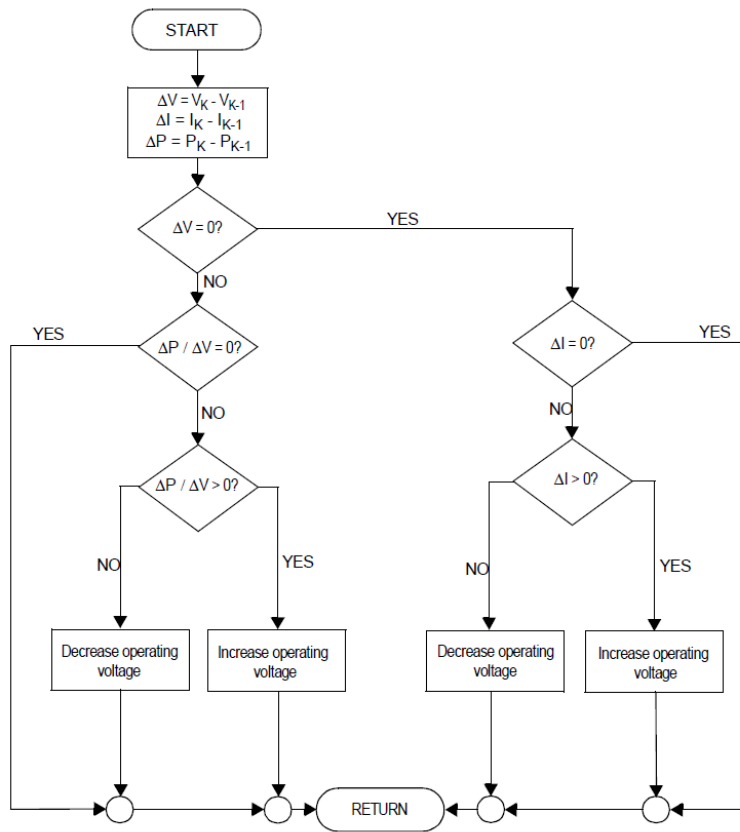


Figure 2.8: Flow chart for the incremental conductance algorithm [6].

Non-inverting Buck-Boost converter design

This chapter contains the analysis of the non-inverting buck-boost converter. The first part contains the selection of converter topology and the requirements which will be used during the design phase of the project. The second part includes the sizing of the passive components and the results of the open-loop simulation of the converter.

3.1 Selection of topology

The selection of converter topology is based on the research made in section 2.1. The converter should be able to allow both higher and lower output voltage compared to the input. This requirement will limit the buck and boost converters, which only convert either up or down. A non-inverting buck-boost converter will therefore be implemented.

By using a 4 transistor buck-boost converter, instead of a 2 transistor, it is possible to further minimize the power loss since the losses on the transistor can be lower than those on the diodes.

The 4 transistor buck-boost converter does also have the advantage of being bidirectional. This means that it is possible to extract current from the PV module and also to inject current into the PV module. When this happens, the PV module acts like a LED, radiating an infrared light when current is injected. If a PV module is damaged and has micro-cracks, the power generation will be affected. By injecting current to the module it is much easier to find this small cracks, allowing the discovery of faulty modules before there is a drop in efficiency. This will increase the overall efficiency of the system and ease the maintenance sequence significantly. [16]

The bidirectional non-inverting buck-boost converter is selected because of these arguments. Although the bidirectional functionality will not be addressed in this project, it could be a part of the further development of the converter.

3.2 System requirements

For the design and test of the MIC it is of great importance to have the requirements of the system defined. The input requirements of the MIC will be based on the specifications of the PV panel *STP300S-24/Vd* from Suntech Power [17].

The specifications of the load of the MIC will be based on the commercial inverter "*Power-one STGU-105*" [18] in order to have the output voltage defined. From the inverter's datasheet it is found that the nominal voltage in the DC-link is 360 V, with a maximum input power of 5500 W. The development of this project will be based on these requirements because they are real commercial products that the user can purchase.

The maximum input power, voltage and current of the converter is decided by P_{max} , V_{oc} and I_{sc} of the chosen PV-panel. The maximum output voltage is decided by the DC-link voltage and minimum PV string length, while the minimum output voltage is decided by the maximum string length. The maximum output current is decided by P_{max} , which ideally also will be the maximum output power, and the minimum output voltage. Table 3.1 shows the requirements of the MIC, extracted from the specifications of the PV panel and the inverter. It defines both the requirements regarding input, output and the length of PV panel strings.

Input	
Maximum input power (P_{max})	300 [W]
Maximum input Voltage (V_{oc})	45 [V]
Maximum input current (I_{sc})	8.67 [A]
Output	
Maximum output voltage ($V_{out,max}$)	90 [V]
Minimum output voltage ($V_{out,min}$)	24 [V]
Maximum output current ($I_{out,max}$)	12.5 [A]
PV system specification	
Minimum string length	4
Maximum string length	15

Table 3.1: MIC requirements.

3.3 Component sizing

The power circuit includes three main passive components which are the inductor, the input capacitor (C_{in}) and the output capacitor (C_{out}). According to these values, the coil will influence the maximum current ripple that will flow through it, while the capacitors will set the voltage ripple at the input and at the output of the MIC. In order to calculate the minimal inductance and capacitance that the components need to have, the worst case scenario was considered. Therefore, in order to calculate these values current and voltage ripples have been set. For the current through the coil, a 10% maximum ripple has been chosen. The output capacitor will have a maximum of 0.5% voltage ripple. However, the input capacitor makes the PV module's voltage flat. Therefore, the ripple found at C_{in} directly influences

the maximum power extracted from the PV since it produces a deviation from the MPP. Giving this, a low input voltage ripple of 0.1% has been selected. The ripple, however, also depends on the working frequency of the switches. In the case of this converter, the switching frequency has been set to 50 kHz.

Since the coil ripple is a percentage of the absolute current, the worst case scenario for calculating it occurs when the current is lowest. A lower limit is then implemented at which the values will be calculated, this is the solar panel working at $400W/m^2$ and at a temperature of $25^\circ C$. Under this conditions, the MPP voltage obtained is $V_{mpp} = 36.19V$ and the MPP current is $I_{mpp} = 3.23A$.

On the other hand, the capacitors will have a higher ripple when the current is maximum, this means that the system is working at the maximum irradiance ($1000W/m^2$). The PV will then output a voltage of $V_{mpp} = 36.9V$ and a current of $I_{mpp} = 8.14A$.

The minimum current flow through the coil is achieved when the boost mode is active. For this, the inductance is calculated for the maximum output voltage, which is when 4 MICs are connected in series. According to the equations, stated in the equation 2.43, section 2.3 of the book *"Fundamentals of Power Electronics"* [19], the inductance has been sized as seen in equation 3.1.

$$L = \frac{V_{in} \cdot (D)}{\Delta I_L \cdot f} = \frac{36.19V \cdot (1 - \frac{36.19V}{90V})}{0.1 \cdot 3.23A \cdot 50kHz} = 1.3 \text{ mH} \quad (3.1)$$

On the other hand, the input and output voltages used for C_{in} is obtained when buck mode is working with 15 MICs connected in series. This is a total output voltage of $24V$. The capacitance required is then found as stated in equation 3.2 (Equation 2.57, section 2.4 of Fundamentals of Power Electronics [19])

$$C_{in} = \frac{I_{in} \cdot (1 - D)}{\Delta V_{in} \cdot f} = \frac{8.14A \cdot (1 - \frac{24V}{36.9V})}{0.001 \cdot 36.9V \cdot 50kHz} = 1.54mF \quad (3.2)$$

Finally, C_{out} is calculated in the worst case scenario of boost mode. The output voltage is then $90V$. The values are calculated with the method found in equation 2.47, section 2.3 of *"Fundamentals of Power Electronics"* [19]. The procedure can be seen in equation 3.3

$$C_{out} = \frac{I_{out} \cdot D}{\Delta V_{out} \cdot f} = \frac{3.34A \cdot (1 - \frac{36.9V}{90V})}{0.005 \cdot 90V \cdot 50kHz} = 88\mu F \quad (3.3)$$

3.4 Simulation Results

To validate that the calculations have been made correctly, an open loop simulation of the circuit was conducted. As it can be seen in figure 3.1 the circuit consists of the 4 MOSFETs, the inductor, the 2 capacitors and a load. The MOSFETs are controlled with two duty cycles D1 and D2. FET1 and FET4 will get the actual duty cycle while FET2 and FET3 uses the complementary duty cycles. With the scope the output voltage and current through the inductor can be visualized.

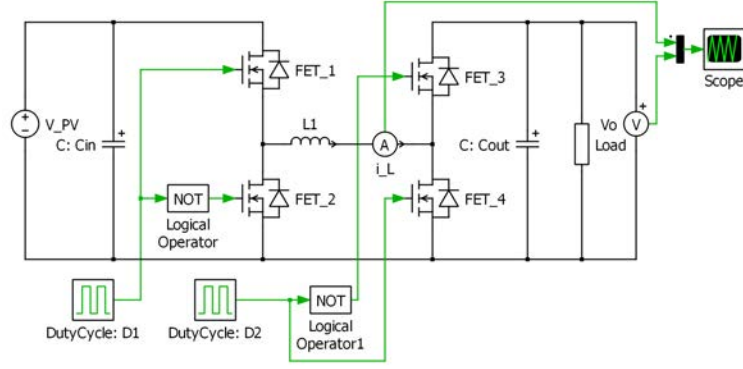


Figure 3.1: Ideal open-loop simulation.

The values for the components are $C_{in} = 1.54mF$, $C_{out} = 88\mu F$ and $L1 = 1.3mH$ as calculated in section 3.3. At first the buck mode is simulated. In this mode D2 is 0. This means that FET4 is off and FET3 is on. To achieve the minimum output voltage at $24V$, the corresponding duty cycle is calculated in equation 3.4. The load resistor is calculated for maximum output power for the PV-panel in equation 3.5.

$$D = \frac{V_{out}}{V_{in}} = \frac{24V}{36.9V} = 0.65 \quad (3.4)$$

$$R_{load} = \frac{V^2}{P_{max}} = \frac{24V^2}{300W} = 1.92\Omega \quad (3.5)$$

Figure 3.2 shows the output voltage and inductor current waveforms from the simulation. The initial transients are not important for an open loop simulation and have been excluded in the figure. With the data, the mean values are calculated such that $\overline{V_{out}} = 23.95V$ and $\overline{I_L} = 12.48A$. In buck mode the current through the inductor should be equal to the output current. With the values used for the simulation, the current at the output should be $12.5A$ as calculated in equation 3.6. The measurements shows that the converter works as expected in buck mode.

$$I_{out} = \frac{V_{out}}{R_{load}} = \frac{24V}{1.92\Omega} = 12.5A \quad (3.6)$$

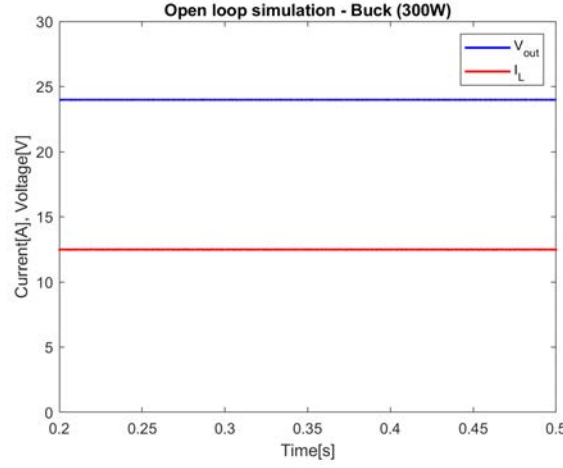


Figure 3.2: Open-loop simulation in buck mode.

The boost mode is simulated using the same values for the components and input voltage. To work in boost mode $D_1 = 1$ and D_2 is calculated in equation 3.7 to achieve an output voltage of 90V. The load resistor is sized in equation 3.8, such that an output power of 300W is obtained.

$$D_2 = 1 - \frac{V_{in}}{V_{out}} = 1 - \frac{36.9V}{90V} = 0.59 \quad (3.7)$$

$$R_{load} = \frac{V^2}{P_{max}} = \frac{90V^2}{300W} = 27\Omega \quad (3.8)$$

Figure 3.3 shows the output voltage and inductor current waveforms from the simulation. With the data, the mean values are calculated such that $\overline{V_{out}} = 89.95V$ and $\overline{I_L} = 8.16A$. The theoretical current through the inductor is calculated in equation 3.9. The measurements shows that the converter works as expected in boost mode.

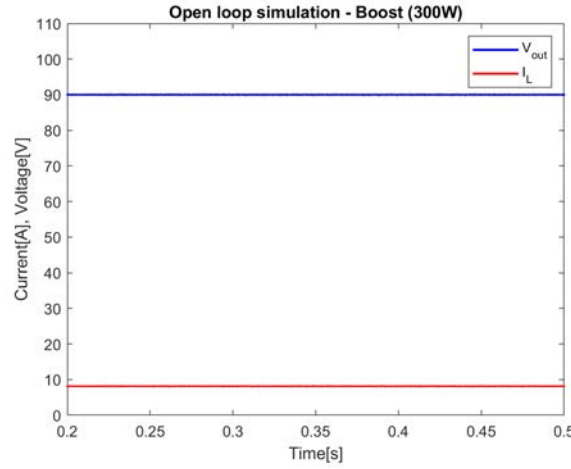


Figure 3.3: Open-loop simulation in boost mode.

$$I_L = \frac{1}{1-D} \cdot \frac{V_{out}}{R_{load}} = \frac{1}{1-0.59} \cdot \frac{90V}{27\Omega} = 8.13A \quad (3.9)$$

The last part of the open-loop simulation is to validate the capacitor and inductor values. This is done by measuring the different ripple values under the conditions as they were calculated in section 3.3. The inductor is tested in boost mode with $V_{in} = 36.19V$, $D_2 = 0.597$ and $R_{load} = 67.54\Omega$. The maximum and minimum currents are measured as $I_{max} = 3.465A$ and $I_{min} = 3.135A$, with a mean at $\bar{I}_L = 3.3A$. The ripple current is calculated in equation 3.10.

$$\Delta I_L = \frac{I_{max} - I_{min}}{\bar{I}_L} \cdot 100 = \frac{3.465A - 3.135A}{3.3A} \cdot 100 = 10\% \quad (3.10)$$

The output voltage ripple is also measured in boost mode, but with the maximum output power of 300W. This means $V_{in} = 36.9V$, $D_2 = 0.59$ and $R_{load} = 27\Omega$, as calculated during the open-loop boost simulation. The maximum and minimum voltages are measured as $V_{max} = 90.22V$ and $V_{min} = 89.77V$, with a mean at $\bar{V}_{out} = 89.995V$. The ripple voltage is calculated in equation 3.11.

$$\Delta V_{out} = \frac{V_{max} - V_{min}}{\bar{V}_{out}} \cdot 100 = \frac{90.22V - 89.77V}{89.995V} \cdot 100 = 0.5\% \quad (3.11)$$

The input voltage ripple is measured in buck mode, with an output voltage of 24V. This means $V_{in} = 36.9V$, $D_1 = 0.65$ and $R_{load} = 1.92\Omega$. This simulation was done using a PV module as input source, to achieve a realistic input. The model behind the PV-panel is explained in section 5.2. The maximum and minimum voltages are measured as $V_{max} = 36.94V$ and $V_{min} = 36.91V$, with a mean at $\bar{V}_{in} = 36.925V$. The ripple is calculated in equation 3.12. The figures for the ripple measurements are included in appendix A.

$$\Delta V_{in} = \frac{V_{max} - V_{min}}{\bar{V}_{in}} \cdot 100 = \frac{36.94V - 36.91V}{36.925V} \cdot 100 = 0.08\% \quad (3.12)$$

Hardware implementation

This chapter contains the hardware implementation of the non-inverting buck-boost converter. This mainly consists of the selection of commercial components, including switches, drivers, sensors, passive components etc. Additional circuits will also be designed to support the selected components. For the switch selection, power loss and temperature dissipation will be considered. This chapter also includes creation of the schematics and the PCB layout for the entire hardware implementation.

4.1 Selection of commercial components

4.1.1 Passive components

Passive components include input and output capacitors and the inductor. The needed values were calculated in section 3.3. However, no tolerance or safety margin are included in those calculations. By the nature of the project, the goal is not to optimize price or size, but to validate the technical feasibility of the PV power optimizer. For this reason, the commercial input and output capacitors chosen has been oversized with the goal of easing the control task. In further work, optimization of these values should be performed.

The necessary input capacitance is $1540\mu F$. A safety margin of 20% has been applied resulting in a necessary input capacitance of $1850\mu F$. In order to achieve this value, 4 capacitors have been associated in parallel. The when paralleling the capacitors the total parasitic inductance and resistance will decrease and ease the heat dissipation task [20]. Four electrolytic capacitors of $470\mu F$ [21] are placed in parallel to get a summed capacitance of $1.880\mu F$. The rating for these is 100V. The capacitors perform well in the working frequency and have low parasitic values, according to the data sheet [21]. Because of an early calculation error the output capacitor was selected to be $820\mu F$ [22], instead of the $88\mu F$ calculated in section 3.3.

Both for the input and output a $100nF$ and a $1\mu F$ capacitors are placed in parallel. These capacitors are SMD technology which have intrinsically low parasitic components. The goal is to support the higher capacitance capacitors during high

frequency current peaks[23].

The calculated inductance is $1.3mH$. The inductor is chosen to be a reused inductor from an earlier project, and is measured to have an inductance at $1.93mH$ at $50kHz$.

4.1.2 Switching circuitry

Selecting the switching circuitry consists of four different parts, the switches, drivers, optocouplers and the heat sink. Additional support circuitry will be designed, when selecting the commercial components.

Switch sizing

The system must regulate the power flow in order to maximize the power generation. In order to achieve this, the system includes switches that control the current flow. The switches consist on MOSFET devices. The switching frequency of the system is selected to be $50kHz$. Although the market has IGBT which can switch at $50kHz$, MOSFET devices allow lower losses than IGBTs for system's current rating [24] [25].

The maximum output voltage of the system is $90V$, however the voltage rating of the transistors was set to $150V$ in order to consider a safety margin, and thus, increase the reliability. The peak current through the transistors happens when the buck mode is active and the maximum number of MICs are used in series. The peak current is equal to $14A$. In order to reduce the conduction losses and the heat sink size, a low on resistance is desired shown in equation 4.1[26]. These constraints were used when searching for the ideal component. The chosen device is the IPB200N15N3. It exhibits the features seen in table 4.1.

Maximum ratings	
Continuous I_D	40 [A]
V_{GS}	± 20 [V]
Power dissipation	150 [W]
V_{DS}	150 [V]
R_{DSon}	20 [m Ω]
Other values of interest	
Input capacitance	1820 [pF]
Package	D2PAK
V_{th} ($V_{GS} = 3V$)	3 [V]
V_{th} ($V_{GS} = 36V$)	4.7 [V]
R_{Gate}	2.4 [Ω]

Table 4.1: MOSFET figures of merit. T = 25 °C [27].

Heat sink sizing

The procedure followed for validating the heat sink might be seen at figure 4.1. If the total temperature increase is within switch's safe operating area, then the heat

sink is providing enough heat dissipation.



Figure 4.1: Heat sink validation procedure.

The power dissipated in the switches is equal to the sum of the conduction losses and the switching losses. The conduction losses might be calculated as seen in equation 4.1.

$$P_{cond} = i(t)^2 \cdot R_{DS} \quad (4.1)$$

The switching losses depend upon the switching frequency and the transistor's manufacturing characteristics[26]. In order to calculate the value, the MOSFET's SPICE model was obtained from the manufacturer's website. The next step was to perform the simulation of the system. The system was simulated in both buck and boost modes. Special attention was put into the dead-band between PWM signals of different switches, to avoid current shoot through. After simulating, the average power dissipation under steady state was calculated in both modes. Within every mode, the simulation was performed under the most unfavorable conditions, this is: buck's output is 24 V and boost's output is 90 V. The results can be seen in table 4.3, column 1.

The datasheet shows that the R_{DS} variation is mainly dependent on the temperature[27]. The models found neglect the temperature difference. Then, in order to get an approximated value considering temperature, the procedure will be to calculate the total losses at constant temperature using the SPICE model and then add the additional conduction losses due to the increase of the resistance, as expressed by equation 4.2.

$$\overline{P} = \overline{P_{loss, T=K}} + \overline{i(t)^2 \cdot \Delta R_{DS}} \quad (4.2)$$

Now the junction temperature based on the power dissipation, calculated using the SPICE model, is calculated. The ambient temperature is set to 50 °C, which is considered a realistic scenario. The thermal circuit can be seen in figure 4.2. The next step is to choose a commercial heat sink. The constraints are thermal resistance, size and price. TDEX6015/TH was found. Its features might be found in table 4.2. The switches temperature will be analysed in order to validate the heat sink. The analysis considers all the transistors as a single power source.

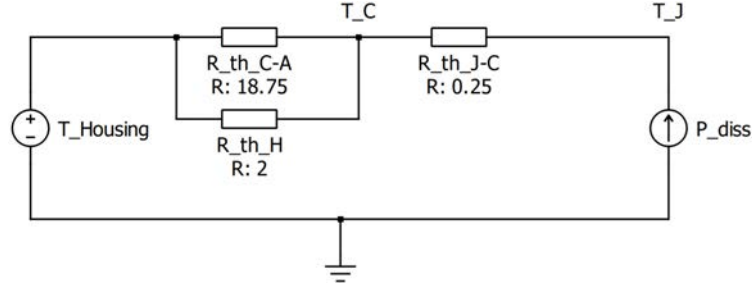


Figure 4.2: Thermal circuit used for sizing the heat sink

$$T_J = T_{housing} + \overline{P_{loss,T=K}} \cdot R_{thermal} \quad (4.3)$$

If no heat sink were used, according to equation 4.3, the junction temperature would become too high and the components would be damaged. See equation 4.4. This is mainly explained due to the fact that the thermal resistance between junction and ambient of the transistor is as high as $75^\circ\text{C}/\text{W}$.

$$T_J = 50^\circ\text{C} + 5.54\text{W} \cdot 75 \frac{^\circ\text{C}}{\text{W}} = 465.5^\circ\text{C} \quad (4.4)$$

Features	
Size	60x60x16 [mm]
Thermal resistance	2.06 [K/W]

Table 4.2: Heat sink figures of merit [28].

$$T_J = 50^\circ\text{C} + 5.54\text{W} \cdot 2.06 \frac{^\circ\text{C}}{\text{W}} = 61.41^\circ\text{C} \quad (4.5)$$

The drain-to-source resistance increase is calculated as explained in equation 4.6. The resistance difference is relatively small. The resistor at every temperature was collected from the component data sheet.

$$\Delta R_{DS} = |R_{DS,T=20^\circ\text{C}} - R_{DS,T=61.41^\circ\text{C}}| = 4 \text{ m}\Omega \quad (4.6)$$

The full power dissipation values can be found on table 4.3. To achieve an exact result, an iterative process should be followed. However, after the first iteration, the change ratio is extremely small and then, neglected. Now that the power dissipation has been calculated, the junction temperature must be checked in order to confirm that the heat sink has been properly sized. Equation 4.3 is used, substitution of values leads to 4.7. The difference is fairly small and the junction temperature remains within safe area. Then, TDEX6015/TH has been validated as a proper heat sink.

$$T_J = 50^\circ\text{C} + 6.72\text{W} \cdot 2.06 \frac{^\circ\text{C}}{\text{W}} = 63.84^\circ\text{C} \quad (4.7)$$

Switches power dissipation			
Switch	$\overline{P_{loss,T=K}}$ [W]	$\overline{i(t)^2 \cdot \Delta R_{DS}}$ [W]	Total [W]
Buck mode			
M1	2.91	0.39	3.30
M2	0.82	0.21	1.03
M3	1.81	0.58	2.39
M4	0	0	0
Total	5.54	1.18	6.72
Boost mode			
M1	0.69	0.28	0.97
M2	0	0	0
M3	0.48	0.12	0.6
M4	3.31	0.18	3.49
Total	4.48	0.58	5.06

Table 4.3: Power dissipation analysis. Column 1, average power dissipation at constant 25 °C temperature. Column 2, extra power dissipation due to the increase of temperature.

Drivers and optocouplers

The control signal is generated by the control platform, which consists on a Plexim RTbox. In order to provide galvanic isolation between the converter and the control signal generator, optocouplers are used. The chosen optocoupler is the ACPL-P302. This optocoupler includes output signal circuitry which allows saving a pull-up or pull-down resistor. The integrated circuit (IC) is not an open collector device. Its main features might be seen at 4.4.

Maximum ratings	
Supply voltage	35 [V]
Average input current	25 [mA]
Peak output current	0.4 [A]
Other values of interest	
Input forward voltage	1.5 [V]
Package	SSOIC6

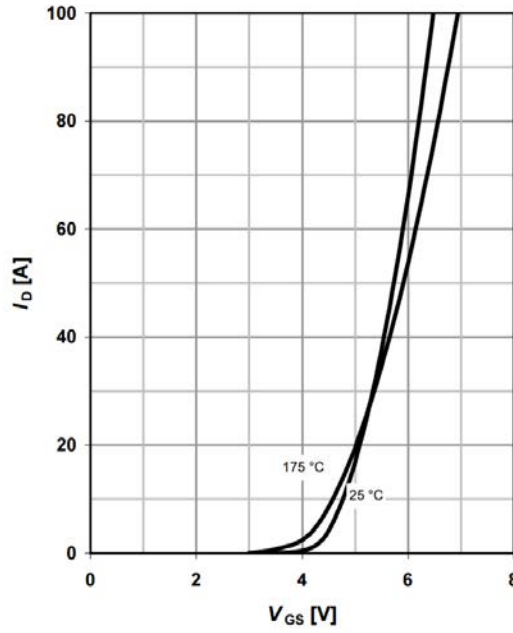
Table 4.4: Optocoupler figures of merit [29].

The signal from the optocoupler has to be amplified in order to drive the switches. The driver provides voltage amplification and current capability. The chosen IC to perform the task is NCP81074B. Find in table 4.5 its main features.

The MOSFET is a voltage controlled device, the relationship between V_{GS} and V_{th} sets the drain to source maximum current, as seen in figure 4.3[27].

Maximum ratings	
Supply voltage	24 [V]
Output current (pulse < 0.5 μ s)	10 [A]
Reverse current (pulse < 1 μ s)	10 [A]
Input signal voltage	-6 to 24 [V]
Other values of interest	
Output resistance	0.4 [Ω]
Package	SOIC8

Table 4.5: Driver figures of merit [30].

Figure 4.3: Drain to source current against gate to source voltage ($V_{DS} > 2 \cdot I_D \cdot R_{DSon}$).

The dynamics of the switching can be modeled as a RC circuit, see figure 4.4. Both $R_{driver\ out}$ and R_{MOSFET} are directly obtained from the components' data sheets, while $R_{limiting}$ is the gate resistor which needs to be sized. C_{iss} is also available in the MOSFET data sheet as input capacitance.

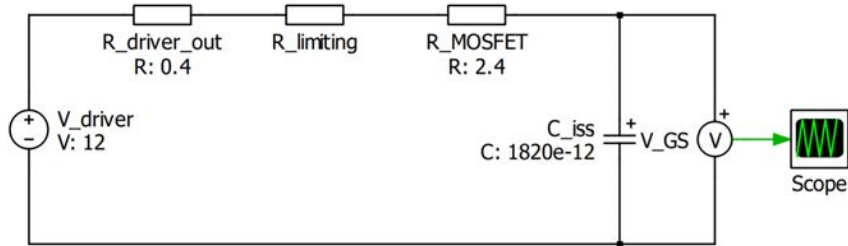


Figure 4.4: Simplified circuit used to model the MOSFET switching dynamics.

The time where the gate capacitor voltage reaches the threshold voltage produces a propagation delay from the driver output to the actual beginning of the MOSFET switching. In order to size the limiting resistor of the RC circuit, a time constraint was needed. This time constraint was arbitrarily set in relation with the switching frequency as described in equation 4.8. The 0.1% constraint results in a limiting resistor of 20 Ω . The average power dissipation, according to simulation, is 13 mW. This value is well under the power rating of the used SMD resistor with 1206 package, which is 250 mW. However the peak power dissipation was also considered, as it is relatively high. According to simulation, the peak is equal to 5.4 W, see figure 4.5. Although this value exceeds the resistor power rating, some manufacturers agree that the peak power dissipation in pulses shorter than 10 μ s using 1206 resistors is 19 W [31], [32]. Then the peak power dissipated shouldn't harm the component. Once the prototype is built, the thermal behaviour of the component is analysed with a thermal camera.

$$t_{delay} = t|_{V_{GS}=V_{th}} = \frac{T_{sw}}{1000} = 0.1\% \text{ of } T_{sw} = 20 \text{ ns} \quad (4.8)$$

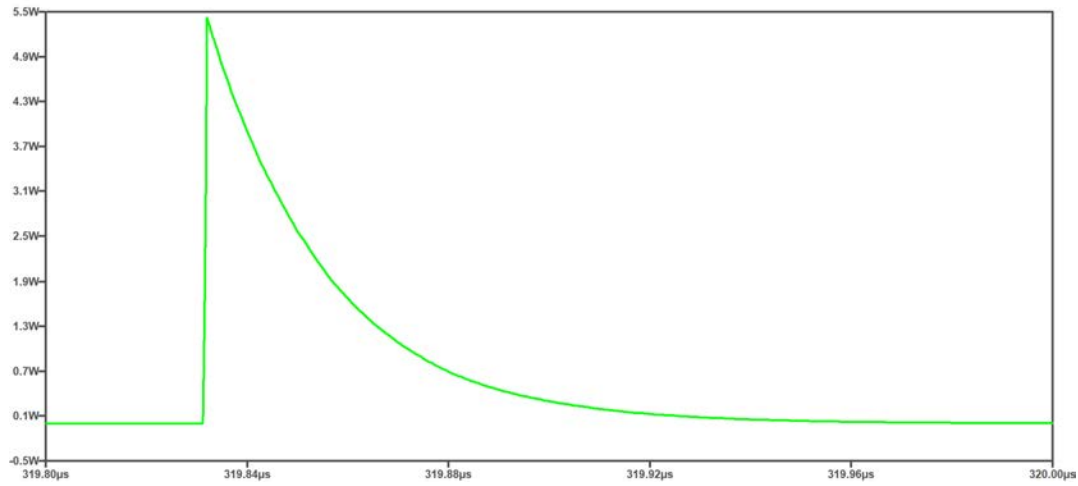


Figure 4.5: Detail of the power dissipated at $R_{limiting}$ during MOSFET turn-on.

The implemented topology has the peculiarity that two MOSFETs' sources are not directly connected to ground. As explained previously, it is the gate to source voltage that determines whether the transistor is conducting or not. In order to get a floating voltage in the high side drivers, one option is to have isolated supplies for those drivers. The ground of this isolated supplies will be tied to the low side MOSFET's drain. More explanation regarding the isolated supplies might be found at 4.1.4.

In case that the drivers were damaged, the residual voltage of the transistor's gate might become undefined, then, in order to ensure that the switch is off, a pull down resistor is added between the gate and the source of the transistor.

4.1.3 Sensing circuitry

To implement the MPPT it's necessary to measure the output voltage and current of the PV-module. These measurements will be obtained by implementing a voltage and current sensor. A second voltage sensor will be implemented to measure the output voltage of the DC/DC converter, for possible future use.

To protect the RT-Box, it has been chosen to fully isolate it from the power stage of the converter. To do so, the sensors will have to include isolation between input and output.

Input voltage sensor

The voltage sensor selected is the ACPL-C870 [33]. This sensor includes an optical isolation amplifier, which makes it well suited for isolated voltage sensing. Some relevant electrical specifications have been included in table 4.6. Figure 4.6 shows the placement of the two voltage sensors, where V_{in} and V_{out} are the input and output sensor respectively.

Recommended ratings		
Supply voltages	V_{DD1}, V_{DD2}	5 [V]
Input voltage range	V_{in}	0 – 2 [V]
Other values of interest		
Voltage gain	G	1 [V/V]
Output common-mode voltage	V_{OCM}	1.23 [V]
Gain tolerance	–	± 3 [%]
Bandwidth	BW	100 [kHz]
Package	SSOP	[–]

Table 4.6: Electrical specifications ACPL-C870 [33].

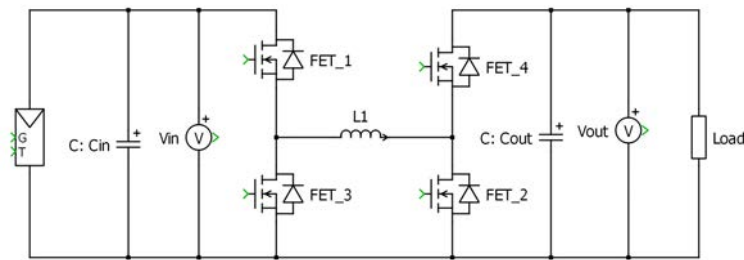


Figure 4.6: Voltage sensors placement.

Voltage divider The input voltage at the voltage sensor is recommended to be in the range of 0V – 2V. To divide the measured voltage into that range, a voltage divider will be implemented.

The maximum output voltage of the PV module is the open-circuit voltage at 45V. To achieve a safety margin and to make the converter adaptable to other types of PV modules, 50V has been selected. The current flow in the voltage divider has

been set at $1mA$, to secure a insignificant power loss. The resistors can be calculated with equation 4.9 and 4.10.

$$R_{17} = \frac{V_{in,max} - V_{out}}{I} = \frac{50V - 2V}{1mA} = 48k\Omega \quad (4.9)$$

$$V_{out} = V_{in,max} \cdot \frac{R_{18}}{R_{17} + R_{18}} \Rightarrow 2V = 50V \cdot \frac{R_{18}}{48k\Omega + R_{18}} \quad (4.10)$$

$$R_{18} = 1.958k\Omega$$

To be able to select commercial resistors the values $R_{17} = 47k\Omega$ and $R_{18} = 2k\Omega$ have been chosen.

Filtering For a stable MPPT control, the measured voltage must have a very low ripple. To ensure this, a low-pass RC filter with a corner frequency at $50Hz$, will be placed between the voltage divider and the sensor. The resistor of the filter will be R_{17} in the voltage divider. The capacitor will be calculated as followed in equation 4.11:

$$C_{17} = \frac{1}{2\pi \cdot f_c \cdot R_{17}} = \frac{1}{2\pi \cdot 50Hz \cdot 47k\Omega} = 67.7nF \quad (4.11)$$

To be able to select a commercial capacitor, $C_{17} = 68nF$ has been chosen.

Amplification The input range of the Analog to Digital Converter (ADC) in the RT-Box is $0V - 5V$. To take advantage of the full range an amplifier will be implemented. The output of the voltage sensor is differential with an offset at $1.23V$. Therefore a differential amplifier will be implemented using a LMC6484 [34] quad operational amplifier. By using a quad amplifier, the same IC can be used for all the sensors. The relevant electrical specifications have been included in table 4.7.

Recommended ratings		
Supply voltage	V_{DD}	$3 - 15.5 [V]$
Input voltage range	V_{in}	$\pm V_{DD} [V]$
Other values of interest		
Slew rate	SR	$1.3 [V/\mu s]$
Gain-Bandwidth product	GBW	$1.5 [MHz]$
Number of amplifiers	–	4 [-]
Package	–	SOIC [-]

Table 4.7: Electrical specifications LMC6484 [34].

The resistors of the differential amplifier will be sized with equation 4.12.

$$V_{out} = \frac{R_{21}}{R_{19}} \cdot (V_2 - V_1) \quad (4.12)$$

Where $V_2 - V_1$ is the difference between the output pins of the voltage sensor. With unity gain in the voltage sensor, the maximum difference at the output will

be 2V. This should correspond to the maximum input voltage of the ADC at 5V. R_{19} is selected to be 11k Ω . The resistor R_{21} is now calculated using equation 4.12.

$$5V = \frac{R_{21}}{11k\Omega} \cdot 2V \quad (4.13)$$

$$R_{21} = 27.5k\Omega$$

To be able to select commercial resistors the value of R_{21} it's rounded to be 27k Ω . Furthermore $R_{20} = R_{19}$ and $R_{22} = R_{21}$, to get a balanced differential amplifier.

The circuit The circuit regarding the input voltage measurement is shown at figure 4.7. All components calculated in this section have been inserted with the same name. V_{in} is the measured voltage from the PV-module. The points $OA1_+$ and $OA1_-$ are connected to the non-inverting and inverting input of the amplifier respectively. $OA1_{out}$ is connected to the output of the amplifier. C_{15} and C_{16} are decoupling capacitors for the two supply voltages. The maximum input voltage of the voltage sensor is 5V. Because of this a 4.7V zener diode has been added at the input, to protect it against over-voltage.

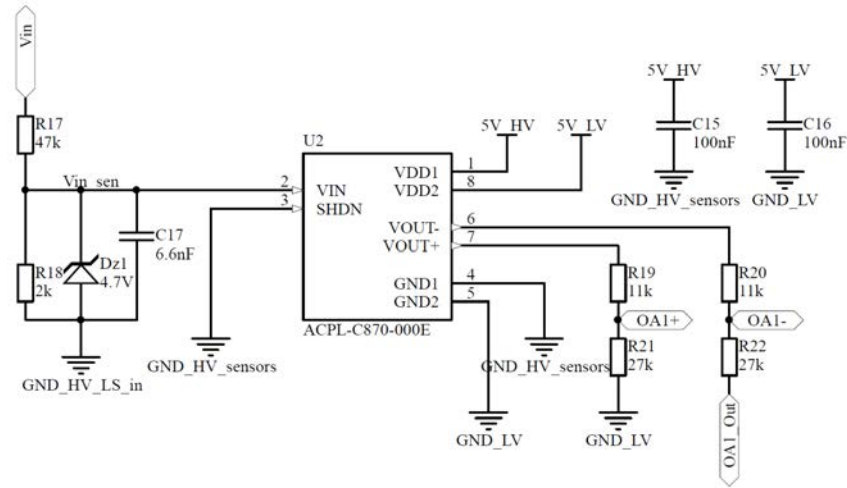


Figure 4.7: Input voltage sensor.

Output voltage sensor

The voltage sensor at the output is design with the same procedure as the input sensor. The voltage divider will designed such that the values of the amplifier can be reused.

Voltage divider The maximum output voltage of the DC-DC converter will be 90V, when only 4 PV modules are used. To insert a safety margin if one converter fails, the maximum sensed voltage will be designed at 120V.

The resistors will be sized by reusing equation 4.9 and 4.10.

$$R_{26} = \frac{V_{in,max} - V_{out}}{I} = \frac{120V - 2V}{1mA} = 118k\Omega \quad (4.14)$$

$$V_{out} = V_{in,max} \cdot \frac{R_{27}}{R_{26} + R_{27}} \Rightarrow 2V = 120V \cdot \frac{R_{27}}{118k\Omega + R_{27}} \quad (4.15)$$

$$R_{27} = 2.03k\Omega$$

To be able to select commercial resistors $R_{26} = 120k\Omega$ and $R_{27} = 2k\Omega$ have been chosen.

Filtering The filter will be design with the same corner frequency at $50Hz$, as for the input sensor.

The resistor of the filter will be R_{26} in the voltage divider. The capacitor will be calculated as followed in equation 4.16:

$$C_{22} = \frac{1}{2\pi \cdot f_c \cdot R_{26}} = \frac{1}{2\pi \cdot 50Hz \cdot 120k\Omega} = 26.5nF \quad (4.16)$$

To be able to select a commercial capacitor $C_{22} = 33nF$ has been chosen. By using these values the actual corner frequency will be $40.2Hz$.

The circuit The circuit regarding the input voltage measurement is shown at figure 4.8.

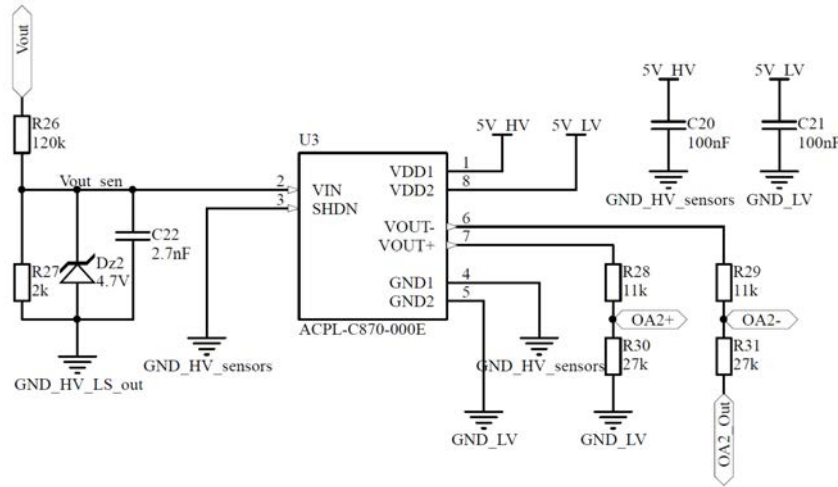


Figure 4.8: Output voltage sensor.

Current sensor

The current along with the voltage of the PV allows the system to perform power calculation, which is needed for the MPPT algorithm. The current will be measured in series with the inductor with a hall effect sensor. Placing it in series with the PV module would be the easiest approach for MPPT, but placing it in parallel with the inductor allows implementing a current controller for possible future use. A hall effect sensor is used to secure isolation between the power traces and the control circuit.

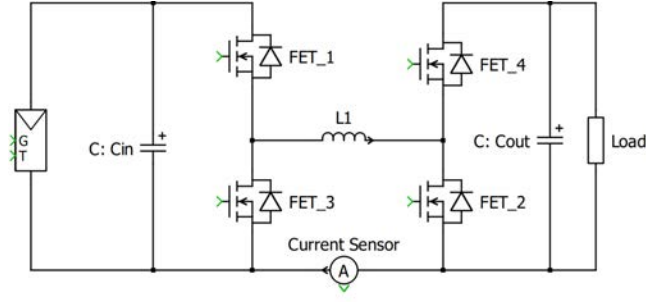


Figure 4.9: Current sensor placement.

The sensor is a ACS723-20AB [35] which is a hall effect sensor. Its features can be found in table 4.8 and its connection can be found in 4.10.

Maximum ratings	
Supply voltage	4.5-5.5 [V]
Gain	100 [mV/A]
Input range	± 20 [A]
Other values of interest	
Bandwidth	20 or 80 [kHz]
Package	SOIC8

Table 4.8: Current sensor figures of merit [35].

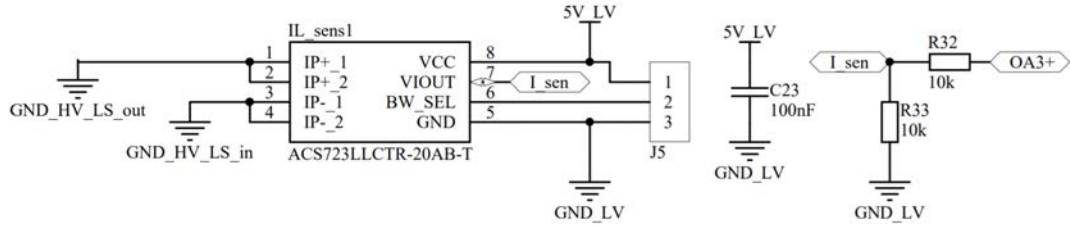


Figure 4.10: Current sensor connection.

The output of the sensor is a voltage proportional to the current following the next equation:

$$V_{current} = \frac{1}{10} i + 2.5 \quad (4.17)$$

In order to ease the task of the control, the signals are filtered by hardware. The current will be used by the MPPT, which frequency is 100Hz. The sensor output is filtered by a low-pass filter which cut-off frequency is 50Hz. The cut-off frequency has been calculated by a thousandth of the switching frequency, which is 50kHz. Also the current might be used in the current controller, this signal will be filtered at 80kHz in order to remove high frequency noise. This cut-off frequency was selected as it is the sensor's bandwidth. The filters are first order low-pass filters implemented with a resistor in series with a capacitor.

In order to calculate the current from the PV module, the converter working mode will have to be taken into account. Assuming continuous conduction mode, the average PV current is:

$$\text{Buck mode} \rightarrow \overline{I_{in}} = \overline{i_{measured}} \cdot D \quad (4.18)$$

$$\text{Boost mode} \rightarrow \overline{I_{in}} = \overline{i_{measured}} \quad (4.19)$$

$$\text{Buck – Boost mode} \rightarrow \overline{I_{in}} = \overline{i_{measured}} \cdot D \quad (4.20)$$

4.1.4 Power Supplies

In the first iteration of the converter, the drivers and the sensors will be supplied by an external 12V voltage source. This source will be used directly to supply the two lower leg MOSFET drivers. To supply the higher leg drivers, two isolating 12V supplies will be used, with the external 12V as input. These will be two TRACO supplies *TMA1212S* [36]. The chosen voltage sensors need a 5V power supply at both input and output of the sensor. These should be isolated from each other. The input side will be supplied by a 5V voltage regulator, *LD1117* [37], and the output side will be supplied by an external 5V source. The current sensor will also be supplied with 5V by the external voltage source. A LED will be added to every voltage source, to indicate if they are working.

4.2 PCB design

4.2.1 PCB structure

In order to proceed with the creation of the PCB, a schematic circuit has been designed. This compiles all the previously mentioned components as well as other components required for current limiting, decoupling, external connections, or safety components for protection. Both PCB and schematic might be found in appendix C.

The schematic has been divided into four main sections, these are *main topology*, *power supplies*, *drivers* and *signal processing*.

The main topology includes the power circuit, this is the MOSFETs, the inductor, the input and output capacitors and the input and output connectors. It also includes discharging resistors for the capacitors which have been sized for one minute discharge time. The gate of the MOSFETs is also connected to the source through a resistor designed for 5ms discharge time. These safety resistors are implemented in order to ensure that the circuit is fully discharged when disconnected. Finally a series Schottky diode is included at the input to protect the components in case of reverse connection. However, this diode can be short-circuited at any moment.

The power supplies include the 12V external input connector and two isolated commutative 12V. These two supplies are necessary to power the gates of the high side transistors and drivers. Lastly, a 5V linear regulator supply has also been connected to feed the sensors. This 5V signal is referred to the power ground, thus the input 5V signal could not be used since it does not share the same ground.

The drivers section is composed of the isolating optocouplers and the MOSFET gate drivers. The PWM signals to the optocouplers come directly from the RT-box, meaning that a connector is also included here. Finally decoupling capacitors are added in the vicinity of the ICs in order to assure that the current peaks needed by these are granted.

The signal processing section is composed by the IC sensors and the operational amplifier. As stated previously, there are 2 isolated voltage sensors and a hall effect sensor for current measuring. Also, voltage dividers are located in this section, these include protection zener diodes limiting 5V output voltage and filtering capacitors, finally amplification resistors are added. The current sensor also includes a selection pin header which will allow different filtering frequencies options. The operational amplifier is also included.

Finally, test points have been added to the signals that might be measured.

4.2.2 Design considerations

Before starting the design of the PCB, some features were considered. First and most importantly, the power side is physically separated from the control side. This separation is done to reduce the electromagnetic coupling that the higher currents and voltages might induce in traces or ICs. A clear differentiation of the hot and cold sides of the PCB is seen in the layout. Also, test points have been located in the periphery of the PCB for easiest and safest testing. Current loops have been minimized as much as possible and ground planes are located across the PCB.

4.2.3 Power Side

One of the most important issues to take into consideration when designing the power traces of the converter has been the size of these. In order to allow a high flow of current through the traces while maintaining a relatively low temperature and a low impedance, the trace minimum width must be properly sized. For that goal a temperature constraint is needed. This constraint was arbitrarily set to 10°C. Which will be the temperature increase of the traces working at full power. This constraint will lead to a high trace width, which is acceptable for a prototype. The calculation of the width has been performed following IPC-2221A[38] recommendations regarding trace width sizing. First, the needed cross sectional area of the trace must be calculated, as explained in equation 4.21.

$$A = \sqrt[0.725]{\frac{I}{0.048 \cdot \Delta T^{0.44}}} \quad (4.21)$$

I stands for the current, and ΔT is the temperature difference constraint. The highest average current will be used. See in equation 4.22 the result.

$$A = \sqrt[0.725]{\frac{12.5A}{0.048 \cdot (10^\circ\text{C})^{0.44}}} = 530,9 \text{ mils}^2 \quad (4.22)$$

When the needed area is known, the width is calculated by dividing the area by the copper thickness. In our case, using 1oz PCB, the thickness is 35μm. See

equation 4.23. It's necessary to perform unit conversion from mils^2 to mm^2 .

$$\text{Width} = \frac{A}{\text{Thickness}} = \frac{0.342\text{mm}^2}{0.035\text{mm}} = 9.78\text{mm} \quad (4.23)$$

Then 10 mm is set as trace minimum width.

The heat sink has conditioned the design of the power side of the PCB since most of the passive components do not fit underneath. The four MOSFETs are located at even distances and at the corners of the heat sink to allow the best possible dissipation. The drivers are also located very close to each one of the transistors to have the shortest path to the gate.

The coil has been cornered since it might induce high interference to other sensible devices. Especially the current sensor, which is hall-effect, has been located as far as possible from its influence. Also the ground plane has been removed from under the inductor in order to reduce interferences.

Finally, the high frequency capacitors are located very close to both power stages and the current loop area has been minimize to reduce the inductive behavior of this loop.

4.2.4 Control Side

The control side has two different parts which are separated according to the ground that they have. On one side are located all the components that share the ground with the power side. This is the power supplies and the voltage dividers. The components that only have the low voltage ground, are located further away from the power circuit and finally some components act as bridges since they have both grounds. These components are the optocouplers and the voltage sensors, both with optical isolation.

This way, it is possible to separate the grounds at both sides reducing the possibility of having a short-circuit which may damage the control unit, in this case, the RT-box. However, the current sensor had to be located directly in the power side of the converter since the main current needs to flow through it. Since the current sensor shares the ground with the control unit, bigger clearances are included in all the traces coming from this sensor to reduce the possibility of short-circuit.

The test points located at the periphery break at some points this isolation clearance that was implemented in most parts of the circuit. However, since the test points are not carrying current and test points would always be removed in a final version of the PCB, this problem has not been considered.

Maximum Power Point Tracking

This chapter contains the control of the non inverting buck-boost converter , so that the PV panel works at the maximum power point during operation. To achieve this, a MPPT algorithm is implemented.

The selection of the MPPT algorithm is based on the knowledge from section 2.2 . The constant voltage method is not applied in the project work. One of the requirements is that the algorithm can track the MPP despite changes in the environmental conditions and this is not possible with an implementation of constant voltage. Since for the algorithm Incremental conductance the program needs more complex commands, the P&O algorithm was chosen due to simpler implementation. At the beginning of the chapter a flow chart of the implemented algorithm is described. To validate the algorithm, a simulation of a non-inverting buck-boost converter with the MPPT algorithm is implemented using the software *PLECS*.

5.1 Perturb and Observe implementation

The basic operation of the P&O algorithm consists of perturbing the operating voltage of the PV module by means of the variation of the duty cycle of the DC-DC converter. After each perturbation the power generated by the PV module is measured (observed) and stored in order to compare it with the previous value of the power. Based on the result of the comparison, the MPP can be tracked by deciding whether the panel's voltage should be increased or decreased in the following perturbation.

There are different techniques for implement the P&O algorithm according to the value of the variable controlled by the MPPT and also whether the perturb value is fixed or variable [39]. The conventional P&O algorithm uses a fixed perturb to generate a voltage or current reference signal for the outer control loop. The outer loop is used to control the switching of the DC-DC converter. Another way of implementing the conventional P&O algorithm is using an adaptive perturb. An example of this could be setting the initial perturbation to 10% of the open-circuit voltage (V_{oc}), after each iteration this value is decreased by 50% until it reaches 0.5% of V_{oc} [39]. A different technique consists on using the duty cycle of the converter

as the variable controlled by the MPPT block. Therefore, it is not necessary to implement the outer control loop. This technique can also be implemented using fix or variable perturb step [39].

The P&O algorithm that will be implemented in this project is the MPPT controlling directly the duty cycle and using a variable perturb step. It was decided to directly control the duty cycle to simplify the control system. On the other hand, an adaptive perturb is selected instead of a fixed one. The reason is that the MPPT takes longer time to reach the MPP, if a small perturb step is implemented. However, using a large perturb step the tracking would be faster but the oscillations around the MPP would be higher [39]. For this reason, it was decided to start with a perturbation step of 10% of the V_{oc} until the system reaches a certain value close to the MPP. At this point the perturbation step is iteratively reduced to one third of its previous value in order to reach accurately the MPP with lower oscillations. Figure 5.1 shows the implementation of the system in PLECS including the MPPT which operates at a frequency of 100 Hz.

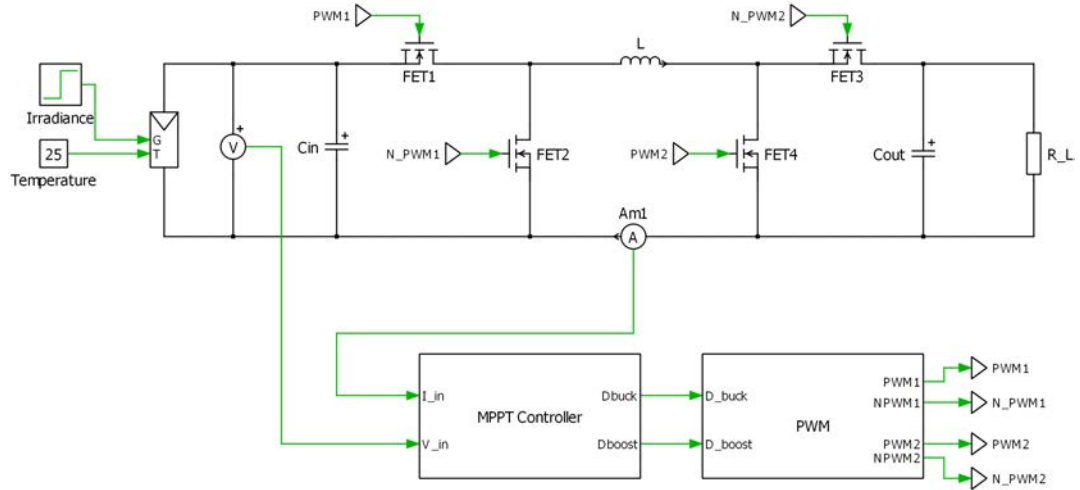


Figure 5.1: Block diagram of the system including the MPPT.

From the previous figure it is observed that the outputs of the MPPT block are the corresponding duty cycles for buck and boost mode.

In order to manage these duties, a control variable called *valg* has been created, it corresponds to the DC conversion ratio of the power converter (V_o/V_i). The conversion ratio has a different dependence on the duty when the MIC is operating in buck or in boost mode. This is shown in equations 5.1 and 5.2, respectively.

The control variable *valg* will be changed to increase or decrease the voltage from the PV panel. When increasing the control variable *valg*, the PV voltage decreases and vice versa. By plotting the corresponding conversion ratios and mapping them as shown in figure 5.2, it is possible to obtain the corresponding duty cycle for the buck or the boost mode. If the control variable from the MPPT is lower than 0.5, it means that the output voltage is lower than the input voltage and thus, the converter will work as a buck converter with duty cycle $D_{buck} = 2 \cdot valg$. On the other hand, if the control variable is $valg \geq 0.5$, the output voltage is higher

or equal than the input voltage and, therefore, the converter will operate in boost mode with duty cycle $D_{boost} = 2 \cdot valg - 1$.

$$\frac{V_o}{V_i} = D_{buck} \quad (5.1)$$

$$\frac{V_o}{V_i} = \frac{1}{1 - D_{boost}} \quad (5.2)$$

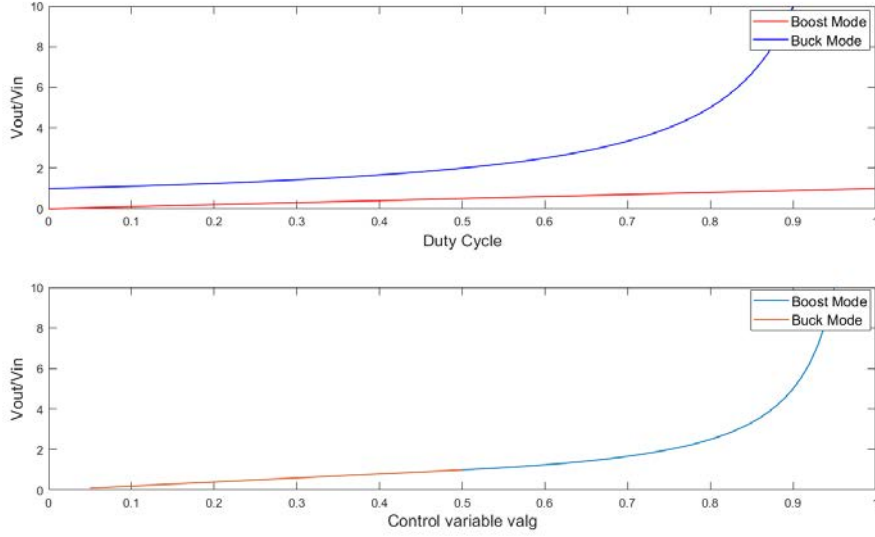


Figure 5.2: Mapping to decide the mode of operation.

The flow chart used for the implementation of the P&O algorithm is shown in figure 5.3. From the flow chart it can be observed that the MPPT is enabled when the panel's voltage has reached the value of the open-circuit voltage. This means that the MPPT detects that the difference between the measured voltage and the previous voltage is lower than 0.1. The MPPT is forced to start at this point to be close to the value of the MPP. Then it starts the open loop behavior. This is done to make the MPPT faster since the algorithm starts with $valg = 0$. The open loop calculation decreases the voltage without evaluating the voltage and power. The condition for starting the MPPT evaluation is that $counter = 15$ to ensure that the point of operation is closer to the MPP.

It is important to notice from figure 5.1 that the current measurement is carried out in the inductor instead of in the PV panel. This is done for possible future implementation of an outer control loop. For this reason, it is necessary to transform the measured current in order to get the corresponding measurement for the PV module's current. This current transformation is just necessary in the case of buck mode as explained in section 4.1.3. If the MPPT detects that the converter is working in buck mode, it multiplies the measured current by the corresponding duty cycle $D_{buck} = 2 \cdot valg$. In boost mode the average current through the inductor corresponds to the PV module's current.

The operation of the algorithm, shown in figure 5.3, is an iterative process. The PV panel's voltage and power, before and after applying a voltage perturbation,

are compared in order to locate the point of operation. This way it is possible to decide if the panel's voltage has to be increased or decreased. Based on the PV characteristic curve shown in figure 1.1, the following situations can occur:

1. Increment of voltage and increment of power means that the point of operation is located to the left of the MPP. Therefore, the perturbation continues in the same direction (voltage is increased) with a fixed perturb step.
2. Increment of voltage and decrement of power means that the point of operation of the panel has gone from being located to the left of the MPP to the right of it. Therefore, the next perturbation is in the opposite direction (voltage is decreased) with a perturb step of one third of the previous step value.
3. Decrement of voltage and increment of power means that the operation point is located to the right of the MPP. Therefore, the perturbation continues in the same direction (voltage is decreased) with a fixed perturb step.
4. Decrement of voltage and decrement of power means that the point of operation of the panel has changed from being located to the right of the MPP to the left of it. Therefore, the next perturbation is in the opposite direction (voltage is increased) with a perturb step as one third of the previous step value.

After the process, once the MPP has been reached, the algorithm oscillates around this optimal point of operation. However in this case, as a variable perturb step is applied, the oscillations around the MPP will be much lower than using fixed perturb step.

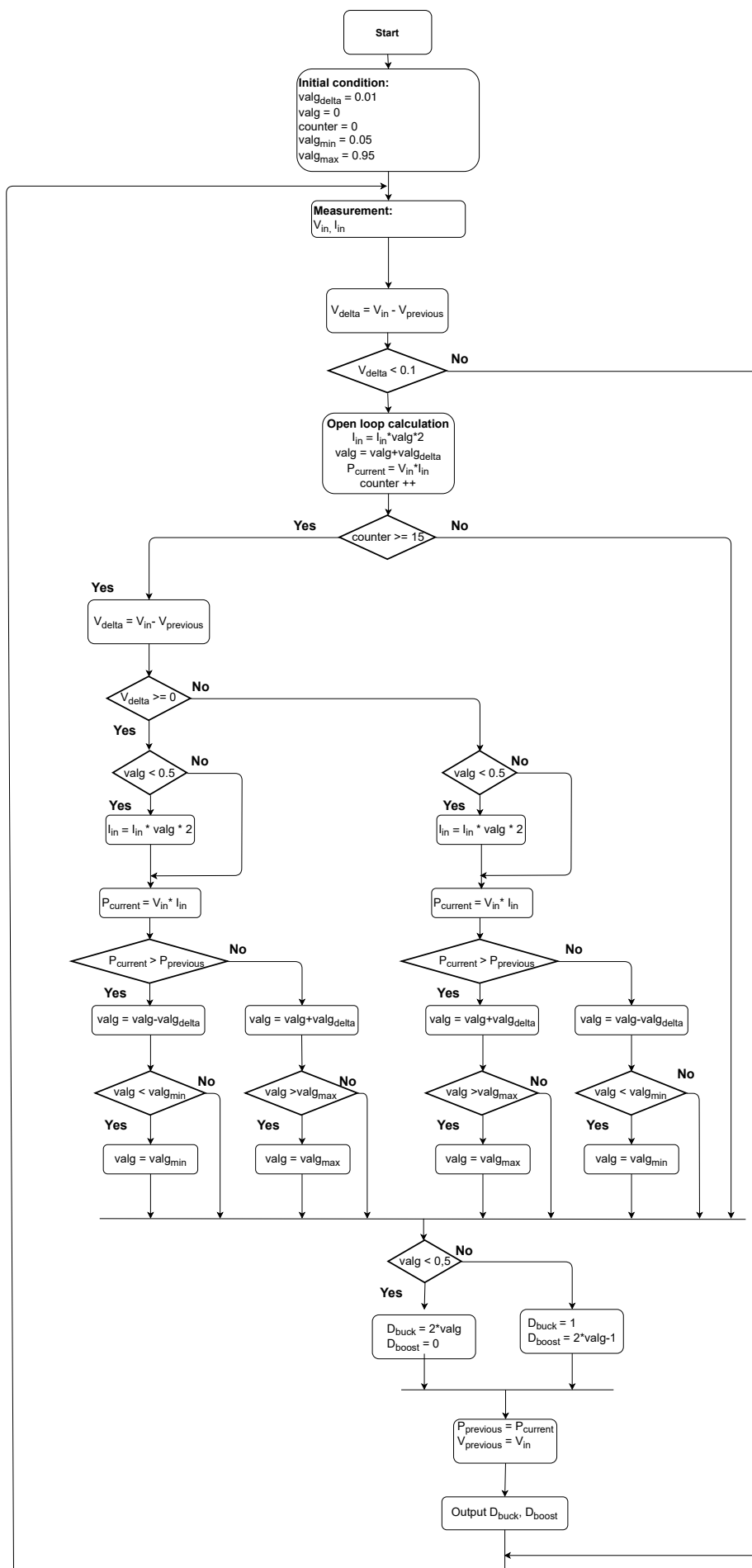


Figure 5.3: Flow chart for the Perturb & Observe algorithm.

5.2 Simulation of the MPPT

The results obtained in simulation for the previously explained P&O algorithm will be shown in this section. First, the results corresponding to the PV panel model will be evaluated without connecting it to the DC-DC converter. Once the model for the PV panel is validated, the results obtained for the complete system will be analyzed in order to show the performance of the MPPT algorithm under different environmental conditions and resistive loads.

5.2.1 Model of the PV panel

This section shows the model and the results obtained from a commercial solar panel selected for the development of this project. The PV panel which will be utilized for the test of the MPPT is *Suntech STP300-24/Vd* [17]. As a result of the PV panel's model, the characteristic curves of the panel will be presented showing its behavior under variations in solar irradiance and temperature.

One of the most common methods for modeling a solar panel is using the equivalent circuit of a solar cell shown in figure 5.4. The model can be represented as a current source connected in antiparallel with a diode [14]. In addition, to model the non-linear behaviour of the solar panel I-V curve the equivalent series and parallel resistance (R_s and R_p) are inserted [14].

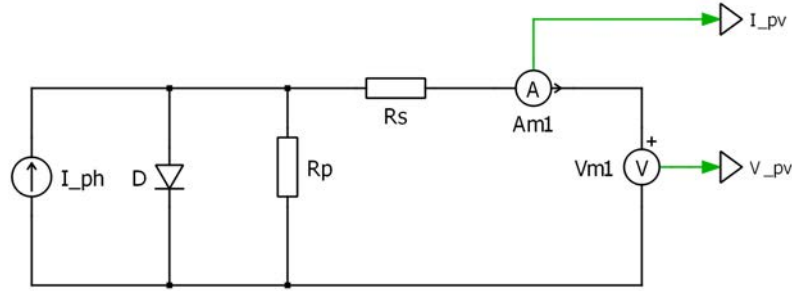


Figure 5.4: Equivalent circuit for modeling a PV cell.

The mathematical equation that describes the circuit is obtained applying Kirchhoff's law to separate the current flowing through the different components of the circuit. This results in equation 5.3 where I_{pv} is the panel's current, I_{ph} is the photogenerated current, the second term is the current flow in the diode and the last term is the current flow in the parallel resistance [14].

$$I_{pv} = I_{ph} - I_o \cdot \left[e^{\left(\frac{V_{pv} + R_s \cdot I_{pv}}{a \cdot V_t} \right)} - 1 \right] - \frac{V_{pv} + R_s \cdot I_{pv}}{R_p} \quad (5.3)$$

The second term corresponds to the Shockley equation where I_o is the saturation current of the diode, a is the diode's quality factor and V_t is the thermal voltage defined by

$$V_t = \frac{N_s \cdot K \cdot T}{q} \quad (5.4)$$

where N_s is the number of series connected cells (in this case 72), K is the Boltzmann constant ($1.38 \cdot 10^{-23} \text{ J/K}$), T is the temperature in kelvins and q is the electrical charge ($1.6 \cdot 10^{-19} \text{ C}$) [14].

However, as the focus of this project is not the modelling of the PV panel, the value of the PV panel's parameters such as R_s , R_p and a required for the model will not be calculated. Instead, these values will be taken from the corresponding PV array block for the selected panel available in *Simulink*. All the values for the PV panel's electrical parameters corresponding to Standard Test Conditions (STC) are shown in table 5.1.

Electrical characteristics under Standard Test Conditions (STC)	
Maximum power (P_{max})	300.4 [W]
Optimum Operating Voltage (V_{mpp})	36.9 [V]
Optimum Operating Current (I_{mpp})	8.14 [A]
Open Circuit Voltage (V_{oc})	45 [V]
Short Circuit Current (I_{sc})	8.67 [A]
Module Efficiency (η)	15.5 %
Operating Module Temperature	-40°C to +85°C
Series Resistance (R_s)	0.266 [Ω]
Parallel Resistance (R_p)	665.2 [Ω]
Diode quality factor (a)	1.1098

Table 5.1: Electrical characteristics PV module *Suntech STP300-24/Vd* [17].

Using the aforementioned model of the PV panel, it is possible to obtain the characteristic curves of the panel. Usually, PV panels are tested under STC to indicate the performance of the PV modules. The STC test is carried out with a cell's temperature of 25°C and at a solar irradiance of 1000 W/m^2 [2]. The higher the solar irradiance, the more power is generated from the PV panel. On the other hand, when the temperature of the PV cell increases the PV panel generates less power than at a lower temperature [2].

Figures 5.5 and 5.6 show the P-V and I-V curves of the solar panel with constant cell temperature ($T = 25^\circ\text{C}$) and varying the level of irradiance. As expected, the lower the level of irradiance the maximum power that the panel is capable of generating decreases. It can be validated that under STC the values for V_{mpp} and I_{mpp} from table 5.1 correspond to the values obtained in simulation. Table 5.2 shows that a change in irradiance has as a consequence a high variation in I_{mpp} but V_{mpp} does not reflect a significant variation.

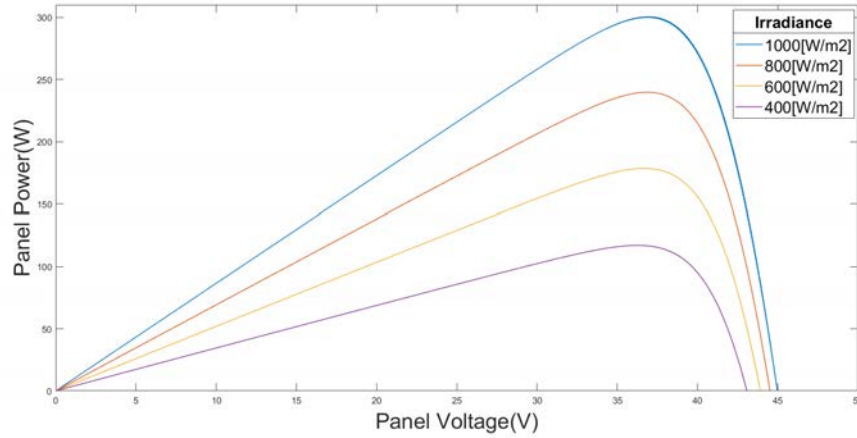


Figure 5.5: P-V curves for constant temperature (25°C) and change in irradiance.

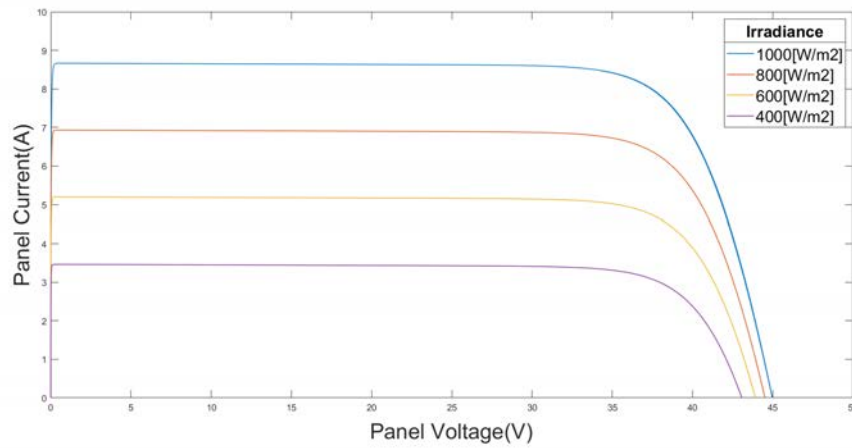


Figure 5.6: I-V curves for constant temperature (25°C) and change in irradiance.

Constant temperature and varying irradiance				
	1000W/m ²	800W/m ²	600W/m ²	400W/m ²
V_{mpp} [V]	36.9	36.87	36.68	36.19
I_{mpp} [A]	8.14	6.49	4.86	3.23
P_{mpp} [W]	300.4	239.5	178.5	117

Table 5.2: PV panel parameters for varying irradiance and constant temperature of 25°C.

On the other hand, figures 5.7 and 5.8 show the characteristic curves with constant irradiance (1000W/m²) and under temperature variation.

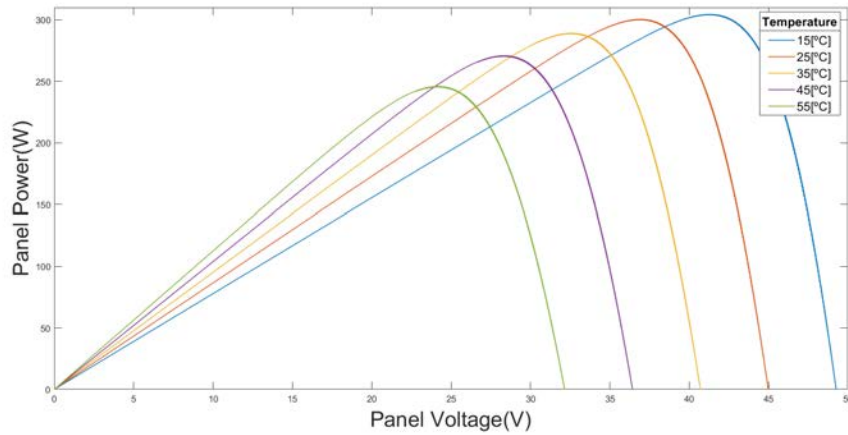


Figure 5.7: P-V curves for constant irradiance ($1000\text{W}/\text{m}^2$) and change in temperature.

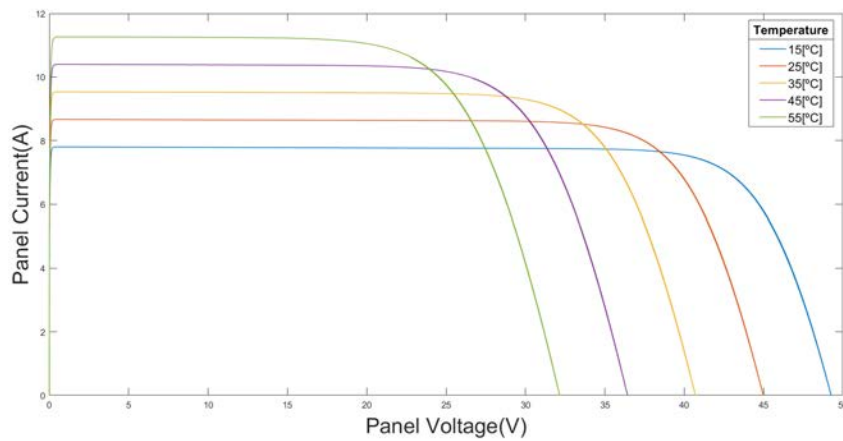


Figure 5.8: I-V curves for constant irradiance ($1000\text{W}/\text{m}^2$) and change in temperature.

It is observed from table 5.3 that an increase in the temperature means that the maximum power that the panel is able to generate decreases. In this case, a change in temperature has as a consequence a high variation of V_{mpp} . However, the variation is not that significant in I_{mpp} .

Constant irradiance and varying temperature					
	T=15°C	T=25°C	T=35°C	T=45°C	T=55°C
V_{mpp} [V]	41.45	36.9	32.59	28.34	24.23
I_{mpp} [A]	7.33	8.14	8.85	9.59	10.12
P_{mpp} [W]	304.3	300.4	289.1	270.7	245.8

Table 5.3: Results of the optimum PV panel parameters for varying temperature and constant irradiance of $1000\text{ W}/\text{m}^2$.

5.2.2 Simulation results

In this section, the results obtained in simulation for the entire system will be presented. The system includes the solar panel, the non-inverting buck-boost converter and the MPPT controller unit as shown in figure 5.1. The simulated results will be analyzed to determine the performance of the MPPT and will be divided in two parts:

- Results obtained under STC. The STC test is carried out at a solar cell's temperature of 25°C and at a solar irradiance of 1000 W/m^2 [2].
- Results obtained under a sudden change in the solar irradiance and temperature.

It was decided to use a resistive load to validate the results obtained in the simulation with the experimental results. All the simulations will be carried out for two different resistive loads: $R_L = 3\Omega$ and $R_L = 27\Omega$. This is done in order to validate the performance of the MPPT controller in both modes of operation.

Standard Test Conditions (STC)

Figure 5.9 shows how the P&O algorithm searches for the MPP. The first graph shows a superposition of the PV panel's voltage and current where it is observed that the panel reaches the open-circuit voltage ($V_{oc} = 45\text{V}$) and at that moment the MPPT starts searching for the MPP by decreasing the PV voltage. The second graph shows the power generated by the panel which approaches the value of the optimal power under this conditions ($P_{mpp} = 300.4\text{W}$). The P&O algorithm converges to the MPP reaching the steady state in 2 seconds. The MPPT allows to reach the optimal power generated by the panel under this conditions with an efficiency of $\eta_{MPPT} = 99.96\%$.

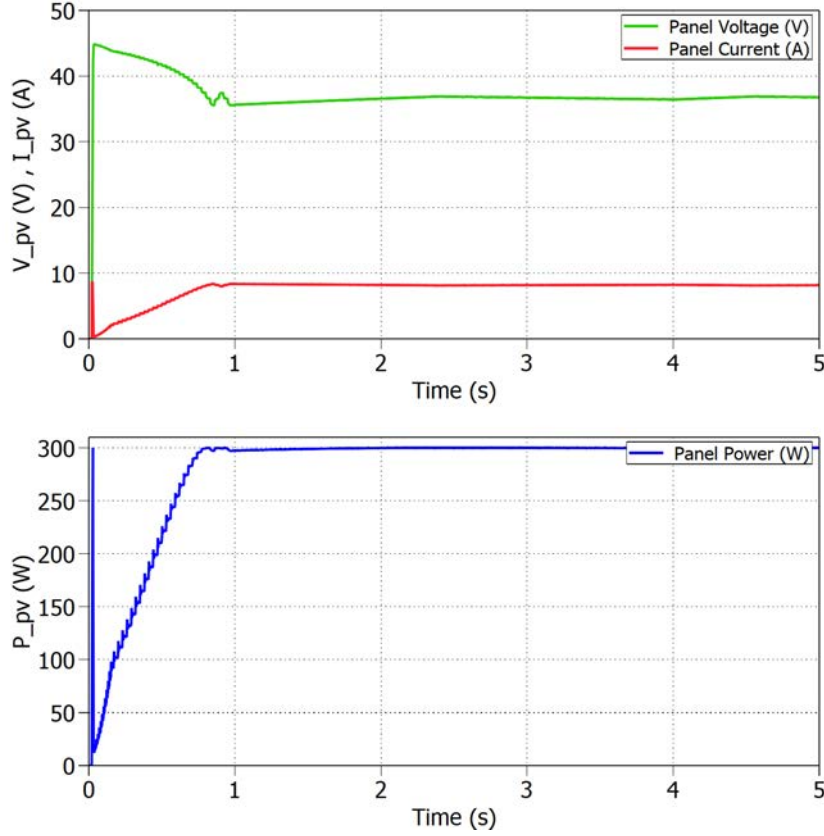


Figure 5.9: Voltage, current and power extracted from the PV panel ($R_L = 3\Omega$).

The simulation is run under STC and using a resistive load of 3Ω . From the first graph of figure 5.10 it is observed that the converter is working in buck mode during all the MPPT process. This is because the output voltage does not exceed the input voltage with this resistive load as shown in the second graph. The value of the duty cycle, obtained in simulation under these load and environment conditions, is $D_{buck} = 0.8155$. Using the transfer function of the converter in buck mode, this value can be validated by calculating the theoretical duty cycle taking as voltage input $V_{mpp} = 36.9V$:

$$D = \frac{V_{out}}{V_{in}} = \frac{30V}{36.9V} = 0.8130 \quad (5.5)$$

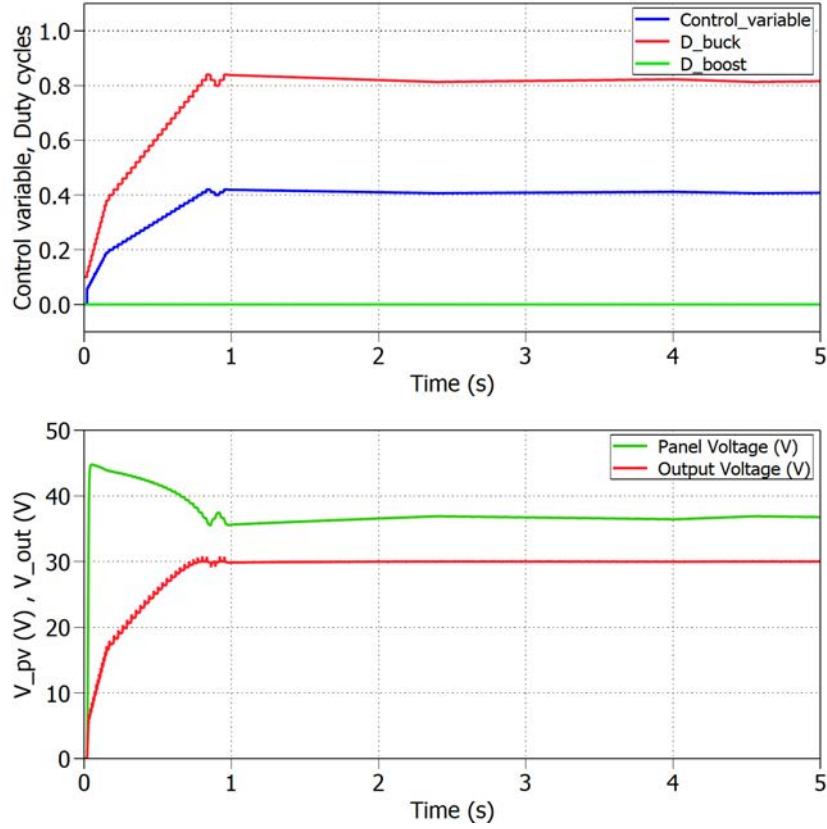


Figure 5.10: Converter's mode of operation as a function of the control variable ($R_L = 3\Omega$).

The same simulation was implemented but in this case using a value of the resistive load of 27Ω . From figure 5.11 it is observed that the MPPT needs more time than before to converge to the MPP. The P&O algorithm needs 4 seconds to reach the MPP which means double of the time than with $R_L = 3\Omega$. This occurs because the output voltage starts increasing from 0 to its final value. This means that the system will start working in buck mode and once the output voltage reaches the value of the input voltage it will switch to boost mode. Despite the higher converging time to the MPP, the P&O algorithm performance has not experience a significant difference. The MPPT is able to operate with an efficiency of $\eta_{MPPT} = 99.82\%$.

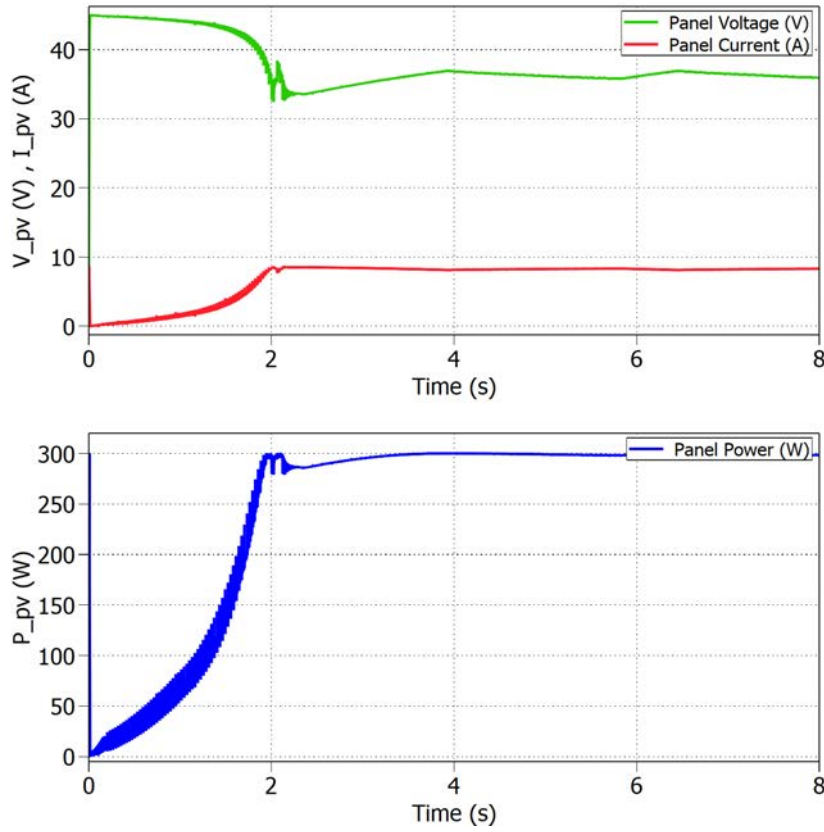


Figure 5.11: Voltage, current and power extracted from the PV panel ($R_L = 27\Omega$).

Figure 5.12 shows how the converter starts operating in buck mode until the output voltage equals the input voltage. At this point is the limit between the two modes of operation and the converter starts working in boost mode. The value of the duty cycle under these load and environment conditions is $D_{boost} = 0.5971$. Using the transfer function of the converter in buck mode, this value can be validated by calculating the theoretical duty cycle taking as voltage input $V_{mpp} = 36.9V$:

$$\frac{V_{out}}{V_{in}} = \frac{1}{1-D} \rightarrow D = 1 - \frac{V_{in}}{V_{out}} = 1 - \frac{36.9}{90} = 0.5900 \quad (5.6)$$

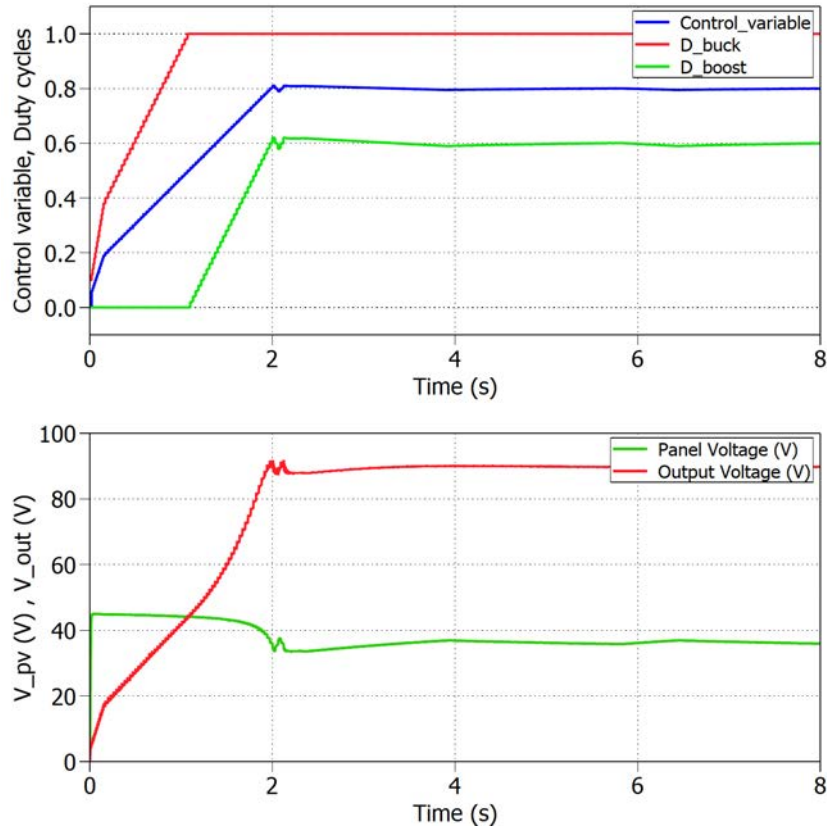


Figure 5.12: Converter's mode of operation as a function of the control variable ($R_L = 27\Omega$).

Change in irradiance and temperature

This section shows the performance of the MPPT when the PV panel is exposed to a sudden change in irradiance and in temperature. First, figures 5.13 and 5.14 show the results obtained for a change in irradiance for the case of buck and boost mode, respectively. The irradiance change is from 1000 W/m^2 to 800 W/m^2 while the cell temperature is kept constant at 25°C . Figures 5.15 and 5.16 show the results for a sudden increase of the solar cell's temperature for both modes of operation. The temperature decreases from 25°C to 15°C by keeping constant the irradiance to a value of 1000 W/m^2 . In all the cases the P&O algorithm can track the MPP by maintaining an efficiency higher than 99%. This way it is validated that the MPPT algorithm works efficiently under sudden changes of irradiance and temperature. However, these situations are not realistic because in real environmental conditions the sunlight and the temperature will not experience such a sudden change.

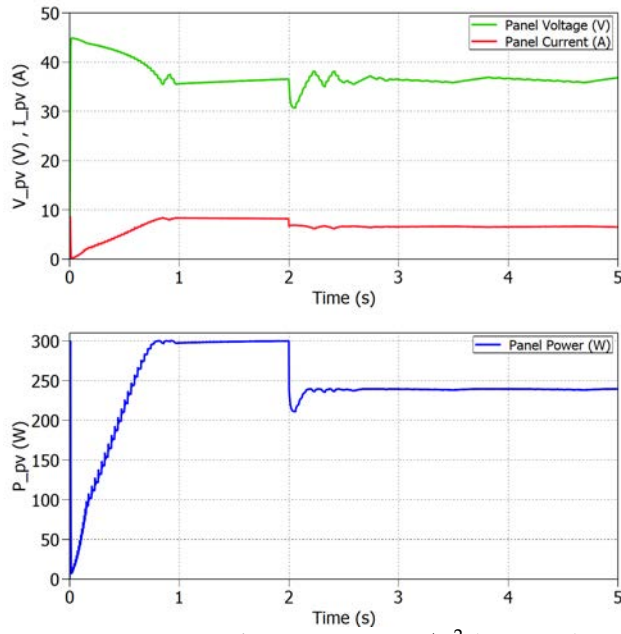


Figure 5.13: Irradiance 1000-800 W/m² ($R_L = 3\Omega$).

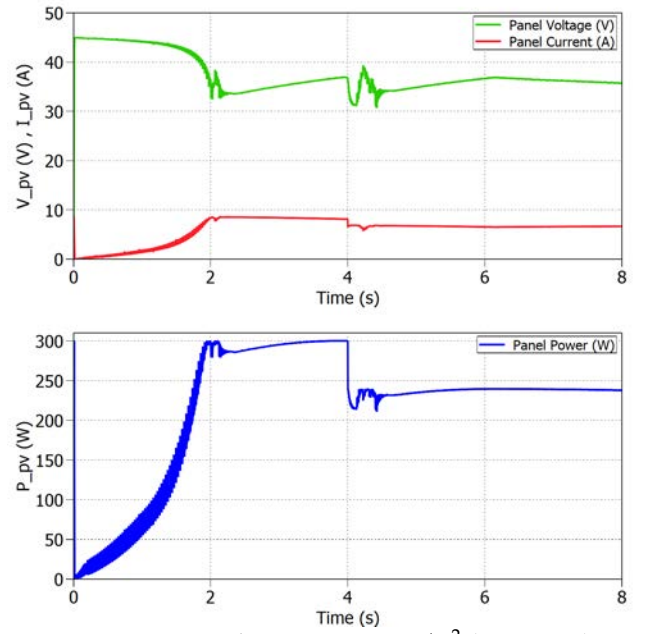


Figure 5.14: Irradiance 1000-800 W/m² ($R_L = 27\Omega$).

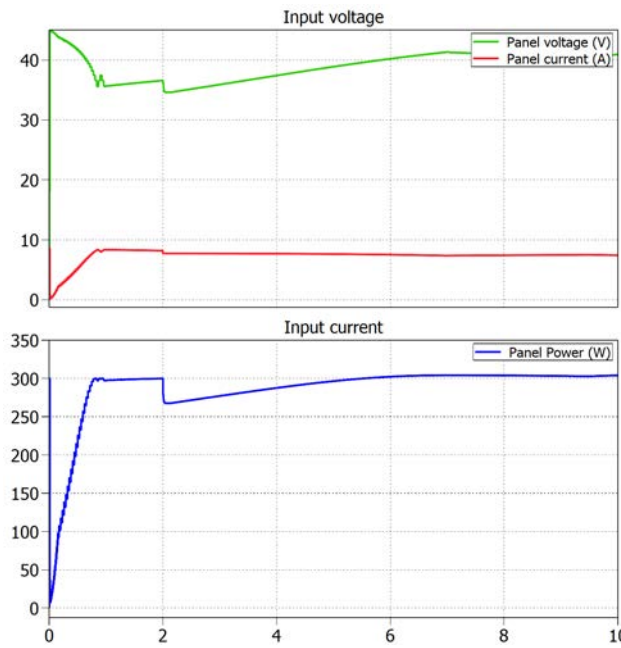


Figure 5.15: Temperature 25-15°C ($R_L = 3\Omega$).

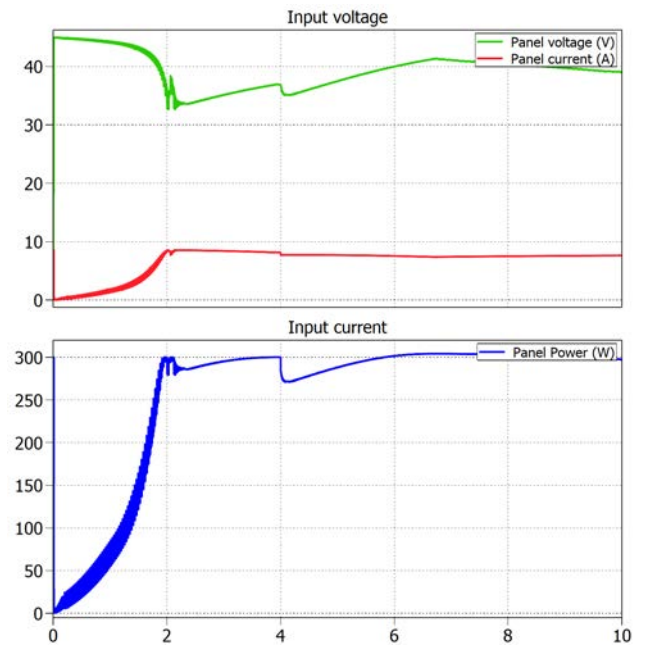


Figure 5.16: Temperature 25-15°C ($R_L = 27\Omega$).

Experimental results

When the design stage is completed, the system must be tested in the PV lab available at Aalborg University. The system design consisted of hardware and control design. The experimental results will show whether the system is compliant with the initial goals. The system test is performed in two steps: first the hardware design is tested without the MPPT controller and, after this step is completed, the complete system will be tested to show the real performance of the MPPT unit.

The hardware design testing is performed following an incremental fashion. The components are individually soldered to the PCB and tested. The tests are short and with clear boundaries. These features ease the errors' finding and troubleshooting. This procedure validates the proper behaviour in the single component but also lets analyse the effect of additional components. The assembly and test procedure will be defined prior to the PCB assembly. The test and its expected results are clear before starting. When the PCB is assembled and all the integration tests are passed, the complete converter is tested. This system test is performed by running the converter with a fixed duty cycle. This test allows the validation of the converter design, including voltage and current ripples, thermal test, gain and losses.

The control design testing must demonstrate that the control signals are properly calculated in order to achieve maximum power generation. These signals are received by the previously tested hardware implementation. The testing consists on black box testing where only a few internal parameters are monitored through the controller's console. The system's stability and dynamic behaviour will be analyzed.

6.1 PCB building

The building of the PCB has been done according to the test described in the following section. It has been divided into smaller tests, to validate that every part of the system works properly. It tests the control part, including the power supplies, optocouplers, drivers and sensors. For this test it has been chosen only to solder the buck leg of the converter to validate the design and discover potential faults. Before starting the test all vias, capacitors and test-points are soldered to

assure connectivity. All components are named according to the schematic placed in Appendix C.

6.1.1 Power supplies

The purpose of the first test is to validate the different power supplies in the converter. For this test it's necessary to solder the in-TRACO and the 5V voltage regulator. The three LEDs and the resistors should also be soldered. Apply 5V at connector J4 and 12V at connector J2. The test is conducted by following table 6.1

Test of power supplies			
ID	Test	Test-points	Pass/Fail
1.1	All LEDs must be lit	DS1-2-4	Pass
1.2	Measure 5V at low-voltage	5V-LV & GND-LV	Pass
1.3	Measure 12V at high voltage, low-side	12V & GND-in	Pass
1.4	Measure 12V at output of in-TRACO	12V-in & L-in	Pass
1.5	Measure 5V at the output of the voltage regulator	5V-HV & GND-sen	Pass

Table 6.1: Test of power supplies.

6.1.2 Optocouplers

The second part of the test is to validate the optocouplers. This tests that the output of the optocoupler should follow the input. For this test it is necessary to solder opto1-2. Start the test by applying 5V at connector J4, 12V at connector J2 and a 5V – 50kHz square waveform with 50% duty-cycle at PWM1-2.

Test of optocouplers			
ID	Test	Test-points	Pass/Fail
2.1	Measure 5V – 50kHz at the input of optocoupler 1	Opto1-in & GND-LV	Pass
2.2	Measure 12V – 50kHz at the output of optocoupler 1	Opto1-out & L-in	Pass
2.3	Measure 5V – 50kHz at the input of optocoupler 2	Opto2-in & GND-LV	Pass
2.4	Measure 12V – 50kHz at the output of optocoupler 2	Opto2-out & GND-in	Pass

Table 6.2: Test of the optocouplers.

6.1.3 Drivers

The next part of the test consist of the drivers. For this it is necessary to solder drv1-2, M1-2 and the resistors R5-R10. Start the test by applying 12V at connector

J2, 5V at J4 and a 5V – 50kHz square waveform with 50% duty-cycle at PWM1-2. The test is conducted by following table 6.3.

Test of drivers			
ID	Test	Test-points	Pass/Fail
3.1	Measure 5V – 50kHz at the output of driver 1	PWM1 & L-in	Pass
3.2	Measure 5V – 50kHz at the output of driver 2	PWM2 & GND-in	Pass

Table 6.3: Test of the drivers.

6.1.4 Sensors

The last part of the control system test consist of the sensor circuits. For this test it's necessary to solder the input voltage sensor U2, the current sensor and the operational amplifier. Furthermore the resistors $R_{17} - R_{22} + R_{25} + R_{32} + R_{33}$ and capacitors $C_{17} + C_{22}$ should be soldered. Before testing a jumper should be placed between J5-2 and J5-3, to select the bandwidth of the current sensor to 80kHz. The inductor, M1 and M3 should also be shorted to achieve a current flow through the current sensor.

Attach a load resistor at 100Ω. With an input voltage at 10V, this should correspond to a output current at 100mA. Because of the differential offset in the current sensor, this should be equal to 2.6V. After test 4.3, raise the input voltage to 20V for validation of linearity in the sensors.

Test of sensors			
ID	Test	Test-points	Pass/Fail
4.1	Measure 10V at the input of the converter	Vin & GND-in	Pass
4.2	Measure 1V at the output of the voltage sensor	Vi-sen & GND-sen	Pass
4.3	Measure 2.6V at the output of the current sensor	IL-sen-Raw & GND-sen	Pass
4.4	Measure 20V at the input of the converter	Vin & GND-in	Pass
4.5	Measure 2V at the output of the voltage sensor	Vi-sen & GND-sen	Pass
4.6	Measure 2.7V at the output of the current sensor	IL-sen-Raw & GND-sen	Pass

Table 6.4: Test of the sensors.

6.2 System test

Once the MPPT algorithm was working as expected, it was tested in the PV lab using the RT Box as the MPPT controller [40]. The RT Box received as analog

inputs the voltage and current measured at the output of the PV simulator. The digital outputs of the RT Box were the PWM signals for switching the MOSFETs. For the tests the PV simulator *E4360* from Keysight Technologies [41] is used to simulate the PV panel *STP300S-24/Vd* from Suntech Power [17]. The experimental setup is shown in figure B.1.

At first the converter is subjected the open-loop test. The reason of this test is to compare the measured voltages and current ripples with the values from the ideal open-loop simulation in appendix A. The second test includes the thermal test. For this test the converter is performed for a longer time to identify which parts of the PCB will be overheated. The last test is about validating the P&O algorithm, if it behaves like in the simulation from section 5.2.

6.2.1 Open-loop test

The open-loop test is carried out to measure the ripples in the inductor current, the input voltage and the output voltage of the converter. The test conditions were explained in section 3.3 and the graphs showing the experimental results are shown in appendix A.

The measured current ripple in the inductor is calculated from figure A.6 and shown in equation 3.10. The minimum current is $I_{min} = 2.7A$ and the maximum current is $I_{max} = 2.98A$. The mean value for the inductor current is $\bar{I}_L = 2.84$.

$$\Delta I_L = \frac{I_{max} - I_{min}}{\bar{I}_L} \cdot 100 = \frac{2.98A - 2.7A}{2.84A} \cdot 100 = 9.86\% \quad (6.1)$$

The result obtained for the output voltage ripple is shown in figure A.5. The ripple percentage is calculated in equation 6.2 using the values obtained from the graph.

$$\Delta V_{out} = \frac{V_{out,max} - V_{out,min}}{\bar{V}_{out}} \cdot 100 = \frac{23.9082V - 23.895V}{23.9V} \cdot 100 = 0.055\% \quad (6.2)$$

6.2.2 Thermal test

For this test, the converter is supplied for 40 minutes a constant input voltage 36.9 V and input current 5.67 A. The converter is performing in buck mode with the fix duty cycles $D1 = 0.96$ and $D2 = 0.04$ in this test. The output power is in this case 250 W. The temperature of the components coil, heat sink are measured during the test because they are the critical components. Figure 6.1 shows that

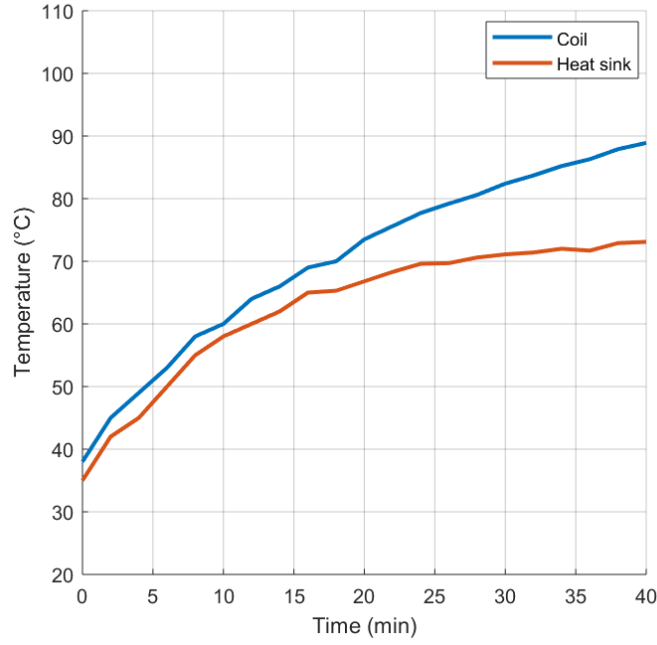


Figure 6.1: Thermal test.

6.2.3 MPPT test

The MPPT test is divided into two parts as it was done for obtaining the simulation results. The test will be implemented for both modes of operation for the converter. For obtaining the results in buck mode a resistive load of 3Ω is used, and for boost mode, 27Ω .

Standard Test Conditions (STC)

For the first test, in both modes, the environmental conditions are set to 1000 W/m^2 of irradiance and temperature 25°C . Figure 6.2 shows how the converter is tracking the MPP in buck mode. The left graph represents the input voltage and current of the converter. At first the input voltage reached the open circuit voltage as in the simulation. After 10 seconds the P&O algorithm reaches the MPP. The maximum average power obtained in the lab from the PV panel is 293.56 W . This can be seen in the right graph in figure 6.2. By comparing the measured value of power with the maximum power that the PV panel can generate under these conditions, the performance of the MPPT can be quantified as shown in equation 6.3.

$$\eta_{MPPT} = \frac{P_{pv}}{P_{mpp}} \cdot 100 = \frac{293.56\text{W}}{300.4\text{W}} \cdot 100 = 97.72\% \quad (6.3)$$

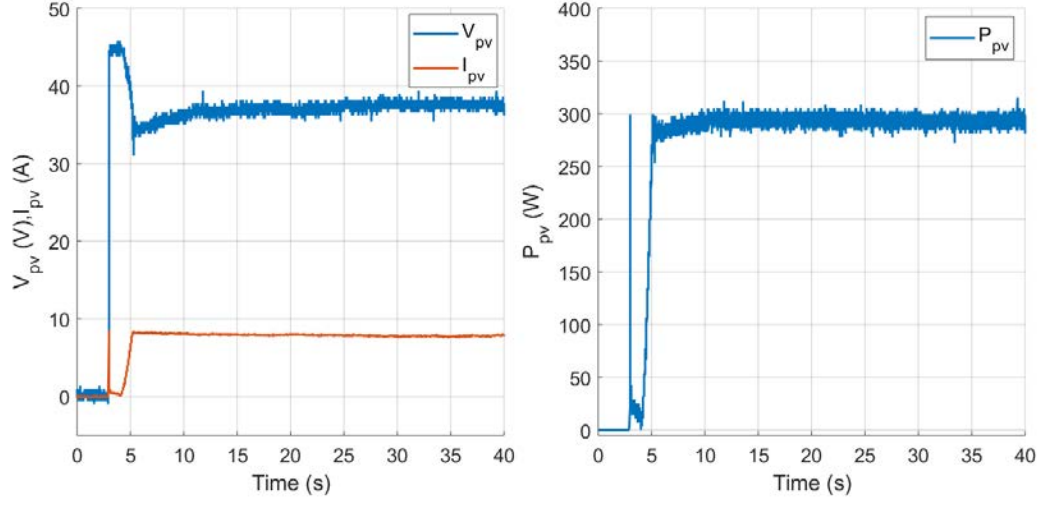


Figure 6.2: Measured voltage, current and power extracted from the PV panel ($R_L = 3\Omega$).

In the left graph in figure 6.3 the relationship between input and output voltage of the converter is observed. From these measurements it is possible to calculate the duty cycle in buck mode for the optimal operating point as in equation 6.4.

$$D_{buck} = \frac{V_{out}}{V_{pv}} = \frac{28.29V}{37.25} = 0.7594 \quad (6.4)$$

The right graph shows the measured input and output power of the converter. From these measurements the efficiency of the converter is calculated in equation 6.5, based on the average values from the graphs.

$$\eta_{converter} = \frac{P_{out}}{P_{pv}} \cdot 100 = \frac{273.44W}{293.56W} \cdot 100 = 93.15\% \quad (6.5)$$

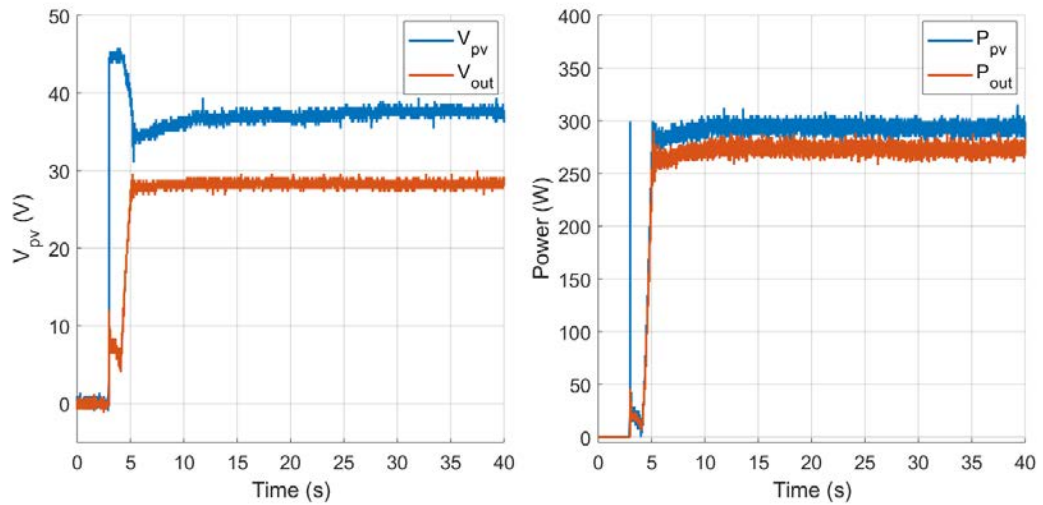


Figure 6.3: Measured voltages and powers at the input and output of the converter ($R_L = 3\Omega$).

Figure 6.4 shows how the converter is tracking the MPP in boost mode. Here again it is observed that the MPPT is enabled after the input voltage has reached the value of open-circuit. The time the MPPT takes to reach the MPP is higher than in buck mode, reaching it in 21 seconds. By comparing the measured power with the maximum power that the PV panel can generate under STC, the MPPT's efficiency is calculated in equation 6.6. It is observed that even though the system needs more time to track the MPP it does not have a significant effect in the efficiency.

$$\eta_{MPPT} = \frac{P_{pv}}{P_{mpp}} \cdot 100 = \frac{292.37W}{300.4W} \cdot 100 = 97.32\% \quad (6.6)$$

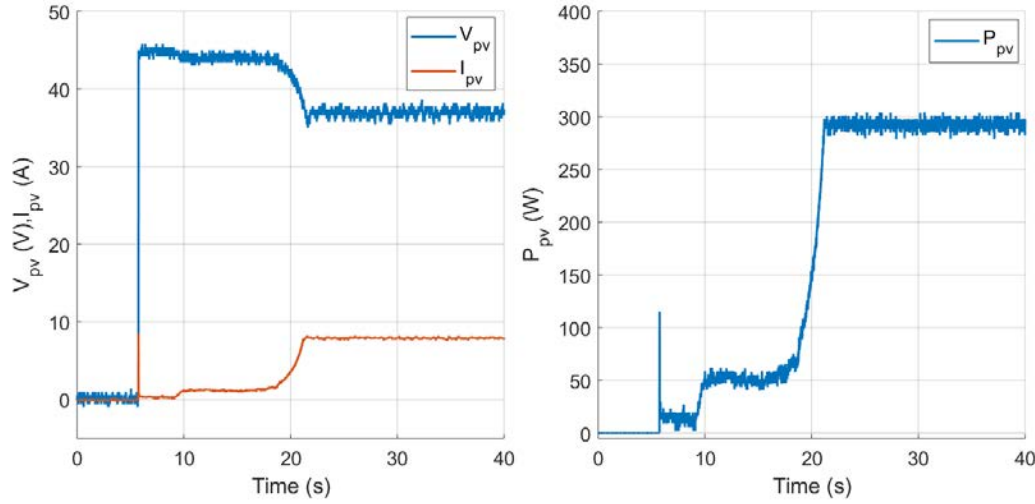


Figure 6.4: Measured voltage, current and power extracted from the PV panel ($R_L = 27\Omega$). picture not right! change axis labels and legend

From figure 6.5 the duty cycle in boost mode for the optimal operating point can be calculated as in equation 6.7. The ideal value of the duty cycle to work in the MPP is 0.59.

$$D_{boost} = 1 - \frac{V_{pv}}{V_{out}} = 1 - \frac{36.93V}{88.41V} = 0.5823 \quad (6.7)$$

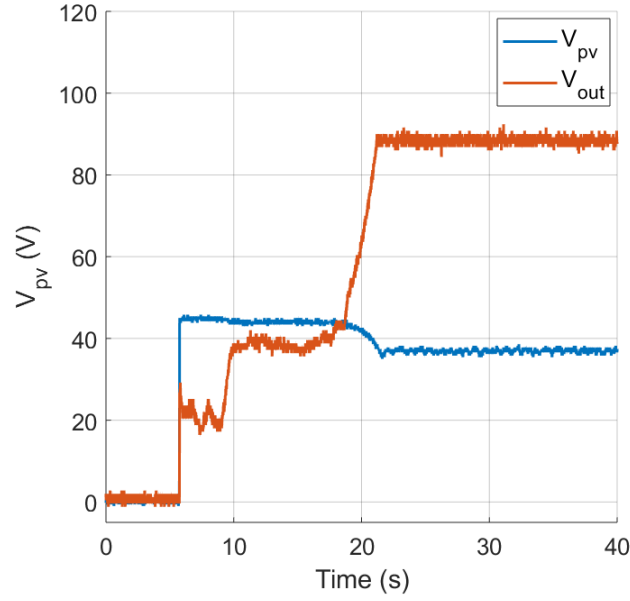


Figure 6.5: Measured voltages at the input and output of the converter ($R_L = 27\Omega$).

Change in irradiance and temperature

For this test the converter was set to work in buck mode by fixing a resistive load of 3Ω . Figure 6.6 shows the measurements obtained for voltage, current and power generated by the PV simulator. It is observed that the MPPT detects the change in irradiance and tracks the MPP. The MPPT's efficiency changes from 95.96% to 93.78% when a sudden change in irradiance from $1000\text{W}/\text{m}^2$ to $800\text{W}/\text{m}^2$ is detected. The time response is 6.6 seconds.

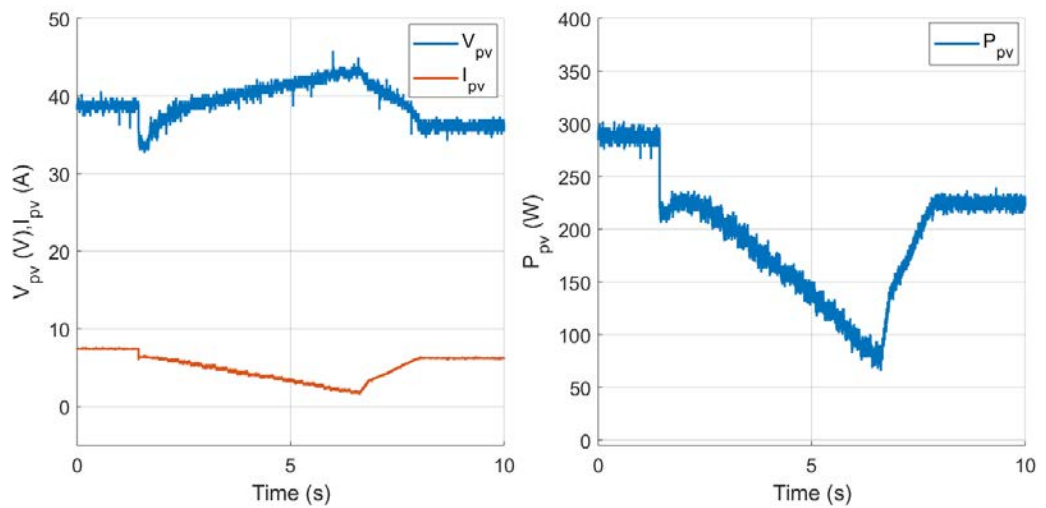


Figure 6.6: Measured voltage, current and powers at the input of the converter with a change in irradiance from $1000\text{W}/\text{m}^2$ to $800\text{W}/\text{m}^2$ ($R_L = 3\Omega$).

Figure 6.7 shows the results obtained for a sudden change in temperature from 25°C to 15°C. It is observed that the generated power increases with decreasing temperature. The MPPT's efficiency improves in this case comparing with the variation in irradiance. It changes from 99.2% to 98.4% in 4.1 seconds.

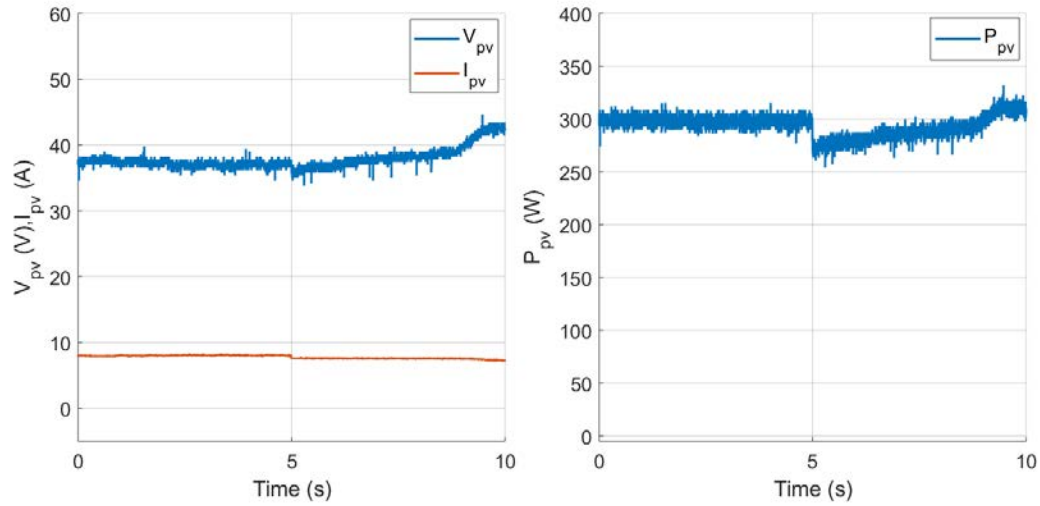


Figure 6.7: Measured voltage, current and power at the input of the converter with a change in temperature from 25°C to 15°C ($R_L = 3\Omega$).

Discussion

In this chapter the technical results of the project are analysed. First, the design verification is performed, showing the simulation and the experimental results. Then, the main impediments found through the project and implementation's limitations are explained. Finally, suggestions for future work are presented.

7.1 Verification of experimental results

In this section the experimental results from the open-loop and MPPT test in section 6.2 are compared with the simulation results from section 3.3 and 5.2.

7.1.1 Open-loop simulation

The table 7.1 compares the values of the ripples from the experiments with the values from the requirements in section 3.3 and the simulation results in appendix A. For the input ripple voltage no simulations have been carried out, since in the ideal case it is a DC voltage source and therefore no ripples can be detected. From the experimental results the signal is noisy and the ripple are too small (or can't detect) to capture values from the figure. The simulation result from the inductor and output voltage ripple have the same value as from the system requirement. This means the components have been selected correctly. For both cases the experiments result for the ripples are smaller than in the simulation. The output capacitor is ten times oversized and so the ripple should be ten times smaller than the calculated one, as you can see in table 7.1. Also the test for the output ripple was tested for buck mode instead of boost mode. This is not the worst case for the output voltage ripple.

	Requirement	Simulation	Experiment
ΔV_{in}	0.1%	0.08%	-
ΔI_L	10%	10%	9.86%
ΔV_{out}	0.5%	0.5%	0.055%

Table 7.1: Voltage and current ripple.

7.1.2 Maximum Power Point Tracking (MPPT)

The proposed Perturb and Observe algorithm was simulated and also tested in the PV lab to show its real performance. The simulation was implemented in PLECS because this software allows to program easily the C-code for the MPPT algorithm. The results obtained showed MPPT's efficiencies higher than 99% for the different levels of irradiance and temperature. As mention in previous chapters, the MPPT algorithm was designed with the objective of increasing the power generated by the PV panel. This was achieved in simulations together with fast MPP tracking and low oscillations around the MPP.

Table 7.2 shows the simulated results together with the experimental results for STC. The experimental results show that the MPPT's efficiency is higher than 97%. Therefore, the performance of the proposed P&O algorithm is in the rate of the most common MPPT algorithm which varies between 96% and 99% [14]. For the case of the conventional P&O algorithm, the MPPT's efficiency is around 96% [14]. Hence, the modifications applied to the conventional P&O algorithm allowed to improve the MPPT's performance.

Standard Test Conditions (STC)				
	Buck Mode		Boost Mode	
	Simulation	Experiment	Simulation	Experiment
η_{MPPT}	99.96 %	97.72 %	99.82 %	97.32 %
t_{MPPT}	2 s	10 s	4 s	21 s

Table 7.2: Simulated and experimental results for the P&O MPPT algorithm under STC.

Comparing the experimental results with the simulated ones, from table 7.2, it is seen that the time the MPPT takes to reach the MPP is five times higher than in simulation . On the other hand, by comparing the efficiency of the MPPT algorithm, it is seen that the absolute error is 2.24% and 2.5% for buck and boost mode, respectively. Therefore, the P&O algorithm is considered accurate enough to validate its performance under STC.

The second test was implemented to observe the performance of the MPPT algorithm under sudden changes in irradiance and temperature. Table 7.3 shows that in the case of change in irradiance, by keeping constant the temperature to 25°C, the measured MPPT's efficiency is reduced. The maximum error is achieved when the P&O is tracking the corresponding MPP for 800W/m². The absolute error is in this case 5.92%. It is also observed that in simulation the response time is much lower than under STC. However, a time ratio between simulation and test is 13.2 in this case. For the sudden change in temperature, by keeping constant the irradiance to 1000W/m², the MPPT's performance is considerably improved. The maximum absolute error is 1.5%. Moreover, a faster MPP tracking is achieved in this case.

IS IT FAST/SLOW? ASK THE SUPERVISORS.

Change in irradiance and constante temperature		
	Simulation	Experiment
η_{MPPT}	99.81% - 99.70%	95.96% - 93.78%
t_{MPPT}	0.5 s	6.6 s
Change in temperature and constant irradiancie		
	Simulation	Experiment
η_{MPPT}	99.81% - 99.90%	99.20% - 98.40%
t_{MPPT}	2 s	4.1 s

Table 7.3: Simulated and experimental results for the P&O MPPT algorithm under sudden change in irradiance ($1000\text{-}800\text{W}/\text{m}^2$) and temperature ($25\text{-}15^\circ\text{C}$) in buck mode ($R_L = 3\Omega$).

7.2 Problems and limitations

7.2.1 Output capacitor

The output capacitor was sized 10 times too big, because of a calculation error. This meant that the voltage ripple at the output was in the range of 10 times lower than the requirements stated. To achieve an output ripple voltage at 0.5% with a margin at 20%, a $100\mu\text{F}$ capacitor should be used. A suggestion could be this $100\mu\text{F}$ electrolytic capacitor from Panasonic [42].

7.2.2 MPPT drifting and improvement and limitations of final control algorithm

The development of an embedded control system requires the proper working of an algorithm. During the development process, the engineer might find that the code doesn't behave as intended. A common way of supporting the debugging process consists on the use of breakpoints, where the code is stopped and the variables' value might be read. However, as this feature is not supported by the used platform, and in the case of controlling physical systems its use would be limited to simulation, alternative techniques had to be used. The adopted approach consisted on outputting the FSMs state and relevant values for the current state at every code execution loop. The 'Timestamp' field is specially important during simulation in order to track specific events at determined times. See figure 7.1.

```

-----
Timestamp: 0.180000
System state: VOLTAGE_EV
Vprevious is: 44.859024
V is: 44.840965
Delta_V is: -0.018059
Control Variable is : 0.200000
****
Delta Duty state: COARSE_POWER_MAPPING
Coarse mapping counter 2
Delta_D is: 0.010000
-----

```

Figure 7.1: Console output.

In initial implementations of the control algorithm, the voltage evaluation was performed in the state next to the duty cycle change. After this change, the system experiences a transient stage where the input voltage and inductor current evolve into the new steady state value. If these variables are read during the transient, the control might infer that the PV panel is in a location of the P-V curve different than where it actually is. The MPPT becomes noisier under this scenario. In order to address this issue, an additional waiting state was added to the FSM governing the system. Another solution to the issue would be to decrease the MPPT algorithm periodicity. However this solution would lead to a decrease in system's responsiveness. This drawback might be bearable by implementing a voltage controller aside from the MPPT.

The noise in measured signals highly influenced the algorithm performance. This noise was addressed by software low pass filtering. The filter caused a dramatic improvement in signal acquisition and system response, further details are explained in the next section.

In order to develop a completely reliable algorithm further testing must be performed. These testing activities require more advanced debugging information than the console output previously shown. RT-box allows SPI communication but the testing activities would still be limited to black-box techniques. In order to reach white-box testing, the implementation would require a microcontroller instead of the RT-box. In that case, the variables' value might be directly accessed with a debugger. Also in the case of black box testing the signals are sent with a known and fixed latency in a microcontroller, which is not the case when using PLECS's console.

The implemented algorithm has more advanced functions than the simplest implementation found in introductory application notes from manufacturers, like [6]. Among the advanced functions are tunable threshold parameters, waiting for the PV to reach open circuit voltage or variable perturb step, among others. However, this additional features add difficulty to testing activities and code comprehension. Under the development of a commercial product, it might be desirable to limit the features in order to decrease test and validation activities' cost. The decrease of the perturb variable itself consists of a FSM with 5 states with a weak coupling with the main FSM. The appropriate testing of the code requires software design and testing knowledge.

The proposed implementation has some variables which might be further optimized, like the initial value of the perturb step value, or the threshold to decrease the perturb step value.

7.2.3 Software filter

Although the voltage and current measurement is filtered, the signal read by the control system was noisy. This noise affected the MPPT algorithm disturbing its ability to reach the MPP. Such noise might have different sources within a lab with such a big amount of hardware equipment. There are many techniques in order to address noise issues, the used technique consists on the use of digital filtering (LPF). This digital filter is a simple code that performs the filtering at a given frequency. Being a first order filter, it was simple and fast to implement. The result

can be seen in 7.2. It consists on an exponential moving average low pass filter.

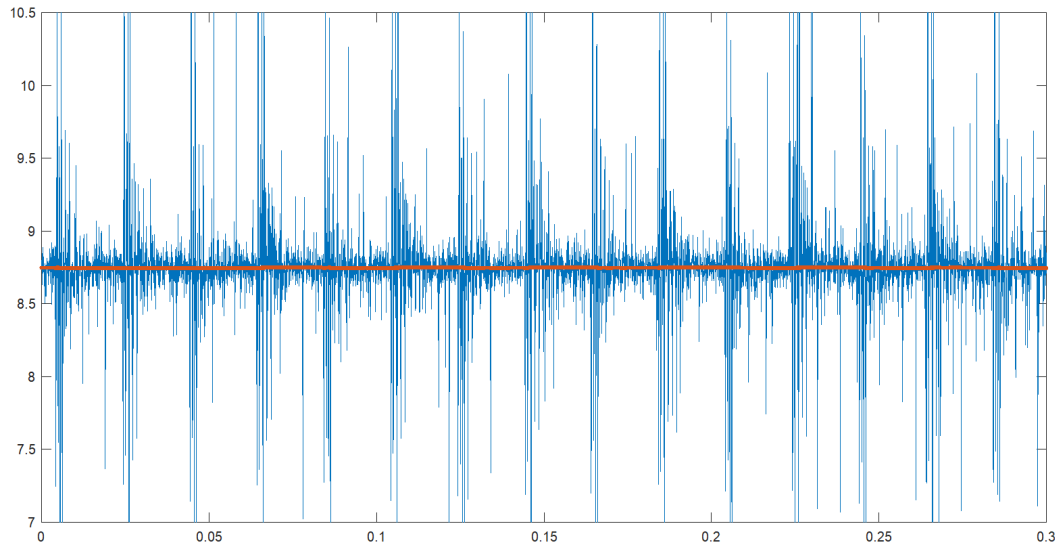


Figure 7.2: Current measurement against time. Both software filtered (red) and raw (blue) signals can be seen. The filtered signal data points' size has been increased to improve readability.

7.2.4 Coil

Since the scope of the project was the validation of the converter, it was decided to implement an existing inductor. A coil was then selected with an approximate inductance of slightly over $1mH$. The PCB was then designed for this initial inductor. However, after some tests under high currents it was shown that the coil was not maintaining its inductance due to saturation of the core. Also, it was reaching temperatures over $100^{\circ}C$. The inductance was then tested under different currents and the behavior was verified as shown in figure 7.3.

It was then decided to implement another inductor which would satisfy the requirements in all cases. The same tests were performed for the new inductor and it was shown that it would fulfill the requirements without problems. Also, some thermal tests were performed on the new inductor. With a constant current of $10A$, it shows a maximum temperature of $60^{\circ}C$ after 10 minutes.

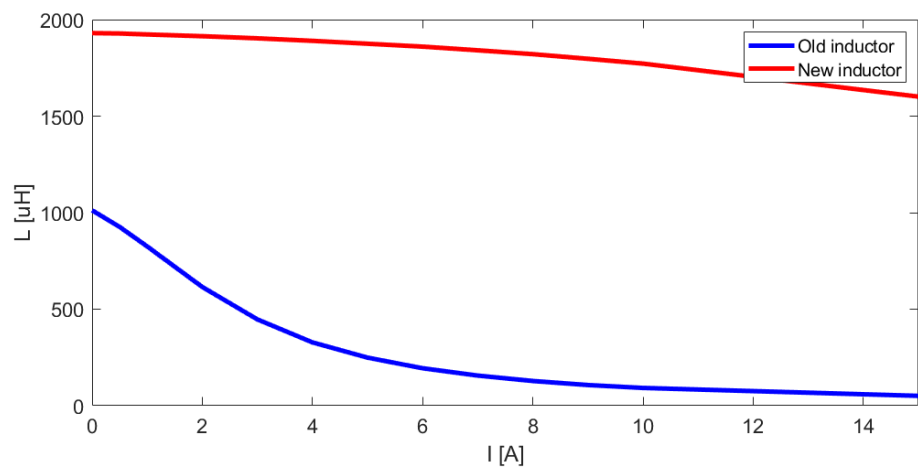


Figure 7.3: Inductor comparison under changes on current flow (50kHz).

However, the size and weight of the new inductor are much higher than those of the previous one. This means that the footprint designed is not valid for the new coil and it hangs loose outside the PCB.

7.2.5 Driver

The converter is not working properly in boost mode. Sometimes we managed to get some test results from it, but at some point it always stopped working. When this happened the Drv4 burned and needed to be changed. The exact reason can be due to many things and is still a concern. 7.4 shows the output voltage of the driver after the gate resistors R11 and R12:

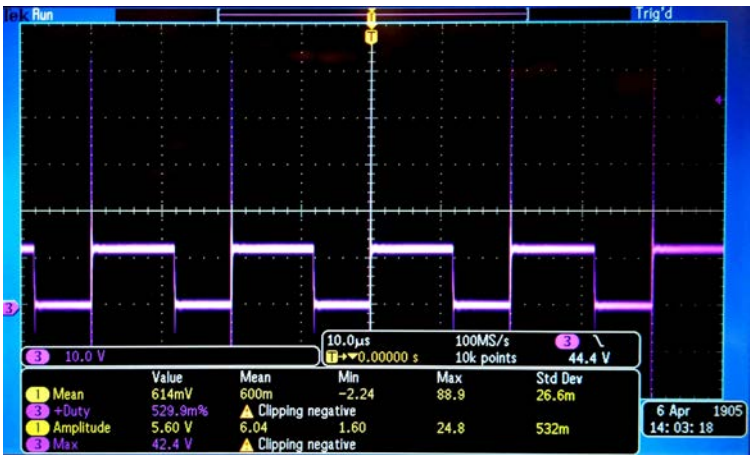


Figure 7.4: Output voltage of driver after gate resistors 20Ω

Looking at the graph it can be seen that the switching spikes is reaching above 50V. This means that a big current will run through the driver and MOSFET while switching which might be why the driver burns. To lower these voltage spikes the gate resistors were changed to two 100Ω instead. This results in the graph at 7.5

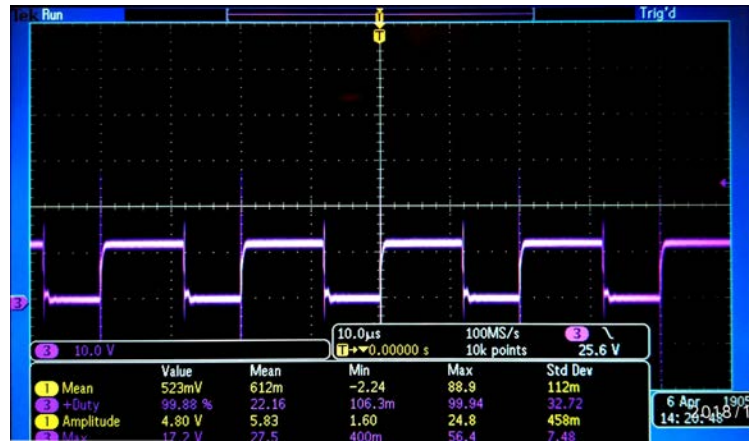


Figure 7.5: Output voltage of driver after gate resistors 100Ω

As expected the changed resistors has decreased the voltage spikes to a bit above 20V. However, this did not solve the problem since the driver still broke. Removing the spikes completely and trying other ways to fix the problem will be done in the future. Because of this issue it was not possible to measure the worst case output ripple voltage of the converter which is in boost mode. Therefore the experimental result of the output voltage ripple has been done for buck mode instead.

7.3 Future work

This section will describe the planned future work of the project. This includes parts that were prioritized low or Simplified to achieve a working converter. Furthermore it includes improvements that was discovered during both the development and testing period of the project.

7.3.1 MPPT technique

Even though the P&O algorithm was implemented, initial research showed that the incremental conductance method could have been a better option. With the Implementation of an incremental conductance algorithm the response is more smooth and the tracking of the operating point is more accurate comparing to the classic P&O. Further research and simulations will have to be made for comparing the two methods. [43]

7.3.2 V/I controller

The developed MPPT algorithm controls system's generated power. However system's transients are not considered. In order to properly govern transients a controller should be added. In that scenario, the MPPT algorithm's output will be the desired PV voltage. This input voltage reference will be feed to the controller, which will output a duty ratio. The controller has a higher execution frequency

than the MPPT. Then this controller is able to control system's transients as desired, the desired system response might be chosen by the designer by tuning appropriately controller's parameters. The use of the controller will reduce system's oscillations reducing wrong MPPT inferences.

7.3.3 Hardware improvements

In the first two iterations of the converter design, the driver circuits have been designed using isolated power supplies for the high side drivers. These are costly both in size and money. Because of that it's preferable to implement a bootstrap circuit for the drivers. An option for a driver including bootstrap could be UCC27211[44]. This includes both a high and low side driver, such that only two IC's are necessary for the converter. The input threshold is below 2.8V for both sides, which means that a 5V optocoupler could be used for isolation. For cost and size optimization the optocouplers should be one quad optocoupler, instead of four singles.

7.3.4 Coil design

The coil used for the converter is reused from an earlier project. Measurements shows that it's oversized regarding current ratings as shown in section 7.2.4. To achieve an optimal inductor, it needs to be designed for the specific requirements for this converter. Both the core size and wire diameter depends on the wanted current rating of the converter[11]. Therefore it should be researched if a physically smaller coil is obtainable.

7.3.5 PCB improvements

The PCB designed for this project is highly focused on easing the tests in the laboratory. For this, test points have been located all around the PCB and LEDs were placed. Also, the width and clearance of the control traces have been oversized since it was going to be created with a CNC. The top overlay was also not going to be visible so text had to be milled in the top layer. The power capacitors could also be reduced in size if a final product was created.

For a commercial version of the PCB, other considerations would be taken into account. By increasing the switching frequency of the converter, an improvement on passive components size could be achieved. Minimizing the packages of ICs and getting rid of others, such as the output voltage sensor, would also reduce cost and size. Finally, by increasing the number of layers on the PCB, better performance and smaller size is achievable.

For these reasons, a commercial version of the product would be much smaller. Also, as explained in section 4.2.4, the removal of the test points and the LEDs would entail a better isolation between the control and power sides.

7.3.6 Converter's efficiency

The main purpose of the MIC is to maximize the output efficiency of a PV-panel. To achieve a good performance of the whole system, the efficiency of the converter

Consider discussing the fact that the inductor is probably the most expensive component around and that an increase of the switching frequency is probably necessary for a real product, for price, size, weight.

itself should be maximized. During the tests, the converter's efficiency was measured to be 93.15% for the worst case. Other papers show that an efficiency of up to 95 – 96% should be achievable[11], [45].

Conclusion

During the last decades, pollution and climate change have become some of the most important issues that human kind is facing. The generation of renewable electric energy will play a major roll in the mitigation of these problems.

One of the most promising technologies that will allow this transition is the photovoltaic generation. In order to maximize the efficiency of solar panels, a module integrated converter was designed. The hardware was created and a maximum power point tracking algorithm was developed.

After coming up with the most adequate power topology, a non-inverting bidirectional buck-boost, the system was divided into three main sections; hardware, control and software. All of which were developed, implemented and tested.

The conception of the hardware consisted on the sizing and selection of all the components, the design of a printed circuit board and the assembly. The PCB has performed according to expectations, the correct sizing of the traces and components have been confirmed and thermal tests show relatively low temperatures in all power components. However, there have been problems with certain components, especially drivers, that have broken down under stress. For this reason, it is concluded that hardware and software protection should have been reinforced to prevent failure during testing. The protection circuitry that was added, like pull down resistors or zenner diodes have proven their importance maintaining the components and the people safe. An implementation of error recognition hardware and software would have solved this problem, saving time and money.

It was also found that testing and validation of the PCB is very time consuming, but the test points added have been very useful for debugging and data collection. One of the biggest obstacles during the development of the project was the lack of error feedback and protections of the hardware during the tests. This problem led to a slowdown on the testing process since the sources of the errors took a long time to be discovered.

The control consisted of the research of existing methods and the development of a suitable algorithm. Since the perturb and observe algorithm is not able to reach very high efficiencies, an improved version was developed. With this new control strategy, average efficiencies up to 99.96% were reached in simulations and up to 97.7% during experimental tests. However, a more advanced kind of control

could lead to better performance.

The design of a software that implements such algorithm was performed. It was discovered that the measured signal noise played an important role in the MPPT accuracy. A software low-pass filter was then integrated and it was found that this is a very convenient method in terms of flexibility and cost. Similarly to the hardware development, it was noticed that in order to develop a more reliable software, many tests would be necessary.

The reasons for making the topology bidirectional included rapid crack recognition on the PVs as well as lower absolute losses when multiple MICs were connected in series, however, these topics were not scoped during the project and thus there is room for future research.

On the road to a more environmentally friendly generation of electrical energy, the goal of this project is fundamental. Improving the efficiency of energy production entails more cost effective products. This will ultimately lead to the viability of renewable energy production worldwide.

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Open-loop ripple results

The measurements and calculations of the current ripple and the voltage ripples are included in this section. Furthermore the section is divided in the simulation result and experiment result.

A.1 Simulation

The figures in this section shows the waveforms of the current and voltage ripples under worst case conditions. These conditions have been described during the calculations of the passive components in section 3.3. The maximum, minimum and mean values will be read and used to calculate the ripples in section 3.4. The data from the simulations have been loaded into Matlab to achieve accurate readings.

Figure A.1 shows the current ripple in the inductor. The maximum and minimum currents are read as $I_{max} = 3.465A$ and $I_{min} = 3.135A$, with a mean at $\bar{I}_L = 3.3A$.

Figure A.2 shows the voltage ripple at the output capacitor. The maximum and minimum voltages are read as $V_{max} = 90.22V$ and $V_{min} = 89.77V$, with a mean at $\bar{V}_{out} = 89.995V$.

Figure A.3 shows the voltage ripple at the input capacitor. The maximum and minimum voltages are measured as $V_{max} = 36.94V$ and $V_{min} = 36.91V$, with a mean at $\bar{V}_{in} = 36.925V$.

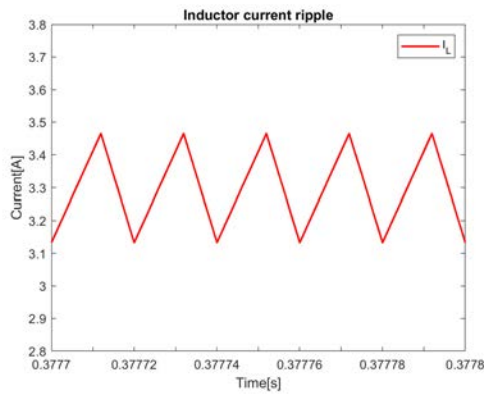


Figure A.1: Inductor current ripple.

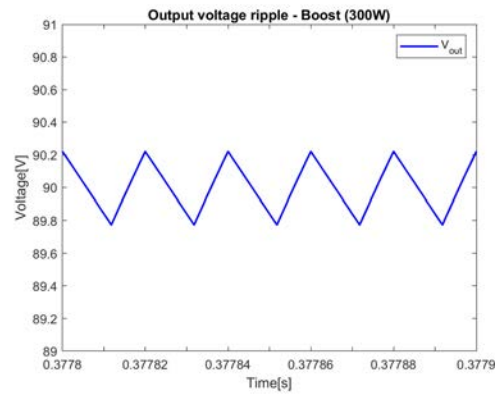


Figure A.2: Output voltage ripple.

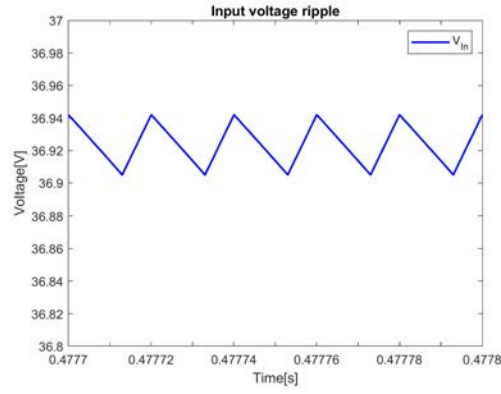


Figure A.3: Input voltage ripple.

A.2 Experiment

The signal of the input capacitor voltage is noisy as you can see in figure A.4. So it is not possible to measure the ripple.

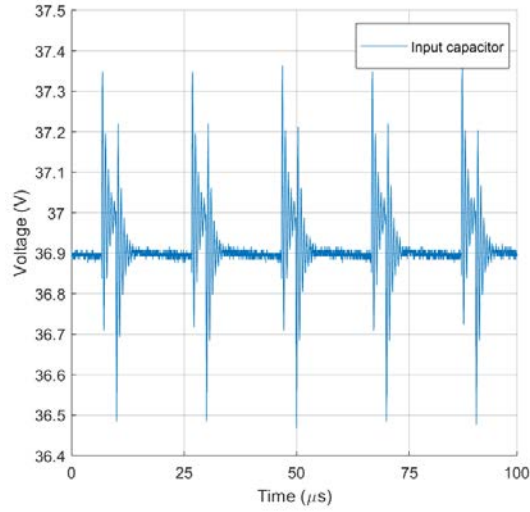


Figure A.4: Open-loop test: Input capacitor ripple.

The figure A.5 presents the voltage ripple at the output capacitor. Because of the noise it is difficult to capture the exactly value for the maximum and minimum voltage from the triangle wave. For the equation 6.2 the values $V_{out,max} = 23.9082V$, $V_{out,min} = 23.895V$ and $\overline{V_{out}} = 23.9V$ are used from the figure A.5.

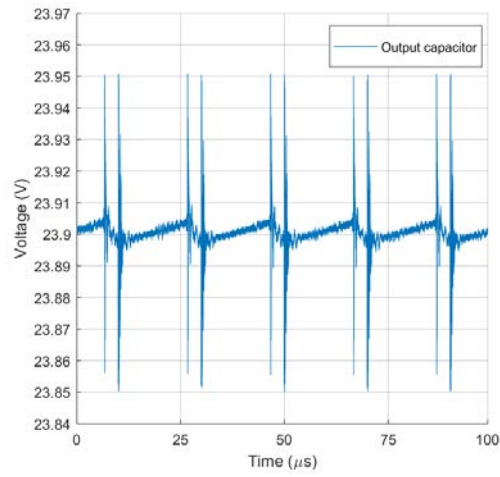


Figure A.5: Open-loop test: Output capacitor ripple.

The figure A.6 shows the current ripple at the inductor. From this figure it can be obtained the minimum current $I_{min} = 2.7A$ and the maximum current $I_{max} = 2.98A$. The mean value for the inductor current is $\bar{I}_L = 2.84$.

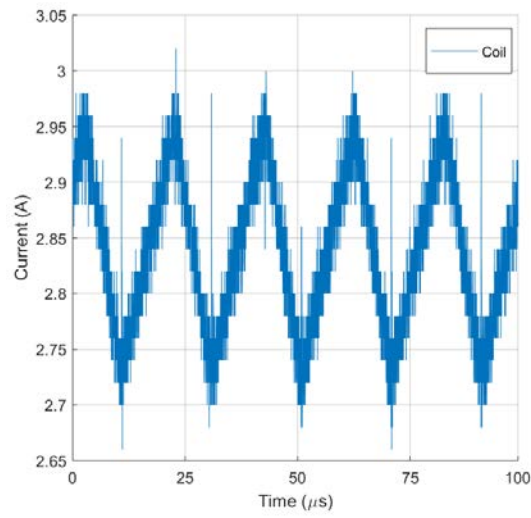


Figure A.6: Open-loop test: Inductor current ripple.

B

Test setup

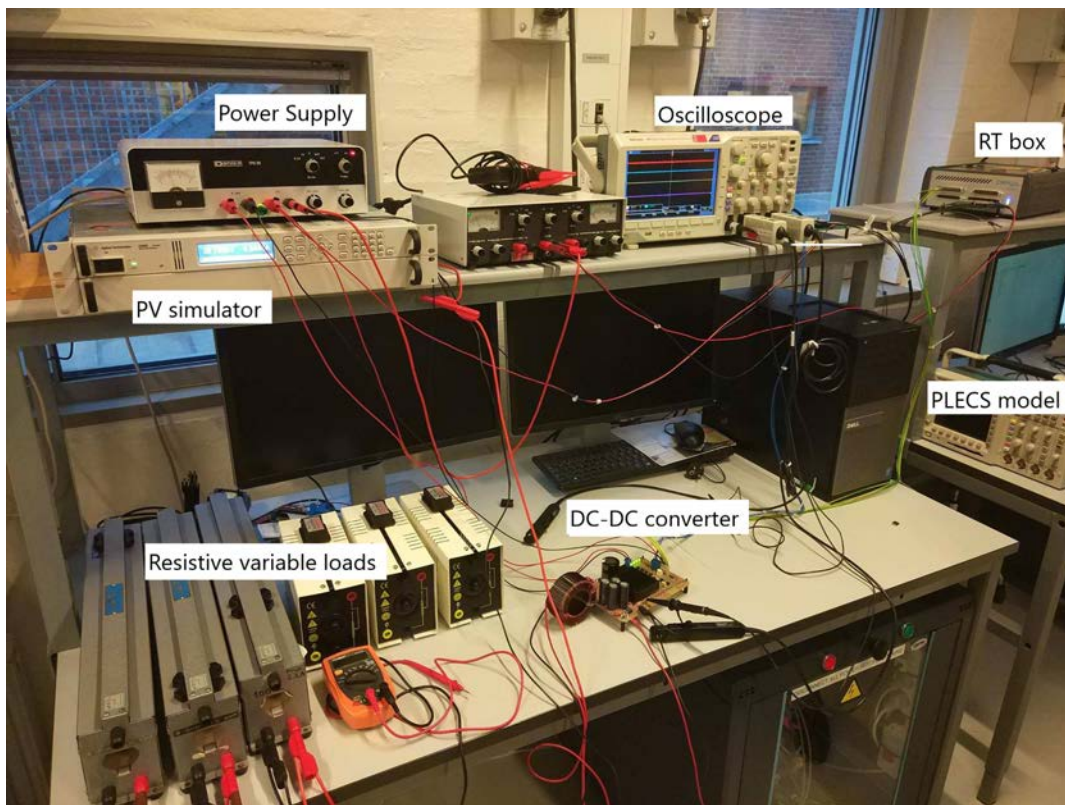


Figure B.1: Test setup for full system test.

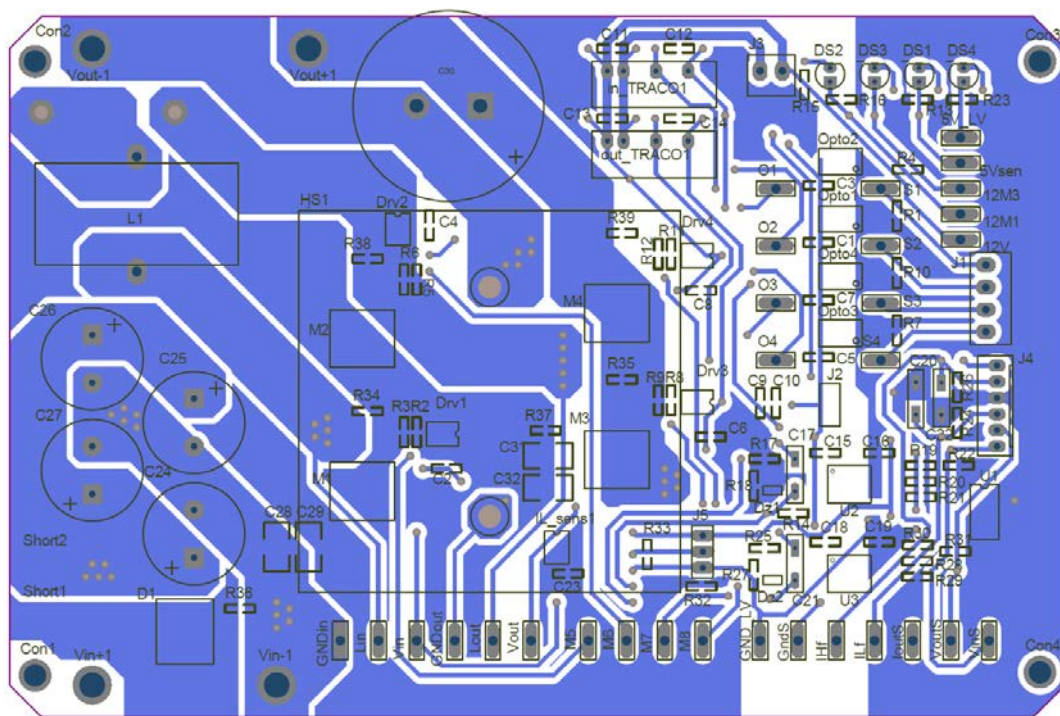
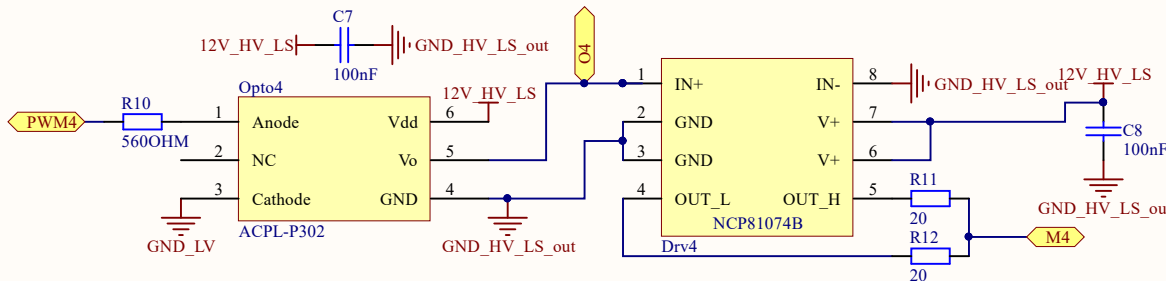
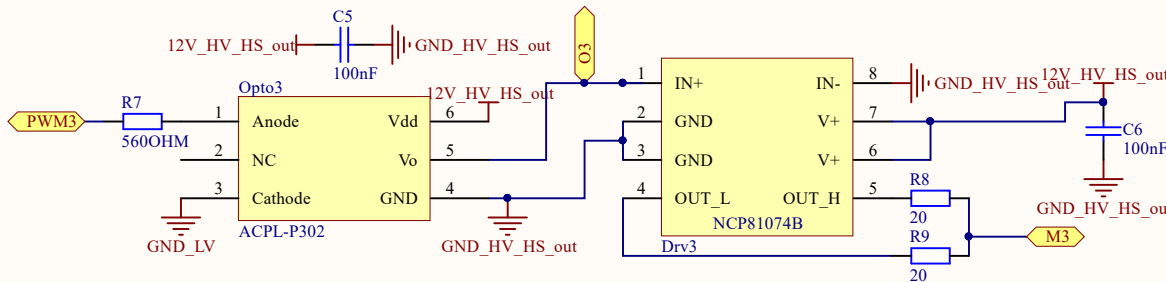
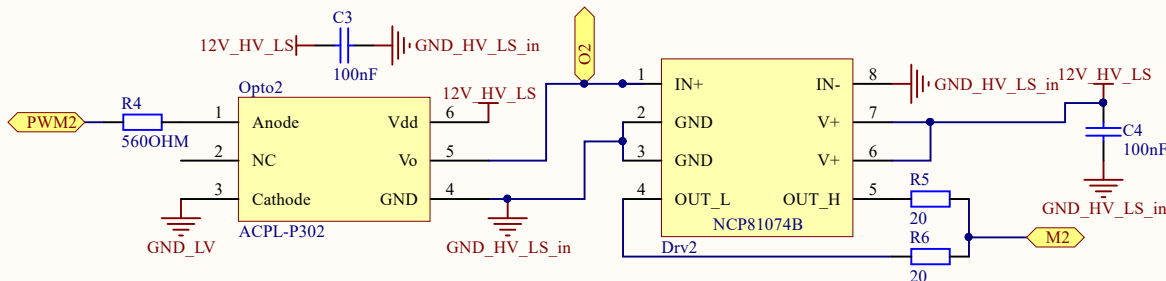
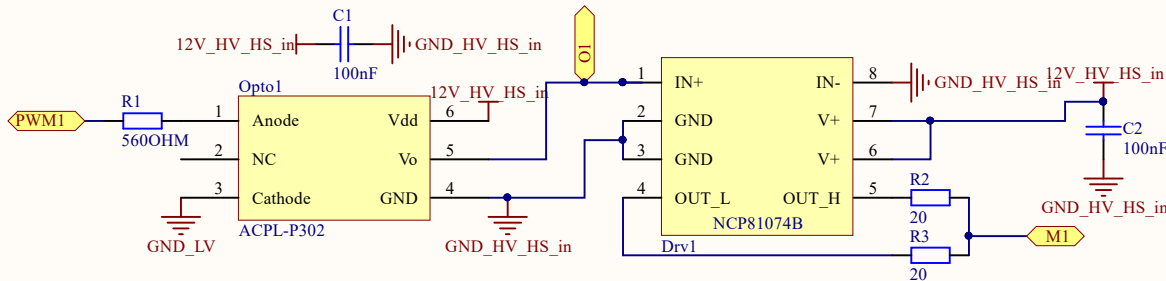
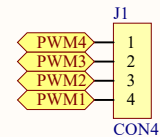


Figure C.2: PCB bottom layer.

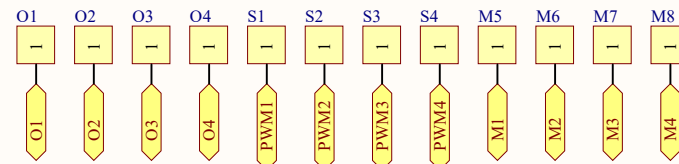
DRIVER CIRCUIT



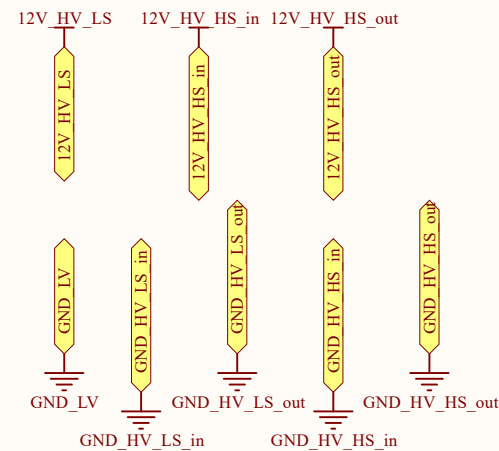
From RT Box



Test Points



Global Connections

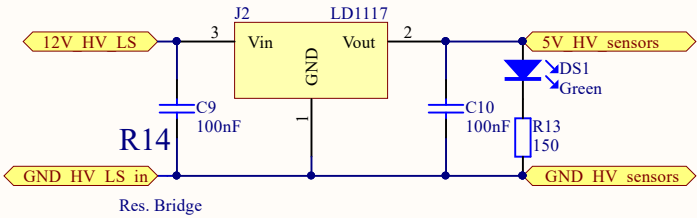


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File: C:\Users\j\Drivers_V2\SchDoc	Drawn By: nsn-760	

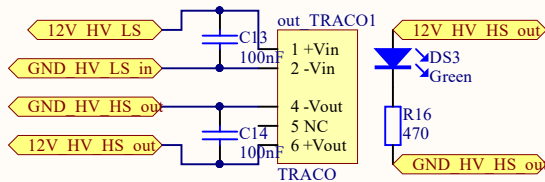
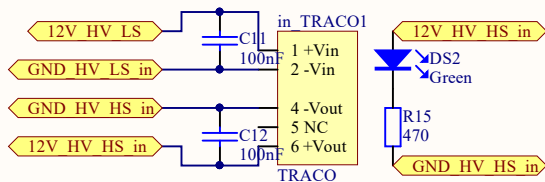
Input Voltage



Sensors 5V signal

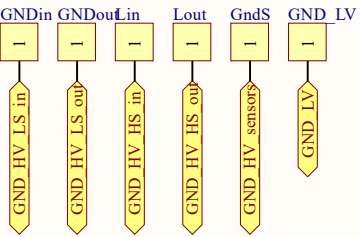


Traco Power

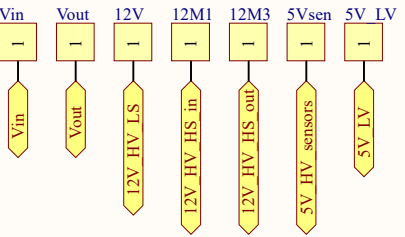


Test Points

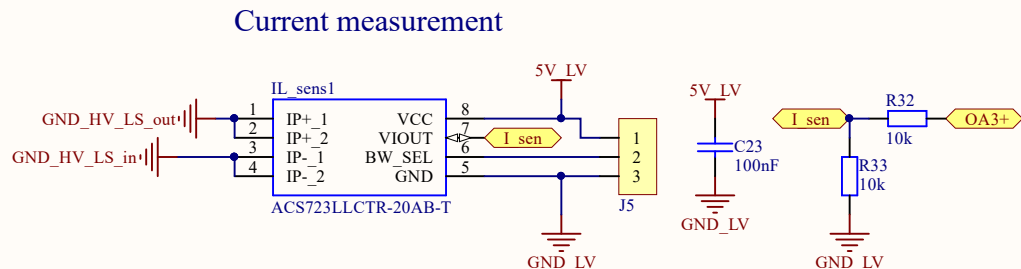
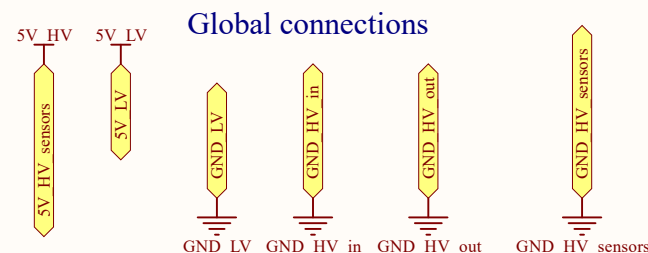
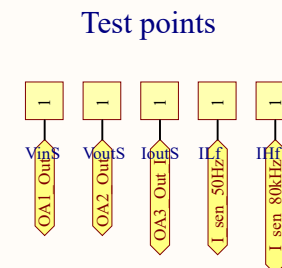
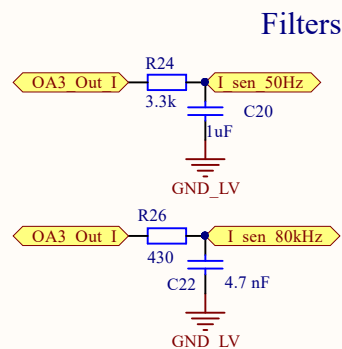
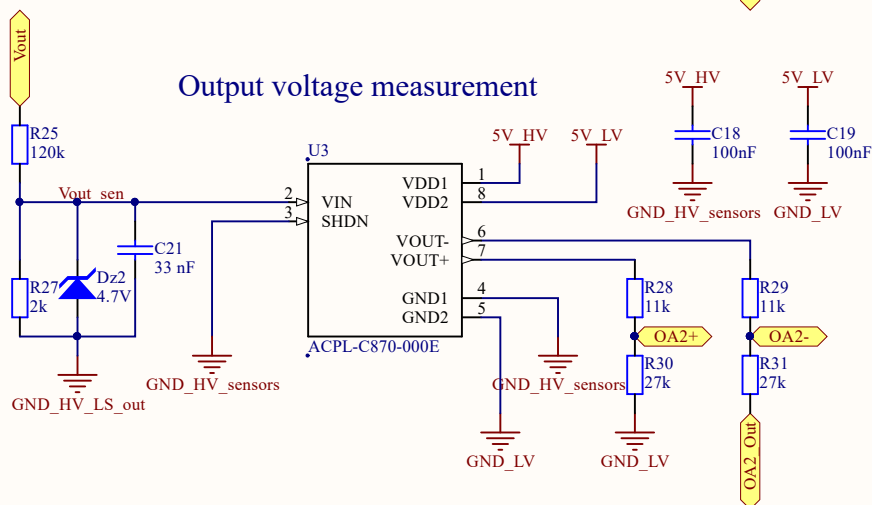
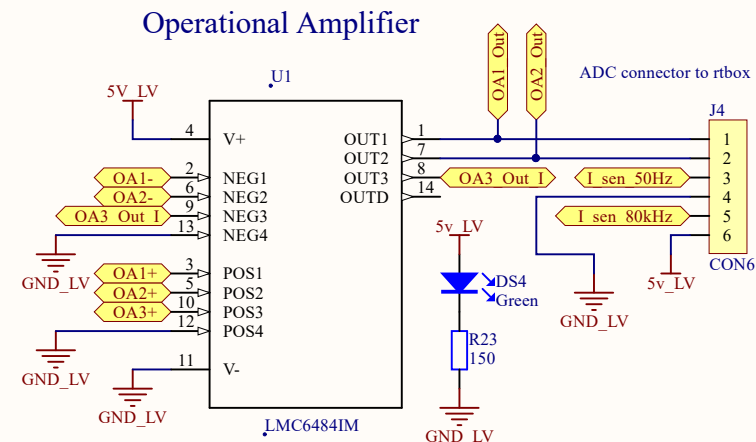
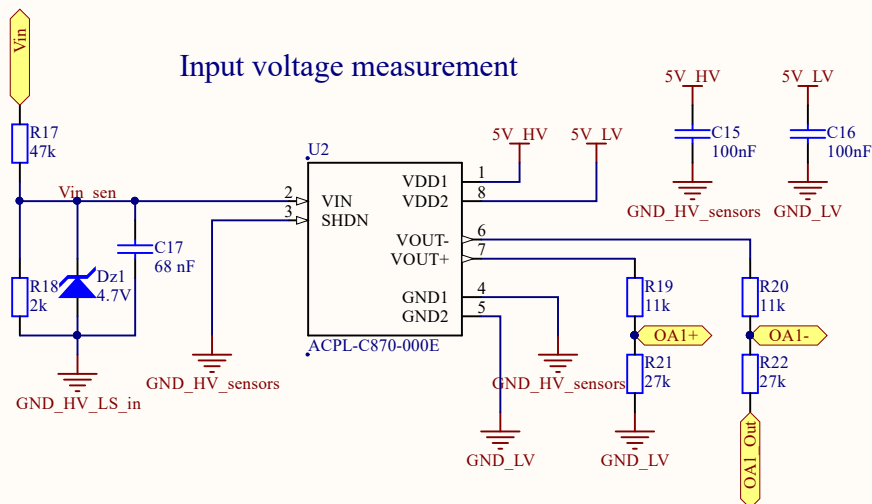
Grounds



Voltages

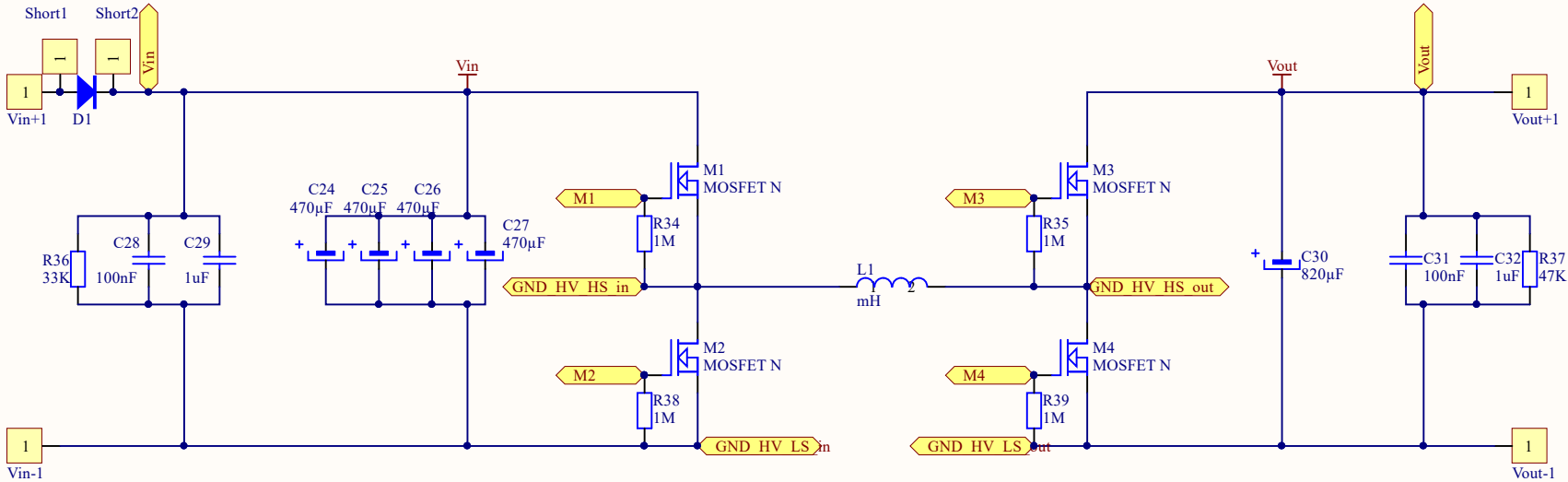


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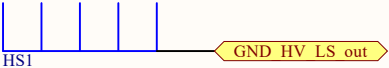


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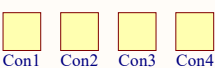
Main Topology



Heatsink



Support holes



Title		
Power switches and passive components		
Size	Number	Revision
A4		
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