

Digital Control Design and Implementation of a DSP Based High-Frequency DC-DC Switching Power Converter

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Abstract

This paper presents a DSP based digital control design and implementation of a high frequency dc-dc switching power supply. Starting with a dc-dc buck converter and a given set of performance specifications, different control blocks and parameters, used as in the analog control design approach, are reviewed prior to the control design in digital domain. The control loop is then analyzed and the digital controllers are designed using different control design approaches. MATLAB based digital control design approaches presented here are finally validated with multiple test results from a prototype converter.

1. Introduction

Digital control of switching power supplies is becoming more and more common in industry today because of the availability of low cost, high performance DSP controller with enhanced and integrated power electronic peripherals such as analog-to-digital (A/D) converters and pulse width modulator (PWM).

DSP based digital control allows for the implementation of more functional control schemes, standard control hardware design for multiple platforms and flexibility of quick design modifications to meet specific customer needs. Digital controllers are less susceptible to aging and environmental variations and have better noise immunity. Modern 32-bit DSP controllers with processor speed up to 150MHz and enhanced peripherals such as, 12-bit A/D converter with conversion speed up to 80nSec, 32x32-bit multiplier, 32-bit timers and real-time code debugging capability gives the power supply designers all the benefits of digital control and allows implementation of high bandwidth, high frequency power supplies without sacrificing performance [1-4]. The extra computing power of such processors also allows implementation of sophisticated nonlinear control algorithms, integrate multiple converter control into the same processor and optimize the total system cost. However, the power supply engineers, mostly familiar with analog control design, are faced with new challenges as they start to adopt these new digital control techniques in their designs.

Since DSPs just started to gain some serious considerations in controlling power supplies, many pertinent factors in the design and implementation of a digital control loop need to be addressed. Re-identification of the control blocks and the associated control parameters is essential for the analog designers in order to enable them to implement the DSP based digital control techniques using the well-known analog control design approaches. This paper, therefore, describes a step-by-step DSP based digital control design and implementation of a high frequency dc-dc converter. Starting with a dc-dc buck converter and a given set of performance specification, it discusses different control design approaches and highlights the significant differences in designing control in the digital domain compared to the analog approach. Two approaches to the control design are illustrated namely, the design by emulation and the direct digital design. These are first shown in MATLAB and then verified by experimental results. In this process the effects of sampling delay and the computation delay are also analyzed in MATLAB and then verified experimentally.

2. Digital Control Implementation for DC-DC Converter

Figure 1 shows a simplified block diagram of a digitally controlled dc-dc converter interfaced to a TMS320F2812 DSP controller. This is a 32-bit, 150MHz DSP from Texas Instruments.

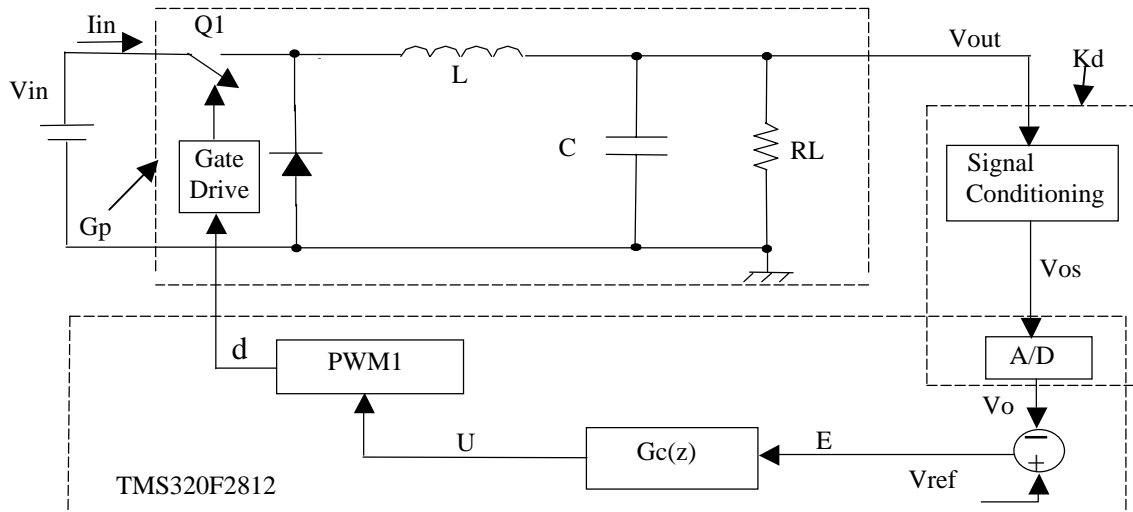


Figure 1. DSP based Digital Control of DC-DC Converter

As indicated in Figure 1, a single signal measurement is needed to implement the voltage mode control of the dc-dc converter. The instantaneous output voltage V_{out} is sensed and conditioned by the voltage sense circuit and then input to the DSP via the ADC channel. The digitized sensed output voltage V_o is compared to the reference V_{ref} . The voltage loop controller G_c is designed to make the output voltage V_{out} track the reference V_{ref} and at the same time achieve the desired dynamic performance. The digitized output U of this controller provides the duty ratio command for the buck regulator switch Q_1 . This command output is used to calculate the appropriate values for the timer compare registers in the on-chip PWM module. The PWM module uses this value to generate the PWM output, PWM1 in this case, that finally drives the buck converter switch Q_1 .

2.1. Digital Sampling Loop Implementation

Figure 2 shows one example of a digital sampling scheme using the DSP on-chip peripherals. The sampling scheme affects the digital controller design and, therefore, needs appropriate attention. PWM output frequency is set up by configuring one of the on-chip Timers, T1 in this case. In this example, T1 generates a dual edge modulated (symmetric), 250 kHz PWM output. These timers have associated compare registers which are used to write the calculated duty ratio values. These values then get compared with the timer counter value in order to generate the PWM output. The time at which a newly written compare value affects the actual PWM output duty ratio is controlled by associated PWM control registers. In this example, the PWM control registers are set up such that a new value written in the compare register, changes the actual PWM output duty ratio at the start of the subsequent timer (T1) period. Also, the ADC control registers are set up such that the AD conversion is triggered at the middle of the ON pulse of the PWM output. As soon as the conversion is complete, the ADC module is set up to

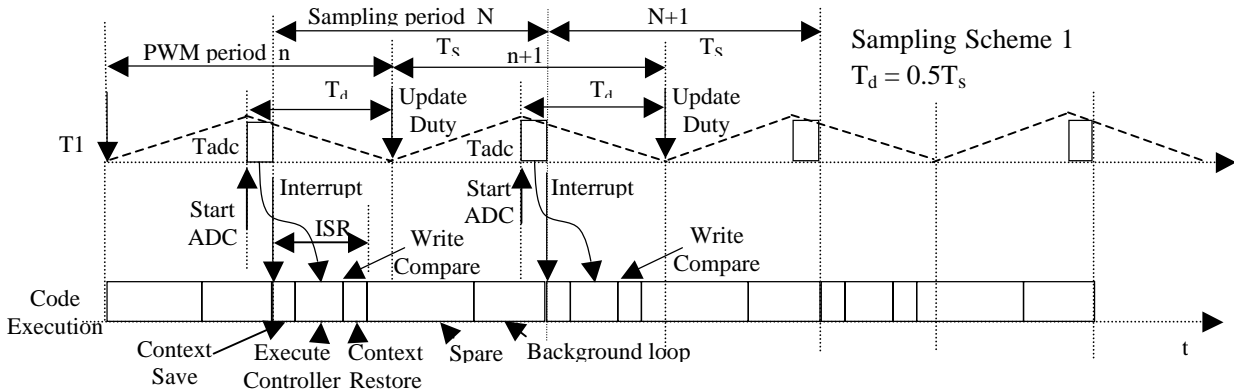


Figure 2 DC-DC Converter Digital Control Loop Sampling Scheme

generate an interrupt. The time delay between the start of AD conversion and this interrupt is shown in Figure 2, as T_{adc} . This time includes the AD conversion time and the processor interrupt latency. Inside the interrupt service routine (ISR), the user software reads the converted value from the ADC result register, implements the controller and then writes the new PWM duty ratio value to the appropriate PWM compare register. However, this new duty ratio value takes affect at the start of the subsequent PWM cycle. From Figure 2, it is clear that the time delay T_d , between the ADC sampling instant and the PWM duty ratio update, is half the PWM period. In this case, the PWM period and the sampling period (T_s) are equal and so the computation delay is, $T_d = T_s/2$. Also shown in Figure 2, the calculation of a new duty ratio value inside the ISR is completed well before a subsequent interrupt is generated. This means that, at this sampling frequency, the processor bandwidth (150 MHz) allows for sufficient spare time for extending the ISR by executing multiple controllers or other time critical tasks. Some of this spare time can also be used for non-time critical tasks by running them from a background loop.

2.2. DC-DC Controller Design

The system parameters used in this design are:

- $V_{in} = 4\sim 6V$, $V_{out} = 1.6V$, Max output current $I_{out} = 16A$
- Maximum output voltage (used for ADC signal scaling) $V_{omax} = 2V$
- PWM frequency $f_{pwm} = 250kHz$; Voltage loop sampling frequency $f_s = 250kHz$
- Output filter components, $L = 1.0\mu H$, $C = 1620\mu F$, $ESR = 4.0\text{ m}\Omega$
- Desired voltage loop bandwidth $f_{cv} = 20kHz$
- Phase Margin = 45 deg, Settling time < 75 μ Sec

In order to design the digital controller, two approaches are discussed. These are, 1. Design by Emulation and 2. Direct Digital Design.

2.2.1 Design by Emulation

This is also known as Digital Redesign Approach. In this method, an analog controller is first designed in the continuous domain as if one were building continuous time control system, by ignoring the effects of sampling and hold associated with the AD converter and the digital PWM circuits. The analog controller is then converted to a discrete-time compensator by some approximate techniques. Figure 3 represents a simplified block diagram of the system in Figure 1. It shows all the different components of this closed loop control system in s-domain.

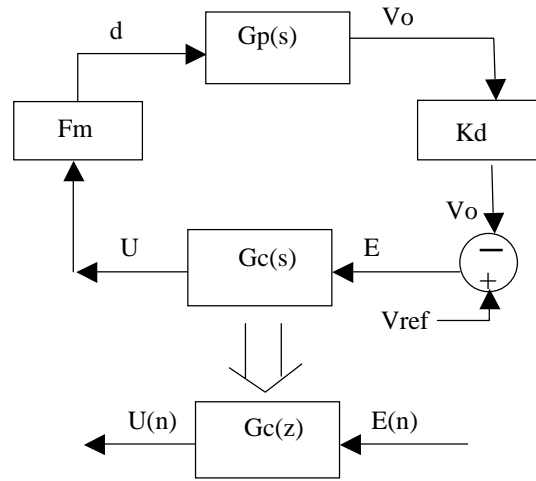


Figure 3 DC-DC Converter Control Loop Block Diagram in s-domain

The small signal power stage model of the buck converter in s-domain is indicated as $G_p(s)$. For the given system parameters, this is derived as,

$$G_p(s) = (3.24 \times 10^{-5} s + 5.0) / (1.685 \times 10^{-9} s^2 + 1.648 \times 10^{-5} s + 1.0)$$

If the maximum output voltage is V_{omax} , then the voltage feedback factor is, $K_d = 1/V_{omax}$, provided that the digital output voltage V_o is represented in Q31 fixed-point format for this 32-bit DSP controller [6]. The PWM modulator gain is $F_m = 1$. This is so because the user software together with the on-chip PWM

hardware can be configured such that as the controller output U (in Q31) varies between 0 ~ 7FFFFFFFh, the PWM output duty ratio d varies between 0 ~ 1, [6].

Now for this plant $G_p(s)$, a suitable analog controller $G_c(s)$ is designed in MATLAB using the available control design tool. This is shown in Figure 4 where the system bandwidth (BW) is 25 kHz and the phase margin (PM) is 71 deg.

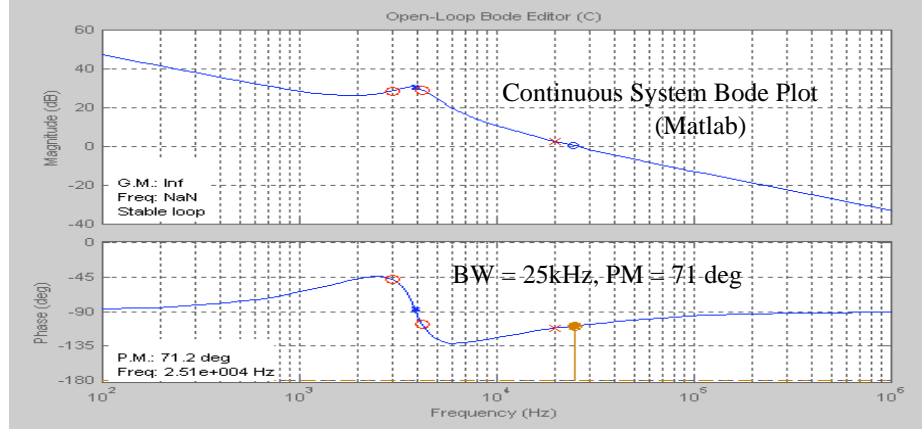


Figure 4 DC-DC Converter Control Loop Bode Plot $G_p(s)*G_{c1}(s)*K_d*F_m$ (MATLAB)

The corresponding controller $G_{c1}(s)$ is derived as,

$$G_{c1}(s) = (14.3s^2 + 6.514 \times 10^5 s + 7.2 \times 10^9) / s(s + 1.256 \times 10^5)$$

This analog controller $G_{c1}(s)$ can be discretized by any of the commonly used discretization methods. Specifying a method such as 'Pole-Zero Match' in MATLAB yields the following digital controller $G_{c1}(z)$:

$$G_{c1}(z) = \frac{U}{E} = \frac{12.34 - 22.53z^{-1} + 10.28z^{-2}}{1 - 1.605z^{-1} + 0.6051z^{-2}}$$

$$\Rightarrow U(n) = 1.605U(n-1) - 0.6051U(n-2) + 12.34E(n) - 22.53E(n-1) + 10.28E(n-2)$$

Where, the sampling time is $T_s = 1/f_s = 4\mu\text{Sec}$. This controller was implemented using DSP instruction set and the dynamic performance of the closed loop converter was tested. This is shown in Figure 5:

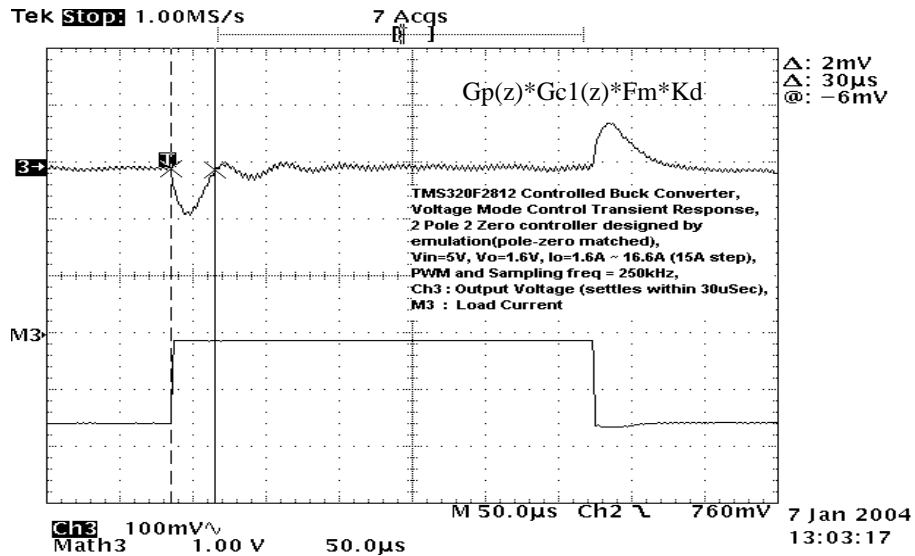


Figure 5 DC-DC Converter Load Transient Response (loop gain = $G_p*G_{c1}*F_m*K_d$)

For a step load change of 15A, the output voltage settles within 30uSec (1% band). The converter has a satisfactory time response. However, the damping of the transient response does not reflect a phase margin of 71 deg as shown in MATLAB Bode plot (Figure 4). This difference in the designed and actual phase margin is because of the fact that we completely ignored the effect of sampling and hold and the computation delay. In digital control design the effect of these delays can be taken into account prior to the control design that results in a more predictable and accurate dynamic performance. This is illustrated next.

2.2.2 Direct Digital Design

Figure 1 is now redrawn as in Figure 6 to show all the different components of this closed loop control system including the effect of sampling and hold.

The sampling process by the on-chip ADC is represented by an ideal sampler with time period T_s . ADC can be represented this way as compared to the model given in [7], since the ADC gain is taken into account in the block labeled K_d and ADC conversion time is included in the computation delay block labeled H_c . The on-chip PWM module acts as a hold device. Representing this as a zero-order-hold (ZOH), the ADC and the PWM module together form a sampling and hold device. The s-domain transfer function of such a device can be expressed as $[1 - \exp(-s \cdot T_s)]/s$. The computation delay block H_c , models the time delay between the ADC sampling instant and the subsequent duty ratio update. If this time delay is denoted by T_d then the transfer function for H_c is, $H_c = \exp(-s \cdot T_d)$. Now, the continuous time power stage model is first discretized with ZOH and the sampler.

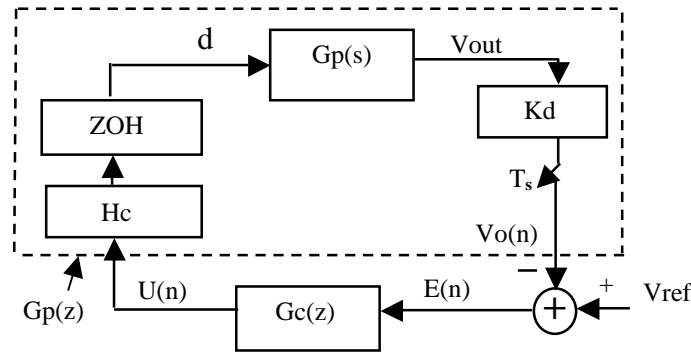


Figure 6 DC-DC Converter Digital Control Loop Block Diagram

Once this is available, the discrete-time compensator, i.e., a digital controller $G_c(z)$ is designed directly in the z-domain using methods similar to the continuous-time frequency response methods. This has the advantage that the poles and zeros of the digital controllers are located directly, resulting in a better load transient response, as well as better phase margin and bandwidth for the closed loop operation of the power converter. The discrete-time transfer function $G_p(z)$ of the converter plant, including the ZOH, the sampler, the voltage sensing gain and the computation delay model H_c is [8],

$$G_p(z) = Z\left\{\frac{1}{s}(1 - e^{-sT_s}) \cdot H_c \cdot G_p(s) \cdot K_d\right\}$$

where, Z denotes the z-transform of the function inside the parenthesis $\{\}$. Using MATLAB, this can be computed as,

$$G_{p1}(z) = 0.0494(z - 0.5283)/(z^2 - 1.952z + 0.962)$$

Where $K_d = 1/V_{omax} = \underline{\quad}$, $T_s = 1/f_s = 4\mu\text{Sec}$ and the computation delay T_d , for now, is taken as $T_d = 0$, i.e., $H_c = 1$.

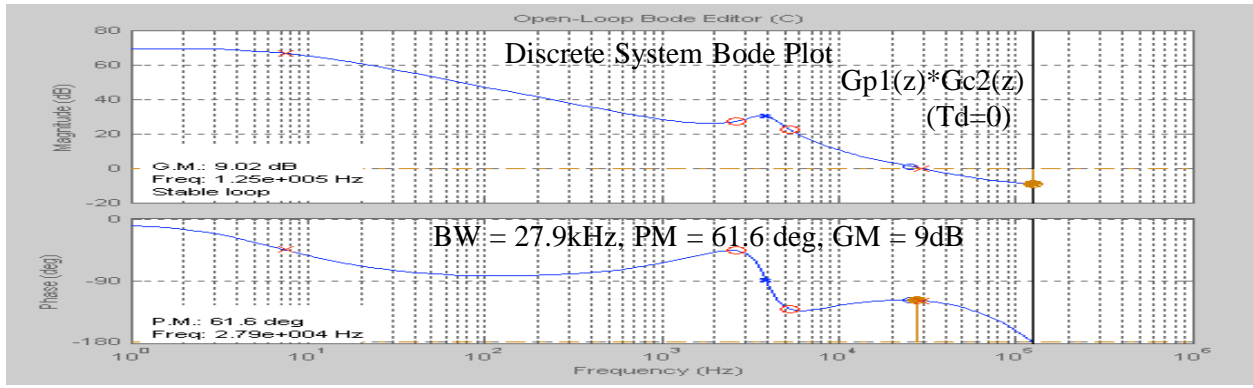


Figure 7 DC-DC Converter Digital Control Loop Bode Plot $G_{p1} * G_{c2}$ (MATLAB)

For this plant G_{p1} , a suitable digital controller is designed in MATLAB. The system bandwidth is set at 27.9 kHz with a phase margin of 61.6 deg. The Bode plot is shown in Figure 7. The corresponding controller G_{c2} is derived from MATLAB as,

$$G_{c2}(z) = \frac{U}{E} = \frac{14.87 - 26.91z^{-1} + 12.16z^{-2}}{1 - 1.473z^{-1} + 0.473z^{-2}}$$

$$\Rightarrow U(n) = 1.473U(n-1) - 0.4731U(n-2) + 14.87E(n) - 26.91E(n-1) + 12.16E(n-2)$$

Case 1 : Computation Delay $T_d = 0.5T_s$

For the controller just designed we assumed $T_d = 0$, which is not the case if we implement this controller using the sampling scheme shown in Figure 2. So, we recalculate $G_p(z)$ for $T = 0.5T_s$ to include the effect of the sampling scheme shown in Figure 2. The modified plant model is,

$$G_{p2}(z) = (0.022z^2 + 0.017z - 0.158) / z(z^2 - 1.952z + 0.962)$$

The corresponding Bode plot for this plant $G_{p2}(z)$ with the controller $G_{c2}(z)$ is shown in Figure 8.

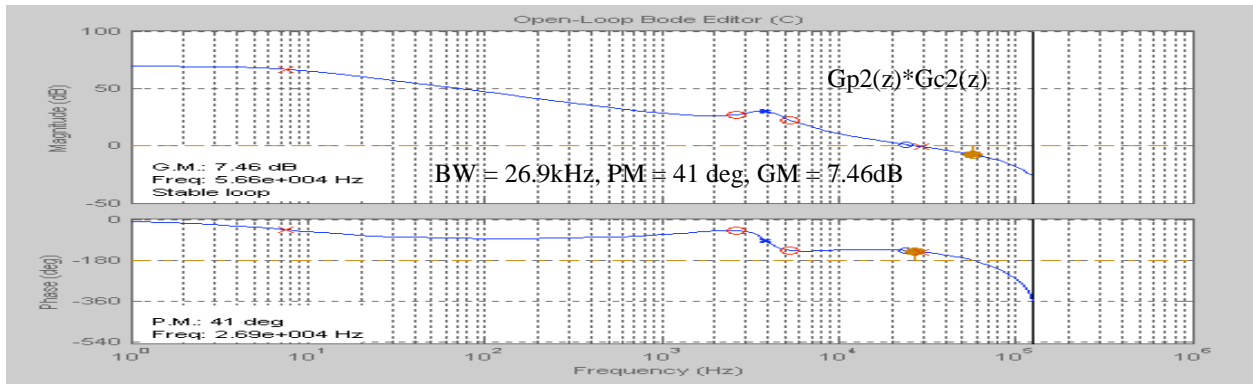


Figure 8 DC-DC Converter Digital Control Loop Bode Plot $G_{p2} * G_{c2}$ (MATLAB)

From the two plots of $G_{p1} * G_{c2}$ and $G_{p2} * G_{c2}$, it is clear that the same controller G_{c2} results in a reduced phase margin of 20.6 deg ($= 61.6 - 41.0$) for the latter system. This reduction in phase margin can be accounted for by the computation time delay of $T_d = 0.5T_s$ associated with G_{p2} . This time delay translates to a phase lag of,

$$\angle H_c = \omega T_d = (360f)(0.5T_s) \approx 20 \text{ deg}$$

where, $T_s = 4\mu s$, and $f \approx 27 \text{ kHz}$ is the frequency of interest at which the phase lag is calculated.

The actual system Bode plot for the digitally controlled dc-dc converter represented by the plant model $G_{p2}(z)$ and controlled by the controller $G_{c2}(z)$ is shown in Figure 9. Notice that the frequency domain performance parameters (bandwidth, phase margin and gain margin) agree quite well between the actual and the designed values. The time domain dynamic performance of the converter is shown in Figure 10. For a step load change of 15A, the output voltage settles within 28uSec (1% band). These test results on the frequency and time domain characteristics of the digitally controlled converter show the validity of the MATLAB based design approach as illustrated by Figures 7 and 8 above.

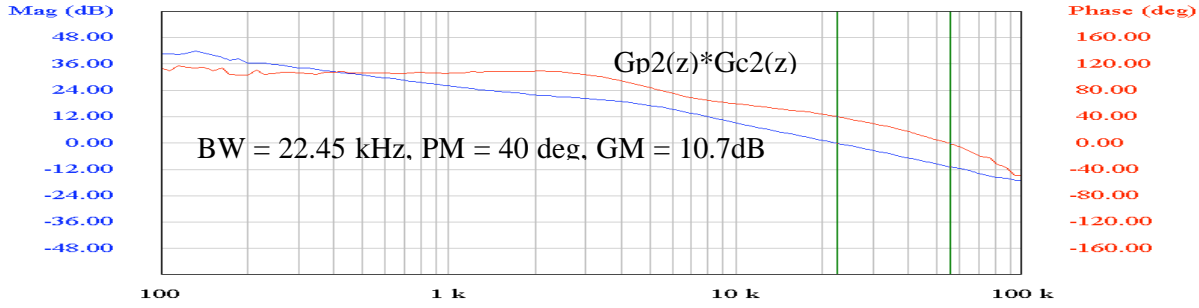


Figure 9 DC-DC Converter Control Loop Bode Plot $G_{p2}^*G_{c2}$ (Test result from prototype h/w)

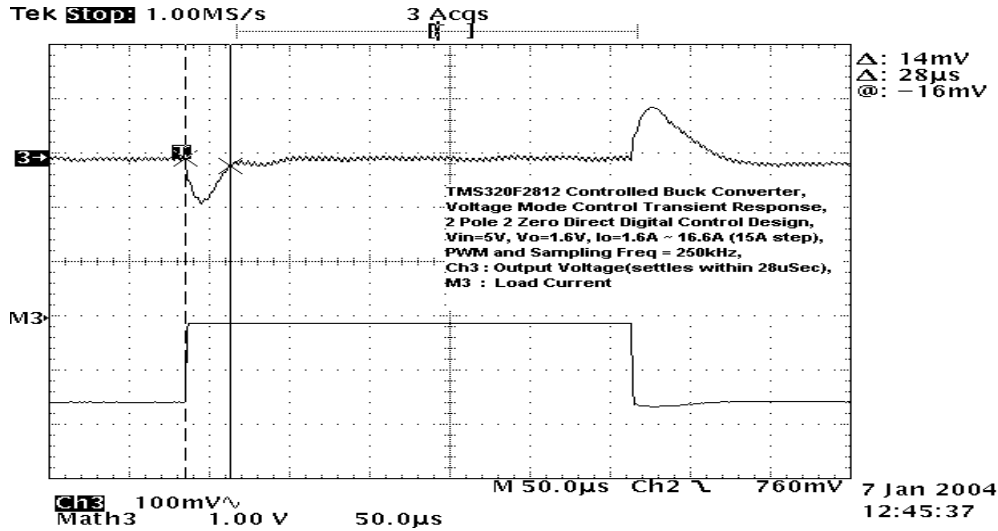


Figure 10 DC-DC Converter Load Transient Response (Loop gain = $G_{p2}^*G_{c2}$)

Case 2 : Computation Delay $T_d = 2.0T_s$

The sampling scheme shown Figure 2 can be modified to investigate the effect of a more severe computation delay of $T_d = 2.0T_s$. This is easily done in software by changing the interrupt scheme and the way the actual PWM duty ratio is updated following a new AD conversion of the output voltage. Once this is done in software, the new plant model G_{p3} , for $T_d = 2T_s$, is computed using MATLAB as,

$$G_{p3}(z) = (0.022z^2 + 0.017z - 0.159) / z^2(z^2 - 1.954z + 0.963)$$

The corresponding Bode plot for this plant $G_{p3}(z)$ with the controller $G_{c2}(z)$ is shown in Figure 11.

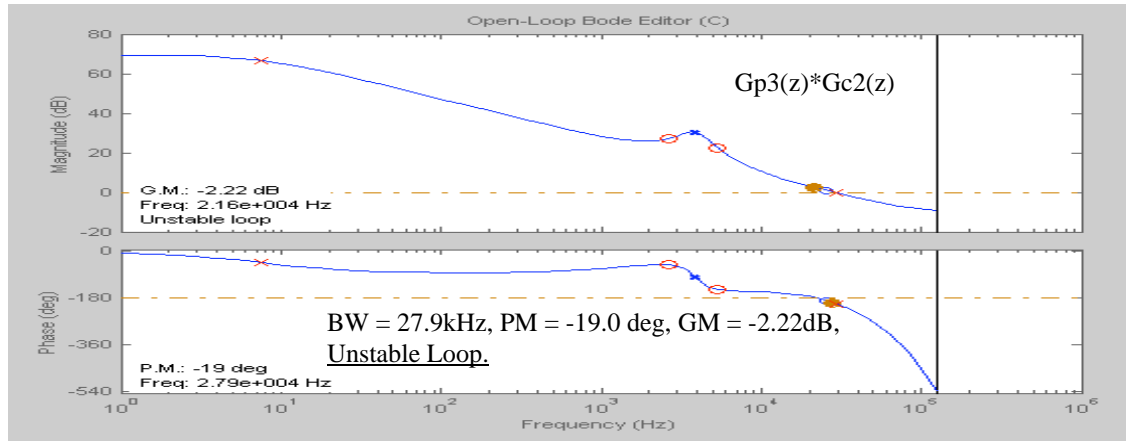


Figure 11 DC-DC Converter Digital Control Loop Bode Plot Gp3*Gc2 (MATLAB)

From the plot of Figure 11 it is clear that this system is completely unstable when controlled by the controller Gc2. From the plots of Gp1*Gc2 and Gp3*Gc2 we note that the controller Gc2 results in a reduced phase margin of 80.6 deg [= 61.6-(-19.0)] for the latter system. This reduction in phase margin is again accounted for by the computation time delay of $T_d = 2.0T_s$ associated with Gp3. This time delay translates to a phase lag of,

$$\angle H_C = \omega T_d = (360 f)(2.0T_s) \approx 80 \text{ deg}$$

where, $T_s = 4\mu s$, and $f \approx 27\text{kHz}$ is the frequency of interest at which the phase lag is calculated. In order to find a stable controller for Gp3, we note that this plant has 4-poles and 2 zeros and, therefore, the 2-pole 2-zero controller Gc2 cannot stabilize the system. So, using MATLAB a new 3-pole 3-zero controller Gc3 is designed as,

$$G_{C3}(z) = \frac{U}{E} = \frac{14.4 - 31.1z^{-1} + 20.1z^{-2} - 3.376z^{-3}}{1 - 1.235z^{-1} + 0.2362z^{-2} - 0.00115z^{-3}}$$

$$\Rightarrow U(n) = 1.235U(n-1) - 0.2362U(n-2) + 0.00115U(n-3) + 14.4E(n) - 31.1E(n-1) + 20.1E(n-2) - 3.376E(n-3)$$

The corresponding Bode plot for this plant Gp3(z) with the new controller Gc3(z) is shown in Figure 12.

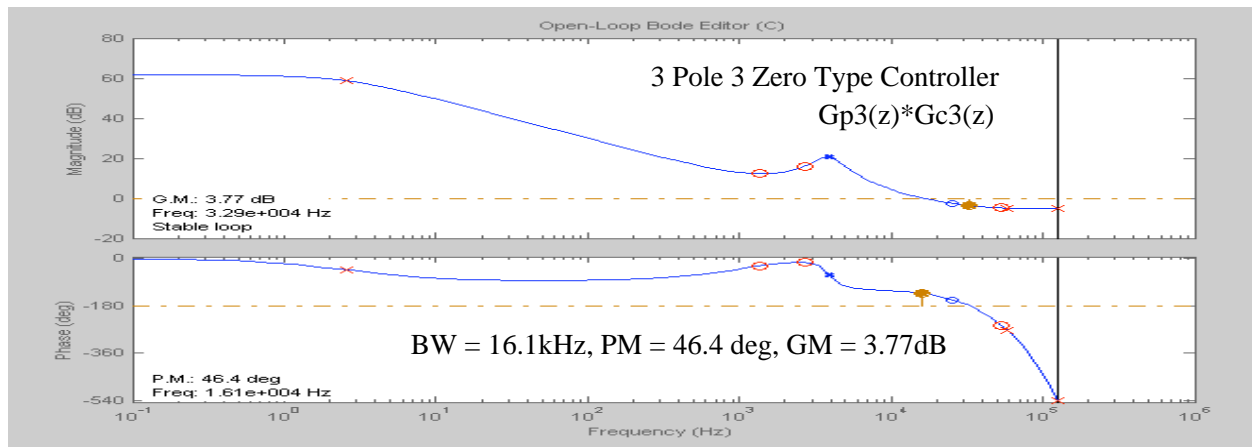


Figure 12 DC-DC Converter Digital Control Loop Bode Plot Gp3*Gc3 (MATLAB)

The actual system Bode plot for the dc-dc converter represented by this plant model $G_{p3}(z)$ and controlled by the redesigned controller $G_{c3}(z)$ is shown in Figure 13. It is again clear that the frequency domain characteristics match very closely between the actual and the designed values. Figure 14 shows the converter output voltage transient response with this controller. For a step load change of 15A, the output voltage settles within 50uSec (1% band). These test results on the frequency and time domain characteristics of the converter again show the validity of the MATLAB based design approach as depicted in Figures 11 and 12 above.

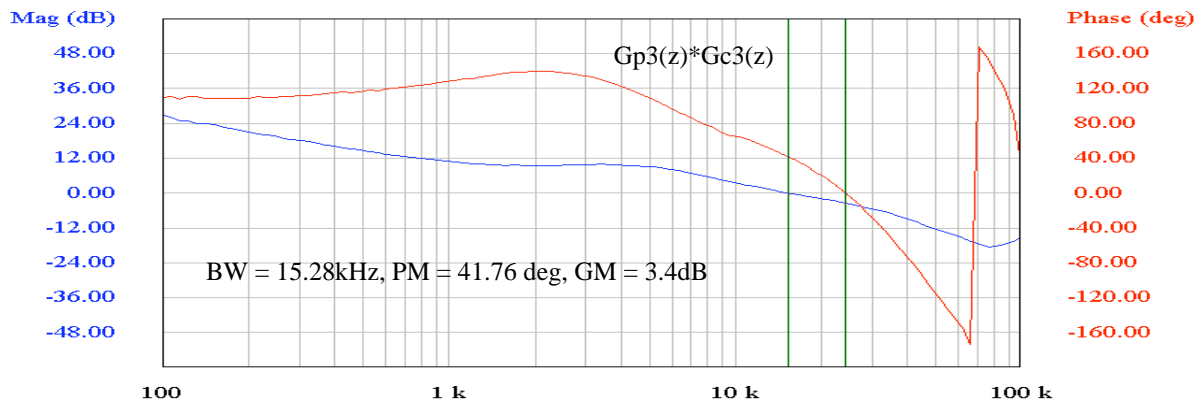


Figure 13. DC-DC Converter Control Loop Bode Plot $G_{p3} \cdot G_{c3}$ (Test result from prototype h/w)

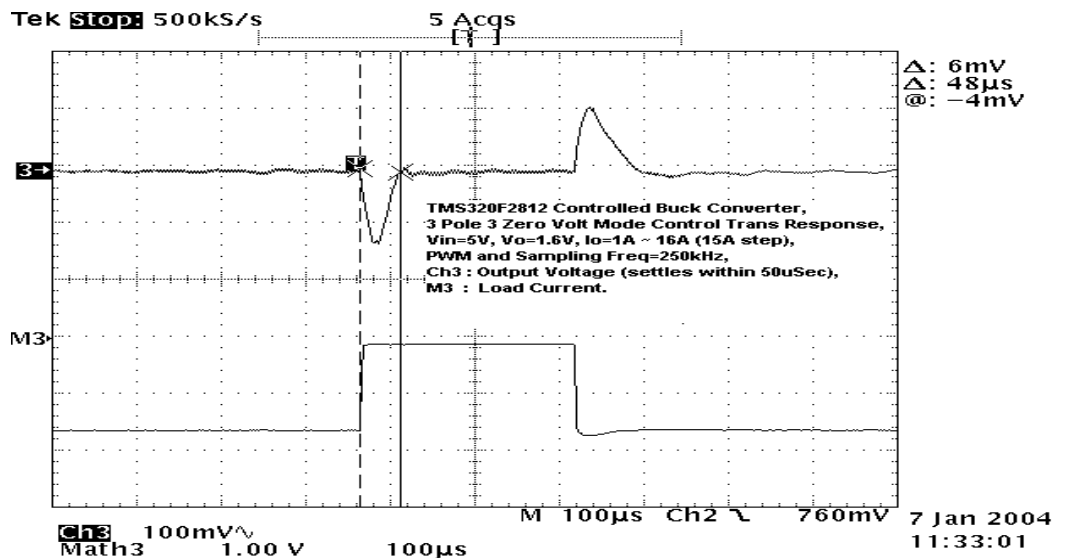


Figure 14. DC-DC Converter Load Transient Response (Loop gain = $G_{p3} \cdot G_{c3}$)

Conclusion

DSP based digital control design methods for high frequency dc-dc buck converter is investigated using MATLAB based control design tools. Starting with a buck converter interfaced to a DSP controller, different control blocks and associated parameters are identified prior to the digital controller design. Two approaches to the digital controller design are presented. The first method, namely design by emulation, allows the power supply designers to do the control design in the familiar s-domain and then convert it to a discrete/digital controller. The second approach known as direct digital design, illustrates digital controller design directly in z-domain. It was found that the later approach results in a better dynamic performance for the closed loop operation of the converter. All of these MATLAB based designed controllers were finally validated by experimental results.

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