EMI/EMC

Overview Questions

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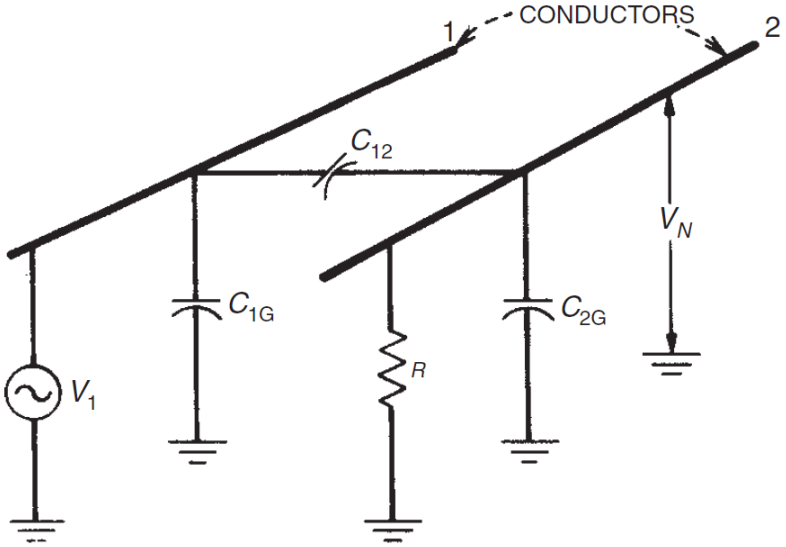
Q1. In following figure the stray capacitance between conductor 1 and 2 is 50 pF, each conductor has a capacitance to ground of 150pF, and conductor 1 has a 10V AC signal at a frequency of 100 kHz on it.

a) Draw the equivalent circuit diagram and calculate the noise voltage (V_N) picked up by the second conductor
b) Calculate V_N if the termination resistance R is:

b.1) 100 kΩ
b.2) 50 Ω



Assumption:
1- Shield thickness is much less than skin depth at the frequency of interest.
2- Cables are short compared with a wavelength.

Answer.

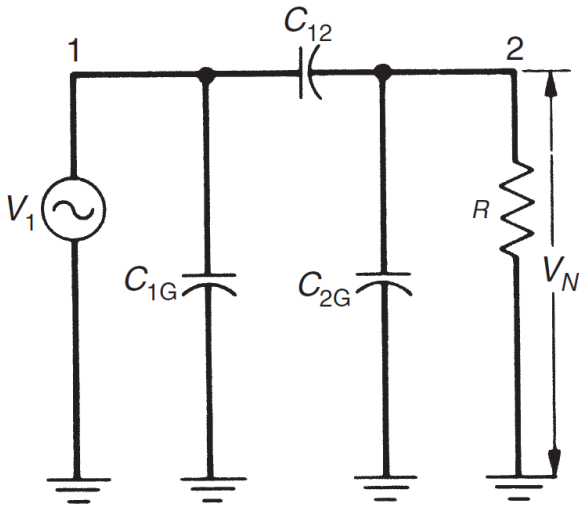
Condition 1

$$R \ll \frac{1}{j\omega(C_{12}+C_{2G})} \longrightarrow V_N = j\omega R C_{12} V_1$$

$$V_N = \frac{j\omega[C_{12}/(C_{12}+C_{2G})]}{j\omega + 1/R(C_{12}+C_{2G})} V_1$$

$$R \gg \frac{1}{j\omega(C_{12}+C_{2G})} \longrightarrow V_N = \left(\frac{C_{12}}{C_{12}+C_{2G}}\right) V_1$$

Condition 2



EQUIVALENT CIRCUIT

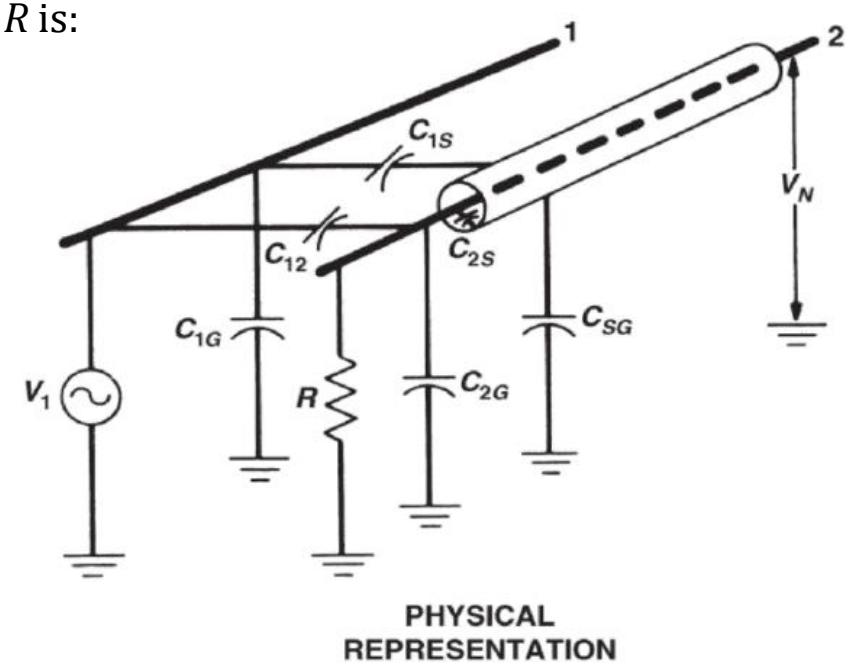
When R = 100 kΩ condition 2 is valid and by substituting the given C_{12} and C_{2G} values the picked up noise V_N = 2.5V

When R = 50 Ω condition 1 is valid and by substituting the given C_{12} and C_{2G} values the picked up noise V_N = 15.7 mV

Q2. A grounded shield is placed around conductor 2. The capacitance from conductor 2 to the shield is 100 pF (C_{2S}). The capacitance between conductor 2 and 1 is 2 pF (C_{12}), and the capacitance between conductor 2 and ground is 5 pF (C_{2G}). Conductor 1 has a 10V AC signal at a frequency of 100 kHz on it.

a) Draw the equivalent circuit diagram and calculate the noise voltage (V_N) picked up by the second conductor
b) Calculate V_N if the termination resistance R is:

b.1) Infinite resistance
b.2) 50 Ω



PHYSICAL REPRESENTATION

Assumption:
1- Shield thickness is much less than skin depth at the frequency of interest.
2- Cables are short compared with a wavelength.

Answer.

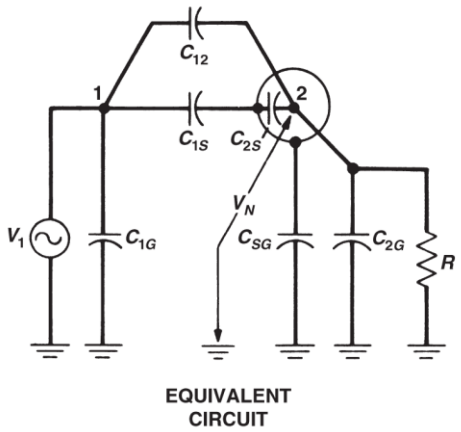
Condition 1

$$R \ll \frac{1}{j\omega(C_{12}+C_{2GT})} \longrightarrow V_N = j\omega R C_{12} V_1$$

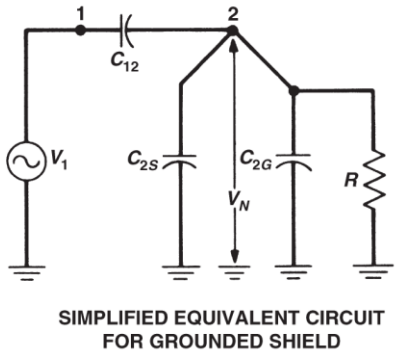
$$V_N = \frac{j\omega[C_{12}/(C_{12}+C_{2GT})]}{j\omega + 1/R(C_{12}+C_{2GT})} V_1 \qquad C_{2GT} = C_{2S} + C_{2G}$$

$$R \gg \frac{1}{j\omega(C_{12}+C_{2GT})} \longrightarrow V_N = \left(\frac{C_{12}}{C_{12}+C_{2GT}}\right) V_1$$

Condition 2



EQUIVALENT CIRCUIT



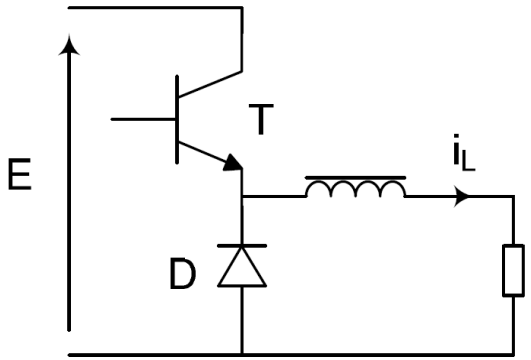
SIMPLIFIED EQUIVALENT CIRCUIT FOR GROUNDED SHIELD

When R is infinite condition 2 is valid and by substituting the given C_{12} and C_{2GT} values the picked up noise V_N = 187mV

When R = 50 Ω condition 1 is valid and by substituting the given C_{12} and C_{2GT} values the picked up noise V_N = 628 µV

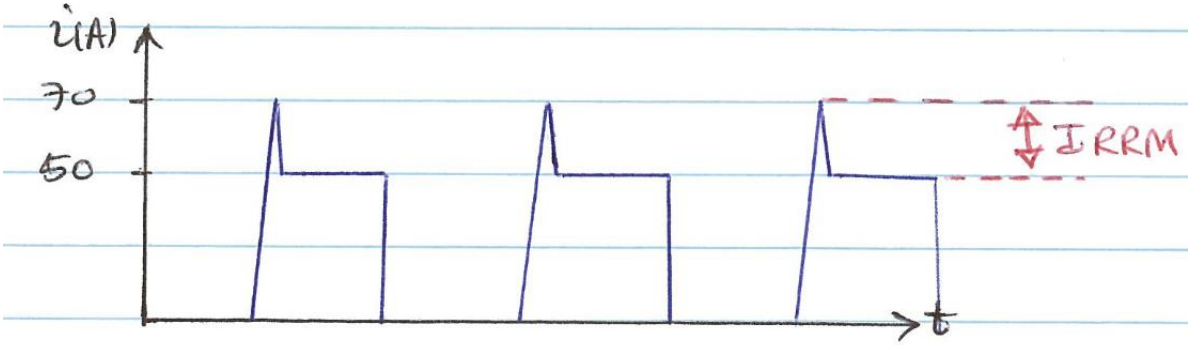
30 min

Q3A. The load current i_L in the following circuit is 50 A constant. The diode in the circuit has a maximum reverse recovery current of 20 A due to a wrong selection of its type. Sketch the waveform of the transistor current. What are the effects of this waveform on the transistor under CCM?



Q3B. The reverse recovery time of a diode is t_{rr} = 3 μs, the rate of fall of the current is 30 A/μs, assuming that $t_a = 2t_b$, determine the storage charge Q_{rr} and the peak reverse current I_{RRM}.

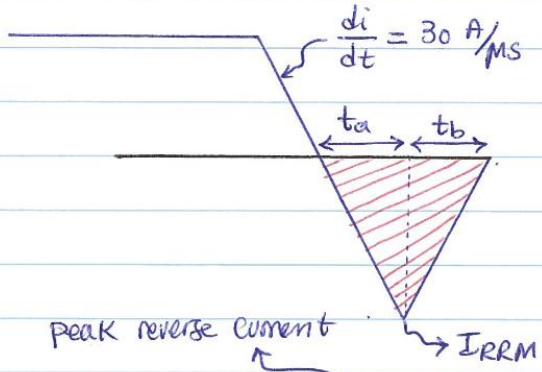
A1.



The current through the transistor is the addition of the load current and the reverse recovery current of the diode.
Transistor is subjected to a repetitive spike current of 20A at each switching cycle. This can cause substantially stress the device and can lead to permanent failure in a very short time. From EMI perspective, the higher the spike the more high frequency EMI issues.

A2.

Q_2 –



$t_{rr} = t_a + t_b = 3\mu s$

$2t_b + t_b = 3\mu s$

$\hookrightarrow t_b = 1\mu s$

$t_a = 2\mu s$

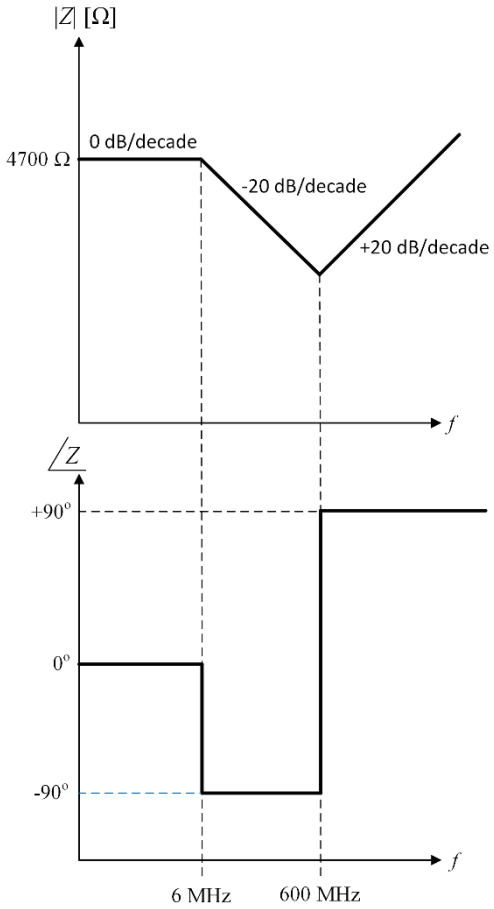
$\frac{I_{RRM}}{t_a} = 30\ \frac{A}{\mu s} \longrightarrow I_{RRM} = 30\ \frac{A}{\mu s} \times 2\mu s = 60A$

Storage charge $Q_{rr} = ?$ $\quad \frac{dQ}{dt} = i \rightarrow dQ = i\,dt =$ Area under the current waveform (negative portion)

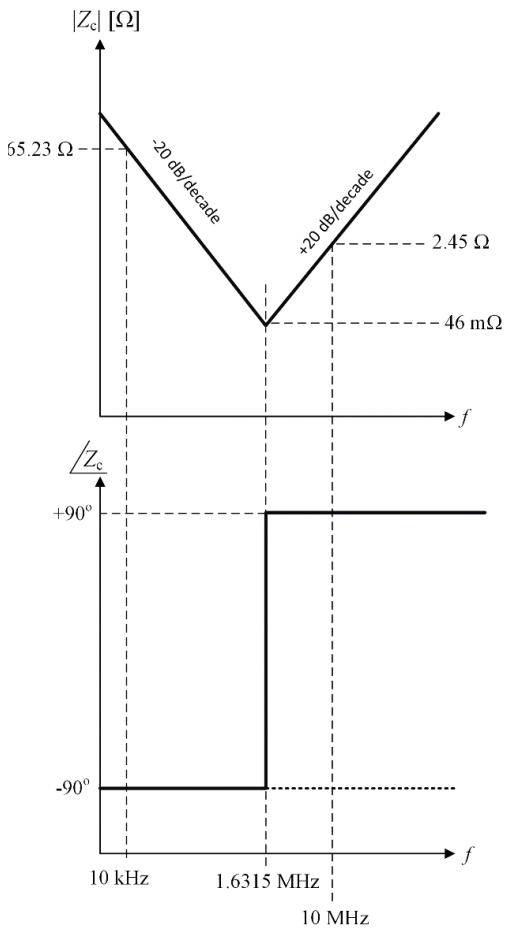
$Q_{rr} = \frac{1}{2} \times I_{RRM} \times t_{rr} = \frac{1}{2} \times 60 \times 3 \times 10^{-6} = 90\mu C$

Q4. Impedance and phase characteristics of two components are given as below.

a) Determine the components
b) Draw equivalent schematic of each component
c) Calculate the component along with its parasitic components values.



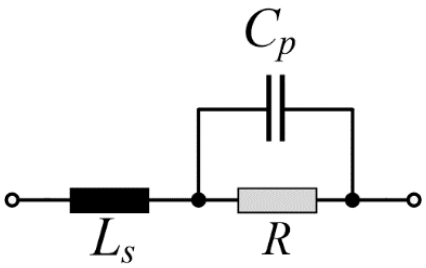
Component 1



Component 2

Component 1

Resistor



6 MHz = 1/(2*π*R*C_p) and R = 4700Ω

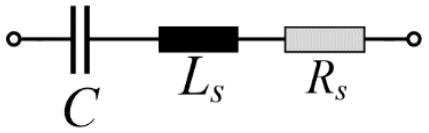
⇨ **C_p = 5.64 pF**

600 MHz = 1/(2*π*$\sqrt{L_s * Cp}$)

⇨ **L_s = 12.5 nH**

Component 2

Capacitor

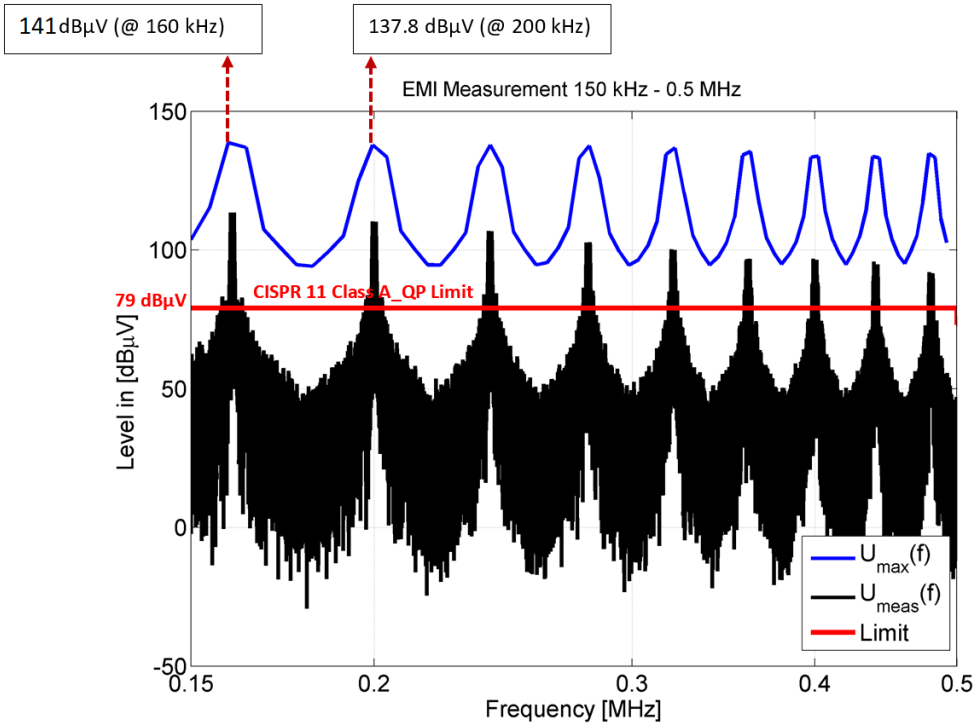


R_s = 46 mΩ based on the value at the resonant frequency of 1.6315 MHz

C = 244 nF calculated based on the 65.23 Ω at 10 kHz and L_s = 39 nH following the

$$f_r = \frac{1}{2\pi\sqrt{L_s C}}$$

Q5. The measured differential mode (DM) conducted emission (peak measurement) of a single-phase PFC circuit is shown as below. It is required to design a two stage differential mode EMI filter (without damping) in order to meet the standard limit CISPR 11_QP_Class A (red-line) which is at 79 dBµV.



a) How much is the required attenuation?

b) Draw a block diagram of the DM EMI filter.

c) Giving the fact that you have L_{DM} = 200 µH, based on the required attenuation how much should be your capacitance value (C_{DM}) using the following approximation for DM filter design?

$$Att_{EMI\_Filter}(f) = (2\pi f)^{2n_s} (L_{DM})^{n_s} C_{DM}{}^{n_s}$$

Answer

(a) Following the Lec 3, the required attenuation should be calculated based on the magnitude of first appearing peak above 150 kHz. Therefore, following the figure above the first peak is at 160 kHz with a magnitude of 141 dBμV. Therefore:

$$Att_{req}(f)[\mathrm{dB}] = U_{\max}(f)[\mathrm{dB}\,\mu\mathrm{V}] - \mathrm{CISPR}_{Limit}(f)[\mathrm{dB}\,\mu\mathrm{V}] + Margin[\mathrm{dB}]$$

Notice that beside the standard limit a margin (typically 6 dB) should be considered. This is due to the uncertainties in practice and also the tolerance of filter components.

$$Att_{req}(f)[\mathrm{dB}] = 141 - 79 + 6 = 68dB$$

Answer

(b) A block diagram of a two stage DM EMI filter for a single-phase PFC circuit is shown below:

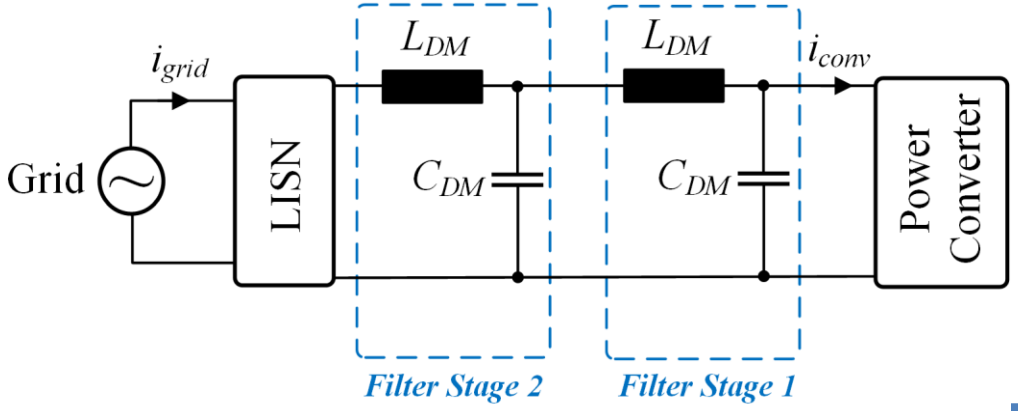


Fig. Block diagram of a two-stage DM filter for a single-phase PFC without damping stage.

Notably, the first filter component after converter is a capacitor. This is due to the fact that following impedance mismatch criteria (explained in Lec3) the first filtering component after a converter with current source behavior (PFC) should be a capacitor in order to provide a low impedance.

A current source has a high impedance.

Answer

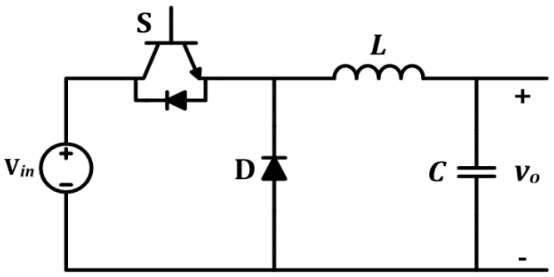
(c) Using the given approximation we have:

$$20log_{10}Att_{EMI\_filter} = Att_{req}(f) = 68\ dB$$

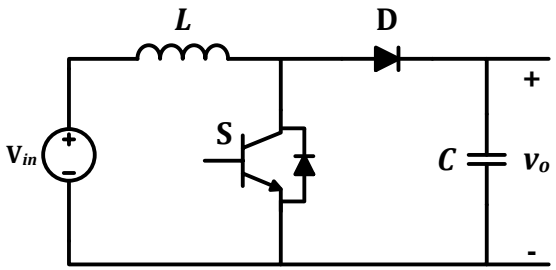
Therefore the required capacitance is C_{DM} = 250 nF.

Q6. Generated EMI emission from the power converters (shown in the figure below) operating in continuous conduction mode (CCM) need to be reduced.

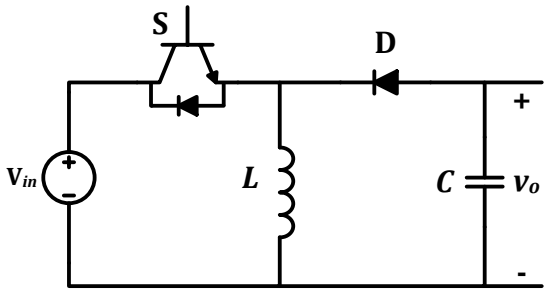
a) Determine the critical paths on all three converters.
b) What is the concern with the critical paths?
c) In the case of the first power converter name possible ways to minimize critical paths effects (name three)?



Converter 1



Converter 2



Converter 3

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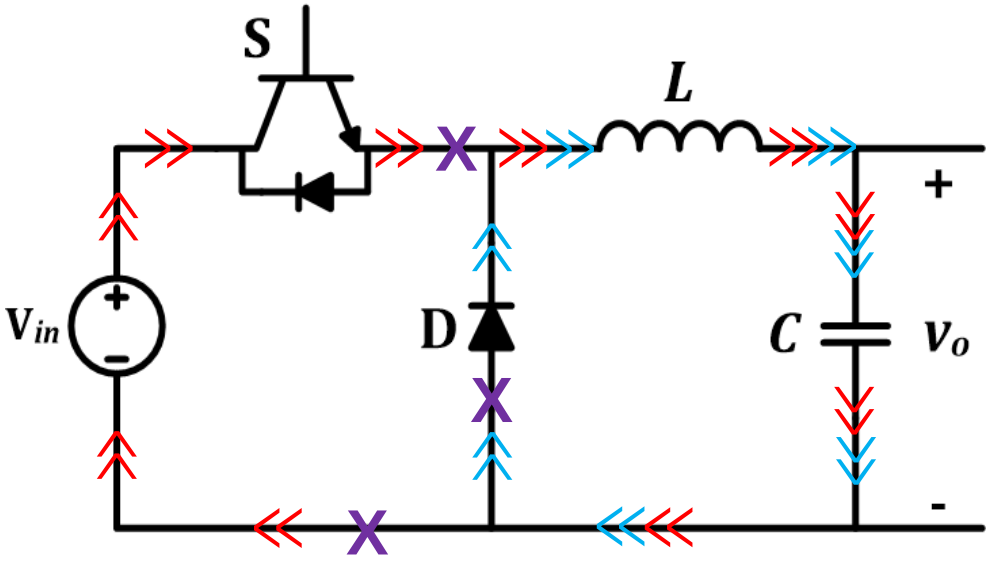
Answer

Critical Trace Sections



Buck Converter

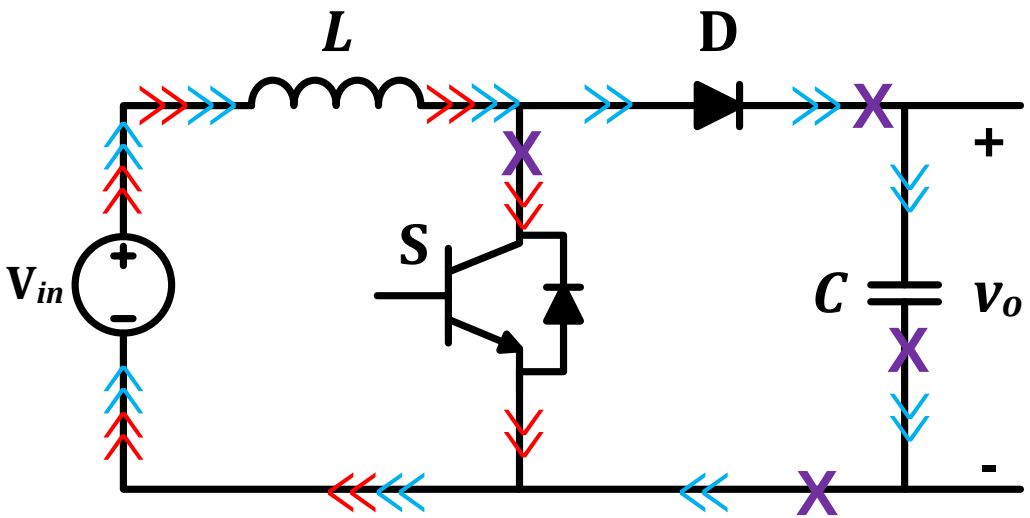
Current Paths:

- Switch-ON
- Switch-OFF
- X Critical

30 min

Answer

Critical Trace Sections



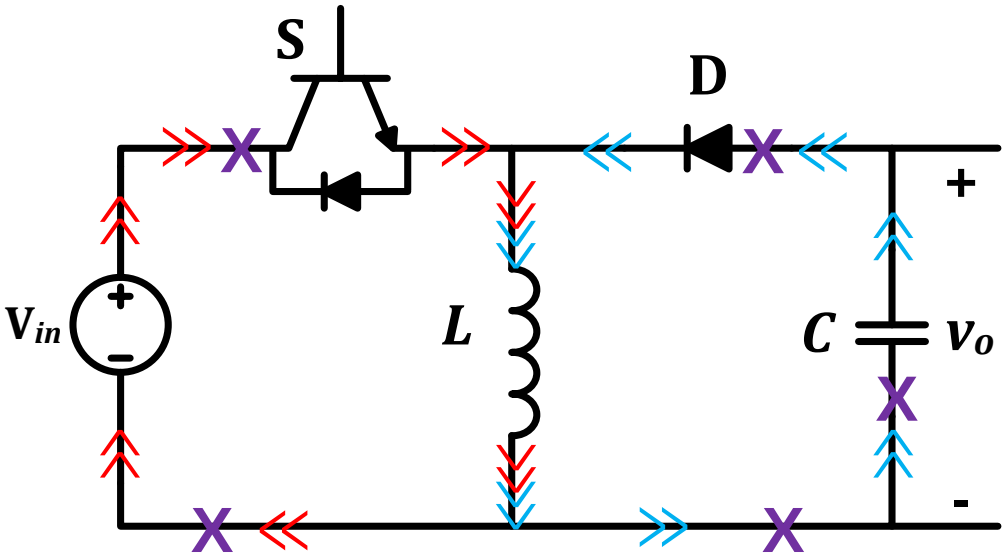
Boost Converter

Current Paths:

- Switch-ON
- Switch-OFF
- X Critical

Answer

Critical Trace Sections



Buck-Boost Converter

Current Paths:

- Switch-ON
- Switch-OFF
- X Critical

Answer

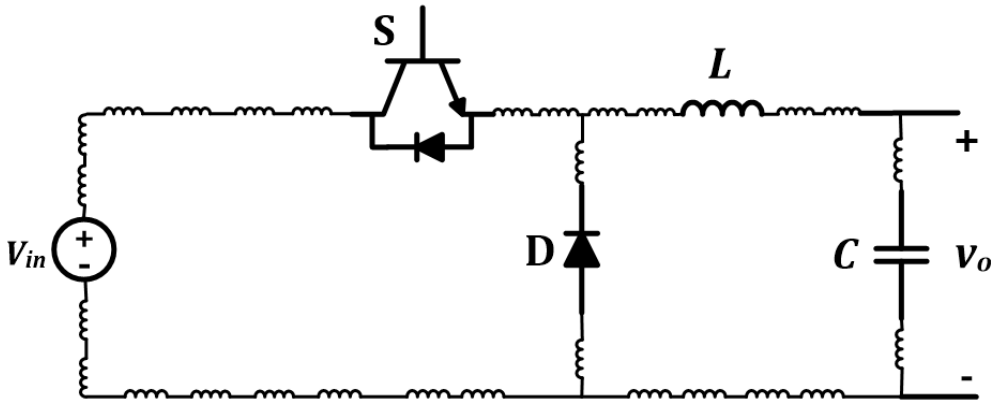
Following Lec 3 (pcb and layout design rules) any trance on the PCB will have inductive behavior therefore the above circuit can be represented as:

Therefore the concern with critical trace paths is generation of voltage spikes

$$v_{spike} = L\frac{di}{dt}$$

The generated voltage spike not only can damage the circuit components but also results in both conducted and radiated emission.

Block diagram of a buck converter topology including parasitic inductance of the PCB trace.

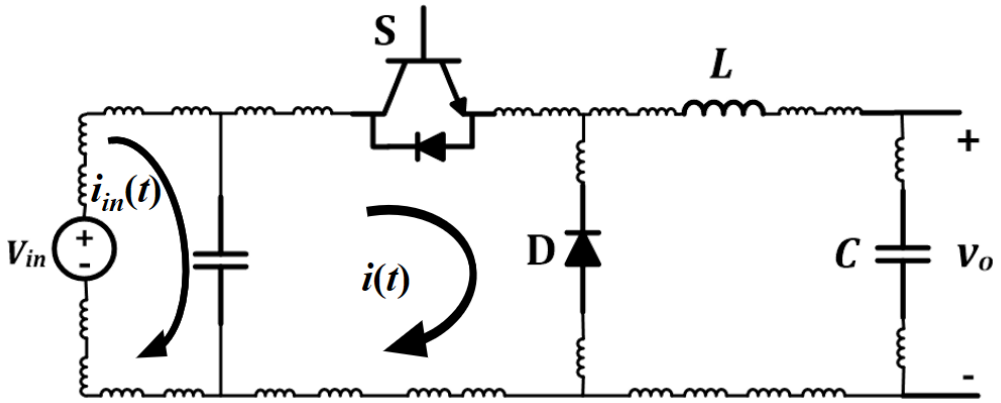


Answer

One of the common ways is to employ a snubber circuit across the power switch devices, however it can results in high losses. Therefore, the effect of the critical paths can be minimized by:

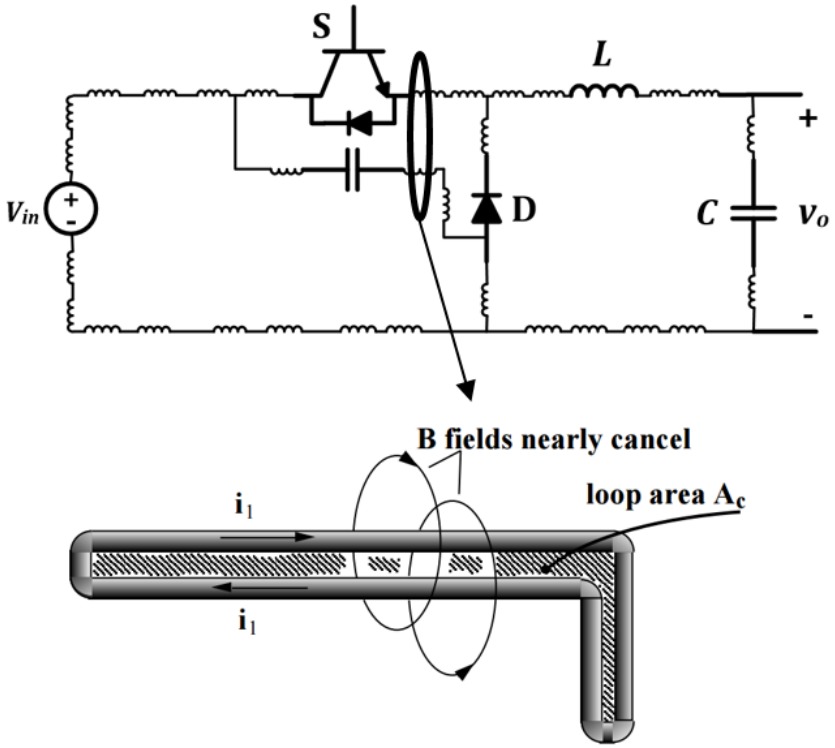
1- Increase the trace width
2- Minimizing the current loop by applying filtering
3- Reducing the loop area using near field cancellation

Minimizing the current loop by applying filtering



Answer

3- Reducing the loop area using near field cancellation



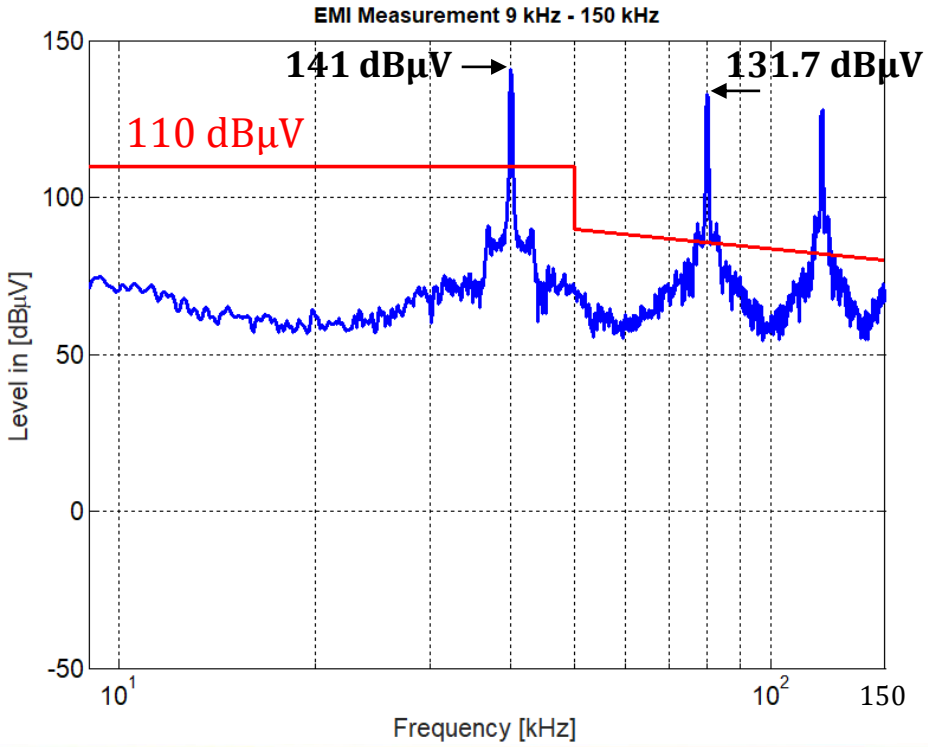
30 min

Q7. The measured differential mode (DM) conducted emission (peak measurement) of a single-phase PFC circuit is shown as below. It is required to design a two stage differential mode EMI filter (without damping) in order to meet the standard limit CISPR 15 (red-line) which is at 110 dBµV.

a) How much is the required attenuation?

b) Draw a block diagram of the DM EMI filter.

c) Giving the fact that you have L_{DM} = 180 µH, based on the required attenuation how much should be your capacitance value (C_{DM}) for DM filter design?



Answer

(a) Following the Lec 3, the required attenuation should be calculated based on the magnitude of first appearing peak below 150 kHz. Therefore, following the figure above the first peak is at 40 kHz with a magnitude of 141 dBµV. Therefore:

$$Att_{req}(f)[\mathrm{dB}] = U_{\max}(f)[\mathrm{dB}\,\mu\mathrm{V}] - \mathrm{CISPR}_{Limit}(f)[\mathrm{dB}\,\mu\mathrm{V}] + Margin[\mathrm{dB}]$$

Notice that beside the standard limit a margin (typically 6 dB) should be considered. This is due to the uncertainties in practice and also the tolerance of filter components.

$$Att_{req}(f)[\mathrm{dB}] = 141 - 110 + 6 = 37dB$$

Answer

(b) A block diagram of a two stage DM EMI filter for a single-phase PFC circuit is shown below:

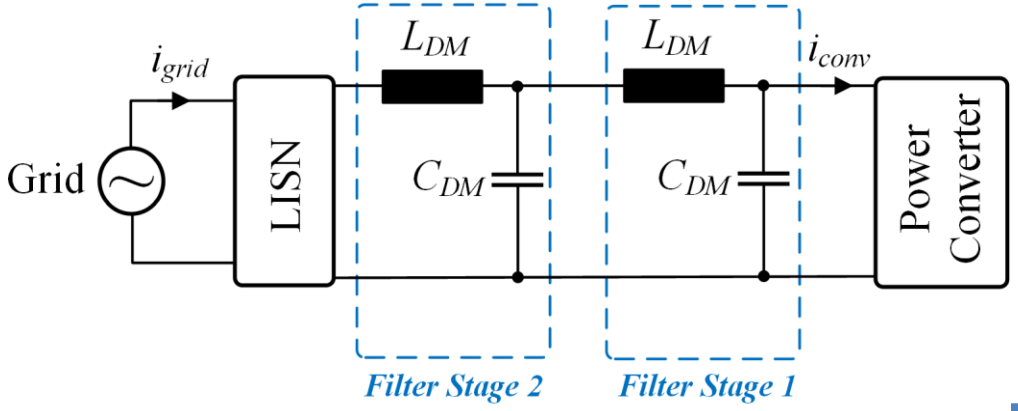


Fig. Block diagram of a two-stage DM filter for a single-phase PFC without damping stage.

Notably, the first filter component after converter is a capacitor. This is due to the fact that following impedance mismatch criteria (explained in Lec3) the first filtering component after a converter with current source behavior (PFC) should be a capacitor in order to provide a low impedance.

A current source has a high impedance.

(c) Following Lec 3 for frequencies below 150 kHz the approximation can not be used. Therefore using the following equation we have:

$$Att_{EMI\_Filter}(f) = \left|\left((j2\pi f)^2 L_{DM} C_{DM} + 1\right)^2 + (j2\pi f)^2 L_{DM} C_{DM}\right|$$

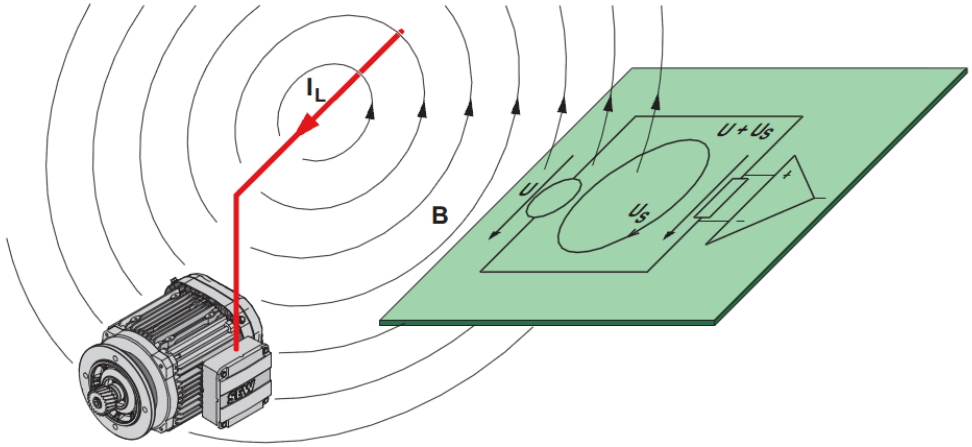
$$20log_{10}Att_{EMI\_filter} = Att_{req}(f) = 37\ dB$$

Therefore the required capacitance is C_{DM} = 880 nF.

Q8. The following figure shows an inductive coupling between a motor cable and a control circuit on a PCB. Knowing the fact that you are not able to apply any changes to the motor drive system and cable:

a) What is equation of the induced voltage?

b) Name three possible ways that can be applied to the control circuit in order to minimize the interference.



I_L	Current in the motor cable
B	Magnetic field
U_S	Interference voltage

Answer:

(b)

Considering the given situation and Fig. 1 and Fig. 2, the interference voltage is affected by the following factors and therefore can be reduced:

- Distance (*r*): The interference voltage is reduced with increasing spacing between motor drive cable/setup and the control circuit board. Due to the reduction of generated field density *B*. *B* is dependent on *r* (distance).

- Orientation (θ): If the conductor loop is parallel to the magnetic field lines, no interference voltage will be induced. The maximum interference voltage occurs when the loop and magnetic filed lines are at right angles (perpendicular).

- Area of the conductor loop (*A*): The interference voltage is proportional to the area of the conductor loop.

Answer:

From Lec 4 we know that the magnetic coupling generated in a conductor is:

$$\phi_T = LI$$

$$L = \frac{\phi_T}{I}$$

$$B = \frac{\mu I}{2\pi r}$$

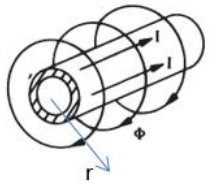


Fig. 1 Showing the produced magnetic flux when current I flows through a conductor. The generated field (B) depends on I and distance r.

When the generated field of one conductor cuts a second circuit we have a situation as in the figure below.

Therefore the answer of first part is the inducted voltage V_N as shown in the figure below.

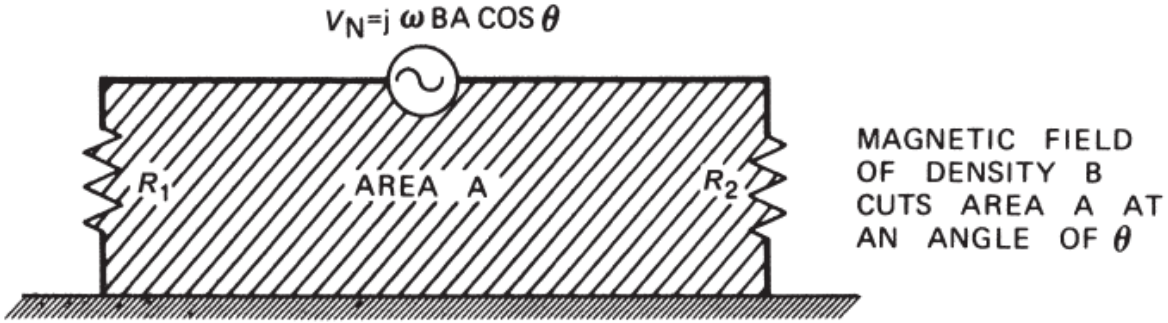


Fig. 2 Induced voltage in the second circuit/conductor when magnetic field of density B cuts area A at an angle of θ.

30 min

Q9. In order to meet the conducted emission requirement the following information are required:

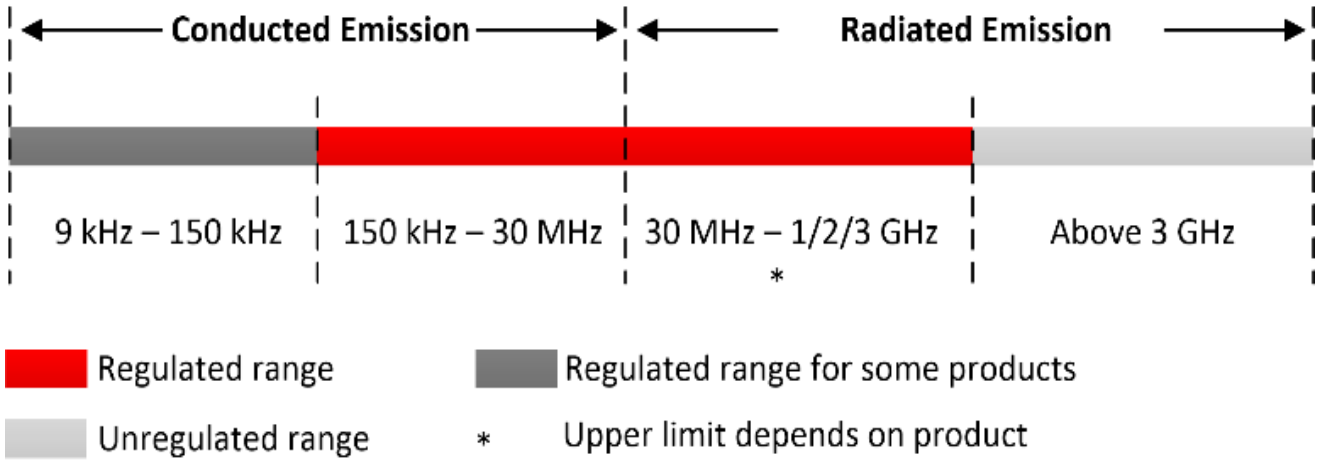
a)What are the frequency ranges of interest for conducted emission?

b) For a grid-connected power converter, draw a simple block-diagram of showing different elements/devices in measuring conducted emission.

c) What are the purposes of LISN/AMN? (name three)

Answer:

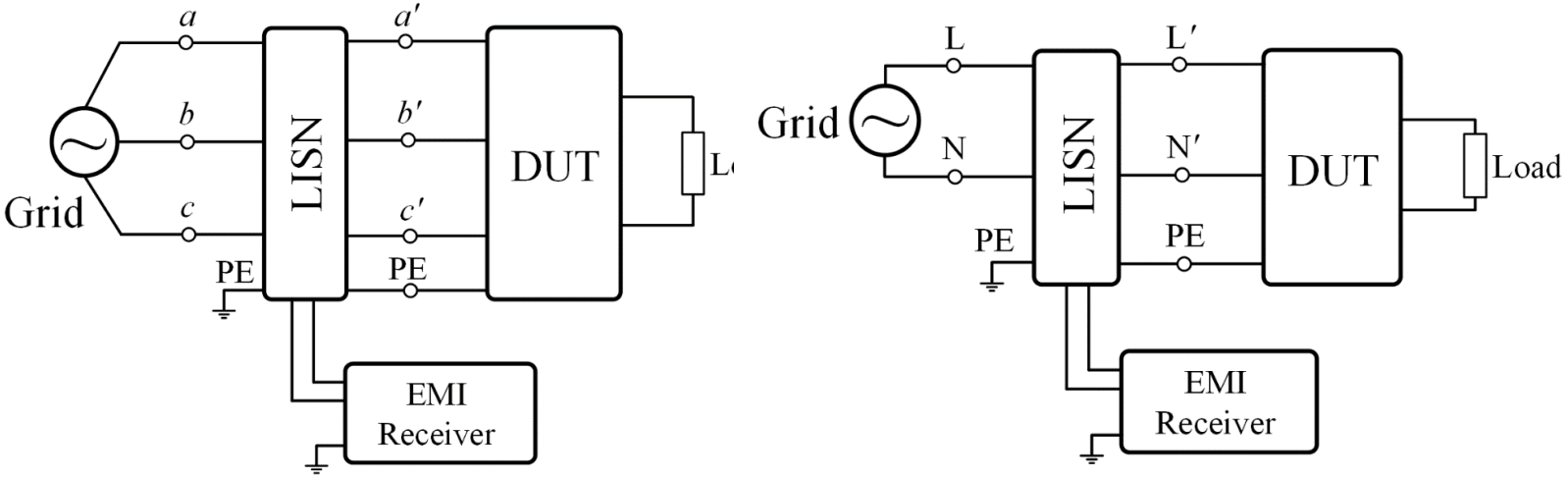
(a) The frequency ranges of conducted emission is shown in the Fig. 1.1 below. This has been mentioned and explained in Lec 1 and Lec 3. Notably, at the moment the conducted emission has two ranges. From 9 kHz-150 kHz which is regulated for some products such as lighting equipment (CISPR 15) and 150 kHz – 30 MHz which is a regulated range for all products/devices.



Conducted and radiated emission frequency ranges.

Answer:

(b) A simple diagram showing a placement of LISN/AMN and EMI receiver for single-phase and three-phase systems is shown in Fig. 1.2. This has been explained during Lec 3.



(a)	(b)

Fig. 1.2. Simplified block diagram for placement of LISN/AMN and EMI receiver for conducted emission measurement in: (a) single-phase and (b) three-phase systems.

Answer:

(C) The main purpose of using LISN/AMS is well covered in Lec 3. Fig. 1.3. exemplify the main purpose of using LISN for conducted emission measurement.

In general, the LISN/AMS is required in order to provide:

1- Fixed impedance for line currents and return path for ground currents
2- High frequency (HF) decoupling of grid and DUT
3- Finally to ensure repeatable measurement