Chapter 2
Inverter Control with Space Vector Modulation

Figure 2.1 shows the principle circuit of an inverter fed 3-phase AC motor with three phase windings u, v and w. The three phase voltages are applied by three pairs of semiconductor switches v_{u+}/v_{u-}, v_{v+}/v_{v-} and v_{w+}/v_{w-} with amplitude, frequency and phase angle defined by microcontroller calculated pulse patterns. The inverter is fed by the DC link voltage U_{DC}. In our example, a transistor inverter is used, which is today realized preferably with IGBTs.

Figure 2.2 shows the spacial assignment of the stator-fixed $\alpha\beta$ coordinate system, which is discussed in Chap. 1, to the three windings u, v and w. The logical position of the three windings is defined as:

0, if the winding is connected to the negative potential, or as
1, if the winding is connected to the positive potential

of the DC link voltage. Because of the three windings eight possible logical states and accordingly eight standard voltage vectors $\mathbf{u}_0$, $\mathbf{u}_1$ … $\mathbf{u}_7$ are obtained, of which the two vectors $\mathbf{u}_0$—*all windings are on the negative potential*—and $\mathbf{u}_7$—*all windings are on the positive potential*—are the so called zero vectors.

The spacial positions of the standard voltage vectors in stator-fixed $\alpha\beta$ coordinates in relation to the three windings u, v and w are illustrated in Fig. 2.2 as well. The vectors divide the vector space into six sectors S_1 … S_6 and respectively into four quadrants Q_1 … Q_4. The Table 2.1 shows the logical switching states of the three transistor pairs.

2.1 Principle of Vector Modulation

The following example will show how an arbitrary stator voltage vector can be produced from the eight standard vectors.

Let us assume that the vector to be realized, $\mathbf{u}_s$ is located in the sector S_1, the area between the standard vectors $\mathbf{u}_1$ and $\mathbf{u}_2$ (Fig. 2.3). $\mathbf{u}_s$ can be obtained from the vectorial addition of the two boundary vectors $\mathbf{u}_r$ and $\mathbf{u}_l$ in the directions of $\mathbf{u}_1$ and $\mathbf{u}_2$, respectively. In Fig. 2.3 mean:

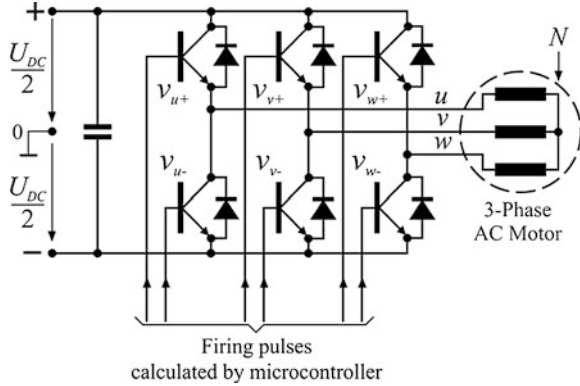**Fig. 2.1** Principle circuit of a
VSI inverter-fed 3-phase AC
motor

Firing pulses
calculated by microcontroller

Fig. 2.2 The standard
voltage vectors $\mathbf{u}_0$, $\mathbf{u}_1$... $\mathbf{u}_7$
formed by the three transistor
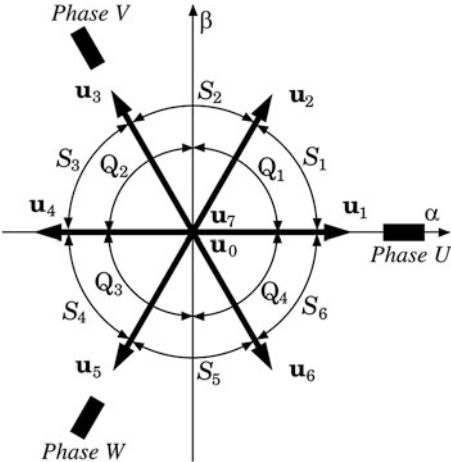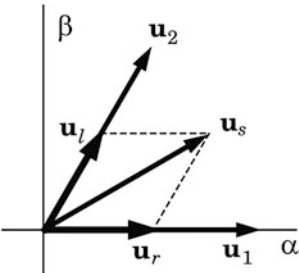pairs (Q_1... Q_4: quadrants,
S_1... S_6: sectors)

Table 2.1 The standard
voltage vectors and the logic
states

	$\mathbf{u}_0$	$\mathbf{u}_1$	$\mathbf{u}_2$	$\mathbf{u}_3$	$\mathbf{u}_4$	$\mathbf{u}_5$	$\mathbf{u}_6$	$\mathbf{u}_7$
u	0	1	1	0	0	0	1	1
v	0	0	1	1	1	0	0	1
w	0	0	0	0	1	1	1	1

Fig. 2.3 Realization of an
arbitrary voltage vector from
two boundary vectors

Subscript r, l: boundary vector on the right, left

Supposed the complete pulse period T_p^* is available for the realization of a vector with the maximum modulus (amplitude), which corresponds to the value $2U_{DC}/3$ of a standard vector, the following relation is valid:

$$|\mathbf{u}_s|_{\text{max}} = |\mathbf{u}_1| = \ldots = |\mathbf{u}_6| = \frac{2}{3}U_{DC} \tag{2.1}$$

From this, following consequences result:

1. $\mathbf{u}_s$ is obtained from the addition of $\mathbf{u}_r + \mathbf{u}_l$
2. $\mathbf{u}_r$ and $\mathbf{u}_l$ are realized by the logical states of the vectors $\mathbf{u}_1$ and $\mathbf{u}_2$ within the time span:

$$T_r = T_p^* \frac{|\mathbf{u}_r|}{|\mathbf{u}_s|_{\text{max}}} \; ; \; T_l = T_p^* \frac{|\mathbf{u}_l|}{|\mathbf{u}_s|_{\text{max}}} \tag{2.2}$$

$\mathbf{u}_1$ and $\mathbf{u}_2$ are given by the pulse pattern in Table 2.1. Only the switching times T_r, T_l must be calculated. From Eq. (2.2) the following conclusion can be drawn:

To be able to determine T_r and T_l, the amplitudes of $\mathbf{u}_r$ and $\mathbf{u}_l$ must be known.

It is prerequisite that the stator voltage vector $\mathbf{u}_s$ must be provided by the current controller with respect to modulus and phase. The calculation of the switching times T_r, T_l will be discussed in detail in Sect. 2.2. For now, two questions remain open:

1. What happens in the rest of the pulse period $T_p^* - (T_r + T_l)$?
2. In which sequence the vectors $\mathbf{u}_1$ and $\mathbf{u}_2$, and respectively $\mathbf{u}_r$ and $\mathbf{u}_l$ are realized?

In the rest of the pulse period $T_p^* - (T_r + T_l)$ one of the two zero vectors $\mathbf{u}_0$ or $\mathbf{u}_7$ will be issued to finally fulfil the following equation.

$$\mathbf{u}_s = \mathbf{u}_r + \mathbf{u}_l + \mathbf{u}_0 \text{ (or } \mathbf{u}_7)$$
$$= \frac{T_r}{T_p^*}\mathbf{u}_1 + \frac{T_l}{T_p^*}\mathbf{u}_2 + \frac{T_p^* - (T_r + T_l)}{T_p^*}\mathbf{u}_0 \text{ (or } \mathbf{u}_7) \tag{2.3}$$

The resulting question is, in which sequence the now three vectors—two boundary vectors and one zero vector—must be issued. Table 2.2 shows the necessary switching states in the sector S_1.

Table 2.2 The switching states in the sector S_1

	$\mathbf{u}_0$	$\mathbf{u}_1$	$\mathbf{u}_2$	$\mathbf{u}_7$
u	0	1	1	1
v	0	0	1	1
w	0	0	0	1

It can be recognized that with respect to transistor switching losses the most favourable sequence is to switch every transistor pair only once within a pulse period.

If the last switching state was $\mathbf{u}_0$, *this would be the sequence*

$$\mathbf{u}_0 \Rightarrow \mathbf{u}_1 \Rightarrow \mathbf{u}_2 \Rightarrow \mathbf{u}_7$$

but if the last switching state was $\mathbf{u}_7$, *this would be*

$$\mathbf{u}_7 \Rightarrow \mathbf{u}_2 \Rightarrow \mathbf{u}_1 \Rightarrow \mathbf{u}_0$$

With this strategy the switching losses of the inverter become minimal. Different strategies will arise if other criteria come into play (refer to Sects. 2.5.1, 2.5.3). If the switching states of two pulse periods succeeding one another are plotted exemplarily a well-known picture from the pulse width modulation technique arises (Fig. 2.4).

Figure 2.4 clarifies that the time period T_p^* for the realization of a voltage vector is only one half of the real pulse period T_p. Actually, in the real pulse period T_p two vectors are realized. These two vectors may be the same or different, depending only on the concrete implementation of the modulation.

Until now the process of the voltage vector realization was explained for the sector S_1 independent of the vector position within the sector. With the other sectors S_2–S_6 the procedure will be much alike: splitting the voltage vector into its boundary components which are orientated in the directions of the two neighboring standard vectors, every vector of any arbitrary position can be developed within the

Fig. 2.4 Pulse pattern of voltage vectors in sector S_1
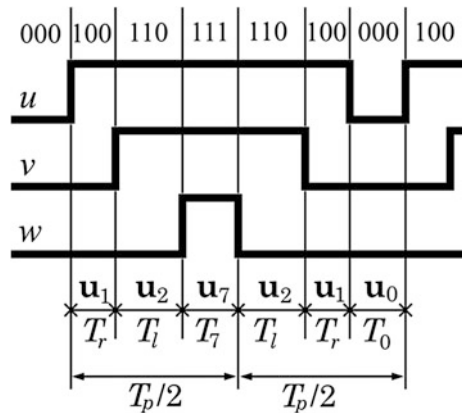
whole vector space. This statement is valid considering the restrictions which will be discussed in Sect. 2.3. The following pictures give a summary of switching pattern samples in the remaining sectors S_2 ... S_6 of the vector space (Fig. 2.5).

Fig. 2.5 Pulse pattern of the voltage vectors in the sectors S_2... S_6
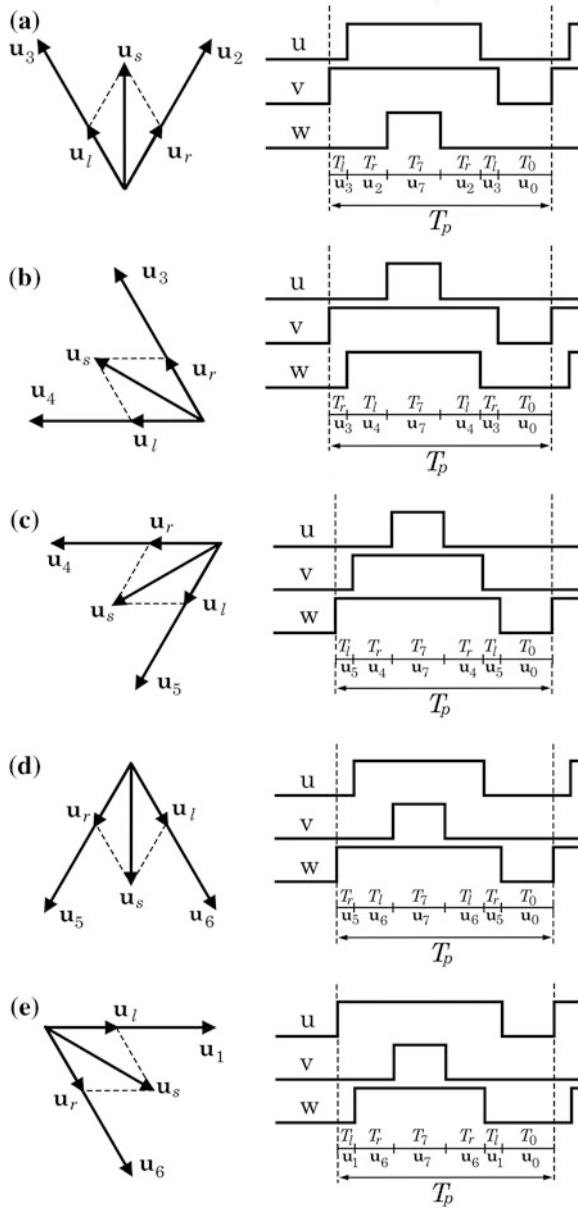
From the fact, that:

1. the current controller delivers the reference value of a new voltage vector $\mathbf{u}_s$ to the modulation after every sampling period T, and
2. every (modulation and) pulse period T_p contains the realization of two voltage vectors,

the relation between the pulse frequency $f_p = 1/T_p$ and the sampling frequency $1/T$ is obtained. The theoretical statement from Fig. 2.4 is that two sampling periods T correspond to one pulse period T_p. However this relationship is rarely used in practice. In principle it holds

> that the new voltage vector $\mathbf{u}_s$ provided by the current controller is realized within at least one or several pulse periods T_p.

Thereby it is possible to find a suitable ratio of pulse frequency to sampling frequency, which makes a sufficiently high pulse frequency possible at a simultaneously sufficiently big sampling period (necessary because of a restricted computing power of the microcontroller). In most systems f_p is normally chosen in the range 2, 5–20 kHz. Figure 2.6 illustrates the influence of different pulse frequencies on the shape of voltages and currents.
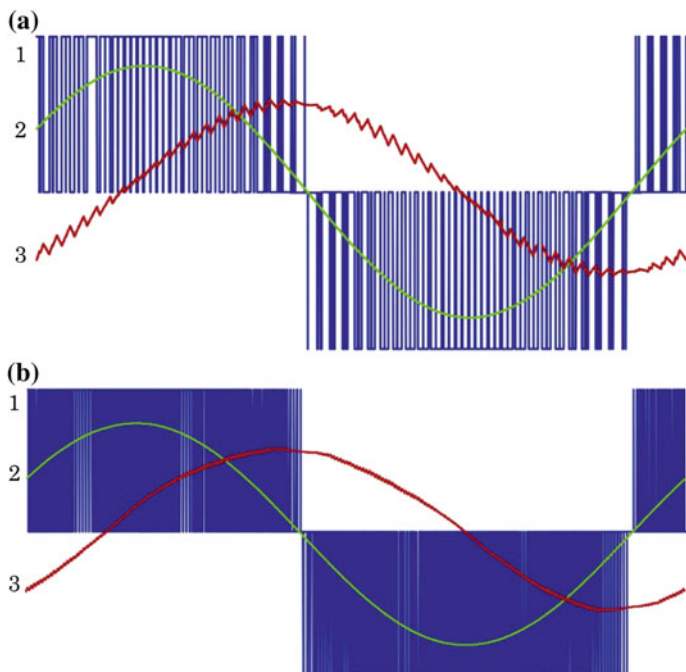

Fig. 2.6 Pulse frequency f_p and the influence on the stator voltage as well as the stator current. *1* pulsed phase-to-phase voltage; *2* fundamental wave of the voltage; *3* current

2.2 Calculation and Output of the Switching Times

After the principle of the space vector modulation has been introduced, the realization of that principle shall be discussed now. Eventually the inverter must be informed on "how" and respectively "how long" it shall switch its transistor pairs, after the voltage vector to be realized is given with respect to modulus and phase angle.

Thanks to the information about phase angle and position (quadrant, sector) of the voltage vector the question "how" can be answered immediately. From the former section the switching samples for all sectors as well as their optimal output sequences with respect to the switching losses are already arranged.

The question "how long" is subject of this section. From Eqs. (2.2), (2.3) it becomes obvious, that the calculation of the switching times T_r, T_l depends only on the information about the moduli of the two boundary vectors $\mathbf{u}_r$, $\mathbf{u}_l$. The vector $\mathbf{u}_s$ (Fig. 2.7) is predefined by:

1. Either the DC components u_{sd}, u_{sq} in dq coordinates. From these, the total phase angle is obtained from the addition of the current angular position ϑ_s of the coordinate system (refer to Fig. 1.2) and the phase angle of $\mathbf{u}_s$ within the coordinate system.

$$\vartheta_u = \vartheta_s + \arctan\left(\frac{u_{sq}}{u_{sd}}\right) \tag{2.4}$$

2. Or the sinusoidal components $u_{s\alpha}$, $u_{s\beta}$ in $\alpha\beta$ coordinates. This representation does not contain explicitly the information about the phase angle, but includes it implicitly in the components.

Therefore two strategies for calculation of the boundary components exist.

1. *Strategy* 1: At first, the phase angle ϑ_u is found by use of the Eq. (2.4), and after that the angle γ according to Fig. 2.7 is calculated, where γ represents the angle ϑ_u reduced to sector 1. Then the calculation of the boundary components can be

Fig. 2.7 Possibilities for the specification of the voltage vector $\mathbf{u}_s$
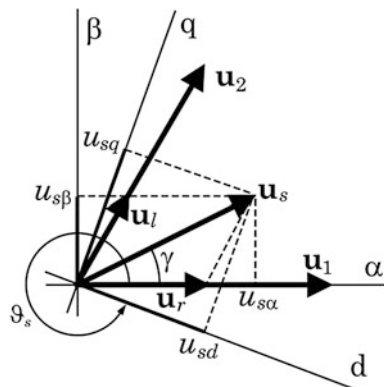
performed by use of the following formulae, which is valid for the whole vector space:

$$|\mathbf{u}_r| = \frac{2}{\sqrt{3}}|\mathbf{u}_s| \sin(60° - \gamma)\,; \ |\mathbf{u}_l| = \frac{2}{\sqrt{3}}|\mathbf{u}_s| \sin(\gamma) \tag{2.5}$$

With:

$$|\mathbf{u}_s| = \sqrt{u_{sd}^2 + u_{sq}^2} \tag{2.6}$$

2. *Strategy* 2: After the coordinate transformation, the stator-fixed components $u_{s\alpha}$, $u_{s\beta}$ are obtained from u_{sd}, u_{sq}. For the single sectors, $\mathbf{u}_r$ and $\mathbf{u}_l$ can be calculated using the formulae in Table 2.3.

The proposed strategies for the calculation of the switching times T_r, T_l are equivalent. The output of the switching times itself depends on the hardware configuration of the used microcontroller. The respective procedures will be explained in detail in the Sect. 2.4.

The application of the 2nd strategy seems to be more complicated in the first place because of the many formulae in Table 2.3. But at closer look it will become obvious that essentially only three terms exist.

$$\mathbf{a} = |u_{s\alpha}| + \frac{1}{\sqrt{3}}|u_{s\beta}|\,; \ \mathbf{b} = |u_{s\alpha}| - \frac{1}{\sqrt{3}}|u_{s\beta}|\,; \ \mathbf{c} = \frac{2}{\sqrt{3}}|u_{s\beta}| \tag{2.7}$$

With the help of the following considerations the phase angle of $\mathbf{u}_s$ can be easily calculated.

1. By the signs of $u_{s\alpha}$, $u_{s\beta}$ one finds out in which of the four quadrants the voltage vector is located.

Table 2.3 Moduli of the boundary components $\mathbf{u}_r$, $\mathbf{u}_l$ dependent on the positions of the voltage vectors

		$|\mathbf{u}_r|$	$|\mathbf{u}_l|$
S_1	Q_1	$|u_{s\alpha}| - \frac{1}{\sqrt{3}}|u_{s\beta}|$	$\frac{2}{\sqrt{3}}|u_{s\beta}|$
S_2	Q_1	$|u_{s\alpha}| + \frac{1}{\sqrt{3}}|u_{s\beta}|$	$-|u_{s\alpha}| + \frac{1}{\sqrt{3}}|u_{s\beta}|$
	Q_2	$-|u_{s\alpha}| + \frac{1}{\sqrt{3}}|u_{s\beta}|$	$|u_{s\alpha}| + \frac{1}{\sqrt{3}}|u_{s\beta}|$
S_3	Q_2	$\frac{2}{\sqrt{3}}|u_{s\beta}|$	$|u_{s\alpha}| - \frac{1}{\sqrt{3}}|u_{s\beta}|$
S_4	Q_3	$|u_{s\alpha}| - \frac{1}{\sqrt{3}}|u_{s\beta}|$	$\frac{2}{\sqrt{3}}|u_{s\beta}|$
S_5	Q_3	$|u_{s\alpha}| + \frac{1}{\sqrt{3}}|u_{s\beta}|$	$-|u_{s\alpha}| + \frac{1}{\sqrt{3}}|u_{s\beta}|$
	Q_4	$-|u_{s\alpha}| + \frac{1}{\sqrt{3}}|u_{s\beta}|$	$|u_{s\alpha}| + \frac{1}{\sqrt{3}}|u_{s\beta}|$
S_6	Q_4	$\frac{2}{\sqrt{3}}|u_{s\beta}|$	$|u_{s\alpha}| - \frac{1}{\sqrt{3}}|u_{s\beta}|$

2. Because the moduli of $\mathbf{u}_r$ and $\mathbf{u}_l$ are always positive, and because the term **b** changes its sign at every sector transition, **b** can be tested on its sign to determine to which sector of the thus found quadrant the voltage vector belongs.

2.3 Restrictions of the Procedure

For practical application to inverter control, the vector modulation algorithm (VM) has certain restrictions and special properties which implicitly must be taken into account for implementation of the algorithm as well as for hardware design.

2.3.1 Actually Utilizable Vector Space

The geometry of Fig. 2.3 may lead to the misleading assumption that arbitrary vectors can be realized in the entire vector space which is limited by the outer circle in Fig. 2.8b, i.e. every vector $\mathbf{u}_s$ with $|\mathbf{u}_s| \le 2\,U_{DC}/3$ would be practicable. The following consideration disproves this assumption: It is known that the vectorial addition of $\mathbf{u}_r$ and $\mathbf{u}_l$ is not identical with the scalar addition of the switching times T_r and T_l. To simplify the explanation, the constant half pulse period which, according to Fig. 2.4, is available for the realization of a vector is replaced by $T_{p/2} = T_p/2$. After some rearrangements of Eq. (2.2) by use of (2.5) the following formula is obtained.

$$T_\Sigma = T_r + T_l = \sqrt{3}\, T_{p/2}\, \frac{|\mathbf{u}_s|}{U_{DC}}\cos(30° - \gamma) \tag{2.8}$$

In case of voltage vector limitation, that is $|\mathbf{u}_s| = 2\,U_{DC}/3$, it follows from (2.8):

$$T_{\Sigma\,\max} = T_{p/2}\frac{2}{\sqrt{3}}\cos(30° - \gamma) \quad \text{with} \quad 0° \le \gamma \le 60° \tag{2.9}$$
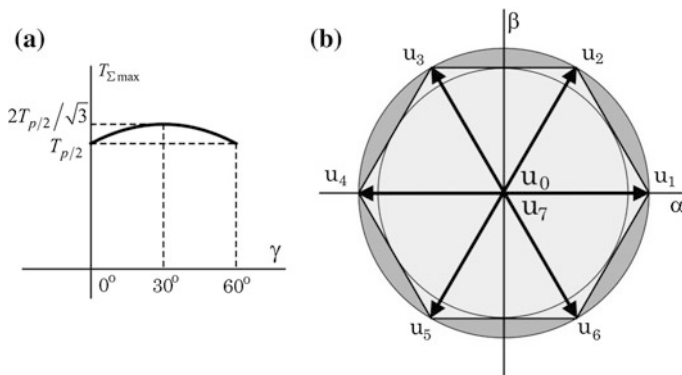

Fig. 2.8 Temporal (**a**) and spacial (**b**) representation of the utilizable area for the voltage vector $\mathbf{u}_s$

The diagram in Fig. 2.8a shows the fictitious characteristic of $T_{\Sigma max}$ at excess of the half pulse period $T_{p/2}$. By limitation of T_Σ to $T_{p/2}$ the actually feasible area is enclosed by the hexagon in Fig. 2.8b.

In some practical cases—e.g. for reduction of harmonics in the output voltage— the hexagon area is not used completely. Only the area of the inner, the hexagon touching circle will be used. The usable maximum voltage is then:

$$|\mathbf{u}_s|_{\max} = \frac{1}{\sqrt{3}} U_{DC} \qquad (2.10)$$

Thus the area between the hexagon and the inner circle remains unused. Utilization of this remaining area is possible if the voltage modulus is limited by means of a *time limitation* from T_Σ to $T_{p/2}$. To achieve this, the zero vector time is dispensed with, and only one transistor pair is involved in the modulation in each sector (refer to Fig. 2.20, right). A *direct modulus limitation* will be discussed later in connection with the current controller design.

An important characteristic for the application of the VM is the voltage resolution Δu, which for the case of limitation to the inner circle or at use of Eq. (2.10) can be calculated as follows:

$$\Delta u = \frac{2}{\sqrt{3}} \frac{\Delta t}{T_p} U_{DC} \; [\text{V}] \qquad (2.11)$$

At deeper analysis, restricted on the hexagon only, it turns out that the zero vector times become very small or even zero if the voltage vector approaches its maximum amplitude. This is equivalent to an (immediate) switch on or off of the concerned transistor pair after it has been switched off or on. For this reason the voltage vector modulus has to be limited to make sure the zero vector times T_0 and T_7 never fall below the switching times of the transistors. For IGBT´s the switching times are approx. <1–4 µs, so that this contraction of the voltage vector for usual switching frequencies of 1–5 kHz can be considered insignificant. However, the situation becomes more critical for higher switching frequencies or if slow-switching semiconductors, such as thyristors, are used.

The values either of T_r or of T_l become very small in the boundary zone between the sectors or near one of the standard vectors $\mathbf{u}_1 \ldots \mathbf{u}_6$. For some commonly used digital signal processing structures (refer to the application example with TMS 320C20/C25 in Sect. 2.4) the PWM synchronization is directly coupled to the interrupt evaluation of the timer counters for T_r and T_l. For these structures the values of T_r and T_l must never fall below the interrupt reaction times causing another limitation of the utilizable area. The arising forbidden zones are shown in Fig. 2.9.

Fig. 2.9 Forbidden zones in the vector space
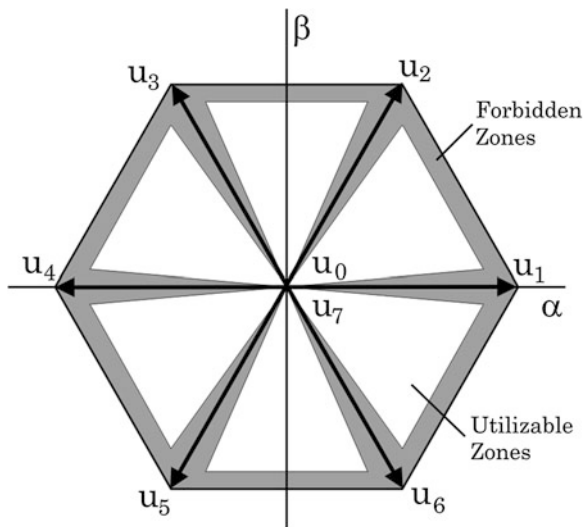
2.3.2 Synchronization Between Modulation and Signal Processing

According to theory (refer to Fig. 2.4) the modulated voltage in the context of control or digital signal processing looks like in Fig. 2.10 for the samplings periods $(k - 1)$, (k) and $(k + 1)$. The voltage output sequence in period (k)

$$T_r\left(\mathbf{u}_r\right) \Rightarrow T_l\left(\mathbf{u}_l\right) \Rightarrow T_7\left(\mathbf{u}_7\right) / T_l\left(\mathbf{u}_l\right) \Rightarrow T_r\left(\mathbf{u}_r\right) \Rightarrow T_0\left(\mathbf{u}_0\right)$$

leads to the following time relation:

$$T_{synch} = T_p - \frac{T_0(k)}{2} + \frac{T_0(k-1)}{2}$$

For a dynamic process with $\mathbf{u}_s(k - 1) \neq \mathbf{u}_s(k)$ is also $T_0(k - 1)/2 \neq T_0(k)/2$. That means, that T_{synch} would be not constant (Fig. 2.10b), making the use of up/down counters—like usually done in PWM units—impossible. Therefore, a different sequence shall be used for voltage output:

$$\frac{T_0}{2}\left(\mathbf{u}_0\right) \Rightarrow T_r\left(\mathbf{u}_r\right) \Rightarrow T_l\left(\mathbf{u}_l\right) \Rightarrow T_7\left(\mathbf{u}_7\right) / T_l\left(\mathbf{u}_l\right) \Rightarrow T_r\left(\mathbf{u}_r\right) \Rightarrow \frac{T_0}{2}\left(\mathbf{u}_0\right)$$

Figure 2.10b shows this alternative sequence. It is obvious from the figure that this sequence is absolutely stable and therefore the use of up/down counters is supported. This means also *a strict synchronization between control and pulse periods* which must be considered already in the design phase of the signal processing hardware.
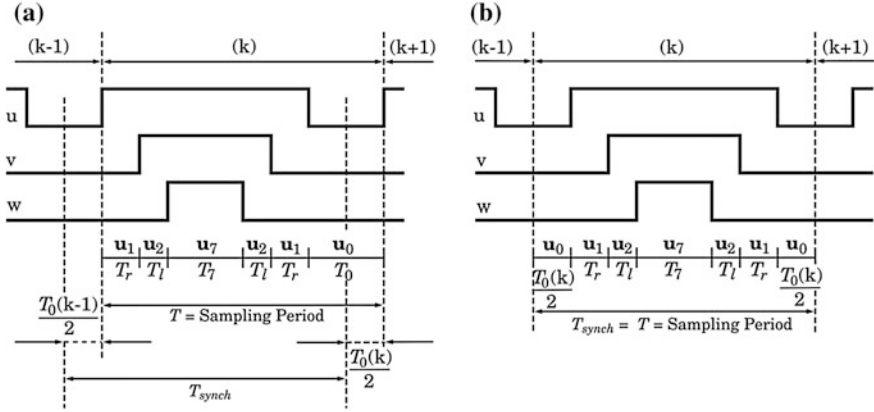
Fig. 2.10 For ensuring synchronization between modulation and control: the theoretical sequence (**a**) must be modified (**b**)

2.3.3 Consequences of the Protection Time and Its Compensation

So far, the semiconductors had been regarded as ideal switches with un-delayed turn-on and turn-off characteristics. However, the IGBT's physically reach their safe switched-on or switched-off state only after a certain turn-on or turn-off period t_{on}, t_{off}. To avoid inverter short circuit, the switch-on edge of the control signal must be delayed for a time t_D which is greater than the turn-off time t_{off}. This time is called protection time or blanking time (Fig. 2.11). In practice t_D is chosen in a way that t_{off} will be nearly 70–80 % of t_D.

Figure 2.11b shows in turn: **1**. The reference voltage $\mathcal{U}_v^*$ for the phase v. **2**. The actual IGBT control signals v_+ and v_-, modified by the protection time t_D. **3**. The actual voltage u_v of phase v. **4**. The voltage errors Δu_v. The influence of t_D on the trajectory of the stator voltage vector $\mathbf{u}_s$ as well as on the fundamental wave of the phase voltage are illustrated in Fig. 2.11c, d.

The voltage error Δu_v, caused by t_D and shown in Fig. 2.11d, can be calculated as follows:

$$\Delta u_v = u_v^* - u_v = \begin{cases} -\frac{t_D}{T_p}\left(\frac{2}{3}U_{DC}\right) & \text{for } i_{sv} > 0 \\ \frac{t_D}{T_p}\left(\frac{2}{3}U_{DC}\right) & \text{for } i_{sv} < 0 \end{cases} \qquad (2.12)$$

The voltage error depends on the sign of the phase current and may be effectively compensated with respect to the voltage mean average value. This compensation can be realized either in hardware or in software. *Software compensation* is more widely used today. Preferably, the compensation is done without using the actual current feedbacks which could be critical because of the pulsed current as
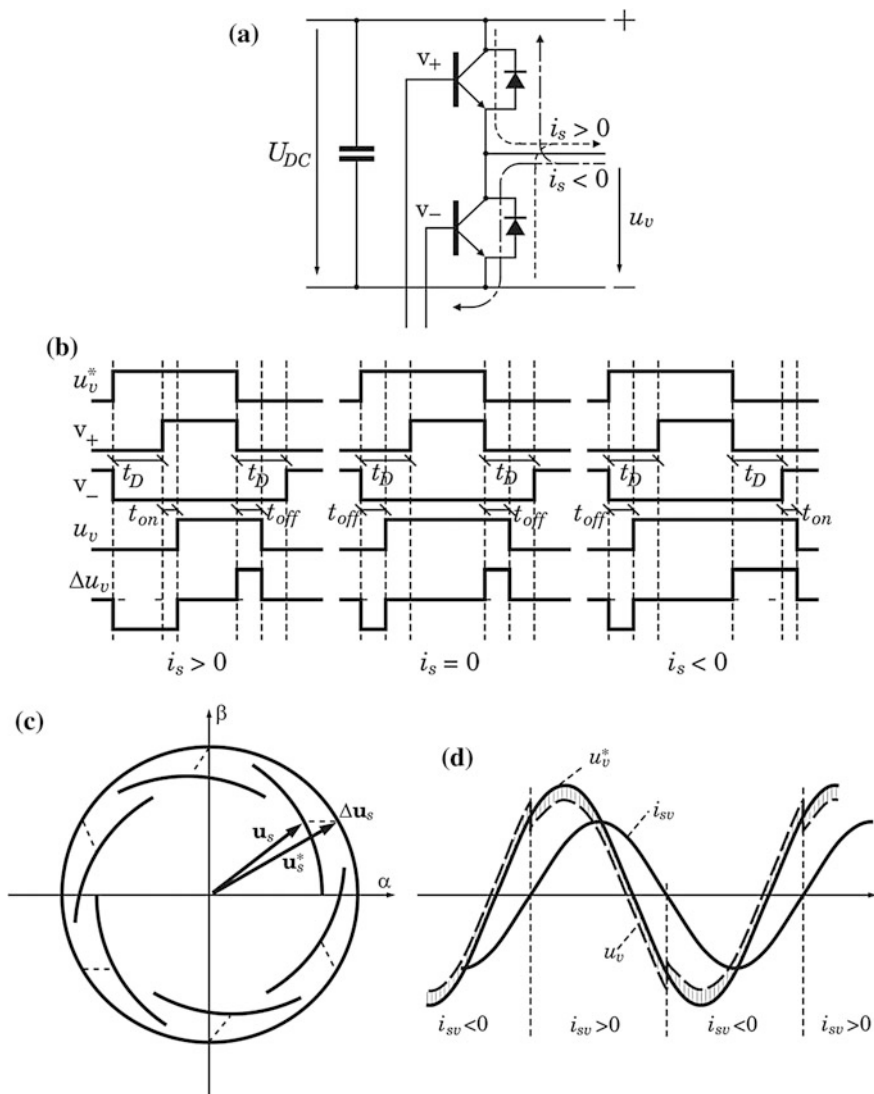
Fig. 2.11 Origin of the protection time t_D and its influence on the output voltage

well as the measuring noise at zero crossings. This is possible if the current controller works without or with predictable delay. In Chap. 5 it will be shown that this condition is largely fulfilled for the control algorithms to be introduced there.

In this case the reference value can be used to capture the sign instead of the actual value. The reference values i_{su}^*, i_{sv}^* and i_{sw}^* of the phase currents can be

calculated from i_{sd}^*, i_{sq}^* by use of a coordinate transformation. With that the error components in αβ-coordinates are obtained as follows:

$$
\begin{cases}
\Delta u_{s\alpha} = \left[-sign\left(i_{su}^*\right) + \tfrac{1}{2}sign\left(i_{sv}^*\right) + \tfrac{1}{2}sign\left(i_{sw}^*\right)\right] \tfrac{t_D}{T_p}\left(\tfrac{2}{3}U_{DC}\right) \\
\Delta u_{s\beta} = \left[-sign\left(i_{sv}^*\right) + sign\left(i_{sw}^*\right)\right] \tfrac{t_D}{T_p}\left(\tfrac{2}{3}U_{DC}\right)\tfrac{\sqrt{3}}{2}
\end{cases}
\tag{2.13}
$$

The error components according to (2.13) are added to the stator-fixed voltage components $u_{s\alpha}$, $u_{s\beta}$ before they are forwarded to the modulation.

2.4 Realization Examples

The realization of the space vector modulation requires a suitable periphery, which has to be added to the processor hardware when normal microprocessors (μP) or digital signal processors (DSP) are used. However, a number of microprocessors with this periphery on chip, so called micro controllers (μC) are available on the market today, allowing implementation of advanced modulation algorithms without additional hardware.

Microcontrollers, which are utilizable for 3-phase AC machine systems due to their internal PWM units as well as other on-chip periphery units, are e.g.

1. SAB 80C166, SAB C167 (Siemens, Infineon): The time resolution Δt of C166 is 400 ns, of C167 50 ns. The upper and the lower transistor of a phase leg are not controllable separately using the C167-PWM unit,[1] which would be necessary for an efficient, software based generation of the protection time. A 32 bit single chip microcontroller of the TC116x series can be used very advantageously today for a high-quality drive.
2. TMS 320C240/F240 (Texas Instruments): Δt = 50 ns. The μC supports the direct generation of the protection time t_D, and the transistors of a pair are controllable independently. Also, chips of the family TMS 320 F281x and F28F3x are used very widely today.

In many systems a double processor configuration is used due to the strong price collapse of the processors in the last years. For such applications, the digital signal processors from Texas Instruments TMS 320C25 (16 Bit, fixed-point arithmetic) or TMS 320C32 (32 Bit, floating-point arithmetic) can be recommended particularly.

The application of the modulation algorithm, described in Sects. 2.1 and 2.2, shall be illustrated now in detail on 4 examples, orientated essentially on the Siemens microcontrollers SAB 80C166, SAB C167 and the Texas Instruments DSP TMS 320C20/C25. The calculation of the switching times is carried out according to the 2nd strategy of Sect. 2.2, i.e. by means of the $\alpha\beta$ voltage components.

---

[1]This is possible, however, if the modulation is not realized with PWM units but with CAPCOM registers.

In principle, the concrete formulae for the computing of the switching times in all sectors shall be worked out first using Table 2.3. These formulae will then be used on-line. The computing and output will be independent of the hardware following the flow chart in the Fig. 2.12. The flow chart clarifies the steps to determine the space vector area in which the voltage vector to be realized is located. After that, the computation dependent on the respective hardware, will follow.

2.4.1 Modulation with Microcontroller SAB 80C166

The microcontroller SAB 80C166 is a special high-performance microprocessor with an extensive periphery on the chip. Particularly the Capture/Compare register unit supports the space vector modulation for 3-phase AC machines. The double register compare mode is used in the following example.

In double register compare mode the 16 CapCom registers CC0-CC15 are configured in two register banks and assigned in pairs to one of the two timers T0 or T1 respectively. E.g. the three pairs CC0/CC8, CC1/CC9 and CC2/CC10 with the inputs/outputs CC0IO/P2.0, CC1IO/P2.1 and CC2IO/P2.2, which are configured as outputs here, shall be used. The simplified hardware structure to control the inverter is shown in the Fig. 2.13. The assignment of the register pairs to the inverter phase legs is represented in the Fig. 2.14.

The modulation works in a fixed time frame with the pulse period T_p, which represents at the same time the reload value T_{reload} for the timer T0. This stable time frame supports the synchronization between the hardware hierarchies as well as between digital control, modulation and current measurement, which shall be discussed later. Thus, the reload register T0REL must be loaded with T_p only once at processor initialization. In the current sampling period (k) the turn-on/turn-off times T_{u_on}, T_{u_off}, T_{v_on}, T_{v_off}, T_{w_on} and T_{w_off} of the inverter legs will be calculated and stored intermediately in a RAM table. An interrupt signal T0IR is triggered at overflow of the timer T0 which causes the transfer of the reload value from the register T0REL into timer T0. The interrupt signal T0IR at the same time activates an interrupt service routine to load the new switching times from the RAM table into the register pair for the following sampling period. In the next sampling period ($k + 1$) and while the timer T0 is counting up, the compare matches between:

  T0 and CC0, CC1 and CC2 as well as
  T0 and CC8, CC9 and CC10
cause the switchover of the phases u, v and w to
  the positive or respectively
  the negative potential
of the DC link voltage U_{DC}. The voltage components $u_{s\alpha}$ and $u_{s\beta}$ are normalized to the maximum value $2U_{DC}/3$ in the following calculations, so that an extra index is neglected following the definition of the times introduced in Fig. 2.14, and using
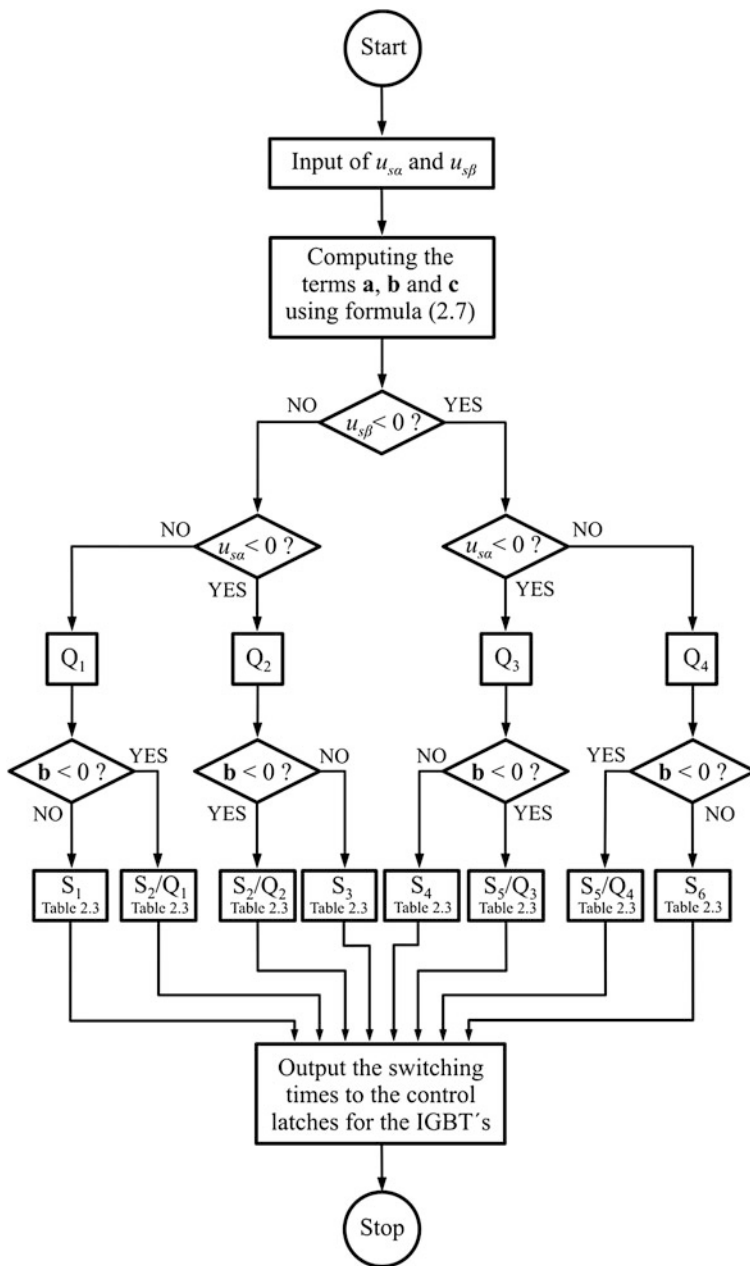
Fig. 2.12 Flow chart for the computing of the switching times according to the space vector modulation

Fig. 2.13 Hardware configuration for the space vector modulation using the microcontroller SAB 80C166 in double register compare mode
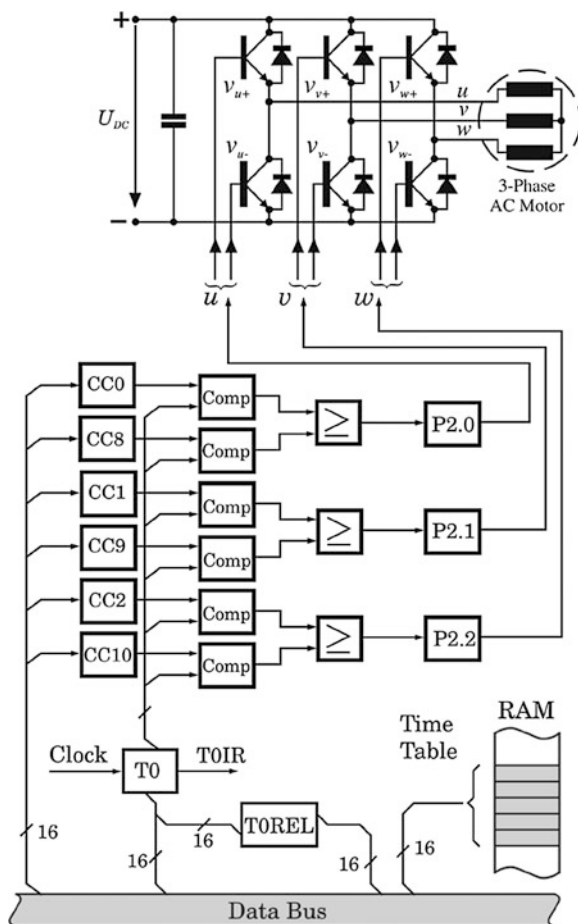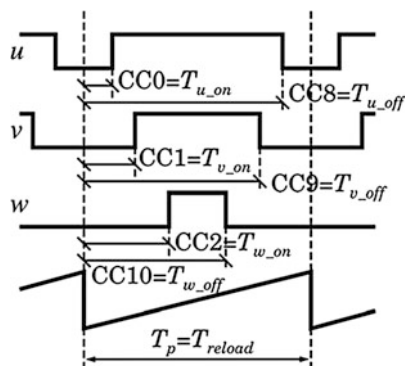

Fig. 2.14 Assignment of the register pairs to the switching times of the inverter legs

Eqs. (2.1), (2.2), (2.7) and Table 2.3 the following formulae are obtained for the different sectors:

1. Sector 1:

$$T_{u\_on} = \frac{T_p}{2}(1 - \mathbf{a}) \; ; \; T_{v\_on} = \frac{T_p}{2}(1 + \mathbf{b} - \mathbf{c}) \; ; \; T_{w\_on} = \frac{T_p}{2}(1 + \mathbf{a})$$
$$T_{u\_off} = \frac{T_p}{2}(3 + \mathbf{a}) \; ; \; T_{v\_off} = \frac{T_p}{2}(3 - \mathbf{b} + \mathbf{c}) \; ; \; T_{w\_off} = \frac{T_p}{2}(3 - \mathbf{a}) \quad (2.14)$$

2. Sector 2:

$$\text{Quadrant 1}: \; T_{u\_on} = \frac{T_p}{2}(1 - \mathbf{a} - \mathbf{b}) \; ; \; T_{u\_off} = \frac{T_p}{2}(3 + \mathbf{a} + \mathbf{b})$$
$$\text{Quadrant 2}: \; T_{u\_on} = \frac{T_p}{2}(1 + \mathbf{a} + \mathbf{b}) \; ; \; T_{u\_off} = \frac{T_p}{2}(3 - \mathbf{a} - \mathbf{b})$$
$$T_{v\_on} = \frac{T_p}{2}(1 - \mathbf{c}) \; ; \; T_{w\_on} = \frac{T_p}{2}(1 + \mathbf{c})$$
$$T_{v\_off} = \frac{T_p}{2}(3 + \mathbf{c}) \; ; \; T_{w\_off} = \frac{T_p}{2}(3 - \mathbf{c})$$
$$(2.15)$$

3. Sector 3:

$$T_{u\_on} = \frac{T_p}{2}(1 + \mathbf{a}) \; ; \; T_{v\_on} = \frac{T_p}{2}(1 - \mathbf{a}) \; ; \; T_{w\_on} = \frac{T_p}{2}(1 - \mathbf{b} + \mathbf{c})$$
$$T_{u\_off} = \frac{T_p}{2}(3 - \mathbf{a}) \; ; \; T_{v\_off} = \frac{T_p}{2}(3 + \mathbf{a}) \; ; \; T_{w\_off} = \frac{T_p}{2}(3 + \mathbf{b} - \mathbf{c}) \quad (2.16)$$

4. Sector 4:

$$T_{u\_on} = \frac{T_p}{2}(1 + \mathbf{a}) \; ; \; T_{v\_on} = \frac{T_p}{2}(1 - \mathbf{b} + \mathbf{c}) \; ; \; T_{w\_on} = \frac{T_p}{2}(1 - \mathbf{a})$$
$$T_{u\_off} = \frac{T_p}{2}(3 - \mathbf{a}) \; ; \; T_{v\_off} = \frac{T_p}{2}(3 + \mathbf{b} - \mathbf{c}) \; ; \; T_{w\_off} = \frac{T_p}{2}(3 + \mathbf{a}) \quad (2.17)$$

5. Sector 5:

$$\text{Quadrant 3}: \; T_{u\_on} = \frac{T_p}{2}(1 + \mathbf{a} + \mathbf{b}) \; ; \; T_{u\_off} = \frac{T_p}{2}(3 - \mathbf{a} - \mathbf{b})$$
$$\text{Quadrant 4}: \; T_{u\_on} = \frac{T_p}{2}(1 - \mathbf{a} - \mathbf{b}) \; ; \; T_{u\_off} = \frac{T_p}{2}(3 + \mathbf{a} + \mathbf{b})$$
$$T_{v\_on} = \frac{T_p}{2}(1 + \mathbf{c}) \; ; \; T_{w\_on} = \frac{T_p}{2}(1 - \mathbf{c})$$
$$T_{v\_off} = \frac{T_p}{2}(3 - \mathbf{c}) \; ; \; T_{w\_off} = \frac{T_p}{2}(3 + \mathbf{c})$$
$$(2.18)$$

6. Sector 6:

$$T_{u\_on} = \frac{T_p}{2}(1 - \mathbf{a}) \; ; \; T_{v\_on} = \frac{T_p}{2}(1 + \mathbf{a}) \; ; \; T_{w\_on} = \frac{T_p}{2}(1 + \mathbf{b} - \mathbf{c})$$

$$T_{u\_off} = \frac{T_p}{2}(3 + \mathbf{a}) \; ; \; T_{v\_off} = \frac{T_p}{2}(3 - \mathbf{a}) \; ; \; T_{w\_off} = \frac{T_p}{2}(3 - \mathbf{b} + \mathbf{c}) \quad (2.19)$$

Using these equations provides an easily comprehensible realization of the space vector modulation following the control flow of the structogram of Fig. 2.12. The afore mentioned limitation to the maximum voltage vector should be already carried out in the current controller because of the necessary feedback correction discussed later. The normalization of the voltage components to $2U_{DC}/3$ permits the calculation of the switching times independent of the motor nominal voltage.

2.4.2 Modulation with Digital Signal Processor TMS 320C20/C25

Unlike the Siemens microcontroller the digital signal processor is not equipped with the intelligent Capture/Compare register unit, but provides a superior computing power instead. In principle, there are two possibilities for the realization of the space vector modulation.

1. Using additional hardware: The processor is extended by a latch-counter-unit providing the process interface to the inverter (refer to Fig. 2.15).
2. Without additional hardware: The internal processor timer is used to generate the pulse pattern.

Since the 2nd variant causes certain disadvantages, such as an inaccurate voltage realization, particularly at the sector boundaries as well as in the area of small stator voltage (important for the low speed region), the 1st variant (following the realization with microcontroller) is discussed first. Figure 2.15 illustrates the hardware configuration. Figure 2.16 shows, representative of the complete vector space, the definition and respectively the assignment of the turn-on/turn-off times to the inverter legs.

According to the definition the switching times of the sampling period (k) can be calculated and stored in a RAM table. In the next period $(k + 1)$ they are output half-pulse wise. Computing and output of the switching times are processed in a time frame with the fixed period $T_p/2$, which is provided by either the internal timer of the signal processor or possibly also by the master-processor in the case of a multi-processor system. At the synchronization instants the switching times for the actual half pulse are automatically transferred from the latches to the down-counters, giving way to write the switching times for the next half pulse from the RAM table into the latch. Thus, output of the switching times independent of the interrupt

Fig. 2.15 Hardware configuration using DSP with external down-counter
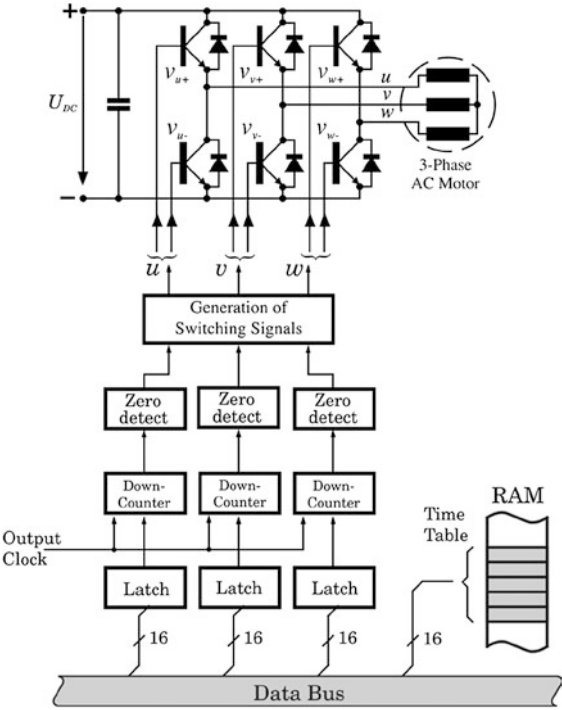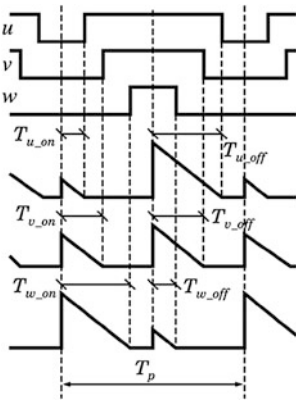

Fig. 2.16 Definition of the turn-on and turn-off times in the version DSP with additional hardware

reaction time is achieved, which results in a very precise voltage realization particularly in the area of small voltage values. After having been loaded with the switching times the counter starts to count backwards. Once the counter reading is zero, a zero detector will generate turn-on/turn-off pulses to control the inverter.

According to the definition in the Fig. 2.16, Eq. (2.2) and Table 2.3 the switching times can be calculated as follows.

1. Sector 1:

$$T_{u\_on} = T_{w\_off} = \frac{T_p}{2}(1 - \mathbf{a}) \; ; \;\; T_{u\_off} = T_{w\_on} = \frac{T_p}{2}(1 + \mathbf{a})$$
$$T_{v\_on} = \frac{T_p}{2}(1 + \mathbf{b} - \mathbf{c}) \; ; \;\; T_{v\_off} = \frac{T_p}{2}(1 - \mathbf{b} + \mathbf{c})$$

(2.20)

2. Sector 2:

$$\text{Quadrant 1} : \; T_{u\_on} = \frac{T_p}{2}(1 - \mathbf{a} - \mathbf{b}) \; ; \;\; T_{u\_off} = \frac{T_p}{2}(1 + \mathbf{a} + \mathbf{b})$$
$$\text{Quadrant 2} : \; T_{u\_on} = \frac{T_p}{2}(1 + \mathbf{a} + \mathbf{b}) \; ; \;\; T_{u\_off} = \frac{T_p}{2}(1 - \mathbf{a} - \mathbf{b})$$
$$T_{v\_on} = T_{w\_off} = \frac{T_p}{2}(1 - \mathbf{c}) \; ; \;\; T_{v\_off} = T_{w\_on} = \frac{T_p}{2}(1 + \mathbf{c})$$

(2.21)

3. Sector 3:

$$T_{u\_on} = T_{v\_off} = \frac{T_p}{2}(1 + \mathbf{a}) \; ; \;\; T_{u\_off} = T_{v\_on} = \frac{T_p}{2}(1 - \mathbf{a})$$
$$T_{w\_on} = \frac{T_p}{2}(1 - \mathbf{b} + \mathbf{c}) \; ; \;\; T_{w\_off} = \frac{T_p}{2}(1 + \mathbf{b} - \mathbf{c})$$

(2.22)

4. Sector 4:

$$T_{u\_on} = T_{w\_off} = \frac{T_p}{2}(1 + \mathbf{a}) \; ; \;\; T_{u\_off} = T_{w\_on} = \frac{T_p}{2}(1 - \mathbf{a})$$
$$T_{v\_on} = \frac{T_p}{2}(1 - \mathbf{b} + \mathbf{c}) \; ; \;\; T_{v\_off} = \frac{T_p}{2}(1 + \mathbf{b} - \mathbf{c})$$

(2.23)

5. Sector 5:

$$\text{Quadrant 3} : \; T_{u\_on} = \frac{T_p}{2}(1 + \mathbf{a} + \mathbf{b}) \; ; \;\; T_{u\_off} = \frac{T_p}{2}(1 - \mathbf{a} - \mathbf{b})$$
$$\text{Quadrant 4} : \; T_{u\_on} = \frac{T_p}{2}(1 - \mathbf{a} - \mathbf{b}) \; ; \;\; T_{u\_off} = \frac{T_p}{2}(1 + \mathbf{a} + \mathbf{b})$$
$$T_{v\_on} = T_{w\_off} = \frac{T_p}{2}(1 + \mathbf{c}) \; ; \;\; T_{v\_off} = T_{w\_on} = \frac{T_p}{2}(1 - \mathbf{c})$$

(2.24)

6. Sector 6:

$$T_{u\_on} = T_{v\_off} = \frac{T_p}{2}(1 - \mathbf{a}) \; ; \;\; T_{u\_off} = T_{v\_on} = \frac{T_p}{2}(1 + \mathbf{a})$$
$$T_{w\_on} = \frac{T_p}{2}(1 + \mathbf{b} - \mathbf{c}) \; ; \;\; T_{w\_off} = \frac{T_p}{2}(1 - \mathbf{b} + \mathbf{c})$$

(2.25)

The shown variant with additional hardware fulfils highest requirements regarding the precision of the voltage realization. The additional hardware costs are faced by a time resolution, which is practically limited only by the word length of the three counters and their clock frequency.

With regard to a very exact and dynamic feedback control this solution has to be preferred to the one with microcontroller if one considers that the controller has a maximum time resolution of only 400 ns (with hardware expansion also 200 ns possible). This time resolution permits a voltage resolution of only 7 bits at a pulse frequency of 10 kHz (approx. 4 V/time increment) and a resolution of 8 bits at 5 kHz (approx. 2 V/time increment). This is a rather coarse resolution. In contrast to this, a time resolution of 50 ns corresponding to a voltage resolution of 10 bits (approx. 0.5 V/time increment) can easily be achieved, which requires just the use of counters with 10 bit word length and 10 MHz clock frequency. Another drawback of the microcontroller solution is due to the fact that the CAP/COM registers of the SAB 80C166 cannot be switched simultaneously because they are subject to a skew of 50 ns from register to register. This necessitates a hardware-based compensation to attain a high precision of the voltage realization. Such a compensation is particularly important at the sector boundaries as well as in the area of small voltages or small speeds.

For the DSP solution, the version without additional hardware offers itself as an alternative possibility. The switching times are generated using the only internal timer. Figure 2.17 shows the used hardware. Figure 2.18 shows the time frame, in which the switching time calculation as well as their output are processed. As familiar, the switching times are calculated and stored into a RAM table already in the period (k) for the following period ($k + 1$). The difference, compared with the two previous solutions, consists in the switching times not being output to the inverter separately for every phase in the form of T_{on} and T_{off}, but in original form as T_r, T_l or $T_{0,7}$ together with the needed switching state. The respective switching state is sent as a 3 bit data block to a buffer latch ahead of the inverter which holds it for the complete period.

From Fig. 2.18 it becomes evident, that two information are relevant about the modulation: the switching time and the switching state. These information are determined using Table 2.3 and the flow chart in the Fig. 2.12, depending on the sector the voltage vector is located in. The hold time of the switching state was fetched from the RAM table and loaded into the period register PRD before. The timer counts backwards and when reaching zero activates the automatic loading of the new time constant from the PRD into its own counter register. At the same time, it triggers an interrupt request Tint, which activates an interrupt routine for handing over the following switching state (pulse pattern) into the latch as well as reloading the PRD.

To output the switching states the following simple algorithm can be used. If again the Fig. 2.18 for the sector S_1 is viewed as an example the following assignment table can be composed.

Fig. 2.17 Hardware
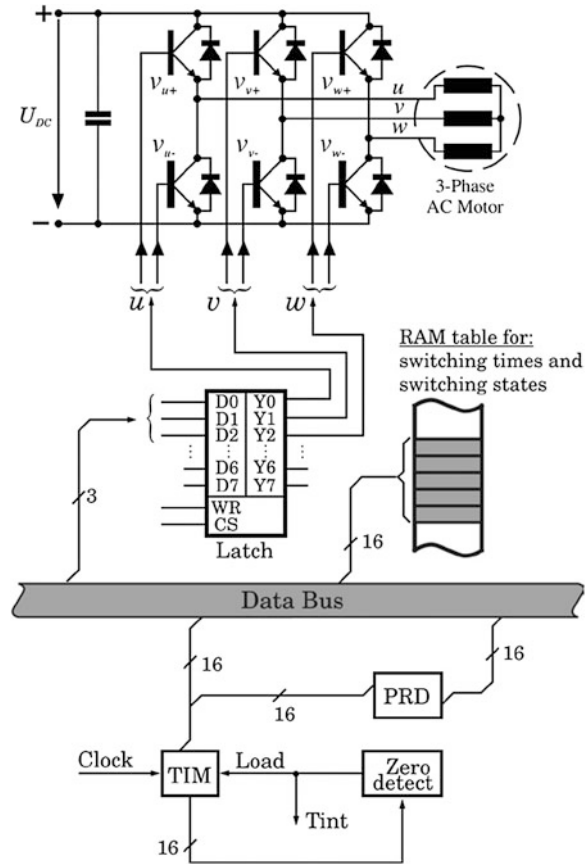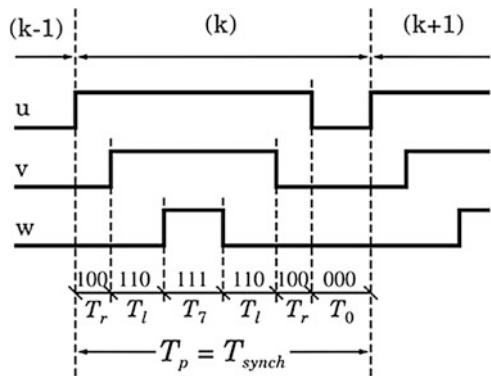configuration using DSP with
its internal timer TIM

Fig. 2.18 Modulation time
frame of the solution without
additional hardware

Switching times	T_r	T_l	T_7	T_l	T_r	T_0
Switching states	100	110	111	110	100	000

The phases u, v and w are assigned to the data bits D0, D1 and D2. If the switching states of the above table are now written in reversed order

$$000/001/011/111/011/001,$$

a so-called control word (CW) results with CW = 17D9 h as a hexadecimal number. The control words for all six sectors can be summarized like in Table 2.4.

The control word, corresponding to the determined sector is loaded by the interrupt routine from the memory into the accumulator, submitted to the latch, shifted three times to the right (to remove the switching state), and then stored back into the RAM. Every time after the control word has arrived in the accumulator, a zero test is carried out. The value zero indicates a new control word for the next sampling period. The described handling of the control words is illustrated again by the flow chart in Fig. 2.19.

Some disadvantages of this method shall be mentioned now. Figure 2.17 is redrawn for two extreme cases:

1. the areas of small voltages at the sector boundaries, and
2. the area of voltage limitation (refer to Fig. 2.20).

Changing the switching states by means of an interrupt routine reacting to T_{int} implies that the interval between two changes must be longer than the interrupt reaction time and respectively the run time of the interrupt routine itself. Figure 2.20 (refer to Fig. 2.7) shows for sector S_1 that:

1. near the sector boundaries one of the two times T_r or T_l, and
2. in case of small voltages both times T_r and T_l

may fall below the reaction time of the interrupt routine. In the 1st case the boundary vector with the smaller switching time must be suppressed, and the second one will be realized for the whole period instead. This, of course, causes an inaccuracy of the voltage realization. In the 2nd case the voltage amplitude in the vicinity of zero is limited on the lower end, which has a negative effect on the speed control at small speeds.

At large voltage amplitudes or during transients (magnetization, field-weakening, speed-up, speed reversal) the zero times T_0 and T_7 can become very small, and also fall below the reaction time of the interrupt routine (Fig. 2.20 right). This means a limitation of the voltage amplitude on its upper end.

Table 2.4 Control words of all sectors

Sectors	S_1	S_2	S_3	S_4	S_5	S_6
Control words	17D9 h	27DA h	2DF2 h	4DF4 h	4BEC h	1BE9 h

Fig. 2.19 Flow chart of the interrupt routine to output switching times and switching states
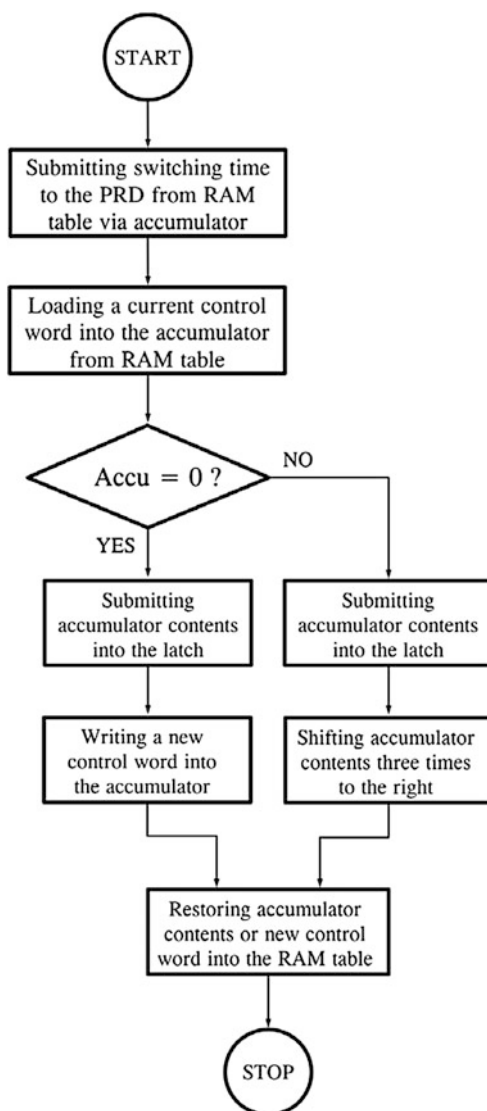
2.4.3 Modulation with Double Processor Configuration

In this section a double processor system is introduced combining harmonically the strength of the digital signal processor TMS 320C25—with respect to computing power—with the strength of the microcontroller SAB C167—with respect to peripheries.

In this configuration the DSP is responsible for the processing of the near-motor control functions, and the µC has to process the tasks of the superposed
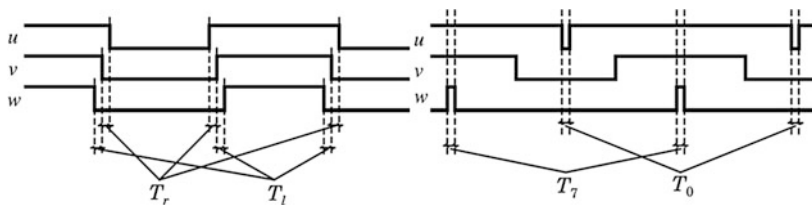
Fig. 2.20 Switching times at sector boundaries, in the area of small voltage (*left*) or of voltage at upper limits (*right*)

control loops. The DSP allows to calculate the extensive real-time algorithms, part of which is also the space vector modulation within a small sampling time of 100–200 µs. In every sampling period the DSP stores the newly calculated switching times into its own RAM, they are read from the µC memory driver using HOLD/HOLDA signals and submitted to the µC-internal PWM units. That means, with respect to the modulation the µC is only responsible for the output of the switching times and for the control of the transistor legs (Fig. 2.21).

The microcontroller SAB C167 contains, different to the earlier SAB 80C166, four timers PT0…PT3. In the symmetrical modulation mode these timers work as up/down counters. After every forward and the following backward counting process, when the counter content has reached the value zero, the timer/counter automatically receives the new maximum counter content from one of the four period registers PP0…PP3 for the new counting period. For the modulation only three registers of each category are needed (Fig. 2.22). It can be easily recognized that the three registers PP0, PP1 and PP2 have to get the same value simultaneously

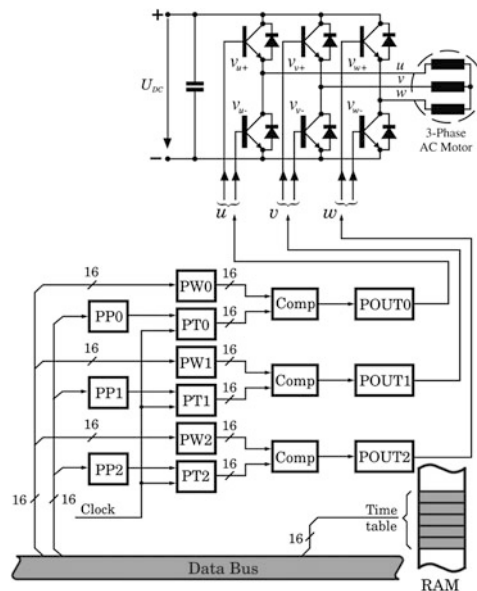**Fig. 2.21** Overview of the double processor configuration DSP—µC
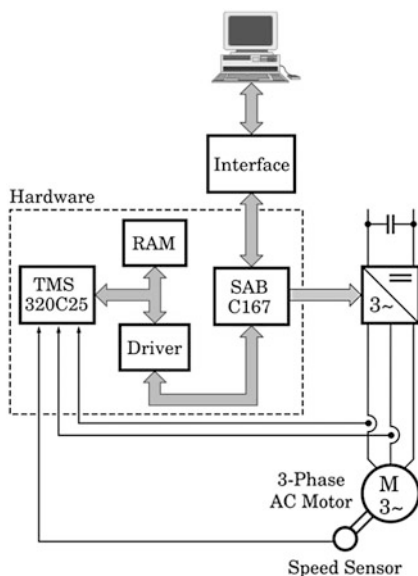
Fig. 2.22 Simplified structure of the modulation registers of the SAB C167

to realize the same counting or modulation periods. Furthermore it can be easily recognized that these three registers have to be initialized only once with the value $T_p = 1/f_p$ because of the constant pulse frequency f_p.

In comparison with the SAB 80C166 the registers PT0, PT1, PT2 play the role of T0, and the registers PP0, PP1, PP2 the role of T0REL (refer to Fig. 2.13). The registers PW0, PW1 and PW2 generate the pulse widths. The assignment of the registers to the transistor legs is shown in the Fig. 2.22.

While PT0, PT1 and PT2, which are represented as PWM timers in Fig. 2.23, are counting forwards and backwards, their values are permanently compared with the
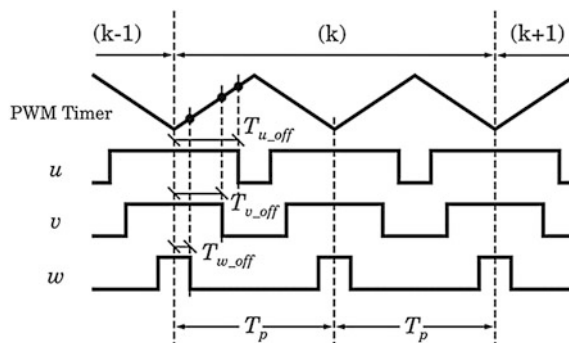

Fig. 2.23 Definition of the switching times for the structure in the Fig. 2.22

contents of the corresponding pulse width registers PW0, PW1 and PW2. Respective compare-match events cause the output ports POUT0, POUT1, POUT2 to toggle and in due course the switchover of the corresponding inverter legs.

Figure 2.23 shows that the pulse width registers PW0, PW1 and PW2 have to be reloaded with new switching times, for turn-on and turn-off, only once per modulation period. The switching times can be calculated according to the definition in Fig. 2.23 as follows.

1. Sector 1:

$$T_u = \frac{T_p}{2}(1 + \mathbf{a}) \; ; \; \; T_v = \frac{T_p}{2}(1 - \mathbf{a} + 2\mathbf{c}) \; ; \; \; T_w = \frac{T_p}{2}(1 - \mathbf{a}) \qquad (2.26)$$

2. Sector 2:

$$\text{Quadrant 1}: \; T_u = \frac{T_p}{2}(1 + 2\mathbf{b} + \mathbf{c}) \; ; \; \; \text{Quadrant 2}: \; T_u = \frac{T_p}{2}(1 - 2\mathbf{a} + \mathbf{c})$$

$$T_v = \frac{T_p}{2}(1 + \mathbf{c}) \; ; \; \; T_w = \frac{T_p}{2}(1 - \mathbf{c}) \qquad (2.27)$$

3. Sector 3:

$$T_u = \frac{T_p}{2}(1 - \mathbf{a}) \; ; \; \; T_v = \frac{T_p}{2}(1 + \mathbf{a}) \; ; \; \; T_w = \frac{T_p}{2}(1 + \mathbf{a} - 2\mathbf{c}) \qquad (2.28)$$

4. Sector 4:

$$T_u = \frac{T_p}{2}(1 - \mathbf{a}) \; ; \; \; T_v = \frac{T_p}{2}(1 + \mathbf{a} - 2\mathbf{c}) \; ; \; \; T_w = \frac{T_p}{2}(1 + \mathbf{a}) \qquad (2.29)$$
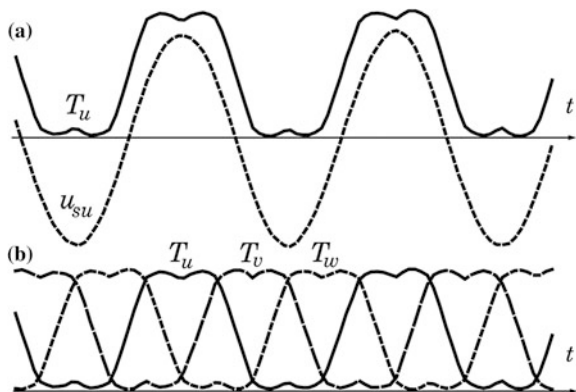
5. Sector 5:

$$\text{Quadrant 3}: \; T_u = \frac{T_p}{2}(1 - 2\mathbf{a} + \mathbf{c}) \; ; \; \; \text{Quadrant 4}: \; T_u = \frac{T_p}{2}(1 + 2\mathbf{b} + \mathbf{c})$$

$$T_v = \frac{T_p}{2}(1 - \mathbf{c}) \; ; \; \; T_w = \frac{T_p}{2}(1 + \mathbf{c}) \qquad (2.30)$$

6. Sector 6:

$$T_u = \frac{T_p}{2}(1 + \mathbf{a}) \; ; \; \; T_v = \frac{T_p}{2}(1 - \mathbf{a}) \; ; \; \; T_w = \frac{T_p}{2}(1 - \mathbf{a} + 2\mathbf{c}) \qquad (2.31)$$

To complete the chapter of the realization examples the Fig. 2.24 shows the switching time plots, produced by the structure in Fig. 2.22, at large voltages. This may be easily recognized by the fact that the switching times also show values near zero.

Fig. 2.24 The phase voltage u_{su} with the corresponding switching time T_u (*top*), and the switching times T_u, T_v, T_w (*bottom*)

2.5 Special Modulation Procedures

2.5.1 Modulation with Two Legs

Starting point for this section is Fig. 2.10, which represents the standard modulation in a stable time frame. The standard modulation realizes the same voltage vector, which is determined by the lengths of its boundary vector times T_r, T_l, twice per pulse period. For the purpose of comparison it is represented again for the sector S_1 in Fig. 2.25a.

We will try now to combine the zero times T_0, T_7 such that their sum is output either equally distributed at the ends (Fig. 2.25b) or concentrated in the center (Fig. 2.25c) of the pulse period. The times T_r, T_l or the voltage vector to be realized remain unchanged. With respect to the mean average value the two new sequences realize the same vector as in Fig. 2.25a.

It is obvious in the newly arisen sequences, that only two inverter legs are actually switched over. If this method, which will be called *modulation with two legs* from now on, is used consistently for the whole vector space, then *the switching losses automatically go down to approx. 2/3 of the original value*.

From the Fig. 2.25b, c it becomes obvious that either *the phase with the smallest pulse width* (for S_1: phase w) or *the phase with the smallest pause time* (for S_1: phase u) would be clamped to *negative potential* (the lower transistor of a phase leg is conducting) or to *positive potential* (the upper transistor is conducting). The formulae for the calculation of the switching times depend on the hardware and can be derived according to the definition from Sect. 2.4.

With the help of the firing pulse patterns in Fig. 2.5a–e, the suitable clamping phases or transistor legs can be found for all sectors and are summarized in the table in Fig. 2.26. For each sector two phases are available alternatively.

To obtain the same switching losses for all transistors, the upper transistor of one leg (corresponding phase on +) and then the lower transistor of the next leg
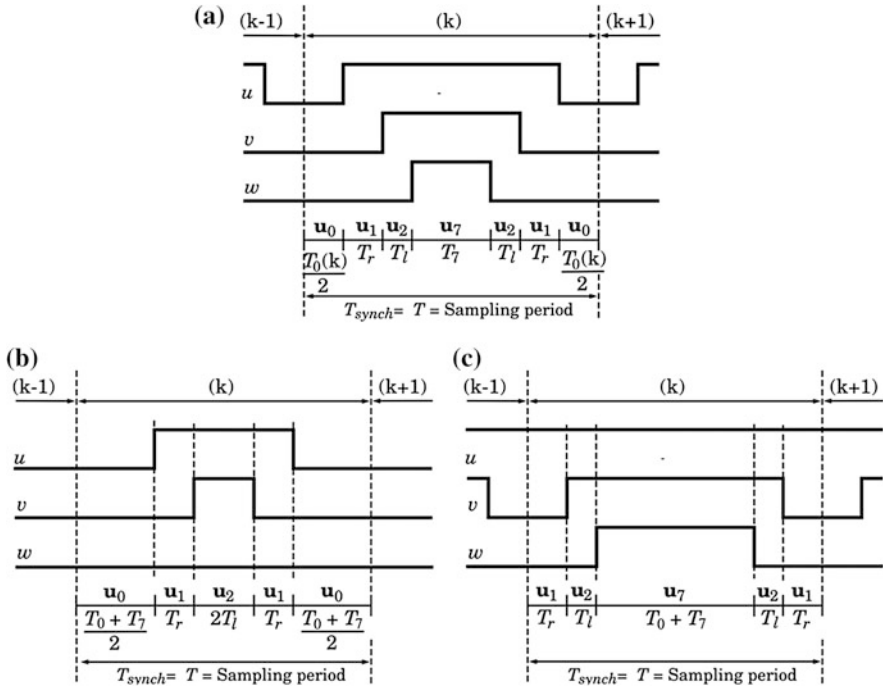
Fig. 2.25 Modulation with two legs for sector S_1

(corresponding phase on $-$) are alternately switched on permanently for an angular range of 60°. To switch-over the clamping to the next phase,

1. either the sector boundaries (Fig. 2.26b),
2. or the middle points of the sectors (Fig. 2.26c)

can be used. For all variants every transistor of the inverter conducts only for 60° per rotation of the voltage vector. With regard to the switching time calculation, which already requires a sector selection (refer to Table 2.3), the version shown in Fig. 2.26b, seems to be more suitable for the practical implementation compared to the one in Fig. 2.26c.

The advantage of the lower switching losses, however, is faced by considerably higher current harmonics, about twice the ripple amplitude has to be expected compared to the standard PWM algorithm.

2.5.2 Synchronous Modulation

For the modulation algorithms discussed so far, it was always assumed that the pulse period T_p or the pulse frequency $f_p = 1/T_p$ is kept constant. However, since the
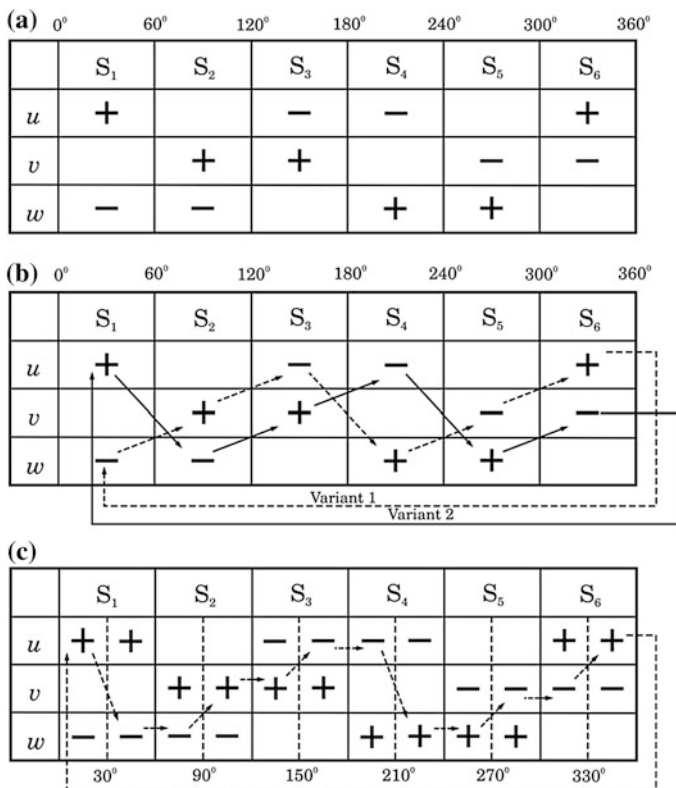
(a)

	0° 60°	120°	180°	240°	300°	360°
	S_1	S_2	S_3	S_4	S_5	S_6
u	+		−	−		+
v		+	+		−	−
w	−	−		+	+	

(b)

	0° 60°	120°	180°	240°	300°	360°
	S_1	S_2	S_3	S_4	S_5	S_6
u	+		−	−		+
v		+	+		−	−
w	−	−		+	+	

Variant 1
Variant 2

(c)

	S_1	S_2	S_3	S_4	S_5	S_6
u	+ +		− −	−		+ +
v		+ + + +			− − −	
w	− −	− −		+ + + +		
	30°	90°	150°	210°	270°	330°

Fig. 2.26 Possibilities of modulation with two legs: possible phases for clamping per sector (**a**), and ways to switchover the clamped phases (**b**, **c**)

fundamental frequency or the stator frequency f_s of the driven motor depends on the speed as well as on the load and is therefore variable, the relationship f_p/f_s is not constant. In this case one speaks of *asynchronous modulation*. The pulse period and the fundamental voltage period are not in any fixed relation.

This asynchronous characteristic causes subharmonics and losses as well as torque oscillations, which do not play an important role, as long as the relationship f_p/f_s is sufficiently large. The negative influence of the asynchronous characteristic may become a significant problem for high-speed drives (centrifuges, vacuum pumps etc.) in the speed range of 30,000–60,000 rpm. This problem can be avoided by keeping f_p and f_s in a fixed relationship.

$$N = \frac{f_p}{f_s} = const$$

$$T_p = \frac{1}{f_p} = \frac{1}{N f_s} = const$$

(2.32)

N is the number of the pulse periods per fundamental wave and may assume—because of the three-phase symmetry of the machines—only values, which fit the following relationship.

$$N = 9 + 6n \quad n = 0, \ 1, \ 2, \ 3, \ \ldots$$
$$N = 9, \ 15, \ 21, \ 27, \ \ldots$$

$$(2.33)$$

In principle the modulation is processed in the same way as for the asynchronous algorithm, only, that the length of the pulse period T_p—depending on the working frequency f_s—must be recalculated permanently. It has to be taken into account for the practical implementation, that the value of the period register cannot be changed during the current pulse period, although the new value is already available after the recalculation is finished. This requires a *double buffering of the period register*. However, not every microcontroller will have the ability of double buffering. Regarding this feature the SAB C167 is very recommendable because the registers PP0, PP1, PP2 and PP3 are doubly buffered[2] by the so-called "*shadow register*".

The following problems must be taken into account for the application of the method:

1. Switching over of the pulse number N is carried out depending on the working (fundamental) frequency, and a *hysteresis—to prevent continuous to—and from-switching*—must be installed.
2. Switching over of the pulse number N as well as switching over between asynchronous and synchronous modulation *must—to reduce transient effects—take place at the sector boundaries* where one of the phase voltages u_{su}, u_{sv} and u_{sw} reaches its peak value. At the sector boundaries the current harmonics pass through their zero crossings.

2.5.3 Stochastic Modulation

In this chapter we shall take a closer look at the switching frequency harmonics produced by the modulation and discuss certain ways to take influence on their appearance. Typical spectra of inverter voltage and current for the standard modulation with fixed pulse width are shown in Fig. 2.27. Their shape depends on the modulation ratio $m = |\mathbf{u}_s|/u_{\max}$ and in case of the current on the load characteristic.

The spectra show pronounced maxima at the pulse frequency and its multiples with the overall maximum at the 2nd harmonic. Because of the low-pass characteristic of the load (R–L) harmonics beyond the 4th are suppressed in the current. Depending on the application and performance requirements, both positive and negative effects arise from this kind of spectrum:

---

[2]Note: This ability is a further development of the SAB C167 in newer versions. The SAB C167 in the first version does not have double buffering for period registers.
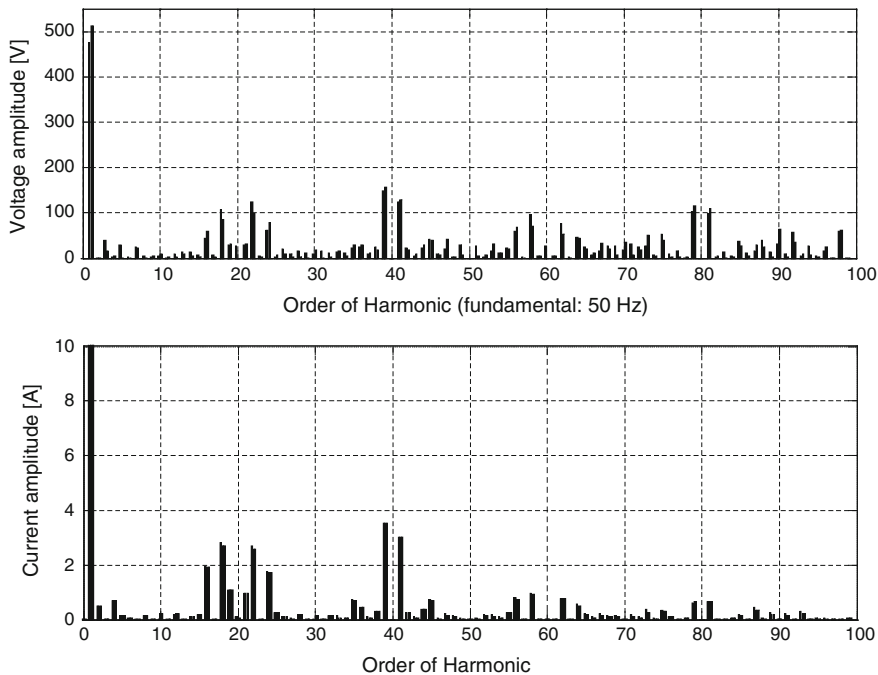
Fig. 2.27 Voltage (*top*) and current (*bottom*) spectra for standard modulation with m = 0.4 and pulse frequency = 1.0 kHz; current fundamental is truncated!

- Below the switching frequency and its sidebands appear only low harmonic amplitudes and consequently their effect on ripple control frequencies in grid applications (active front-end converters) is negligible.
- The maximum harmonic current amplitudes are concentrated around two specific frequencies (1st and 2nd order), which facilitates filtering.
- Especially for grid applications, the maxima at 1st and 2nd switching frequency harmonic may exceed the limits specified in the applicable grid codes, which requires additional filtering for their suppression.
- The pronounced single-frequency harmonics produce acoustical noise which may be unwanted and experienced as disturbing in many environments.

To overcome the mentioned negative effects, it would in the first place be necessary to get rid of the pronounced 1st and 2nd harmonics and to obtain a more uniformly distributed spectrum. A straightforward solution could be to elude to control strategies with variable pulse period, such as bang-bang control, predictive control or direct torque/flux control. This is however outside the scope of this book, since we want to rely on the current control procedures to be discussed in the later chapters. So the question is how we can achieve a distributed spectrum while keeping a constant pulse period at the same time.

To derive respective procedures, it is first necessary to take a closer look on how the harmonic frequencies originate. Figure 2.28 shall help to do this. In both phase voltage and inverter control signals two repeating patterns may be identified:

1. The first pattern is formed by the ever repeating sequence of zero and active vectors … 0-R-L-7-7-L-R-0 … which appears with switching frequency and multiples of it.
2. The second one is formed by regular blocks of the active vectors R and L which are interrupted by zero vectors 0/7 with symmetric distribution within one period. This pattern is responsible for the especially strong 2nd harmonic in the spectrum and its multiples.
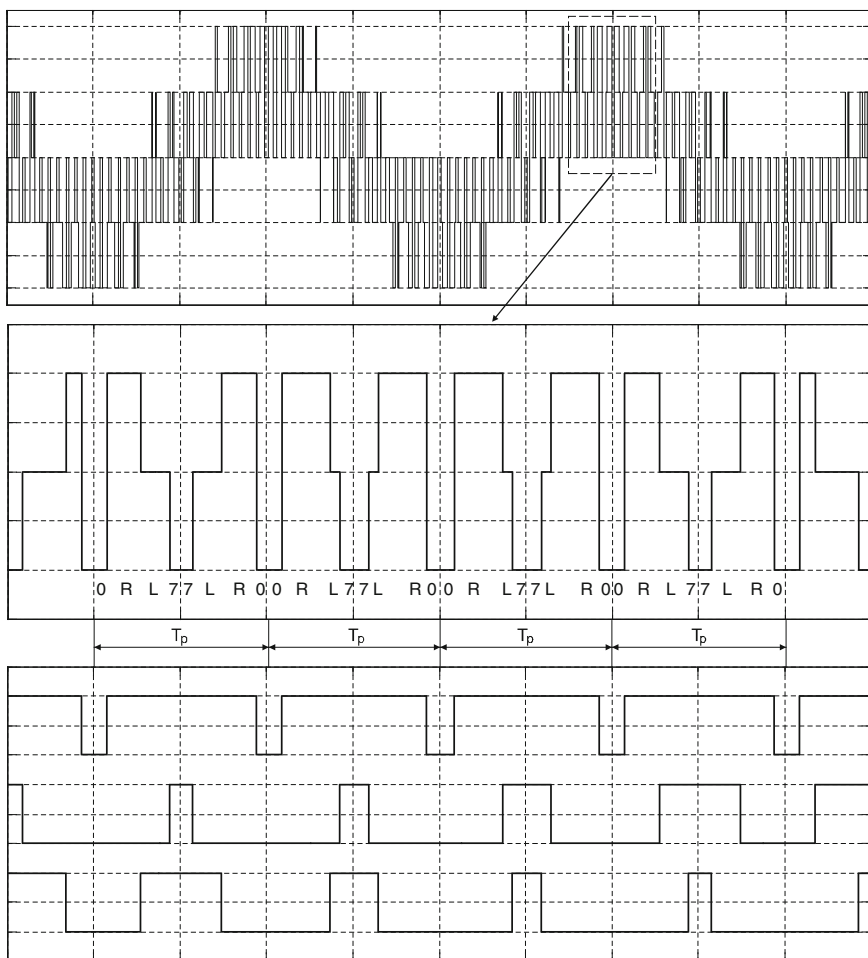

Fig. 2.28 Switching pattern of phase voltage (*top*, *center*) and phase control signals *u/v/w* (*bottom*) for standard modulation

To shape a distributed spectrum, the regularity of these patterns has to be overcome, we have to "break the symmetries". Two methods shall be discussed to achieve this task.

The first approach, "sequence randomizing", breaks the first symmetry pattern by randomly changing the start vector of the pulse period between 0 and 7. This implies to add an additional simultaneous switchover of all three phase legs at the beginning of the pulse period. The start vector for each period is determined by a pseudo-random binary sequence (PRBS) which can easily be generated in a microcontroller. The resulting pulse patterns and spectra are shown in Figs. 2.29 and 2.30.

The described change of the vector sequence occurs in the example between first and second pulse period in Fig. 2.29. The peak value of the first harmonic is clearly reduced but, since nothing is changed on the zero vector lengths, the second symmetry pattern and therefore the second harmonic remain largely unaffected.

The 2nd harmonic is addressed with a different approach, which we will call "zero vector randomizing". The symmetrical distribution of u_0 and u_7 inside one period in the standard modulation scheme is dropped in favor of a randomly chosen ratio between both vectors, while keeping their symmetry with regard to the center of the pulse period. The latter is an important condition to maintain the coincidence between sampling instant of the phase current and the current fundamental (refer to Chap. 4.1). With an uniformly distributed random number $r(k)$ where $0 \leq r(k) \leq 1$
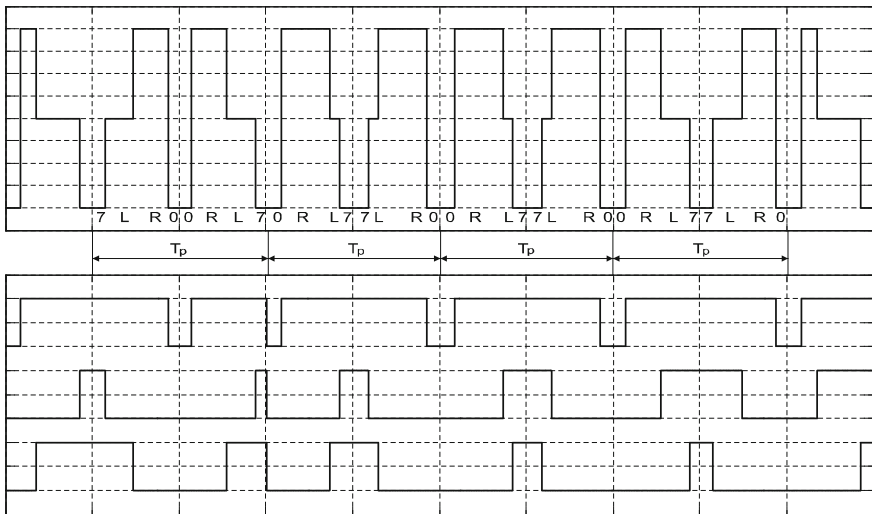

Fig. 2.29 Switching pattern of phase voltage (*top*) and phase control signals *u/v/w* (*bottom*) for modulation with sequence randomizing
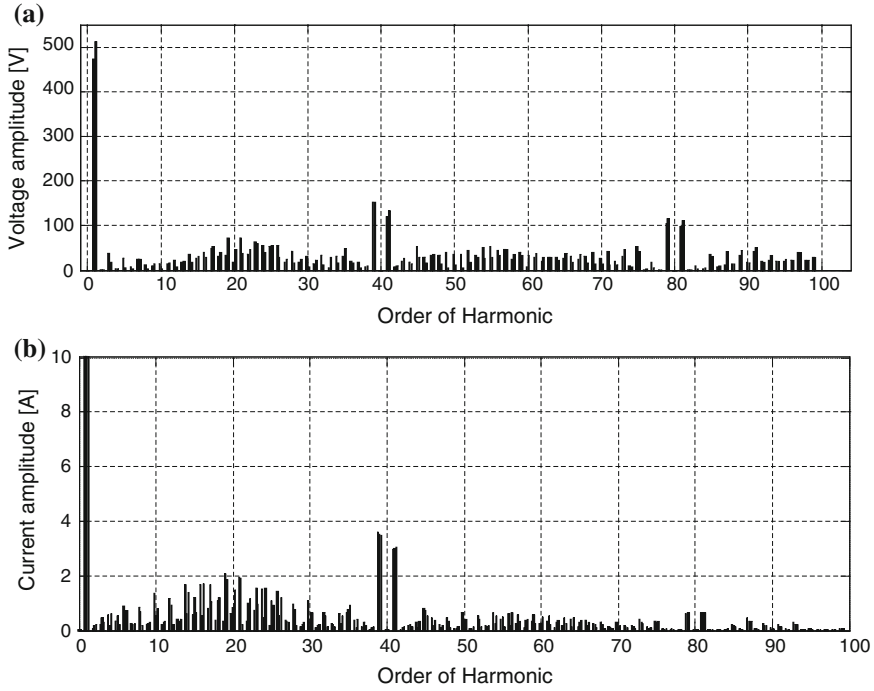
(a)

(b)

Fig. 2.30 Voltage (*top*) and current (*bottom*) spectra for modulation with sequence randomizing

and the original zero vector time T_{00}, the resulting zero vector times can be calculated from:

$$
\begin{aligned}
T_0 &= r(k)T_{00} \\
T_7 &= (1 - r(k))T_{00}
\end{aligned}
\tag{2.34}
$$

As it turns out in the practical implementation, the results become more impressive when the extremes of the $r(k)$ interval {0; 1} are stronger emphasized, i.e. $r(k)$ is calculated by:

$$
\begin{aligned}
&r(k) = k_r(r_1(k) - 0.5) + 0.5 \\
&k_r = 2, 3, \ldots, 8 \\
&0 \leq r(k) \leq 1 \\
&0 \leq r_1(k) \leq 1 \text{ an uniformly distributed random number}
\end{aligned}
\tag{2.35}
$$

It must be mentioned, that the effectiveness of zero vector randomizing of course depends on the modulation ratio $m = |\mathbf{u}_s|/u_{\max}$, since m determines the available space for the zero vector variation. Near the maximum voltage vector the effect will be minimal.
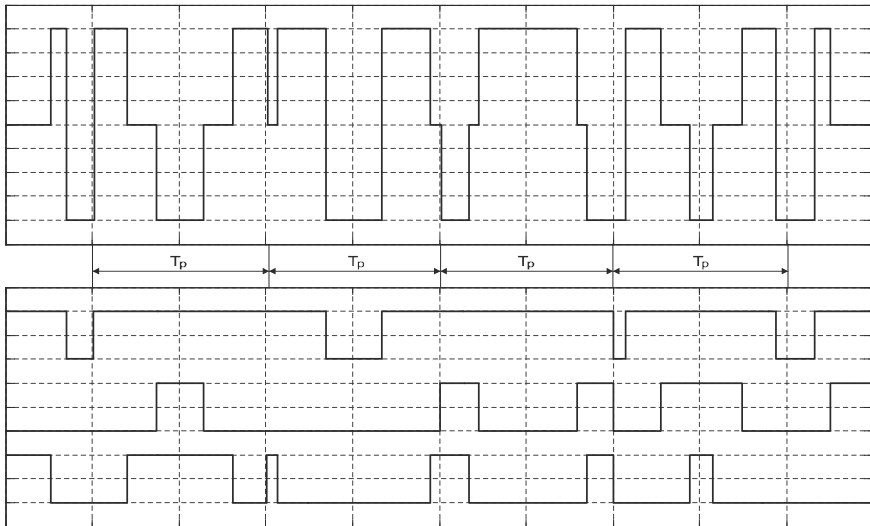
Fig. 2.31 Switching pattern of phase voltage (*top*) and phase control signals *u/v/w* (*bottom*) for modulation with combined sequence randomizing and zero vector randomizing

It must also be noted, that the total harmonic current, and therefore the total harmonic distortion (THD) value cannot essentially be changed by modifying the modulation scheme. Thus, reducing harmonics in one area of the spectrum inevitably will shift them to and increase them in another area.

Figures 2.31 and 2.32 again show resulting sample pulse patterns and spectra, both figures for combined sequence randomizing and zero vector randomizing and at the same operating point as in the figures above.

2.6 Degrees of Freedom in Modulation

Jenni and Wüest (1995, Sect. 8.2), has introduced the concept of "*degrees of freedom*" as a general description of the voltage vector modulation. There are three degrees of freedom:

1. The voltage vector $\mathbf{u}_s$ can be created from different combinations of component vectors (logic states in Table 2.1).
2. During modulation, the sequences of component vectors can be selected differently.
3. The zero voltages can be created by use of one or both of zero vectors $\mathbf{u}_0$ and $\mathbf{u}_7$.

These three degrees of freedom are the tool to change the modulation strategies, aiming to reach the specific technical performance.
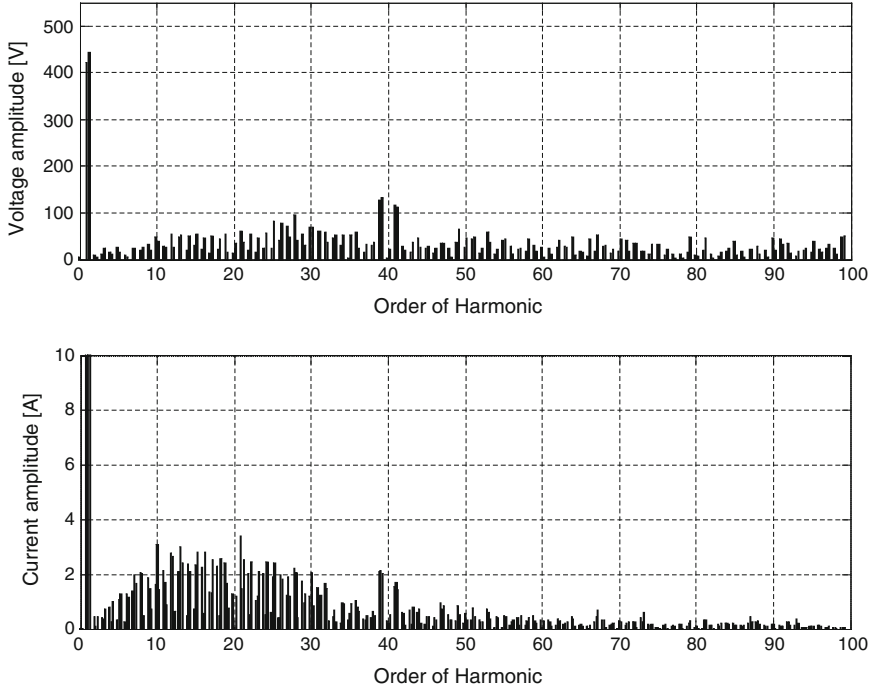
Fig. 2.32 Voltage (*top*) and current (*bottom*) spectra for modulation with combined sequence randomizing and zero vector randomizing

### 2.6.1 Modulation with Different Combinations of Component Vectors

The first degree of freedom is explained by the Fig. 2.33. In this example the voltage vector $\mathbf{u}_s$ is replaced by the following combination:

$$\mathbf{u}_s = \mathbf{u}_{a1} + \mathbf{u}_{c1} + \mathbf{u}_{a2} + \mathbf{u}_{c2} + \mathbf{u}_b \tag{2.36}$$

Following the approach of (2.3), (2.36) can be extended to:

$$
\begin{aligned}
\mathbf{u}_s &= \mathbf{u}_{a1} + \mathbf{u}_{c1} + \mathbf{u}_{a2} + \mathbf{u}_{c2} + \mathbf{u}_b + \mathbf{u}_0 \ (\text{or } \mathbf{u}_7) \\
&= \frac{T_{a1}}{T_p^*}\mathbf{u}_1 + \frac{T_{c1}}{T_p^*}\mathbf{u}_2 + \frac{T_{a2}}{T_p^*}\mathbf{u}_1 + \frac{T_{c2}}{T_p^*}\mathbf{u}_2 + \frac{T_b}{T_p^*}\mathbf{u}_3 \\
&\quad + \frac{T_p^* - (T_{a1} + T_{c1} + T_{a2} + T_{c2} + T_b)}{T_p^*}\mathbf{u}_0 \ (\text{or } \mathbf{u}_7)
\end{aligned}
\tag{2.37}
$$

Fig. 2.33 Voltage vector $\mathbf{u}_s$ can be created by use of any one combination of component vectors
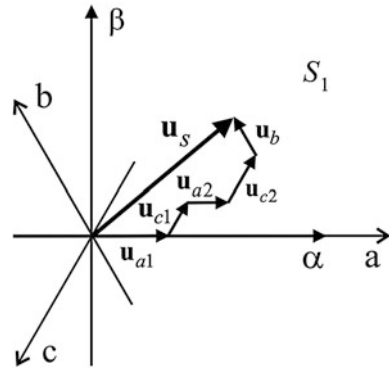
The example in Fig. 2.33, with $\mathbf{u}_s$ within the sector S_1, shows that not only the two standard vectors $\mathbf{u}_1$ and $\mathbf{u}_2$ of S_1 are used for modulation. Equation (2.37) also contains $\mathbf{u}_3$, the standard vector of S_2. But, as Jenni and Wüest 1995 has demonstrated: to make sure that the total time will not become greater than the pulse period, the vector $\mathbf{u}_s$ shall be created by combinations of component vectors only using the standard vectors of the sector which contains $\mathbf{u}_s$. That means the vector $\mathbf{u}_b$ from the example in Fig. 2.33 must be zero.

2.6.2 Modulation with Different Sequences of Component Vectors

This degree of freedom has been used a lot in the previous sections, in order to achieve different effects. We can list here as examples:

- Figure 2.4: The sequence $\mathbf{u}_0 \Rightarrow \mathbf{u}_1 \Rightarrow \mathbf{u}_2 \Rightarrow \mathbf{u}_7$ was changed into $\mathbf{u}_7 \Rightarrow \mathbf{u}_2 \Rightarrow \mathbf{u}_1 \Rightarrow \mathbf{u}_0$ to switch every transistor pair only once within a pulse period.
- Figure 2.10: The voltage output sequence was changed from Fig. 2.10a to Fig. 2.10b not only to ensure strict synchronization between modulation and control, but also to make the use of PWM units in microcontrollers possible.
- Figure 2.25: The standard output sequence in Fig. 2.25a was changed into the sequences in Fig. 2.25b, c to reduce switching losses.
- Section 2.5.3 "Stochastic modulation": The standard output sequence was changed twice by combined zero vector and sequence randomizing, to reduce the 1st and 2nd switching frequency harmonics.

The above examples illustrate the conclusion: Thanks to this degree of freedom, the modification of the voltage output sequence becomes a powerful tool to achieve different effects. However, when changing from one logic state (switching state) to

Fig. 2.34 Transition between
logic states
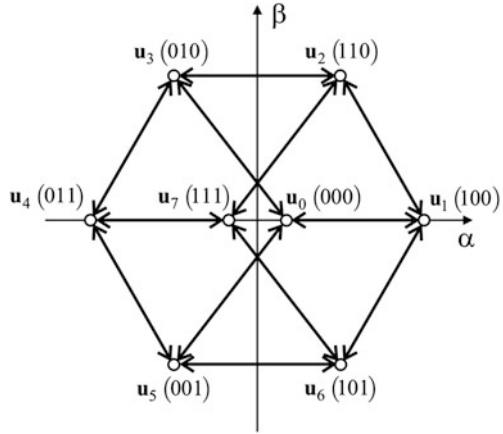
another, one or two or three switching transitions will take place. Figure 2.34
illustrates this, whereby each arrow means that one inverter leg will be switched.

- Transition from one logic state to the state nearby: Only one inverter leg will be
  switched.
- Transition with jump over the logic state nearby: Two inverter legs will be
  switched.
- Transition from one logic state to the inverse logic state: Three inverter legs will
  be switched.

Figure 2.34 illustrates, that, if the inverter has to be operated by the lowest
switching frequency then sequences with only one switching transition should be
used.

If the voltage component vectors for a pulse period are fixed, then the next
question about the optimal output sequence will arise. For the sector S_1 there are the
three following sequences possible:

- Sequence 1 (Fig. 2.25a): 6 switch-over processes per pulse period (sampling
  period). This sequence is the standard modulation.

$$\underbrace{\frac{T_0}{2}\left(\mathbf{u}_0\right) \Rightarrow T_r\left(\mathbf{u}_1\right) \Rightarrow T_l\left(\mathbf{u}_2\right) \Rightarrow T_7\left(\mathbf{u}_7\right) \Rightarrow T_l\left(\mathbf{u}_2\right) \Rightarrow T_r\left(\mathbf{u}_1\right) \Rightarrow \frac{T_0}{2}\left(\mathbf{u}_0\right)}_{T_p}$$

- Sequence 2 (Fig. 2.25b, c): Only 4 switch-over processes per pulse period. Both
  sequences belong to the modulation with two legs (Sect. 2.5.1).

$$\underbrace{T_0\left(\mathbf{u}_0\right) \;\Rightarrow\; T_r\left(\mathbf{u}_1\right) \;\Rightarrow\; 2T_l\left(\mathbf{u}_2\right) \;\Rightarrow\; T_r\left(\mathbf{u}_1\right) \;\Rightarrow\; T_0\left(\mathbf{u}_0\right)}_{T_p}$$

$$\underbrace{T_r\left(\mathbf{u}_1\right) \;\Rightarrow\; T_l\left(\mathbf{u}_2\right) \;\Rightarrow\; 2T_7\left(\mathbf{u}_7\right) \;\Rightarrow\; T_l\left(\mathbf{u}_2\right) \;\Rightarrow\; T_r\left(\mathbf{u}_1\right)}_{T_p}$$

- Sequence 3: The two examples hereunder show sequences with 8 and more switch-over processes per pulse period. Here each voltage creating logic state can be adopted, different for the two time periods. By this way of modulation the pulse frequency can be increased.

$$\underbrace{\mathbf{u}_0 \;\Rightarrow\; \mathbf{u}_1 \;\Rightarrow\; \mathbf{u}_0 \;\Rightarrow\; \mathbf{u}_2 \;\Rightarrow\; \mathbf{u}_7 \;\Rightarrow\; \mathbf{u}_7 \;\Rightarrow\; \mathbf{u}_2}_{T_p}$$

$$\underbrace{\mathbf{u}_0 \;\Rightarrow\; \mathbf{u}_1 \;\Rightarrow\; \mathbf{u}_0 \;\Rightarrow\; \mathbf{u}_1 \;\Rightarrow\; \mathbf{u}_2 \;\Rightarrow\; \mathbf{u}_7 \;\Rightarrow\; \mathbf{u}_7 \;\Rightarrow\; \mathbf{u}_2}_{T_p}$$

2.6.3 Execution Time of Zero Vectors

After the voltage creating logic states and their sequence are defined, the last degree of freedom is the allocation of the remaining time for the two zero vectors $\mathbf{u}_0$ and $\mathbf{u}_7$.

$$T_0 + T_7 = T_p - \sum_{i=1}^{6} T_i = T_p - \sum_{i=1}^{2} T_i \quad (i = 1, 2 : \text{ standard modulation in } S_1)$$

$$(2.38)$$

This allocation does not affect the short-term average value[3] of the modulated voltage, but the average value of the neutral point voltage. Let's take a look to the case when standard modulation[4] is applied.

The neutral point voltage $\overline{\mathbf{u}}_{N0}$ is the voltage between the neutral point of the 3-phase AC motor and the virtual zero potential of the DC link (Fig. 2.1).

---

[3]Definition of the short-term average value is in (Jenni and Wüest 1995, Sect. 3.3.1).

[4]The symbols T_1, T_2 replace T_r, T_l in this section.

According to (Jenni and Wüest 1995, Sect. 8.2.3) the average value of the neutral point voltage is given by the following equation:

$$\overline{\mathbf{u}}_{N0} = \frac{U_{DC}}{2} \frac{1}{T_p} \left(-T_0 - \frac{T_1}{3} + \frac{T_2}{3} + T_7 \right) \tag{2.39}$$

Using (2.38) to eliminate T_7 in (2.39) will obtain:

$$\overline{\mathbf{u}}_{N0} = \frac{U_{DC}}{2} \frac{1}{T_p} \left(T_p - 2T_0 - \frac{4}{3}T_1 - \frac{2}{3}T_2 \right)$$
$$\rightarrow \ T_0 = \left(\frac{1}{2} - \frac{\overline{\mathbf{u}}_{N0}}{U_{DC}} \right) T_p - \frac{2}{3}T_1 - \frac{1}{3}T_2 \tag{2.40}$$

Equation (2.40) shows an interesting relation between $\overline{\mathbf{u}}_{N0}$ and T_0, T_7. The value of $\overline{\mathbf{u}}_{N0}$ is defined by T_0, T_1 and T_2. Because T_1 and T_2 are given by $|\mathbf{u}_s|$, the choice of T_0 will decide the value of $\overline{\mathbf{u}}_{N0}$. Together with (2.38) "the choice of T_0" practically means the allocation of the remaining time for the two zero vectors $\mathbf{u}_0$ and $\mathbf{u}_7$. In the practice three different variants of this allocation are applicable.

- *Variant* 1: Allocation for $\overline{\mathbf{u}}_{N0} = 0$. In this case we have:

$$T_0 = \frac{1}{2}T_p - \frac{2}{3}T_1 - \frac{1}{3}T_2; \ T_7 = T_p - T_0 - T_1 - T_2 \tag{2.41}$$

- *Variant* 2: Equal distribution to both T_0 and T_7. This division is used in standard modulation. According (2.39) the value of $\overline{\mathbf{u}}_{N0}$ will be:

$$\overline{\mathbf{u}}_{N0} = \frac{U_{DC}}{2} \frac{1}{T_p} \left(-\frac{T_1}{3} + \frac{T_2}{3} \right) \tag{2.42}$$

- *Variant* 3: Using only one of both zero vectors $\mathbf{u}_0$ and $\mathbf{u}_7$, which means only one T_0 or T_7. This solution is the modulation with two legs in Sect. 2.5.1 with lower pulse frequencies.

References

Choi JW, Yong SI, Sul SK (1994) Inverter output voltage synthesis using novel dead time compensation. In: Proceedings of the IEEE applied power electronics conference, pp 100–106
Jenni F, Wüest D (1995) Steuerverfahren für selbstgeführte Stromrichter (Kap. 8.2). vdf Hochschulverlag AG an der ETH Zürich und B.G. Teubner Stuttgart
Kiel E (1994) Anwendungsspezifische Schaltkreise in der Drehstrom-Antriebstechnik. Dissertation, TU Carolo-Wilhemina zu Braunschweig

Lipp A (1989) Beitrag zur Erarbeitung und Untersuchung von online Algorithmen für die digitale Ansteuerung von Pulsspannungswechselrichtern zur Drehzahlstellung von Drehstromasynchronmaschinen. Dissertation, TU Ilmenau

Mohan N, Undeland TM, Robbins WP (1995) Power electronics: converters, applications, and design, 2nd edn, Wiley

Pollmann A (1984) Ein Beitrag zur digitalen Pulsbreitenmodulation bei pulswechselrichtergespeisten Asynchronmaschinen. Dissertation, TU Carolo-Willhelmina zu Braunschweig

Quang NP (1991) Schnelle Drehmomenteinprägung in Drehstromstellantrieben. Dissertation, TU Dresden

Quang NP, Wirfs R (1995) Mehrgrößenregler löst PI-Regler ab: Ein Umrichterkonzept für Drehstromantriebe. Elektronik (H.7):S. 106–110

Rashid MH (2001) Power electronics handbook. Academic Press, New York

Schröder D (1998) Elektrische Antriebe: Leistungselektronische Schaltungen. Springer, Berlin

Siemens AG (1990) Microcomputer components SAB 80C166/83C166. User's Manual

Siemens AG (2003) C167CR derivatives 16-bit single-chip microcontrollers. User'Manual, V3.2

Siemens AG (2005) TC116x series 32-bit single-chip microcontrollers. User'Manual, V1.2

Texas Instruments (1990) Digital signal processing products TMS 320C2×. User's Guide

Texas Instruments (2004) TMS 320F2812 digital signal processors. Data Manual

Yen-Shin L (1999) Sensorless vector-controlled IM drives using random switching technique, In: Proceedings EPE '99 Lausanne