Proceso	Llegada	CPU	Prioridad	I/O (rec, ins, dur)	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31		TR	TE
P1	0	9	1	(R1, 4, 2) (R2, 6, 3) (R1, 8 3)	>1	2	3	4	R1	R1				5	6	R2	R2	R2	7	8	R1	R1	R1			9<												22	13
P2	1	5	2	(R3, 3, 2) (R3, 4, 2)		>			1	2	3	R3	R3								4	R3	R3				5<											22	17
P3	2	5	3	(R1, 4, 1)			>																						1	2	3			4	R1	5<		30	25
P4	3	7	2	(R2, 1, 2) (R2, 5, 3)				>								1			R2	R2			2	3	4			5	R2	R2	R2	6	7<					26	19
P5	5	5	1	(R1, 2, 3) (R3, 4, 5)						>		1	2	R1	R1	R1	3	4	R3	R3	R3	5<																13	8
RR-TV	Q=3	31		R Qeue1	4	4	5	4	5	4	5	4																									2	22,6	16,4
				R Qeue2	2	4	2	4	2	4	4																												
				R Qeue3	3	3	3																																

I C QCCCL	_	-	_		- 1	_	-	
R Qeue3	3	3	3					
R1 Qeue	4	5	4	3				
R2 Qeue	4	4	4					
R3 Qeue	2	5	2					
·								

Proceso	Llegada	CPU	Prioridad	I/O (rec,ins,dur)	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	TR	TE
P1	0	9	1	(R1, 4, 2) (R2, 6, 3) (R1, 8, 3)	>1	2	3	4	R1	R1		5	6	R2	R2	R2	7	8	R1	R1	R1	9<															18	9
P2	1	5	2	(R3, 3, 2) (R3, 4, 2)		>			1										2				3	R3	R3		4	R3	R3	5<							25	20
P3	2	5	3	(R1, 4, 1)			>																					1	2				3	4	R1	5<	30	25
P4	3	7	2	(R2, 1, 2) (R2, 5, 3)				>						1			R2	R2			2			3	4	5	R2	R2	R2		6	7<					25	18
P5	5	5	1	(R1, 2, 3) (R3, 4, 3)						>1	2	R1	R1	R1	3	4	R3	R3	R3	5<																	11	6
TV	Q=3			R1 Qeue	4	4	5	4	5	4	5	4																									21.8	15.6
				R Qeue 2	2	4	2	4	2	4	2	2	4																									
				R Qeue 3	3	3																																

I QUU L	_		_	 - 1	_	_	- 1	
R Qeue 3	3	3						
R1 Qeue								
R2 Qeue								
R3 Qeue								