AX88772C/AX88772B USB to 100Base-TX Ethernet Demo Board
Reference Schematic System Block

Page 1

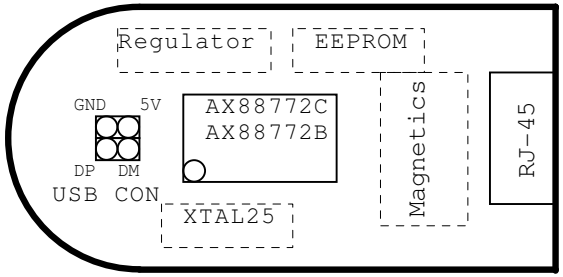
System Block (This page)

Page 2

AX88772C_AX88772B
(25MHz Crystal,EEPROM,RJ-45 Transformer, USB Connector, Power/Reset Circuit)

Page 3

Revision History



Note:
1.Please refer to AX88772C/AX888772B USB to LAN Application Design Note for more AX88772C/AX88772B PCB layout design notes.

2.Please deliver us your AX88772C/AX88772B schematic and PCB layout file for further review.

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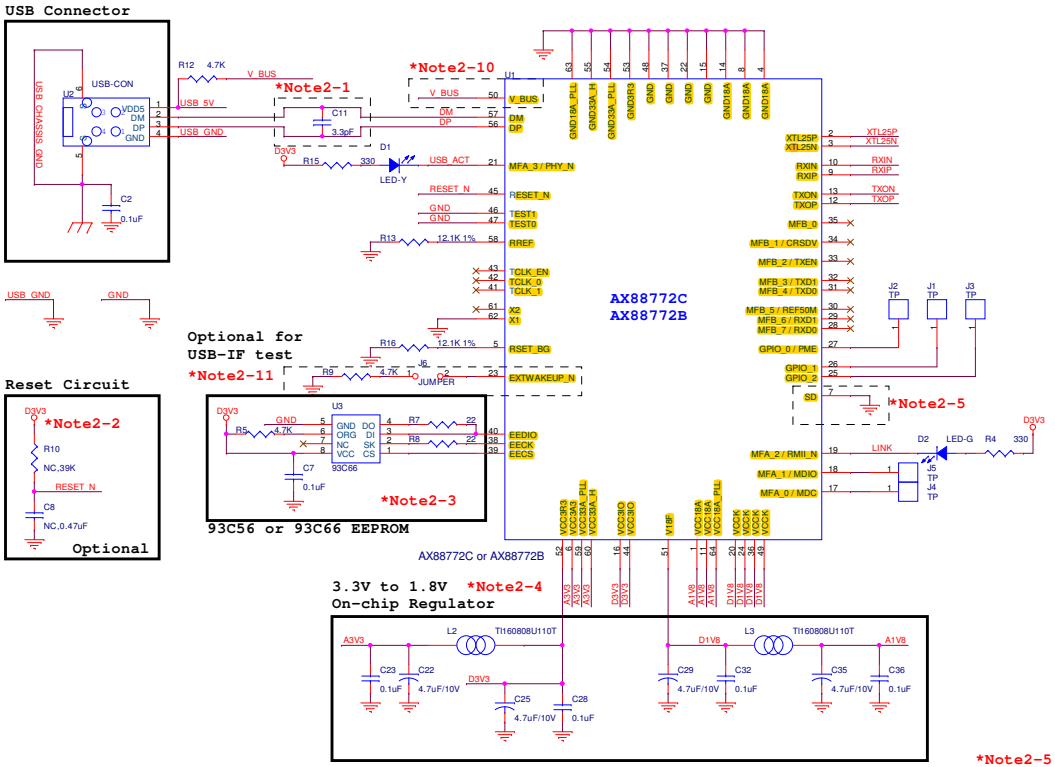
Date: Tuesday, September 20, 2016	Sheet 1 of 3	



*Note2-1:
The C11 cap between the DP and DM pins is used to filter the differential-mode noise
and should be placed as close as pin #57 and #56.

*Note2-2:
The RC reset circuit is optional for AX88772C/AX88772B applications. You can reserve the RC
reset circuit on your AX88772C/AX88772B schematic to fine tune the reset timing if necessary.

*Note2-3:
The AX88772C/AX88772B supports 16-bit mode 93C56/93C66 EEPROM. The R5 resistor is mounted
to set the ATMEL AT93C66A EEPROM to 16-bit mode.

*Note2-4:
AX88772C/AX88772B on-chip 3.3V to 1.8V regulator is a low dropout regulator (LDO),
which requires some large external compensating capacitors on its input (pin #52)
and output (pin #51) pins. The C25, C28, C29 and C32 capacitors are the compensating
capacitors for the on-chip regulator.
The analog powers and digital powers should be isolated with a Ferrite Bead (L2, L3).
The VCC3R3 trace should be wider than 40mil for good power regulation.
The V18F trace should be wider than 20mil for good power regulation.

*Note2-5:
The SD signal should be connected to GND directly or through a 4.7K resistor
at copper mode.

*Note2-6:
The 1M feedback resistor is necessary for 25MHz crystal circuit. The reference
25MHz crystal is the NSK NXH-32 SMD 25MHz crystal with CL 20pF and ESR max. 70 Ohm.
The 25MHz clock signals should be within 25MHz +- 50ppm.
Please reserve the R17 0 Ohm resistor on 25MHz crystal circuit for fine tuning
the 25MHz crystal circuit if necessary.

*Note2-7:
Please refer to Section 4 of AX88772C/AX88772B USB to LAN Application Design Note
for more details of the Ethernet magnetics reference circuits.

*Note2-8:
The C1 capacitor can be 1uF or 1000pF/2KV(for a better ESD protection).

*Note2-9:
All power pins should be implemented with a by-pass capacitor, and the by-pass
capacitors should be as close as the power pins.
The C9/C13 capacitors and C10 capacitor should be 10uF and 1uF respectively
for USB-IF compliant test.

*Note2-10:
For self-power applications, please refer to below suggestions to design the V_BUS signal
circuit,
(1)While the USB interface was connected to USB host/hub controller,
the V_BUS signal MUST be pulled high to set AX88772C/AX88772B at normal operation stage.
(2)While the USB interface was disconnected from USB host/hub controller,
the V_BUS signal MUST be pulled down to set AX88772C/AX88772B at reset stage.

*Note2-11:
Please reserve the EXTWAKE_N circuit location if you need to run the USB-IF compliant test
(mount R9 4.7K resistor and J6 jumper). Don't need mount R9, J6 in production.

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Title: AX88772C/AX88772B		
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Date: Tuesday, September 20, 2016	Sheet 2 of 3	

Revision History

Revision	Date	Comment
V1.00	2010/06/21	Initial release.
V1.01	2011/08/10	1.Updated F.B. L1/L2/L3 to Tl160808U110T.
V2.00	2013/03/19	1.Modified to support AX88772C. 2.Modified 25MHz crystal circuit. 3.Modified the RJ-45 Connector + Transform circuit. 4.Added Note2-10 for the VBUS circuit design note.
V2.01	2013/04/10	1.Modified some descriptions in Note2-10.
V2.02	2014/05/20	1.Corrected a typo on NS0013LF pin #15 & #16 naming.
V2.03	2016/09/20	1.Added Note2-11 in page 2. 2.Modified some descriptions in Note2-1.