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A UNIFIED APPROACH TO ELECTRONIC CIRCUIT ANALYSIS USING THE INDEFINITE ADMITTANCE MATRIX

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1 INTRODUCTION

Most books on electronic circuits[1,2] deal with the analysis of various transistor and F.E.T. circuits in a conventional way. Chirlian[3] uses a generalized approach in the analysis of tube, F.E.T. and transistor circuits. However, it turns out to be a very cumbersome approach. Using the indefinite admittance matrix (also known as the floating admittance matrix and the zero sum matrix in the literature)[4,5,6,7] one can solve electronic circuits, the active ones in particular, in an elegant way. For solving active circuits, one obtains the indefinite admittance matrix of the device and adds the same to that of the rest of the circuits to obtain the overall indefinite admittance matrix. In fact, the process of filling[7] the indefinite admittance matrix is very simple and one can do this just by inspection. Once the indefinite admittance matrix is obtained the input and the output impedances, transfer impedances, voltage, current and power gains are easily obtained in terms of the co-factors of the elements of the indefinite admittance matrix. The easy adaptability for computer-aided analysis and design makes it all the more important. Solution of circuits containing four nodes and less can be obtained analytically with less effort using the indefinite admittance matrix than by conventional methods, and for circuits with more nodes, a computer can be used to advantage. It is hoped that a student, if taught via this approach, would be better equipped to assimilate the analysis

2 THE INDEFINITE ADMITTANCE MATRIX

Any linear n-terminal, the K^{th} ($K = 1,2, \ldots . n$) terminal of which is associated with a current I_K, a potential V_K (defined with respect to a reference terminal not belonging to the network element), and a current I_K^0 (when all the terminals are connected to the reference terminal i.e. $I_K^0 = I_K \mid_{V_K = 0}$), can be described by

$$I] = [Y_i]\ V] + I^0]$$

where $[Y_i]$, the indefinite admittance matrix ($n \times n$)

$$= \begin{bmatrix} y_{11} & y_{12} & \cdots & y_{1n} \\ y_{21} & y_{22} & \cdots & y_{2n} \\ \cdot & \cdot & & \cdot \\ \cdot & \cdot & & \cdot \\ \cdot & \cdot & & \cdot \\ y_{n1} & y_{n2} & & y_{nn} \end{bmatrix}$$

The y_{ii}'s are Laplace transformed short circuit self admittances of node i. y_{ij}'s are Laplace transformed short circuit mutual admittances between terminals i and j.
$I]$, the current column vector (n elements)

$$= [I_1, I_2, \ldots\ldots I_n]^T$$

The I_K's are Laplace transformed current variables.

T stands for transpose.
$V]$, the voltage column vector (n elements)

$$= [V_1, V_2 \ldots\ldots\ldots V_n]^T$$

The V_K's are Laplace transformed voltage variables and $I^0]$, the current column vector (n elements)

$$= [I_1^0, I_2^0 \ldots\ldots I_n^0]^T$$

The I_K^0's are the Laplace transformed currents.

2.1 *Properties of the indefinite admittance matrix*[4,5,6]

(i) The indefinite admittance matrix is singular i.e.

$$\det [Y_i] = |Y_i| = 0$$

(ii) Zero sum property, i.e.

$$\sum_{j=1}^{n} y_{jk} = 0 \qquad k = 1,2, \ldots\ldots n$$

$$\sum_{k=1}^{n} y_{jk} = 0 \qquad j = 1,2, \ldots\ldots n$$

(iii) If a terminal K is specified as the voltage reference then the matrix obtained by deleting the K^{th} row and K^{th} column, $[Y_K^K]$, is the $(n-1) \times (n-1)$ admittance matrix of the system with the terminal K grounded.

(iv) The first co-factors are equal to each other

$$[Y_j^j] = [Y_k^k] \text{ for } k = 1,2, \ldots\ldots n$$

(v) The $n \times n$ matrix can be reduced to a $(n-m) \times (n-m)$ matrix either by contraction or suppression.

Contraction of a multiterminal is the joining of the two or more of its terminals to form a single terminal. This union forces the potential of the connected terminals to be equal. The matrix of a contracted multiterminal is obtained by adding the respective elements of the rows and the columns corresponding to the terminals being joined together.

Suppression of a multiterminal is the operation by which some terminals are made inaccessible and the currents associated with the suppressed terminals are made zero. If for the n-terminal described by the admittance equation

$$I_1] = [Y_{11}]\ V_1] + [Y_{12}]\ V_2] + I_1^0]$$

$$I_2] = [Y_{21}]\ V_1] + [Y_{22}]\ V_2] + I_2^0]$$

where,

$I_1]$ is a column vector of order k representing the currents associated with the k accessible terminals, and

$I_2]$ is a column vector of order $(n - k)$ representing the currents associated with the terminals being suppressed.

If $I_2]$ is made zero and solved for $I_1]$ one gets

$$I_1] = \{[Y_{11}] - [Y_{12}]\ [Y_{22}^{-1}]\ [Y_{21}]\}\ V_1] + \{I_1^0] - [Y_{12}]\ [Y_{22}^{-1}]\ I_2^0]\},$$

where

$\{[Y_{11}] - [Y_{12}]\ [Y_{22}^{-1}]\ [Y_{21}]\}$, is the new indefinite admittance matrix.

(vi) If m multiterminals are connected in parallel, the admittance of the composite multiple terminal is given in a matrix form as

$$I] = \left\{ \sum_{k=1}^{m} [Y^{(k)}] \right\}\ V] + \left\{ \sum_{k=1}^{m} I^{0(k)} \right\}$$

A p terminal where $p < n$, can be considered as an n-terminal by adding $(n - p)$ terminals to the p-terminal. Such additional terminals are floating. In admittance description, this amounts to adding rows and columns of zeros at appropriate places. Hence, it is possible to connect a multiterminal having an unequal number of terminals in parallel.

2.2 *Expressions of network functions*

The following expressions can be easily derived[5,6].

$$\text{The transfer impedance} = Z_{mn}^{ij} = \frac{E_{ij}}{I_{mn}} = \text{sgn}\,(m - n)\ \text{sgn}\,(i - j)\ \frac{[Y_{ij}^{mn}]}{[Y_n^n]} \tag{A}$$

$$\text{Driving point impedance} = Z_{mn} = \frac{E_{mn}}{I_{mn}} = \frac{[Y_{mn}^{mn}]}{[Y_n^n]} \tag{B}$$

$$\text{Voltage gain} = A_v\,|_{mn}^{ij} = \frac{E_{ij}}{E_{mn}} = \text{sgn}\,(m - n)\ \text{sgn}\,(i - j)\ \frac{[Y_{ij}^{mn}]}{[Y_{mn}^{mn}]} \tag{C}$$

$$\text{Current gain} = A_i\,|_{mn}^{ij} = \frac{I_{ij}}{I_{mn}} = \text{sgn}\,(m - n)\ \text{sgn}\,(i - j)\ G_L\ \frac{[Y_{ij}^{mn}]}{[Y_n^n]} \tag{D}$$

$$\text{Power gain} = A_p\,|_{mn}^{ij} = \frac{E_{ij}}{E_{mn}} \times \frac{I_{ij}}{I_{mn}} = A_v\,|_{mn}^{ij} \times A_i\,|_{mn}^{ij} \tag{E}$$

where, sgn $(x) = +1$ for $x > 0$
$= -1$ for $x < 0$

$$[Y_{ij}^{mn}] = (-1)^{i+j+m+n} \times \begin{bmatrix} \text{determinant of the submatrix} \\ \text{obtained by omitting } m^{th} \text{ row,} \\ n^{th} \text{ row, } i^{th} \text{ column and } j^{th} \\ \text{column of } [Y_i] \end{bmatrix}$$

m, n is the excitation terminal pair and i, j is the response terminal pair.

3 APPLICATIONS IN CIRCUIT ANALYSIS

3.1 *Parameter conversion*

Using the indefinite admittance matrix parameter, conversion[4] can be conveniently made. If the admittance matrix of the device shown in Fig. 1 is

$$[Y_b] = \begin{matrix} \begin{bmatrix} y_{11_b} & y_{12_b} \\ y_{21_b} & y_{22_b} \end{bmatrix} & \begin{matrix} E \\ C \end{matrix} \\ \begin{matrix} E & C \end{matrix} & \end{matrix}$$

where the subscript b denotes that the base is grounded, then, using the zero sum property, the indefinite admittance matrix for the device can be written as

$$[Y_b] = \begin{matrix} \begin{bmatrix} y_{11_b} & y_{12_b} & -y_{11_b} - y_{12_b} \\ y_{21_b} & y_{22_b} & -y_{21_b} - y_{22_b} \\ -y_{11_b} - y_{21_b} & -y_{12_b} - y_{22_b} & y_{11_b} + y_{12_b} + y_{21_b} + y_{22_b} \end{bmatrix} & \begin{matrix} E \\ C \\ B \end{matrix} \\ \begin{matrix} E & C & B \end{matrix} & \end{matrix}$$

For grounded emitter case, using property (iii), we have

$$[Y_e] = [Y_e^e] = \begin{bmatrix} y_{22_b} & -y_{21_b} - y_{22_b} \\ -y_{12_b} - y_{22_b} & y_{11_b} + y_{12_b} + y_{21_b} + y_{22_b} \end{bmatrix}$$

Similarly for grounded collector transistor also the admittance matrix can be found.

3.2 *Solution of F.E.T. and transistor amplifier circuits*

The overall indefinite admittance matrix of the F.E.T. and the external circuit of Fig. 2 can be written by inspection as

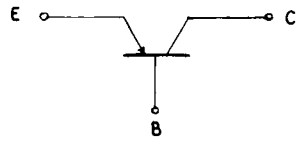

FIG. 1 Symbolic representation of the transistor.

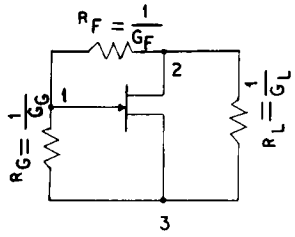

FIG. 2 Most general form of the F.E.T. amplifier.

$$[Y_i] = \begin{bmatrix} g_g + G_F + G_G & -G_F & -g_g - G_G \\ g_m - G_F & g_d + G_F + G_L & -g_m - g_d - G_L \\ -g_g - g_m - G_G & -g_d - G_L & g_g + g_m + g_d + G_L + G_G \end{bmatrix} \quad (1)$$

The most general amplifier configuration of Fig. 2 can be reduced to any specific configuration by choosing one of the three terminals common to both input and output circuits. For the common-source amplifier analysis, terminal 3 is assumed to be grounded, terminal 1 to be the input terminal and terminal 2 the output terminal and $G_F = 0$. Using equations (B), (C), (D), (E) and (1), one can solve for the following impedence functions, voltage, current and power gains as

$$\text{Voltage gain} = A_v\Big|_{13}^{23} = \text{sgn}\,(1-3)\,\text{sgn}\,(2-3)\,(-1)^9\,\frac{|Y_{23}^{13}|}{|Y_{13}^{13}|} = -g_m(r_d \parallel R_L) \quad (2)$$

$$\text{Current gain} = A_i\Big|_{13}^{23} = \text{sgn}\,(1-3)\,\text{sgn}\,(2-3)\,(-1)^9 G_L\,\frac{|Y_{23}^{13}|}{|Y_3^3|}$$

$$= -g_m\,G_L(r_d \parallel R_L)\,(r_g \parallel R_G) \quad (3)$$

$$\text{Input impedance} = Z_i = Z_{13} = \frac{|Y_{13}^{13}|}{|Y_3^3|}\,G_G = 0 = r_g \quad (4)$$

$$\text{Output impedance} = Z_0 = Z_{23} = \frac{|Y_{23}^{23}|}{|Y_3^3|}\,G_L = 0 = r_d \quad (5)$$

$$\text{Power gain} = A_p\Big|_{13}^{23} = A_i\Big|_{13}^{23} \times A_v\Big|_{13}^{23} = g_m^2\,G_L(r_d \parallel R_L)^2\,(r_g \parallel R_G) \quad (6)$$

Similarly the various network functions for the common-gate and common drain F.E.T. amplifiers can be obtained using equation (1) saving much of the time in solving for the different amplifier configurations by the conventional methods.

The general configuration of a transistor amplifier circuit is shown if Fig. 3. The overall indefinite admittance matrix of the transistor as well as the external circuit of Fig. 3 can be written as

$$[Y_i] = \begin{bmatrix} g_i + G_B + G_F & -G_F & -g_i - G_B \\ g_m - G_F & g_o + G_L + G_F & -g_m - g_o - G_L \\ -g_m - g_i - G_B & -g_o - G_L & g_i + g_m + g_o + G_B + G_L \end{bmatrix} \quad (7)$$

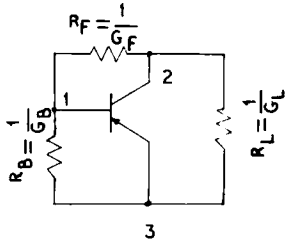

FIG. 3 Most general form of the transistor amplifier.

where $g_i = 1/h_{ie}, g_o = h_{oe}, g_m = h_{fe}/h_{ie}$
Fig. 3 can be reduced to a common-emitter amplifier configuration with 1 & 3 as input terminals, and 2 & 3 as output terminals and $G_F = 0$. Again using equation (1) the following expressions are derived:

$$A_v\Big|_{13}^{23} = \operatorname{sgn}(1-3)\operatorname{sgn}(2-3)(-1)^9 \frac{|Y_{23}^{13}|}{|Y_{13}^{13}|} = \frac{-h_{fe} R_L}{(1+h_{oe} R_L)h_{ie}} \tag{8}$$

$$A_i\Big|_{13}^{23} = \operatorname{sgn}(1-3)\operatorname{sgn}(2-3)(-1)^9 G_L \frac{|Y_{23}^{13}|}{|Y_3^3|} = \frac{-h_{fe} R_B}{(h_{ie}+R_B)(1+h_{oe}R_L)} \tag{9}$$

$$Z_{in} = Z_{13} = \frac{|Y_{13}^{13}|}{|Y_3^3|\,G_B = 0} = h_{ie} \tag{10}$$

$$Z_o = Z_{23} = \frac{|Y_{23}^{23}|}{|Y_3^3|\,G_L = 0} = 1/h_{oe} \tag{11}$$

$$A_p\Big|_{13}^{23} = A_i\Big|_{13}^{23} \times A_v\Big|_{13}^{23} = \frac{h_{fe}^2 R_L R_B}{h_{ie}(h_{ie}+R_B)(1+h_{oe}R_L)^2} \tag{12}$$

Similarly all the network functions for both common-base and common-collector transistor amplifier configurations can be obtained easily from equation (7). Use of the indefinite admittance matrix approach clearly suggests a short-cut method for the analysis of all the amplifier configurations.

3.3 *Solution for the passive circuits (Lattice equalizer design)*
The indefinite admittance matrix for the circuit of Fig. 4 is

$$[Y_i] = \begin{bmatrix} Y_1+Y_2 & -Y_1 & 0 & -Y_2 \\ -Y_1 & Y_1+Y_2+Y_0 & -Y_2 & -Y_0 \\ 0 & -Y_2 & Y_1+Y_2 & -Y_1 \\ -Y_2 & -Y_0 & -Y_1 & Y_1+Y_2+Y_0 \end{bmatrix} \tag{13}$$

Using formulae (B), (C) and equation (13) one can solve for

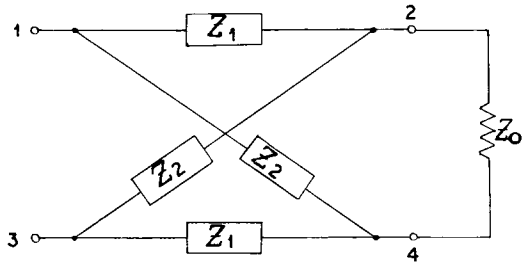

FIG. 4 Lattice equalizer circuit.

$$Z_{in} = Z_{13} = \frac{|Y_{13}^{13}|}{|Y_3^3|} = 1/Y_0 \left\{ \frac{Y_1 + Y_2 + 2Y_0}{Y_1 + Y_2 + 2Y_1\ Y_2/Y_0} \right\} \tag{14}$$

and the voltage-gain $= A_v \Big|_{13}^{24} = \frac{E_{24}}{E_{13}} = \text{sgn}(1-3)\,\text{sgn}(2-4)(-1)^{10}\ \frac{|Y_{24}^{13}|}{|Y_{13}^{13}|}$

$$= \frac{Y_1 - Y_2}{Y_1 + Y_2 + 2Y_0} \tag{15}$$

From the definition of the characteristic impedance, $Z_{13} = Z_0$

This is possible only if $Y_1 Y_2 = Y_0^2$ (16)

After substituting equation (16) in equation (15), one obtains,

$$e^{\gamma} = \frac{E_{13}}{E_{24}} = \frac{Y_0 + Y_2}{Y_0 - Y_2} \quad \text{where } \gamma = \alpha + j\beta \tag{17}$$

with $Y_2 = G_2 + j\omega C_2$, the expression for attenuation constant is obtained as

$$e^{2\alpha} = \frac{[(Y_0 + G_2)/2\pi\, C_2]^2 + f^2}{[(Y_0 - G_2)/2\pi\, C_2]^2 + f^2} = F \tag{18}$$

$$\text{If } P_0 = \left\{ \frac{Y_0 + G_2}{2\pi\, C_2} \right\}^2, \text{ and } Q_0 = \left\{ \frac{Y_0 - G_2}{2\pi\, C_2} \right\}^2 \tag{19}$$

Equation (18) can now be modified as

$$F = e^{2\alpha} = \frac{P_0 + f^2}{Q_0 + f^2} \tag{20}$$

From equation (19) one can obtain

$$C_2 = \frac{Y_0}{\pi(\sqrt{P_0} + \sqrt{Q_0})} \text{ and } G_2 = \frac{Y_0(\sqrt{P_0} - \sqrt{Q_0})}{\sqrt{P_0} + \sqrt{Q_0}} \tag{21}$$

From equations (16) and (21) the following elements of Y_1 can be obtained

$$R_1 = Z_0 \frac{\sqrt{P_0} - \sqrt{Q_0}}{\sqrt{P_0} + \sqrt{Q_0}} \tag{22}$$

and

$$L_1 = Z_0 \frac{1}{\pi(\sqrt{P_0} - \sqrt{Q_0})} \tag{23}$$

It may be realized that the analysis of the ladder network using the indefinite admittance matrix approach saves a lot of time and effort in comparison with the conventional method.

4 CONCLUSIONS

The indefinite admittance matrix approach proposed in this paper can be conveniently used in the analysis of both active and passive circuits. For an active circuit, one needs to find the indefinite admittance matrix of the device first and then use the analysis procedure, which is the same for all types of circuits. The examples clearly illustrate that this technique is straightforward and circuits with four terminals or less can be solved without much difficulty. Circuits with a larger number of terminals can be solved with the help of a computer. Since this approach can be readily adapted for computer-aided analysis and design, the authors strongly recommend this technique for teaching electronic circuits. The teaching of Electronic Circuits is being conducted by the authors along these lines. The indefinite admittance matrix approach has been used to advantage by the authors for the measurement of device parameters[8] and analysis of oscillator circuits.

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ABSTRACTS–ENGLISH, FRENCH, GERMAN, SPANISH

A unified approach to electronic circuit analysis using the indefinite admittance matrix
A unified approach to transistor, F.E.T. and passive circuit analysis using the indefinite admittance matrix is presented in this paper. The indefinite admittance matrix with its easy adaptability for computer-aided analysis and design makes it a suitable basis for teaching active and passive networks.

Une approche unifiée de l'analyse des circuits électroniques par l'utilisation de la matrice complète des admittances
Une approche unifiée de l'analyse des circuits passifs, de transistors ou F.E.T. par l'utilisation de la matrice indéfinie des admittances nodales est présentée dans cet article. La matrice indéfinie des admittances, par sa facilité d'utilisation dans l'analyse et la conception aidée par ordinateur, forme une base convenant à l'enseignement des circuits actifs et passifs.

Eine vereinheitlichte Methode der elektronischen Stromkreisanalysis unter Benutzung der unbestimmten Admittanz-Matrix
Diese Arbeit gibt eine vereinheitlichte Methode zur Transistor-, F.E.T- und passiven Stromkreisanalysis unter Benutzung der unbestimmten Admittanz-Matrix. Diese Matrix mit ihrer leichten Anpassungsfähigkeit für computer-unterstützte Analysis und Konstruktion macht sie eine geeignete Grundlage im Unterricht aktiver und passiver Netzwerke.

Una exposición unificada del análisis de los circuitos electrónicos que utiliza la matriz indefinida de admitancias
Se presenta en este artículo un estudio unificado del análisis de circuitos pasivos, de transistores y F.E.T., utilizando la matriz indefinida de admitancias. La facilidad con la que la matriz indefinida de admitancias se adapta al análisis y diseño ayudado por computador hace que haya que tenerlo en cuenta en la docencia de redes activas y pasivas.

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