[Product Folder](http://www.ti.com/product/LMT84-Q1?dcmp=dsproject&hqs=pf)

[Order Now](http://www.ti.com/product/LMT84-Q1?dcmp=dsproject&hqs=sandbuy&&samplebuy)

[Technical Documents](http://www.ti.com/product/LMT84-Q1?dcmp=dsproject&hqs=td&&doctype2)

[Tools & Software](http://www.ti.com/product/LMT84-Q1?dcmp=dsproject&hqs=sw&&desKit)

[Support & Community](http://www.ti.com/product/LMT84-Q1?dcmp=dsproject&hqs=support&&community)

### Features

LMT84-Q1 1.5-V, SC70,



Analog Temperature Sensors

### 3 Description

##### [LMT84-Q1](http://www.ti.com/product/lmt84-q1?qgpn=lmt84-q1)

SNIS178 – OCTOBER 2017

* LMT84-Q1 is AEC-Q100 Qualified for Automotive Applications:
  + Device Temperature Grade 0: –40°C to

+150°C

* + Device HBM ESD Classification Level 2
  + Device CDM ESD Classification Level C6
* Very Accurate: ±0.4°C Typical
* Low 1.5-V Operation
* Average Sensor Gain of -5.5 mV/°C
* Low 5.4-µA Quiescent Current
* Wide Temperature Range: –50°C to 150°C
* Output is Short-Circuit Protected
* Push-Pull Output With ±50-µA Drive Capability
* Footprint Compatible With the Industry-Standard LM20/19 and LM35 Temperature Sensors
* Cost-Effective Alternative to Thermistors

### Applications

* Automotive
* Infotainment and Cluster
* Powertrain Systems
* Smoke and Heat Detectors
* Drones
* Appliances

##### Thermal Time Constant

100%

LMT8xLPG

Thermistor

90%

80%

FINAL TEMPERATURE

70%

60%

50%

40%

30%

20%

10%

0

The LMT84-Q1 is a precision CMOS temperature sensor with ±0.4°C typical accuracy (±2.7°C maximum) and a linear analog output voltage that is inversely proportional to temperature. The 1.5-V supply voltage operation, 5.4-μA quiescent current, and 0.7-ms power-on time enable effective power- cycling architectures to minimize power consumption for battery-powered applications such as drones and sensor nodes.The LMT84-Q1 device is AEC-Q100 Grade 0 qualified and maintains ±2.7°C maximum accuracy over the full operating temperature range without calibration; this makes the LMT84-Q1 suitable for automotive applications such as infotainment, cluster, and powertrain systems. The accuracy over the wide operating range and other features make the LMT84-Q1 an excellent alternative to thermistors.

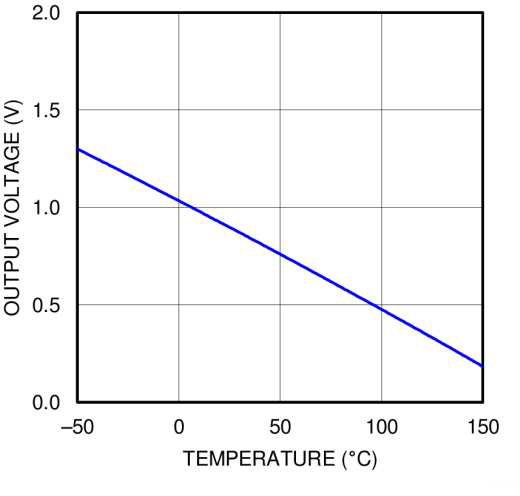
For devices with different average sensor gains and comparable accuracy, refer to [*Comparable*](#_bookmark4)[*Alternative Devices*](#_bookmark4)for alternative devices in the LMT8x family.

##### Device Information(1)

|  |  |  |
| --- | --- | --- |
| **PART NUMBER** | **PACKAGE** | **BODY SIZE (NOM)** |
| LMT84-Q1 | SOT (5) | 2.00 mm x 1.25 mm |

1. For all available packages, see the orderable addendum addendum at the end of the data sheet.

##### Output Voltage vs Temperature

VDD (+1.SV to +S.SV)

GND

VDD

**LMT84**

OUT

CBP

0 20 40 60 80 100

TIME (s)

\* Fast thermal response NTC

D003

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### Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

|  |  |  |
| --- | --- | --- |
| **DATE** | **REVISION** | **NOTES** |
| October 2017 | \* | Initial release. Moved the automotive device from the SNIS167 to a standalone data sheet. |

### Device Comparison Tables

##### Table 1. Available Device Packages

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **ORDER NUMBER(1)** | **PACKAGE** | **PIN** | **BODY SIZE (NOM)** | **MOUNTING TYPE** |
| LMT84DCK | SOT (AKA(2): SC70, DCK) | 5 | 2.00 mm × 1.25 mm | Surface Mount |
| LMT84LP | TO-92 (AKA(2): LP) | 3 | 4.30 mm × 3.50 mm | Through-hole; straight leads |
| LMT84LPG | TO-92S (AKA(2): LPG) | 3 | 4.00 mm × 3.15 mm | Through-hole; straight leads |
| LMT84LPM | TO-92 (AKA(2): LPM) | 3 | 4.30 mm × 3.50 mm | Through-hole; formed leads |
| LMT84DCK-Q1 | SOT (AKA(2): SC70, DCK) | 5 | 2.00 mm × 1.25 mm | Surface Mount |

1. For all available packages and complete order numbers, see the Package Option addendum at the end of the data sheet.
2. AKA = Also Known As

**Table 2. Comparable Alternative Devices**

|  |  |  |
| --- | --- | --- |
| **DEVICE NAME** | **AVERAGE OUTPUT SENSOR GAIN** | **POWER SUPPLY RANGE** |
| [LMT84-Q1](http://www.ti.com/product/lmt84-q1) | –5.5 mV/°C | 1.5 V to 5.5 V |
| [LMT85-Q1](http://www.ti.com/product/lmt85-q1) | –8.2 mV/°C | 1.8 V to 5.5 V |
| [LMT86-Q1](http://www.ti.com/product/lmt86-q1) | –10.9 mV/°C | 2.2 V to 5.5 V |
| [LMT87-Q1](http://www.ti.com/product/lmt87-q1) | –13.6 mV/°C | 2.7 V to 5.5 V |

### Pin Configuration and Functions

**DCK Package**

**5-Pin SOT (SC70)**

**(Top View)**

1

GND

2

GND

3

OUT

5

GND

**LMT84**

4 VDD

##### Pin Functions

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **PIN** | | **TYPE** | **DESCRIPTION** | |
| **NAME** | **SOT (SC70)** | **EQUIVALENT CIRCUIT** | **FUNCTION** |
| GND | 1, 2(1) , 5 | Ground | N/A | Power Supply Ground |
| OUT | 3 | Analog Output | VDD  GND | Outputs a voltage that is inversely proportional to temperature |
| VDD | 4 | Power | N/A | Positive Supply Voltage |

(1) Direct connection to the back side of the die

### Specifications

#### Absolute Maximum Ratings

See (1) (2)

|  |  |  |  |
| --- | --- | --- | --- |
|  | **MIN** | **MAX** | **UNIT** |
| Supply voltage | –0.3 | 6 | V |
| Voltage at output pin | –0.3 | (VDD + 0.5) | V |
| Output current | –7 | 7 | mA |
| Input current at any pin(3) | –5 | 5 | mA |
| Maximum junction temperature (TJMAX) | 150 | | °C |
| Storage temperature Tstg | –65 | 150 | °C |

1. Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. *Soldering process must comply with Reflow Temperature Profile specifications. Refer to* [www.ti.com/packaging](http://focus.ti.com/quality/docs/qualityhome.tsp).
3. When the input voltage (VI) at any pin exceeds power supplies (VI < GND or VI > V), the current at that pin should be limited to 5 mA.

#### ESD Ratings

|  |  |  |  |
| --- | --- | --- | --- |
|  | | **VALUE** | **UNIT** |
| LMT84DCK-Q1 in SC70 package | | | |
| V(ESD) Electrostatic discharge | Human-body model (HBM), per AEC Q100-002 (1) | ±2500 | V |
| Charged-device model (CDM), per AEC Q100-011 | ±1000 |

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

#### Recommended Operating Conditions

|  |  |  |
| --- | --- | --- |
|  | **MIN MAX** | **UNIT** |
| Specified temperature | TMIN ≤ TA ≤ TMAX | °C |
| −50 ≤ TA ≤ 150 | °C |
| Supply voltage (VDD) | 1.5 5.5 | V |

* 1. **Thermal Information(1)**

|  |  |  |  |
| --- | --- | --- | --- |
| **THERMAL METRIC(2)** | | **LMT84-Q1** | **UNIT** |
| **DCK (SOT/SC70)** |
| **5 PINS** |
| RθJA | Junction-to-ambient thermal resistance (3)(4) | 275 | °C/W |
| RθJC(top) | Junction-to-case (top) thermal resistance | 84 | °C/W |
| RθJB | Junction-to-board thermal resistance | 56 | °C/W |
| ψJT | Junction-to-top characterization parameter | 1.2 | °C/W |
| ψJB | Junction-to-board characterization parameter | 55 | °C/W |

1. For information on self-heating and thermal response time, see section [*Mounting and Thermal Conductivity*](#_bookmark23).
2. For more information about traditional and new thermal metrics, see the [*IC Package Thermal Metrics*](http://www.ti.com/lit/pdf/spra953) application report.
3. The junction to ambient thermal resistance (RθJA) under natural convection is obtained in a simulation on a JEDEC-standard, High-K board as specified in JESD51-7, in an environment described in JESD51-2. Exposed pad packages assume that thermal vias are included in the PCB, per JESD 51-5.
4. Changes in output due to self-heating can be computed by multiplying the internal dissipation by the thermal resistance.

#### Accuracy Characteristics

These limits do not include DC load regulation. These stated accuracy limits are with reference to the values in [Table 3](#_bookmark19).

|  |  |  |  |
| --- | --- | --- | --- |
| **PARAMETER** | **TEST CONDITIONS** | **MIN(1) TYP(2) MAX(1)** | **UNIT** |
| Temperature accuracy (3) | 70°C to 150°C; VDD = 1.5 V to 5.5 V | –2.7 ±0.6 2.7 | °C |
| 0°C to 70°C; VDD = 1.5 V to 5.5 V | –2.7 ±0.9 2.7 | °C |
| –50°C to +0°C; VDD = 1.6 V to 5.5 V | –2.7 ±0.9 2.7 | °C |
| –50°C to +150°C; VDD = 2.3 V to 5.5 V | ±0.4 | °C |

1. Limits are specified to TI's AOQL (Average Outgoing Quality Level).
2. Typicals are at TJ = TA = 25°C and represent most likely parametric norm.
3. Accuracy is defined as the error between the measured and reference output voltages, tabulated in [Table 3](#_bookmark19) at the specified conditions of supply gain setting, voltage, and temperature (expressed in °C). Accuracy limits include line regulation within the specified conditions. Accuracy limits do not include load regulation; they assume no DC load.

#### Electrical Characteristics

Unless otherwise noted, these specifications apply for VDD = +1.5 V to +5.5 V. minimum and maximum limits apply for TA = TJ

= TMIN to TMAX; typical values apply for TA = TJ = 25°C.

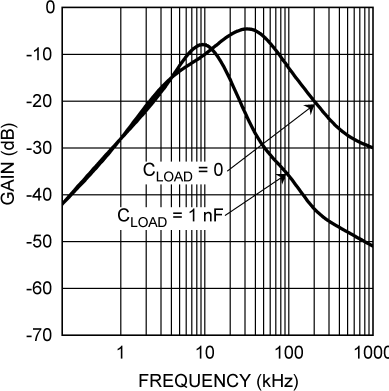
|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **PARAMETER** | | **TEST CONDITIONS** | **MIN(1)** | **TYP(2)** | **MAX (1)** | **UNIT** |
| Sensor gain | |  | –5.5 | | | mV/°C |
| Load regulation (3) | | Source ≤ 50 μA, (VDD – VOUT) ≥ 200 mV | –1 | –0.22 |  | mV |
| Sink ≤ 50 μA, VOUT ≥ 200 mV | 0.26 1 | | | mV |
| Line regulation (4) | |  | 200 | | | μV/V |
| IS | Supply current | TA = 30°C to 150°C, (VDD – VOUT) ≥ 100 mV |  | 5.4 | 8.1 | μA |
| TA = –50°C to 150°C, (VDD – VOUT) ≥ 100 mV | 5.4 9 | | | μA |
| CL | Output load capacitance |  | 1100 | | | pF |
| Power-on time (5) | | CL= 0 pF to 1100 pF |  | 0.7 | 1.9 | ms |
| Output drive | |  | ±50 | | | µA |

1. Limits are specific to TI's AOQL (Average Outgoing Quality Level).
2. Typicals are at TJ = TA = 25°C and represent most likely parametric norm.
3. Source currents are flowing out of the LMT84-xx. Sink currents are flowing into the LMT84-xx.
4. Line regulation (DC) is calculated by subtracting the output voltage at the highest supply voltage from the output voltage at the lowest supply voltage. The typical DC line regulation specification does not include the output voltage shift discussed in [*Output Voltage Shift*](#_bookmark27).
5. Specified by design and characterization.

#### Typical Characteristics

TEMPERATURE ERROR (ºC)

|  |  |
| --- | --- |
| 4  3  2  1  0  -1  -2  -3  -4  -50 -25 0 25 50 75 100 125 150  TEMPERATURE (ºC)  **Figure 1. Temperature Error vs Temperature** | **Figure 2. Minimum Operating Temperature vs Supply Voltage** |
| **Figure 3. Supply Current vs Temperature** | **Figure 4. Supply Current vs Supply Voltage** |
| 100  **Figure 5. Load Regulation, Sourcing Current** | **Figure 6. Load Regulation, Sinking Current** |

**Typical Characteristics (continued)**

|  |  |
| --- | --- |
| **Figure 7. Change in Vout vs Overhead Voltage** | 1000  **Figure 8. Supply-Noise Gain vs Frequency** |
| **Figure 9. Output Voltage vs Supply Voltage** | |

### Detailed Description

#### Overview

The LMT84-Q1 is an analog output temperature sensor. The temperature-sensing element is comprised of a simple base emitter junction that is forward biased by a current source. The temperature-sensing element is then buffered by an amplifier and provided to the OUT pin. The amplifier has a simple push-pull output stage thus providing a low impedance output source.

#### Functional Block Diagram

Full-Range Celsius Temperature Sensor (−50°C to +150°C)

VDD

OUT



Thermal Diodes

GND

#### Feature Description

##### LMT84 Transfer Function

The output voltage of the LMT84-Q1, across the complete operating temperature range, is shown in [Table 3](#_bookmark19). This table is the reference from which the LMT84-Q1 accuracy specifications (listed in the [*Accuracy*](#_bookmark11)[*Characteristics*](#_bookmark11) section) are determined. This table can be used, for example, in a host processor look-up table. A file containing this data is available for download at the [LMT84-Q1](http://www.ti.com/product/lmt84-q1) product folder under *Tools and Software Models*.

**Table 3. LMT84-Q1 Transfer Table**

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **TEMP (°C)** | **VOUT (mV)** |  | **TEMP (°C)** | **VOUT (mV)** |  | **TEMP (°C)** | **VOUT (mV)** |  | **TEMP (°C)** | **VOUT (mV)** |  | **TEMP (°C)** | **VOUT (mV)** |
| –50 | 1299 |  | -10 | 1088 |  | 30 | 871 |  | 70 | 647 |  | 110 | 419 |
| –49 | 1294 |  | -9 | 1082 |  | 31 | 865 |  | 71 | 642 |  | 111 | 413 |
| –48 | 1289 |  | -8 | 1077 |  | 32 | 860 |  | 72 | 636 |  | 112 | 407 |
| –47 | 1284 |  | -7 | 1072 |  | 33 | 854 |  | 73 | 630 |  | 113 | 401 |
| –46 | 1278 |  | -6 | 1066 |  | 34 | 849 |  | 74 | 625 |  | 114 | 396 |
| –45 | 1273 |  | -5 | 1061 |  | 35 | 843 |  | 75 | 619 |  | 115 | 390 |
| –44 | 1268 |  | -4 | 1055 |  | 36 | 838 |  | 76 | 613 |  | 116 | 384 |
| –43 | 1263 |  | -3 | 1050 |  | 37 | 832 |  | 77 | 608 |  | 117 | 378 |
| –42 | 1257 |  | -2 | 1044 |  | 38 | 827 |  | 78 | 602 |  | 118 | 372 |
| –41 | 1252 |  | -1 | 1039 |  | 39 | 821 |  | 79 | 596 |  | 119 | 367 |
| –40 | 1247 |  | 0 | 1034 |  | 40 | 816 |  | 80 | 591 |  | 120 | 361 |
| –39 | 1242 |  | 1 | 1028 |  | 41 | 810 |  | 81 | 585 |  | 121 | 355 |

#### Feature Description (continued)

##### Table 3. LMT84-Q1 Transfer Table (continued)

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **TEMP (°C)** | **VOUT (mV)** |  | **TEMP (°C)** | **VOUT (mV)** |  | **TEMP (°C)** | **VOUT (mV)** |  | **TEMP (°C)** | **VOUT (mV)** |  | **TEMP (°C)** | **VOUT (mV)** |
| –38 | 1236 |  | 2 | 1023 |  | 42 | 804 |  | 82 | 579 |  | 122 | 349 |
| –37 | 1231 |  | 3 | 1017 |  | 43 | 799 |  | 83 | 574 |  | 123 | 343 |
| –36 | 1226 |  | 4 | 1012 |  | 44 | 793 |  | 84 | 568 |  | 124 | 337 |
| –35 | 1221 |  | 5 | 1007 |  | 45 | 788 |  | 85 | 562 |  | 125 | 332 |
| –34 | 1215 |  | 6 | 1001 |  | 46 | 782 |  | 86 | 557 |  | 126 | 326 |
| –33 | 1210 |  | 7 | 996 |  | 47 | 777 |  | 87 | 551 |  | 127 | 320 |
| –32 | 1205 |  | 8 | 990 |  | 48 | 771 |  | 88 | 545 |  | 128 | 314 |
| –31 | 1200 |  | 9 | 985 |  | 49 | 766 |  | 89 | 539 |  | 129 | 308 |
| –30 | 1194 |  | 10 | 980 |  | 50 | 760 |  | 90 | 534 |  | 130 | 302 |
| –29 | 1189 |  | 11 | 974 |  | 51 | 754 |  | 91 | 528 |  | 131 | 296 |
| –28 | 1184 |  | 12 | 969 |  | 52 | 749 |  | 92 | 522 |  | 132 | 291 |
| –27 | 1178 |  | 13 | 963 |  | 53 | 743 |  | 93 | 517 |  | 133 | 285 |
| –26 | 1173 |  | 14 | 958 |  | 54 | 738 |  | 94 | 511 |  | 134 | 279 |
| –25 | 1168 |  | 15 | 952 |  | 55 | 732 |  | 95 | 505 |  | 135 | 273 |
| –24 | 1162 |  | 16 | 947 |  | 56 | 726 |  | 96 | 499 |  | 136 | 267 |
| –23 | 1157 |  | 17 | 941 |  | 57 | 721 |  | 97 | 494 |  | 137 | 261 |
| –22 | 1152 |  | 18 | 936 |  | 58 | 715 |  | 98 | 488 |  | 138 | 255 |
| –21 | 1146 |  | 19 | 931 |  | 59 | 710 |  | 99 | 482 |  | 139 | 249 |
| –20 | 1141 |  | 20 | 925 |  | 60 | 704 |  | 100 | 476 |  | 140 | 243 |
| –19 | 1136 |  | 21 | 920 |  | 61 | 698 |  | 101 | 471 |  | 141 | 237 |
| –18 | 1130 |  | 22 | 914 |  | 62 | 693 |  | 102 | 465 |  | 142 | 231 |
| –17 | 1125 |  | 23 | 909 |  | 63 | 687 |  | 103 | 459 |  | 143 | 225 |
| –16 | 1120 |  | 24 | 903 |  | 64 | 681 |  | 104 | 453 |  | 144 | 219 |
| –15 | 1114 |  | 25 | 898 |  | 65 | 676 |  | 105 | 448 |  | 145 | 213 |
| –14 | 1109 |  | 26 | 892 |  | 66 | 670 |  | 106 | 442 |  | 146 | 207 |
| –13 | 1104 |  | 27 | 887 |  | 67 | 664 |  | 107 | 436 |  | 147 | 201 |
| –12 | 1098 |  | 28 | 882 |  | 68 | 659 |  | 108 | 430 |  | 148 | 195 |
| –11 | 1093 |  | 29 | 876 |  | 69 | 653 |  | 109 | 425 |  | 149 | 189 |
|  |  |  |  |  |  |  |  |  |  |  |  | 150 | 183 |

Although the LMT84-Q1 is very linear, the response does have a slight umbrella parabolic shape. This shape is very accurately reflected in [Table 3](#_bookmark19). The transfer table can be calculated by using the parabolic equation ([Equation 1](#_bookmark20)).

V mV  870.6mV  5.506 mV T  30C  0.00176 mV T  30C2 

TEMP

 C

 

C2 

(1)

The parabolic equation is an approximation of the transfer table and the accuracy of the equation degrades slightly at the temperature range extremes. [Equation 1](#_bookmark20) can be solved for T, resulting in:

T  2  (0.00176)

5.506   5.5062  4  0.00176  870.6  VTEMP mV

 30

(2)

For an even less accurate linear approximation, a line can easily be calculated over the desired temperature range from the table using the two-point equation ([Equation 3](#_bookmark21)):

V - V =

V2 - V1  (T - T )

1

where

T2 - T1  1

* + - * V is in mV,
      * T is in °C,
      * T1 and V1 are the coordinates of the lowest temperature,
      * and T2 and V2 are the coordinates of the highest temperature. (3)

For example, if the user wanted to resolve this equation, over a temperature range of 20°C to 50°C, they would proceed as follows:

V - 925 mV =

760 mV - 925 mV  (T - 20oC)

50oC - 20oC 

V - 925 mV = (-5.50 mV / oC)  (T - 20oC) V = (-5.50 mV / oC)  T + 1035 mV

(4)

(5)

Using this method of linear approximation, the transfer function can be approximated for one or more temperature ranges of interest.

#### Device Functional Modes

##### Mounting and Thermal Conductivity

The LMT84-Q1 can be applied easily in the same way as other integrated-circuit temperature sensors. It can be glued or cemented to a surface.

To ensure good thermal conductivity, the backside of the LMT84 die is directly attached to the GND pin. The temperatures of the lands and traces to the other leads of the LMT84-Q1 will also affect the temperature reading.

Alternatively, the LMT84-Q1 can be mounted inside a sealed-end metal tube, and can then be dipped into a bath or screwed into a threaded hole in a tank. As with any IC, the LMT84 and accompanying wiring and circuits must be kept insulated and dry, to avoid leakage and corrosion. This is especially true if the circuit may operate at cold temperatures where condensation can occur. If moisture creates a short circuit from the output to ground or VDD, the output from the LMT84-Q1 will not be correct. Printed-circuit coatings are often used to ensure that moisture cannot corrode the leads or circuit traces.

The thermal resistance junction to ambient (RθJA or θJA) is the parameter used to calculate the rise of a device junction temperature due to its power dissipation. Use [Equation 7](#_bookmark24) to calculate the rise in the LMT84-Q1 die temperature:

TJ = TA + JA (VDDIS ) + (VDD - VO ) IL 

where

* TA is the ambient temperature,
* IS is the supply current,
* ILis the load current on the output,
* and VO is the output voltage. (7)

For example, in an application where TA = 30°C, VDD = 5 V, IS = 5.4 μA, VOUT = 871 mV, and IL = 2 μA, the junction temperature would be 30.015°C, showing a self-heating error of only 0.015°C. Because the junction temperature of the LMT84 device is the actual temperature being measured, take care to minimize the load current that the LMT84 is required to drive. [*Thermal Information(1)*](#_bookmark10) shows the thermal resistance of the LMT84- Q1.

##### Output Noise Considerations

A push-pull output gives the LMT84-Q1 the ability to sink and source significant current. This is beneficial when, for example, driving dynamic loads like an input stage on an analog-to-digital converter (ADC). In these applications the source current is required to quickly charge the input capacitor of the ADC. The LMT84 is ideal for this and other applications which require strong source or sink current.

The LMT84-Q1 supply-noise gain (the ratio of the AC signal on VOUT to the AC signal on VDD) was measured during bench tests. The typical attenuation is shown in [Figure 8](#_bookmark14) found in the [*Typical Characteristics*](#_bookmark13) section. A load capacitor on the output can help to filter noise.

For operation in very noisy environments, some bypass capacitance should be present on the supply within approximately 5 centimeters of the LMT84-Q1.

(1) For information on self-heating and thermal response time, see section [*Mounting and Thermal Conductivity*](#_bookmark23).

#### Device Functional Modes (continued)

##### Capacitive Loads

The LMT84-Q1 handles capacitive loading well. In an extremely noisy environment, or when driving a switched sampling input on an ADC, it may be necessary to add some filtering to minimize noise coupling. Without any precautions, the LMT84-Q1 can drive a capacitive load less than or equal to 1100 pF as shown in [Figure 10](#_bookmark25). For capacitive loads greater than 1100 pF, a series resistor may be required on the output, as shown in [Figure 11](#_bookmark26).

VDD



**LMT84**

OPTIONAL BYPASS CAPACITANCE

GND

OUT

CLOAD :: 1100 pF

##### Figure 10. LMT84-Q1 No Decoupling Required for Capacitive Loads Less Than 1100 pF

VDD



RS

**LMT84**

OPTIONAL BYPASS CAPACITANCE

GND

OUT

CLOAD > 1100 pF

##### Figure 11. LMT84-Q1 With Series Resistor for Capacitive Loading Greater Than 1100 pF

**Table 4. Recommended Series Resistor Values**

|  |  |
| --- | --- |
| **CLOAD** | **MINIMUM RS** |
| 1.1 nF to 99 nF | 3 kΩ |
| 100 nF to 999 nF | 1.5 kΩ |
| 1 μF | 800 Ω |

##### Output Voltage Shift

The LMT84-Q1 is very linear over temperature and supply voltage range. Due to the intrinsic behavior of an NMOS or PMOS rail-to-rail buffer, a slight shift in the output can occur when the supply voltage is ramped over the operating range of the device. The location of the shift is determined by the relative levels of VDD and VOUT. The shift typically occurs when VDD – VOUT = 1 V.

This slight shift (a few millivolts) takes place over a wide change (approximately 200 mV) in VDD or VOUT. Because the shift takes place over a wide temperature change of 5°C to 20°C, VOUT is always monotonic. The accuracy specifications in the [*Accuracy Characteristics*](#_bookmark11) table already include this possible shift.

### Application and Implementation

##### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

* 1. **Applications Information**

The LMT84-Q1 features make it suitable for many general temperature-sensing applications. It can operate down to 1.5-V supply with 5.4-µA power consumption, making it ideal for battery-powered devices.

#### Typical Applications

##### Connection to an ADC

Simplified Input Circuit of SAR Analog-to-Digital Converter

+1.5V to +5.5V



Reset

Input Pin

RMUX

RSS Sample

CFILTER

CMUX

CSAMPLE

CBP

**LMT84**

**VDD OUT GND**

##### Figure 12. Suggested Connection to a Sampling Analog-to-Digital Converter Input Stage

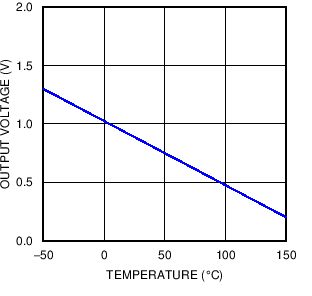
###### *Design Requirements*

Most CMOS ADCs found in microcontrollers and ASICs have a sampled data comparator input structure. When the ADC charges the sampling cap, it requires instantaneous charge from the output of the analog source such as the LMT84-Q1 temperature sensor and many op amps. This requirement is easily accommodated by the addition of a capacitor (CFILTER).

###### *Detailed Design Procedure*

The size of CFILTER depends on the size of the sampling capacitor and the sampling frequency. Because not all ADCs have identical input stages, the charge requirements will vary. This general ADC application is shown as an example only.

* + - * ***Application Curve***



**Figure 13. Analog Output Transfer Function**

#### Typical Applications (continued)

##### Conserving Power Dissipation With Shutdown



**LMT84**

SHUTDOWN

Any logic device output

VDD

VOUT

##### Figure 14. Simple Shutdown Connection of the LMT84-Q1

###### *Design Requirements*

Because the power consumption of the LMT84-Q1 is less than 9 µA, it can simply be powered directly from any logic gate output and therefore not require a specific shutdown pin. The device can even be powered directly from a microcontroller GPIO. In this way, it can easily be turned off for cases such as battery-powered systems where power savings are critical.

###### *Detailed Design Procedure*

Simply connect the VDD pin of the LMT84-Q1 directly to the logic shutdown signal from a microcontroller.

* + - * ***Application Curves***

|  |  |
| --- | --- |
| Time: 500 µs/div; Top trace: VDD 1 V/div; Bottom trace: OUT 1 V/div  **Figure 15. Output Turnon Response Time Without a Capacitive Load and VDD= 3.3 V** | Time: 500 µs/div; Top trace: VDD 2 V/div; Bottom trace: OUT 1 V/div  **Figure 16. Output Turnon Response Time Without a Capacitive Load and VDD= 5 V** |
| Time: 500 µs/div; Top trace: VDD 1 V/div; Bottom trace: OUT 1 V/div  **Figure 17. Output Turnon Response Time With 1.1-Nf Capacitive Load and VDD= 3.3 V** | Time: 500 µs/div; Top trace: VDD 2 V/div; Bottom trace: OUT 1 V/div  **Figure 18. Output Turnon Response Time With 1.1-Nf Capacitive Load and VDD= 5 V** |

### Power Supply Recommendations

The low supply current and supply range (1.5 V to 5.5 V) of the LMT84-Q1 allow the device to easily be powered from many sources. Power supply bypassing is optional and is mainly dependent on the noise on the power supply used. In noisy systems, it may be necessary to add bypass capacitors to lower the noise that is coupled to the output of the LMT84-Q1.

### Layout

#### Layout Guidelines

The LMT84-Q1 is extremely simple to layout. If a power-supply bypass capacitor is used, is should be connected as shown in the [*Layout Examples*](#_bookmark34).

#### Layout Examples

 VIA to ground plane  VIA to power plane

OUT



GND



0.01µ F

VDD

GND



GND

**Figure 19. SC70 Package Recommended Layout**

### Device and Documentation Support

#### Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

#### Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of](http://www.ti.com/corp/docs/legal/termsofuse.shtml) [Use](http://www.ti.com/corp/docs/legal/termsofuse.shtml).

[**TI E2E™ Online Community**](http://e2e.ti.com/) ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

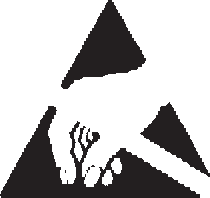
[**Design Support**](http://support.ti.com/) ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

#### Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

#### Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

#### Glossary

[SLYZ022](http://www.ti.com/lit/pdf/SLYZ022) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

### Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

# PACKAGE OPTION ADDENDUM

[www.ti.com](http://www.ti.com/) 10-Dec-2020

#### PACKAGING INFORMATION

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Orderable Device** | **Status**  (1) | **Package Type** | **Package Drawing** | **Pins** | **Package Qty** | **Eco Plan**  (2) | **Lead finish/ Ball material**  (6) | **MSL Peak Temp**  (3) | **Op Temp (°C)** | **Device Marking**  (4/5) | **Samples** |
| LMT84QDCKRQ1 | ACTIVE | SC70 | DCK | 5 | 3000 | RoHS & Green | SN | Level-1-260C-UNLIM | -50 to 150 | BOA |  |
| LMT84QDCKTQ1 | ACTIVE | SC70 | DCK | 5 | 250 | RoHS & Green | SN | Level-1-260C-UNLIM | -50 to 150 | BOA |  |

**(1)** The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

**(2) RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**(6)** Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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Addendum-Page 1

# PACKAGE OPTION ADDENDUM

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**OTHER QUALIFIED VERSIONS OF LMT84-Q1 :**

* Catalog: [LMT84](http://focus.ti.com/docs/prod/folders/print/lmt84.html)

NOTE: Qualified Version Definitions:

* Catalog - TI's standard catalog product

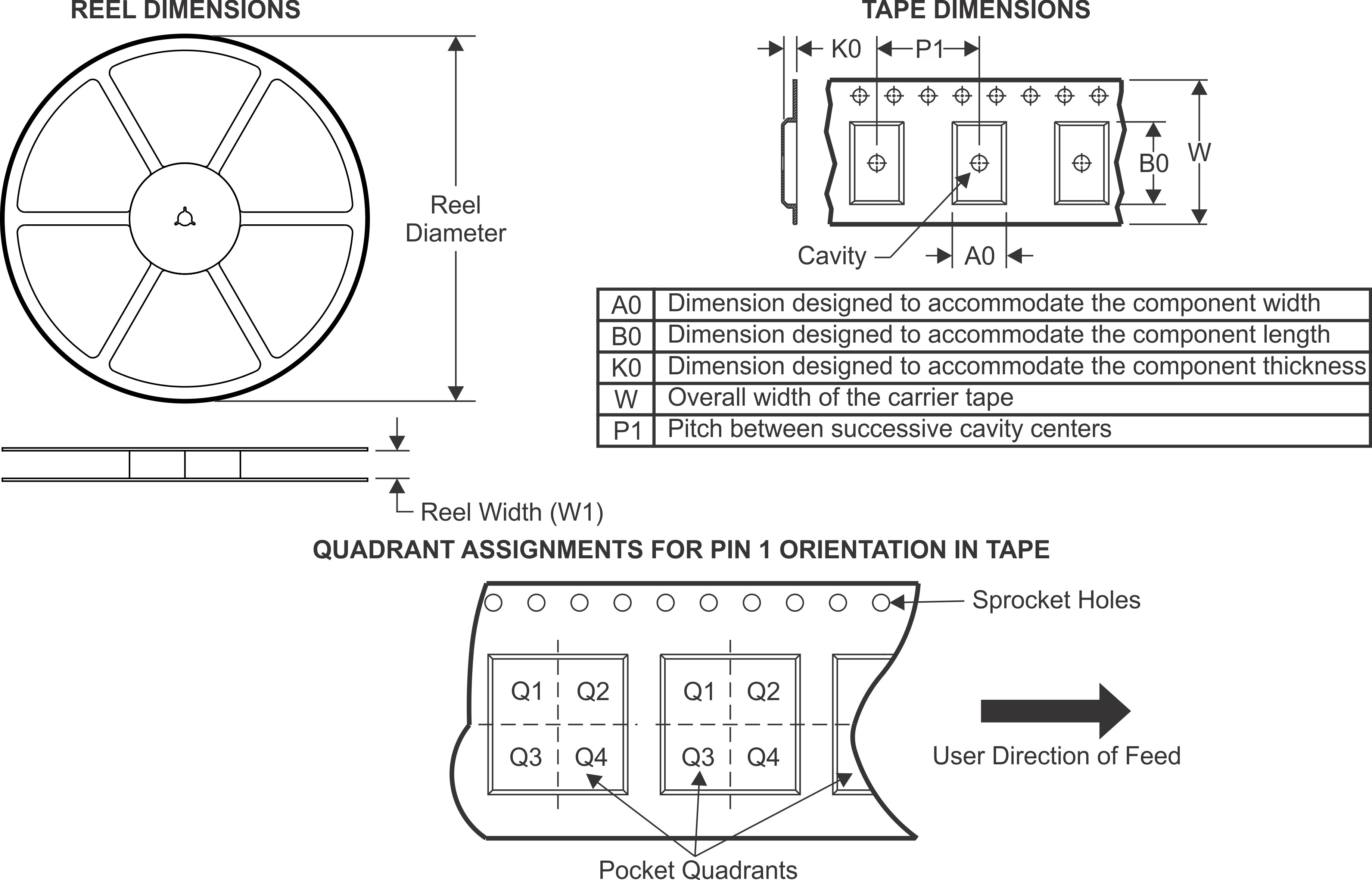
Addendum-Page 2

# PACKAGE MATERIALS INFORMATION



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#### TAPE AND REEL INFORMATION



\*All dimensions are nominal

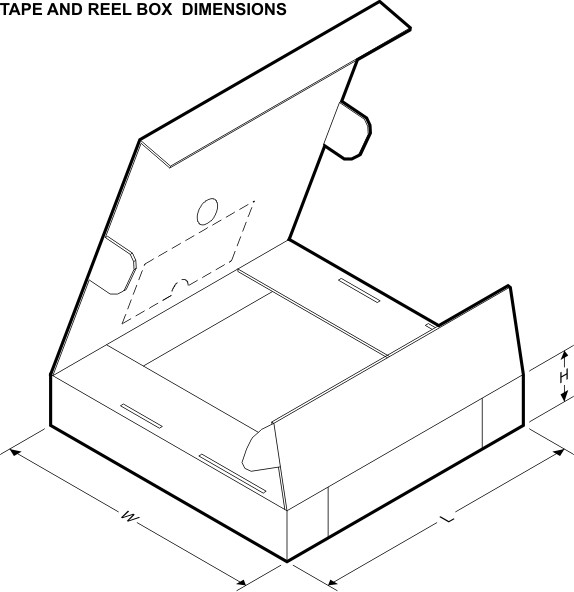
|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Device** | **Package Type** | **Package Drawing** | **Pins** | **SPQ** | **Reel Diameter (mm)** | **Reel Width W1 (mm)** | **A0**  **(mm)** | **B0**  **(mm)** | **K0**  **(mm)** | **P1**  **(mm)** | **W**  **(mm)** | **Pin1 Quadrant** |
| LMT84QDCKRQ1 | SC70 | DCK | 5 | 3000 | 178.0 | 8.4 | 2.25 | 2.45 | 1.2 | 4.0 | 8.0 | Q3 |
| LMT84QDCKTQ1 | SC70 | DCK | 5 | 250 | 178.0 | 8.4 | 2.25 | 2.45 | 1.2 | 4.0 | 8.0 | Q3 |

Pack Materials-Page 1

# PACKAGE MATERIALS INFORMATION



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\*All dimensions are nominal

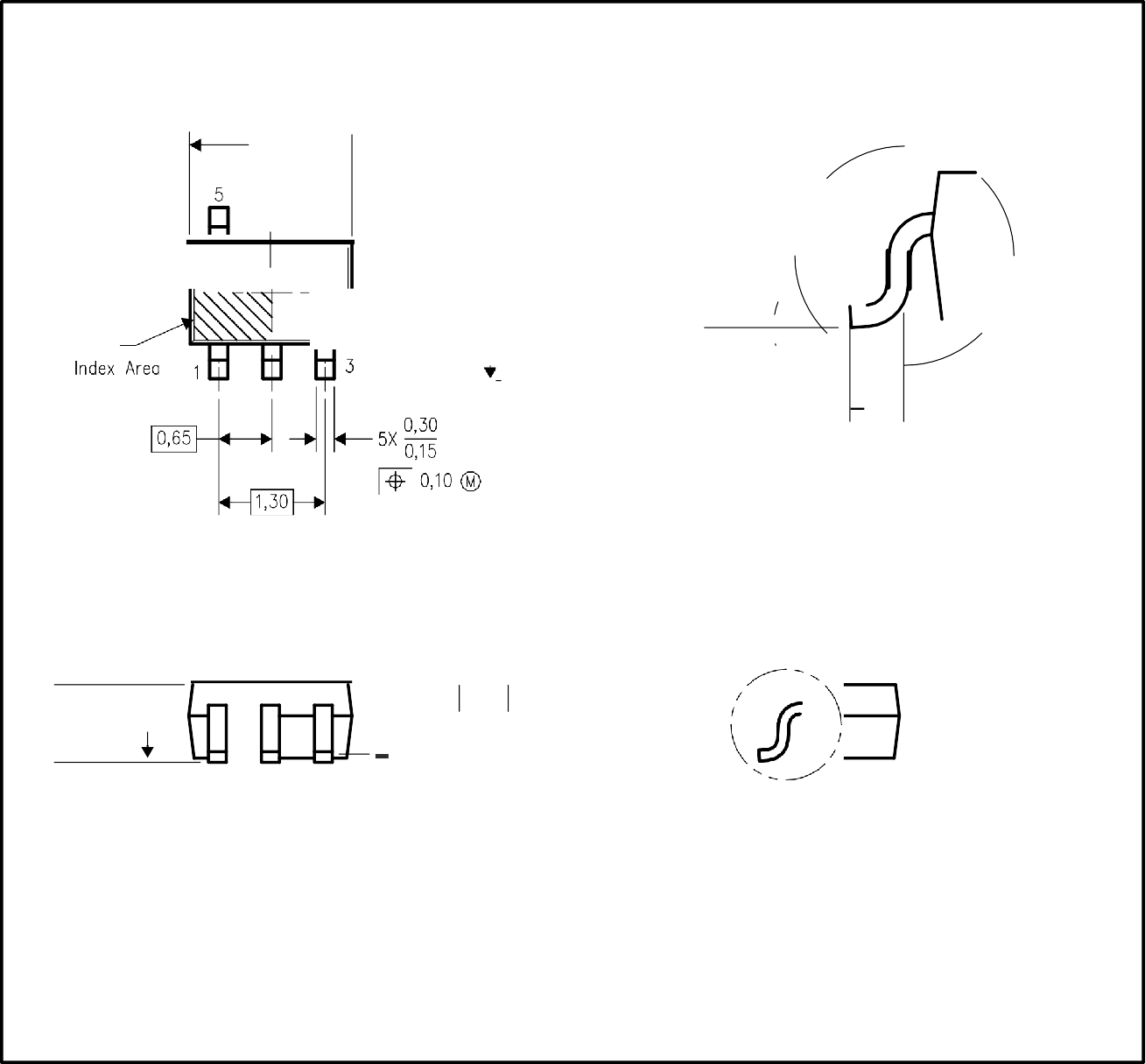
|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Device** | **Package Type** | **Package Drawing** | **Pins** | **SPQ** | **Length (mm)** | **Width (mm)** | **Height (mm)** |
| LMT84QDCKRQ1 | SC70 | DCK | 5 | 3000 | 208.0 | 191.0 | 35.0 |
| LMT84QDCKTQ1 | SC70 | DCK | 5 | 250 | 208.0 | 191.0 | 35.0 |

Pack Materials-Page 2

## MECHANICAL DATA



**DCK (R-PDSO-G5) PLASTIC SMALL-OUTLINE PACKAGE**



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2,40

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Sealing Pla e

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**~~t~~** Seating Pl ane

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4093553-3/G 01/2007

NOTES: A. AII linear dimensions are in millimeters.

1. This drawing is sub ject to change wi t hout notice.
2. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
3. Falls within JEDEC M0 - 203 variation AA.



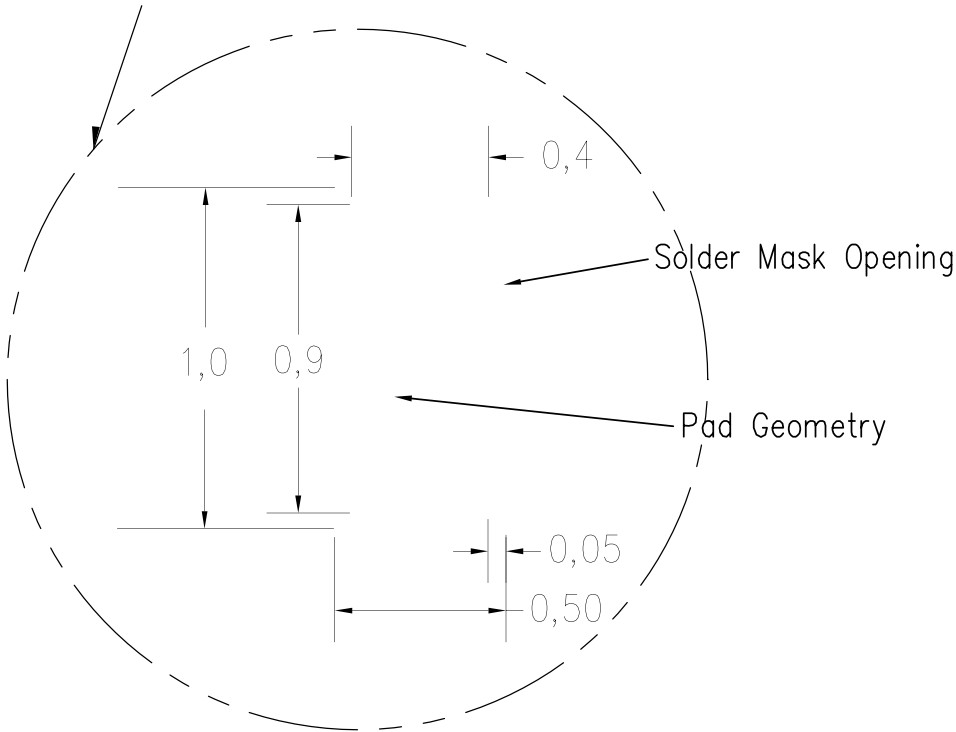
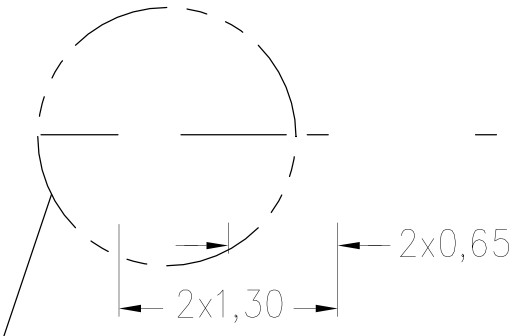
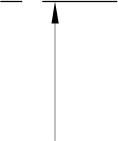


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## LAND PATTERN DATA

OCK (R-PDSO-GS) PLASTIC SMALL OU TLINE



Example Board Layout

Stenc il Openings

Based on a stencil thickness

of .127mm (.005inch).

6 x 0,.35- -¡ ¡-­

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0,85

1

**\_L\_**

2,2

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**L** 2x1, .30 -J

**----1**

I

**1--** 2x0, 65

4210356-2/C 07/11

NOTES: A. AII li near dimensions are in millimeters.

1. This drawing is sub ject to change without notice.
2. Customers should place a note on the circuit board fabrication drawing not to alt er the center solder mask defined pad.
3. Publicatian IPC- 7351 is recammended far alternate designs.
4. Laser cutting apertures with trapezoidal walls and al so rounding corners will offer better paste release. Customers should contact their board assembly site far stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC- 7525 far other stencil recommendations.

***j:,.* TEY/\C-.**



**INS nUMEN-**

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