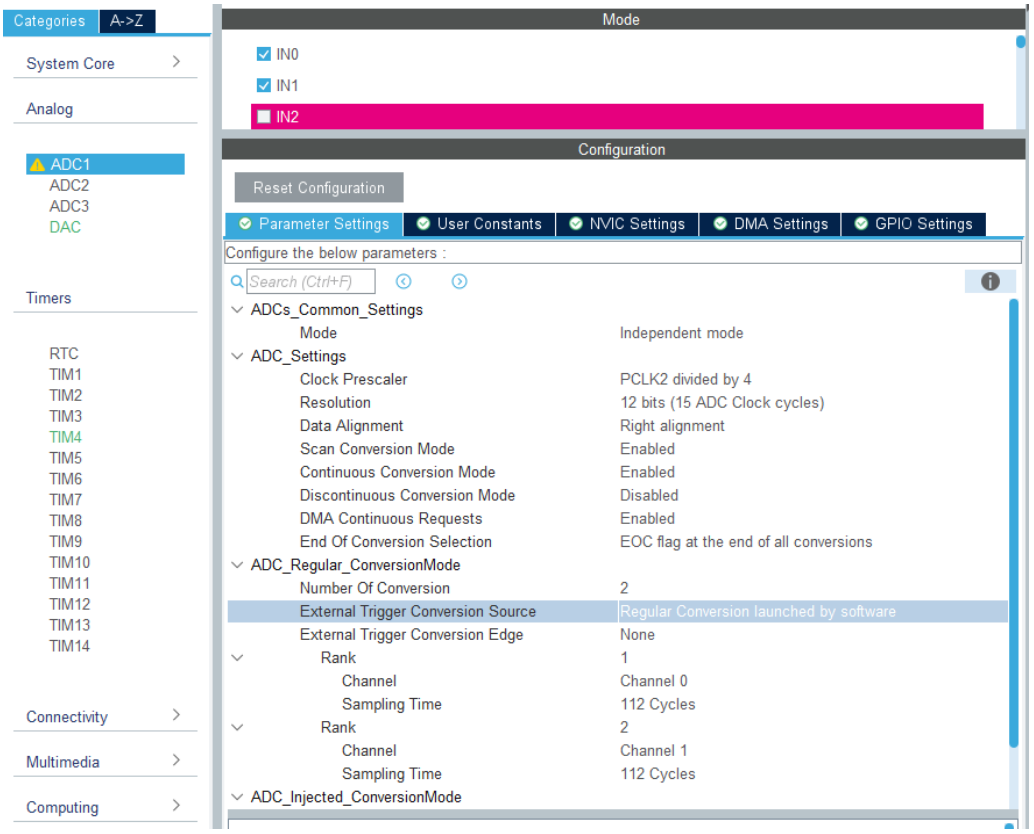
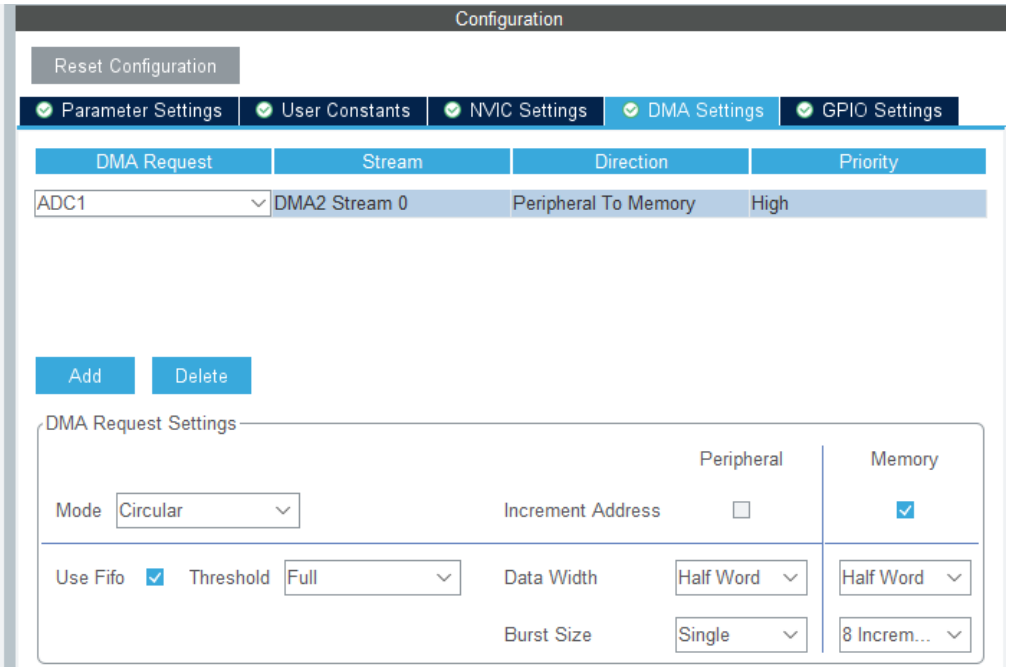
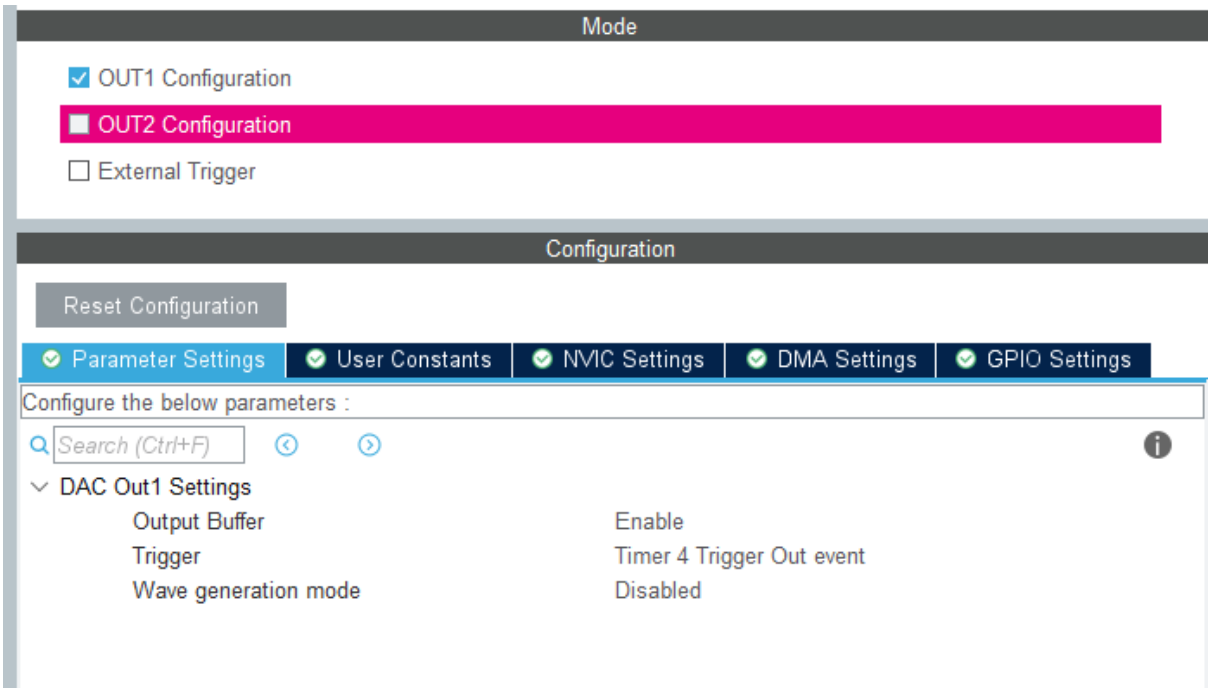
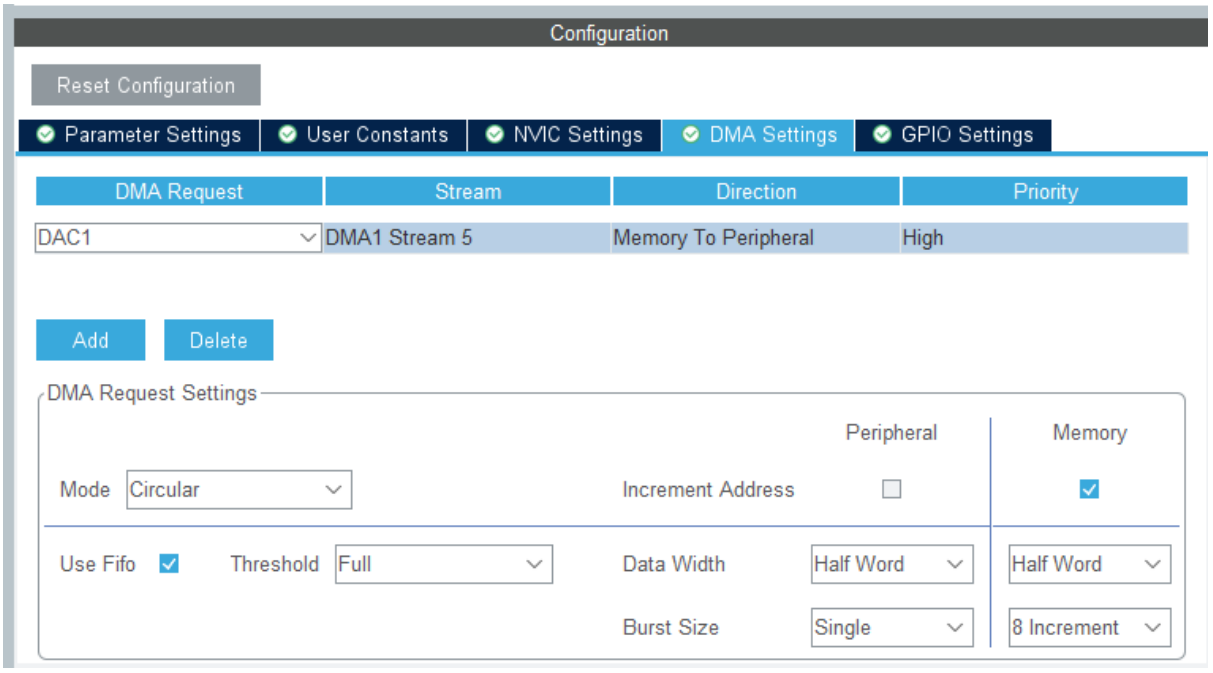
ADC:


Categories
A->Z
System Core
Analog
ADC1
ADC2
ADC3
DAC
Timers
RTC
TIM1
TIM2
TIM3
TIM4
TIM5
TIM6
TIM7
TIM8
TIM9
TIM10
TIM11
TIM12
TIM13
TIM14
Connectivity
Multimedia
Computing
Mode
IN0
IN1
IN2
Configuration
Reset Configuration
Parameter Settings
User Constants
NVIC Settings
DMA Settings
GPIO Settings
Configure the below parameters :
Search (Ctrl+F)
ADCs_Common_Settings
Mode
Independent mode
ADC_Settings
Clock Prescaler
PCLK2 divided by 4
Resolution
12 bits (15 ADC Clock cycles)
Data Alignment
Right alignment
Scan Conversion Mode
Enabled
Continuous Conversion Mode
Enabled
Discontinuous Conversion Mode
Disabled
DMA Continuous Requests
Enabled
End Of Conversion Selection
EOC flag at the end of all conversions
ADC_Regular_ConversionMode
Number Of Conversion
2
External Trigger Conversion Source
Regular Conversion launched by software
External Trigger Conversion Edge
None
Rank
1
Channel
Channel 0
Sampling Time
112 Cycles
Rank
2
Channel
Channel 1
Sampling Time
112 Cycles
ADC_Injected_ConversionMode


Configuration
Reset Configuration
Parameter Settings
User Constants
NVIC Settings
DMA Settings
GPIO Settings
DMA Request
Stream
Direction
Priority
ADC1
DMA2 Stream 0
Peripheral To Memory
High
Add
Delete
DMA Request Settings
Peripheral
Memory
Mode
Circular
Increment Address
Use Fifo
Threshold
Full
Data Width
Half Word
Half Word
Burst Size
Single
8 Increm...

DAC:


Mode
OUT1 Configuration
OUT2 Configuration
External Trigger
Configuration
Reset Configuration
Parameter Settings
User Constants
NVIC Settings
DMA Settings
GPIO Settings
Configure the below parameters :
Search (Ctrl+F)
DAC Out1 Settings
Output Buffer
Enable
Trigger
Timer 4 Trigger Out event
Wave generation mode
Disabled


Configuration
Reset Configuration
Parameter Settings
User Constants
NVIC Settings
DMA Settings
GPIO Settings
DMA Request
Stream
Direction
Priority
DAC1
DMA1 Stream 5
Memory To Peripheral
High
Add
Delete
DMA Request Settings
Peripheral
Memory
Mode
Circular
Increment Address
Use Fifo
Threshold
Full
Data Width
Half Word
Half Word
Burst Size
Single
8 Increment

TIM 4:

Mode

Slave Mode: Disable

Trigger Source: Disable

☑ Internal Clock

Channel1: Disable

Channel2: Disable

Channel3: Disable

Channel4: Disable

Combined Channels: Disable

☐ *XOR activation*

☐ One Pulse Mode

Configuration

Reset Configuration

Parameter Settings | User Constants | NVIC Settings | DMA Settings

Configure the below parameters :

Search (Ctrl+F)

Counter Settings

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	9
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Update Event