THAKUR COLLEGE OF ENGINEERING AND TECHNOLOGY

S. E. SEMESTER IV (CBCGS-HME 2020) MAY 2022

Subject: Computer Organization & Microprocessor | Branch: AI&ML

Q.P. Code: B-46005 | Total Marks: 60

Time : (2 hours)

Instructions: 1. All Sections are compulsory.
2. Figures to the right indicate full marks.
3. Assume suitable data if necessary and state the assumptions clearly.

Que No	Section-I (08 Marks) Multiple choice question(Answer any 08 questions out of 10)	Marks
1	In 8086 microprocessor the overflow flag is set when _____. a) The sum is more than 16 bits. b) Signed numbers go out of their range after an arithmetic operation. c) Carry and sign flags are set. d) Auxiliary Carry and zero flags are set	1
2	In 8086 microprocessor one of the following statements is not true? a) Coprocessor is interfaced in max mode. b) Coprocessor is interfaced in min mode. c) I /O can be interfaced in max / min mode. d) supports pipelining	1
3	The signal sent to the device from the processor to the device after receiving an interrupt is _____ a) Service signal b)Return signal c) Interrupt-acknowledge d) Permission signal	1
4	The DMA transfers are performed by a control circuit called as _____ a) Device interface b) DMA controller c) Data controller d) Over looker	1
5	Number of chips (128 x 8 RAM) needed to provide a memory capacity of 2048 bytes a) 32 b) 16 c) 8 d)4	1
6	Which of the following is the fastest means of memory access for CPU? a) Virtual Memory b) Cache c) Main memory d) Registers	1

7	_____ is to fetch the instruction stored in main memory. a) Output unit b) Input unit c) Control unit d) Memory unit	1
8	Increasing the RAM of a computer typically improves performance because a) Virtual memory increases b) Larger RAMs are faster c) Fewer page faults occur d) Fewer segmentation faults occur	1
9	Those attributes of the system which is visible to programmer is referred as: a) Computer architecture b) Computer organization c) Computer fundamental d) Computer manufacturing	1
10	---------- provide a path for moving data between system modules a) System lines b) Address lines c) Control lines d) Data lines	1
	Section-II (12 Marks)	
	Objective questions(Answer any 4)	
1.	Sketch Von-Neumann architecture & discuss it.	3
2.	Differentiate between Hardwired and Micro programmed control unit.	3
3.	Explain I/O modules with its function in detail.	3
4.	List features of 8086 microprocessor.	3
5.	Discuss is the purpose of cache memory.	3
6	Describe flag register of 8086 microprocessor.	
	Section-III (20 Marks)	
	Short Answer question(Answer any 04)	
1.	Describe various characteristics of memory.	5
2	What is cache coherency? How to resolve it?	5
3.	Solve 11 X 3 using booth's multiplication algorithm.	5
4.	Illustrate physical address generation mechanism of 8086 microprocessor with example.	5
5.	Explain various Flynn's classification of parallel processing in detail.	5
6	Discuss memory banking concept of 8086 microprocessor.	
	Section-IV (20 Marks)	
	Long Answer question (answer any 2)	
1.	Draw flowchart of Non- restoring division algorithm & solve 21 divide by 6.	10
2.	Evaluate $(-0.0400)_{10}$ in IEEE 754 single & double precision standard of floating point number representation.	10
3	Design and discuss maximum mode of 8086 microprocessor.	10