Laxdu Singh Charitable Trust's (Regd.)
THAKUR COLLEGE OF ENGINEERING & TECHNOLOGY
Website : www.tcetmumbai.in
Autonomous College Affiliated to University of Mumbai
Approved by All India Council for Technical Education(AICTE) and Government of Maharashtra(GoM)
Conferred Autonomous Status by University Grants Commission (UGC) for 10 years w.e.f. A.Y 2019-20
Amongst Top 200 Colleges in the Country, Ranked 193rd in NIRF India Ranking 2019 in Engineering College category
• ISO 9001:2015 Certified • Programmes Accredited by National Board of Accreditation (NBA), New Delhi
• Institute Accredited by National Assessment and Accreditation Council (NAAC), Bangalore
Estd. in 2001

ISE III (ST-AI&ML)
Computer Organization and Microrpocessor

Date :20/04/2022 **Time: 10:00 am to 11: 00 am**

Instructions:

1. Test begins at 10:00 am
2. Duration is 1 hr
3. You should end your ISA writing at 11:00 am
4. 5 minutes window timing is given for scanning answer sheets (preferably A4)
5. Upload your answer sheet in PDF named as **ISE_Branch_roll no_Subject name**
6. Only pdf with above name format will be considered for evaluation
7. For question no 1 solve any 10 MCQs out of 12 carries 1 marks each.(Solve in Google form).
8. Solve any one from Q2a and Q2b carries 5 marks each(to be uploaded on GCR).
9. Solve any one from Q3a and Q3b carries 5 marks each(to be uploaded on GCR).
10. Figures to the right column indicate full marks.
11. Draw a neat diagram wherever necessary.

Q 2 (A)	A block-set associative cache memory consists of 256 blocks divided into four way sets . The main memory consists of 16,384 blocks and each block contains 256 eight bit words. 1. How many bits are required for addressing the main memory? 2. How many bits are needed to represent the TAG, SET and WORD fields? 3. How many bits are needed to represent the TAG, BLOCK and WORD fields?
	OR
Q 2 (B)	Explain DMA data transfer technique in detail
Q 3 (A)	Solve following problems with FIFO, LRU and Optimal page replacement method and find page hits and page faults. Consider the page references 7, 0, 1, 2, 0, 3, 0, 4, 2, 3, 0, 3, 2, with frame size 3.
	OR
Q 3 (B)	Discuss cache coherency and Interleaved memory

Q2a. Consider six memory partitions of size 200 KB, 400 KB, 600 KB, 500 KB, 300 KB and 250 KB. These partitions need to be allocated to four processes of sizes 357 KB, 210 KB, 468 KB and 491 KB in that order. Perform the allocation of processes using-

1. First Fit Algorithm
2. Best Fit Algorithm
3. Worst Fit Algorithm 5 marks

OR

Q2b. A block-set associative cache memory consists of 128 blocks divided into four way sets . The main memory consists of 16,384 blocks and each block contains 256 eight bit words.

1. How many bits are required for addressing the main memory?
2. How many bits are needed to represent the TAG, SET and WORD fields?
3. How many bits are needed to represent the TAG, BLOCK and WORD fields? 5 marks

Q3a. Solve following problems with FIFO, LRU and Optimal page replacement method and find page hits and page faults. Consider the page references 7, 0, 1, 2, 0, 3, 0, 4, 2, 3, 0, 3, 2, with frame size 4. 5 marks

OR

Q3b. Explain different data transfer techniques in Input output management. 5 marks