**Experiment / Assignment / Tutorial No. 4**

**Grade: AA / AB / BB / BC / CC / CD /DD**

**Signature of the Staff In-charge with date**

|  |
| --- |
| **Batch: A1 Roll No.: 1911004 Experiment / assignment / tutorial No.: 4** |

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| **Title:** 4 bit Magnitude Comparator |

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**Objective:** Design a 2-bit comparator using logic gates and verify 4-bit magnitudecomparator using IC 7485

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**Expected Outcome of Experiment:**

**CO2:** Use different minimization technique and solve combinational circuits, synchronous & asynchronous sequential circuits.

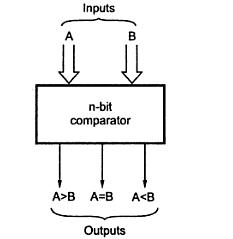
**\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_**

**Books/ Journals/ Websites referred:**

* VLab Link: <http://vlabs.iitb.ac.in/vlabs-dev/labs/dldesignlab/experimentlist.html>
* R. P. Jain, “Modern Digital Electronics”, Tata McGraw Hill
* M .Morris Mano, “Digital Logic & computer Design”, PHI
* http://elnsite.teilam.gr/ebooks/digital\_design/lab/dataSheets\_page/7485.pdf

**Pre Lab/ Prior Concepts:**

The comparison of two numbers is an operator that determines one number is greater than, less than (or) equal to the other number. A magnitude comparator is a combinational circuit that compares two numbers A and B and determines their relative magnitude. The outcome of the comparator is specified by three binary variables that indicate whether A>B, A=B (or) A<B.



**Two Bit Magnitude Comparator Implementation Details:**

**Truth Table**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **INPUT** | | | | **OUTPUT** | | |
| **A1** | **A0** | **B1** | **B0** | **A > B** | **A = B** | **A < B** |
|  |  |  |  |  |  |  |
| **0** | **0** | **0** | **0** | **0** | **1** | **0** |
|  |  |  |  |  |  |  |
| **0** | **1** | **0** | **0** | **1** | **0** | **0** |
|  |  |  |  |  |  |  |
| **1** | **0** | **0** | **0** | **1** | **0** | **0** |
|  |  |  |  |  |  |  |
| **1** | **1** | **0** | **0** | **1** | **0** | **0** |
|  |  |  |  |  |  |  |
| **0** | **0** | **0** | **1** | **0** | **0** | **1** |
|  |  |  |  |  |  |  |
| **0** | **1** | **0** | **1** | **0** | **1** | **0** |
|  |  |  |  |  |  |  |
| **1** | **0** | **0** | **1** | **1** | **0** | **0** |
|  |  |  |  |  |  |  |
| **1** | **1** | **0** | **1** | **1** | **0** | **0** |
|  |  |  |  |  |  |  |
| **0** | **0** | **1** | **0** | **0** | **0** | **1** |
|  |  |  |  |  |  |  |
| **0** | **1** | **1** | **0** | **0** | **0** | **1** |
|  |  |  |  |  |  |  |
| **1** | **0** | **1** | **0** | **0** | **1** | **0** |
|  |  |  |  |  |  |  |
| **1** | **1** | **1** | **0** | **1** | **0** | **0** |
|  |  |  |  |  |  |  |
| **0** | **0** | **1** | **1** | **0** | **0** | **1** |
|  |  |  |  |  |  |  |
| **0** | **1** | **1** | **1** | **0** | **0** | **1** |
|  |  |  |  |  |  |  |
| **1** | **0** | **1** | **1** | **0** | **0** | **1** |
|  |  |  |  |  |  |  |
| **1** | **1** | **1** | **1** | **0** | **1** | **0** |
|  |  |  |  |  |  |  |

**From the Truth Table:**

**(A<B) =** A1’A0’B1’B0 + A1’A0’B1B0’ + A1’A0B1B0’ + A1’A0’B1B0 + A1’A0B1B0 + A1A0’B1B0= (A1’A0’B1’B0 + A1’A0’B1B0) + (A1’A0’B1B0’ + A1’A0’B1B0) + (A1’A0B1B0’ + A1’A0B1B0) + (A1A0’B1B0 + A1’A0’B1B0)

= A1’A0’B0 + A1’A0’B1 + A1’A0B1 + A0’B1B0

= A1’A0’B0 + (A1’A0’B1 + A1’A0B1) + A0’B1B0

= **A1’A0’B0 + A1’B1 + A0’B1B0**

**(A=B) = A1’A0’B1’B0’ + A1’A0B1’B0 + A1A0’B1B0’ + A1A0B1B0**

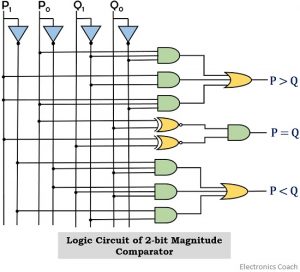
**(A>B) =** A1’A0B1’B0’ + A1A0’B1’B0’ + A1A0B1’B0’ + A1A0’B1’B0 + A1A0B1’B0 + A1A0B1B0’

= (A1’A0B1’B0’ + A1A0B1’B0’) + (A1A0’B1’B0’ + A1A0B1’B0’) + (A1A0B1’B0 + A1A0’B1’B0) + (A1A0B1B0’ + A1A0B1’B0’)

= A0B1’B0’ + A1B1’B0’ + A1B1’B0 + A1A0B0’ = A0B1’B0’ + (A1B1’B0’ + A1B1’B0) + A1A0B0’

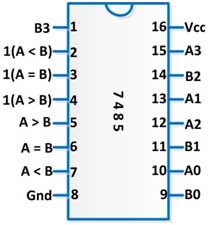
= **A0B1’B0’ + A1B1’ + A1A0B0’**

**Logic Diagram (2 bit Comparator)**

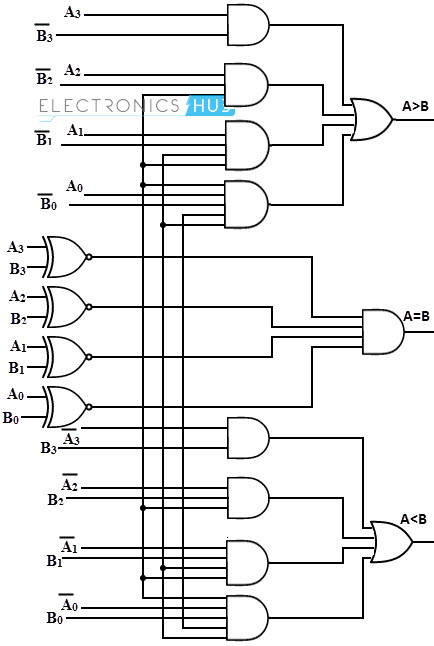


**Four Bit Magnitude Comparator Implementation Details**

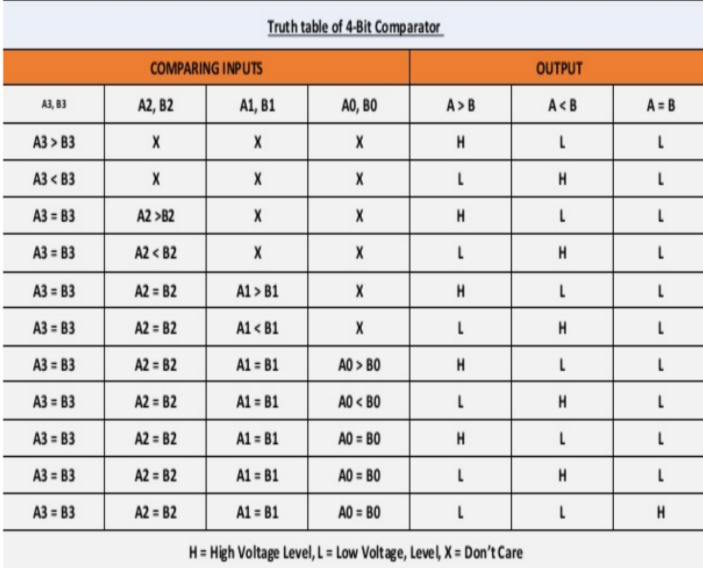
**Pin Diagram of IC 7485**



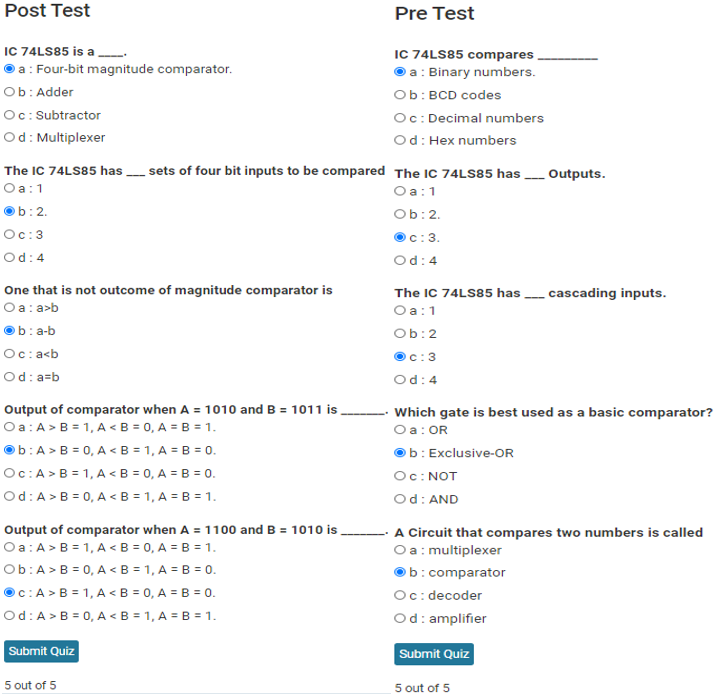
**Logic Diagram of IC 7485**



**Comparing Truth Table**



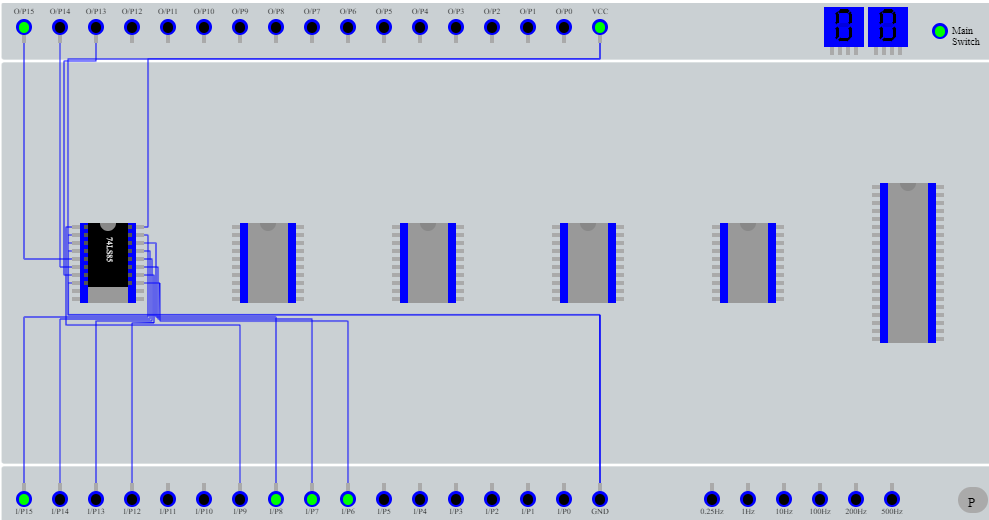
**VLAB (4-BIT COMPARATOR )**

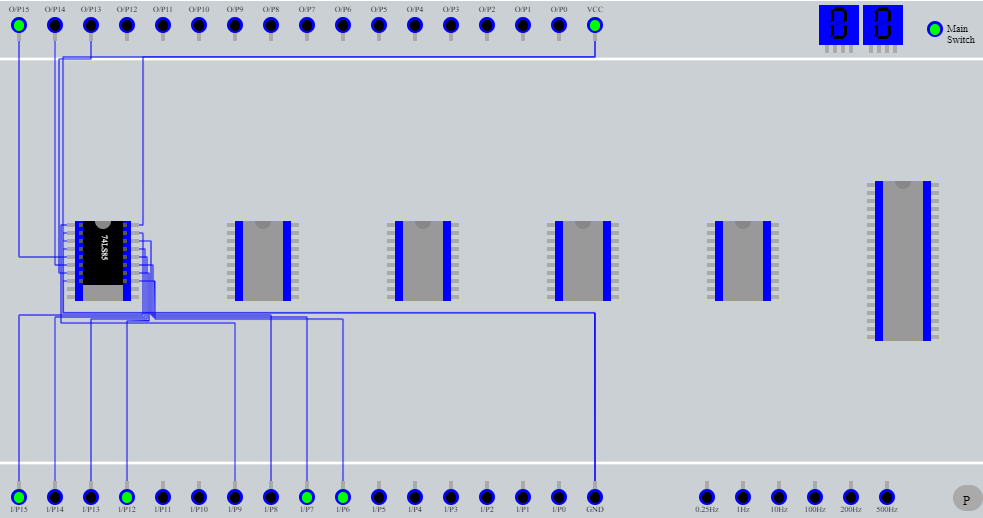


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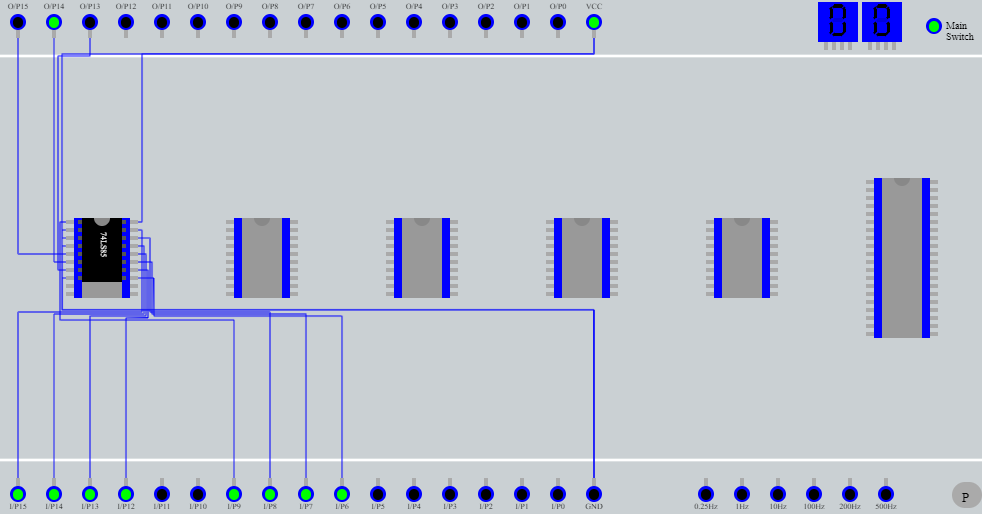
|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **INPUT**   * Input A : I/P15 to I/P12 * Input B : I/P9 to I/P6 | | | | | | | | **OUTPUT**   * A > B : O/P15 * A = B : O/P14 * A < B : O/P13 | | | |
| **A** | | | | **B** | | | | **A>B** | **A=B** | **A<B** | |
| **I/P 15** | **I/P 14** | **I/P 13** | **I/P 12** | **I/P 9** | **I/P 8** | **I/P 7** | **I/P 6** | **O/P 15** | **O/P 14** | **O/P 13** |
| **1** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **1** | **0** | **0** |
| **1** | **0** | **0** | **1** | **0** | **0** | **1** | **1** | **1** | **0** | **0** |
| **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **0** | **1** | **0** |
| **0** | **0** | **1** | **1** | **0** | **0** | **1** | **1** | **0** | **1** | **0** |
| **0** | **0** | **1** | **1** | **1** | **1** | **0** | **0** | **0** | **0** | **1** |
| **1** | **1** | **0** | **0** | **1** | **1** | **1** | **1** | **0** | **0** | **1** |

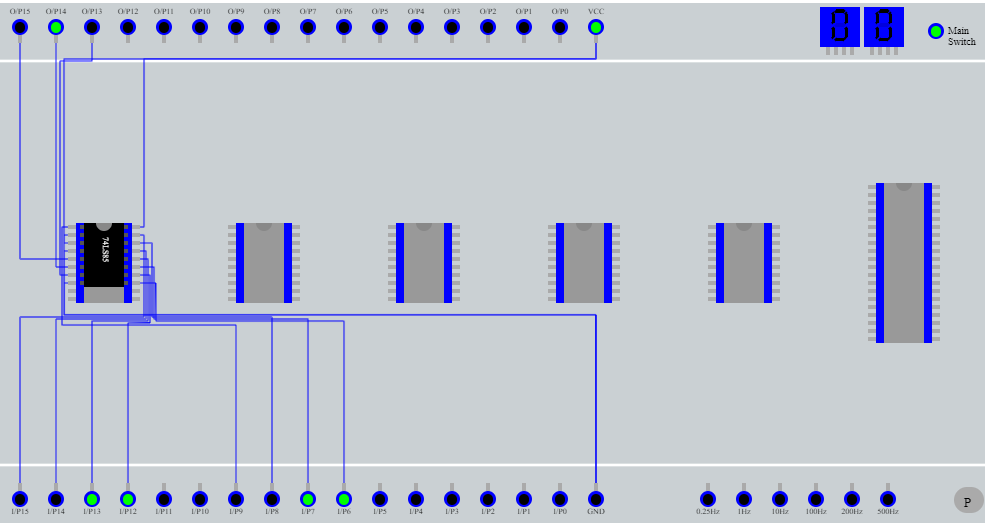
1. **A>B (O/P 15=1** **)**

**A=1000 B=0111** 

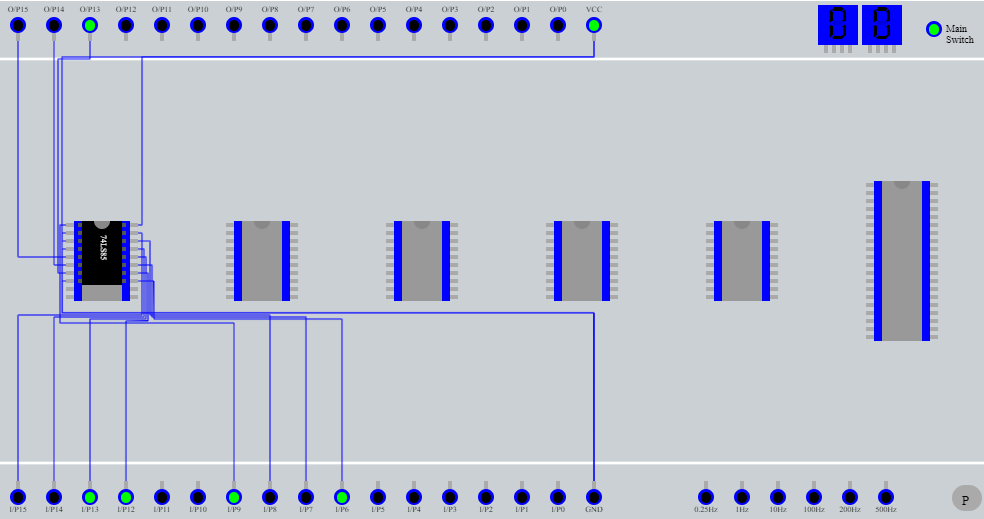
**A=1001 B=0011** 

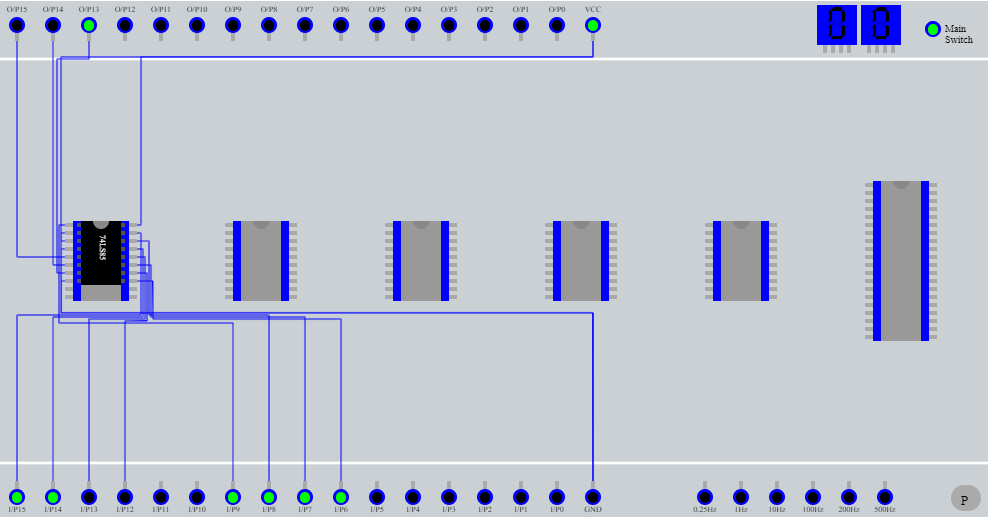
1. **A=B (O/P 14=1** **)**

**A=1111 B=1111** 

**A=0011 B=0011** 

1. **A<B (O/P 13=1** **)**

**A=0011 B=1001** 

**A=1100  B=1111**

**Conclusion:**

**We understood the concept of Comparator & their truth tables; 4-bit comparator was implemented in Virtual lab and necessary output was obtained.**

**Post Lab Descriptive Questions**

* 1. **Design a 1- bit magnitude comparator using logic gates.**

