**Experiment / Assignment / Tutorial No . 5**

**Grade: AA / AB / BB / BC / CC / CD /DD**

**Signature of the Staff In-charge with date**

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| **Batch: A1 Roll No.: 1911004 Experiment / assignment / tutorial No.: 5** |

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| **Title:** Flip Flops |

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**Objective:**Design of JK Flip flop, D flip flop, T flip flop using NAND Gates & verification of the same flip flop using IC7476

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**Expected Outcome of Experiment:**

**CO2:** Use different minimization technique and solve combinational circuits, synchronous & asynchronous sequential circuits.

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**Books/ Journals/ Websites referred:**

* VLab Link: [http://vlabs.iitkgp.ernet.in/dec/#](http://vlabs.iitkgp.ernet.in/dec/)
* R. P. Jain, “Modern Digital Electronics”, Tata McGraw Hill
* M .Morris Mano, “Digital Logic & computer Design”, PHI
* A.P.Godse, D.A.Godse, “Digital Logic Design”

**Pre Lab/ Prior Concepts:**

Flip-flop is the common name given to two-state devices which offer basic memory for sequential logic operations. Flip-flops are heavily used for digital data storage and transfer and are commonly used in banks called "registers" for the storage of binary numerical data.

**JK-flip flop:** has two inputs, traditionally labeled J and K. IC 7476 is a dual JK master slave flip flop with preset and clear inputs. If J and K are different then the output Q takes the value of J at the next clock edge. If J and K are both low then no change occurs. If J and K are both high at the clock edge, then the output will toggle from one state to the other. It can perform the functions of the set/reset flip-flop and has the advantage that there are no ambiguous states.

**D Flip Flop:** tracks the input, making transitions with match those of the input D. The D stands for "data"; this flip-flop stores the value that is on the data line. It can be thought of as a basic memory cell. D flip-flop can be made from J-K flip-flop by connecting both inputs through a not gate.

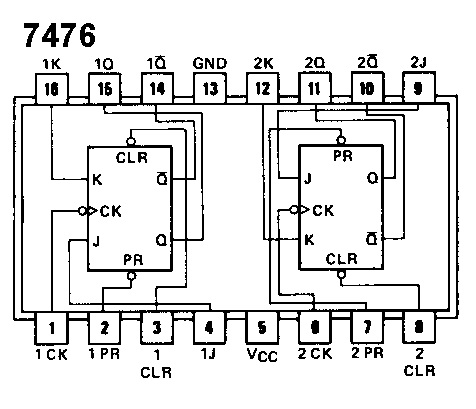
**T Flip Flop:** T or "toggle" flip-flop changes its output on each clock edge, giving an output which is half the frequency of the signal to the T input. It is useful for constructing binary counters, frequency dividers, and general binary addition devices. It can be made from a J-K flip-flop by tying both of its inputs high.

**Implementation Details:**

**Procedure**

1. Locate IC 7476 on Digital trainer kit
2. Apply various inputs to J & K pins by means of the output on logic output indicator.
3. Connect a pulsar switch to the clock input.
4. Connect the J&K as D and T flip flop as shown in diagrams and verify the respective truth tables.

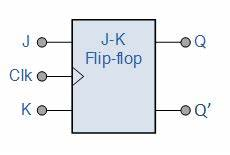
**Pin Diagram of IC 7476 JK Master- Slave FF**



**Logic Symbol Truth Table**

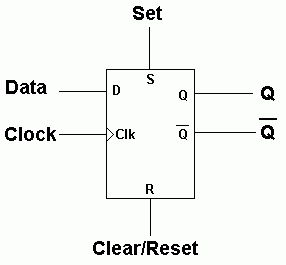
|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **J** | **K** | **Q** | **Q’** | **Qn+1** | **Qn+1’**  **n+1** |
| 0 | 0 | 0 | 1 | 0 | 1 |
| 0 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 | **1** |

**JK Flip Flop**



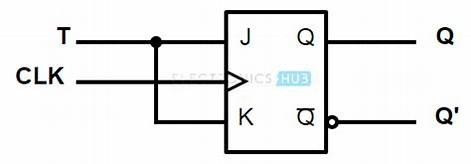
**D Flip Flop** **Truth Table**

|  |  |  |
| --- | --- | --- |
| **D**  **x** | **O/P** | |
| **Q** | **Q’** |
| **x** | **0** | **1** |
| 0 | 0 | 1 |
| 1 | 1 | 0 |

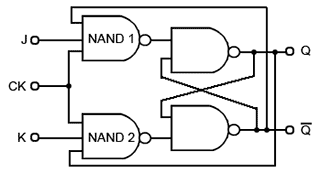


|  |  |  |
| --- | --- | --- |
| **T** | **O/P** | |
| Q | Q ‘ |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

**T Flip Flop** **Truth Table**



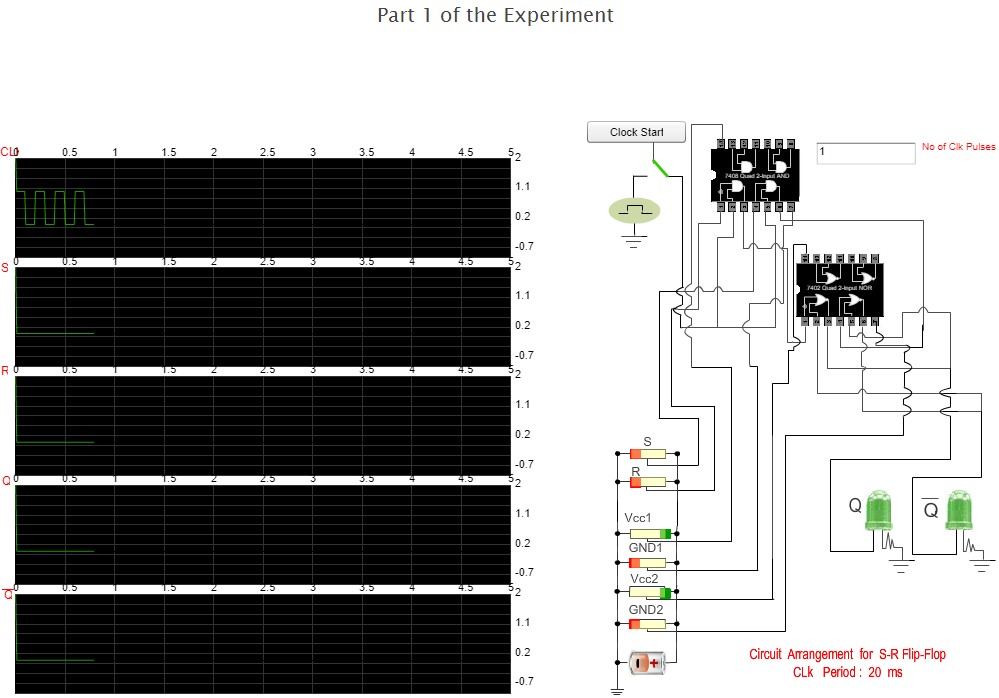
**Diagram of JK Flip Flop using NAND gates**

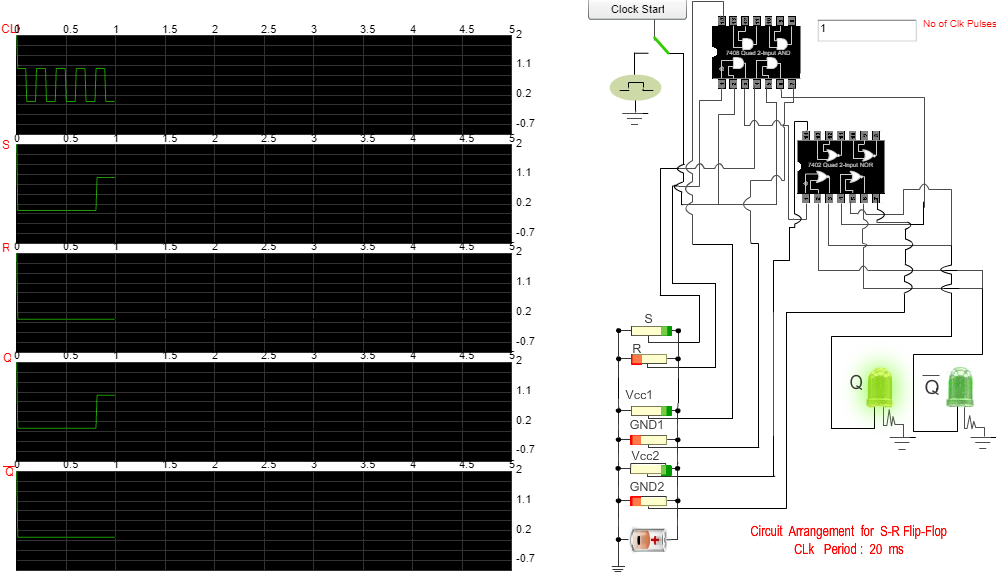


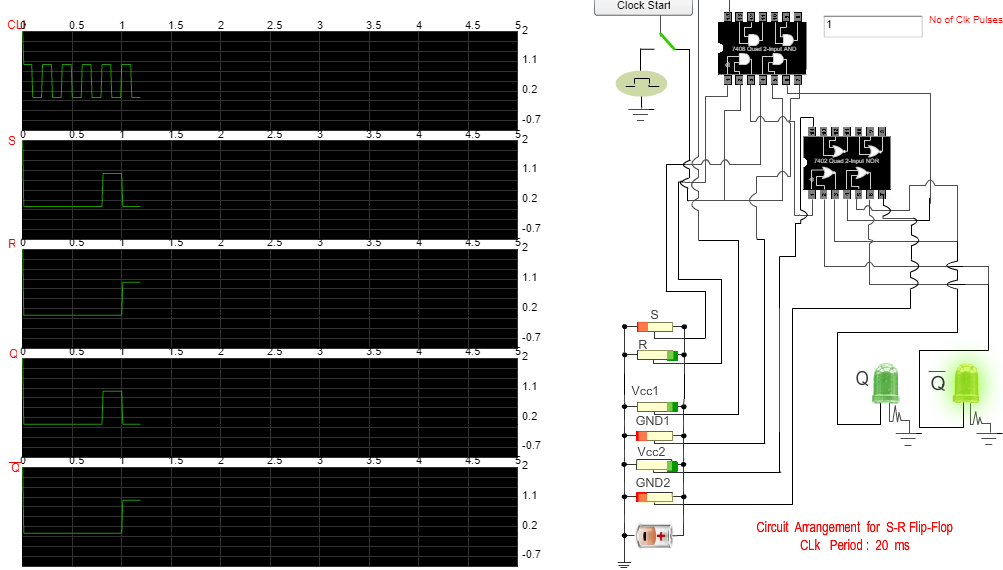
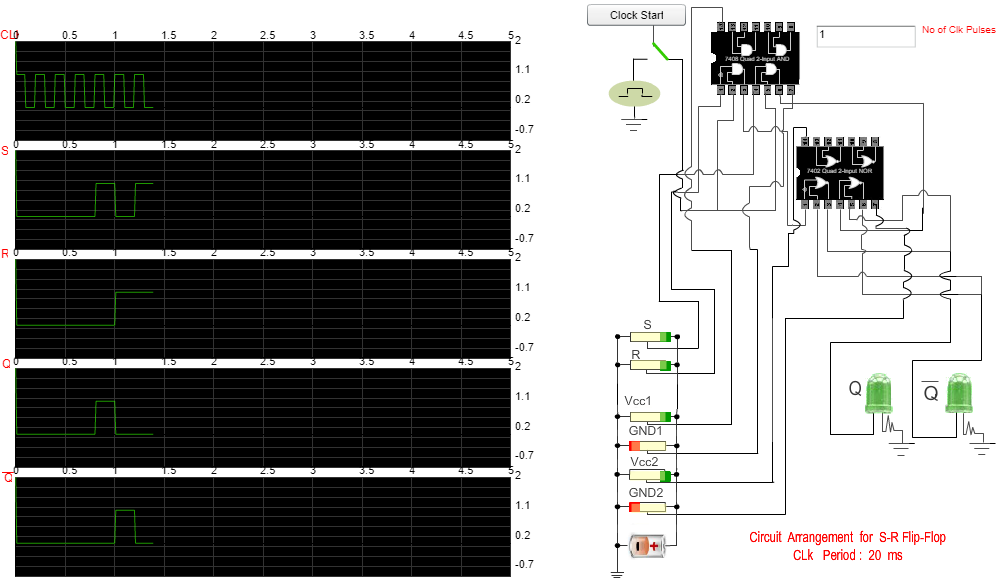
**VIRTUAL LAB:**

**Part 1: NUMBER OF CLOCK PULSES = 1**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **CLOCK PULSE** | **S** | **R** | **Q** | **Q’** |
| **1** | **0** | **0** | **0** | **0** |
| **1** | **0** | **1** | **0** | **1** |
| **1** | **1** | **0** | **1** | **0** |
| **1** | **1** | **1** | **-** | **-** |

**S=0 , R=0** 



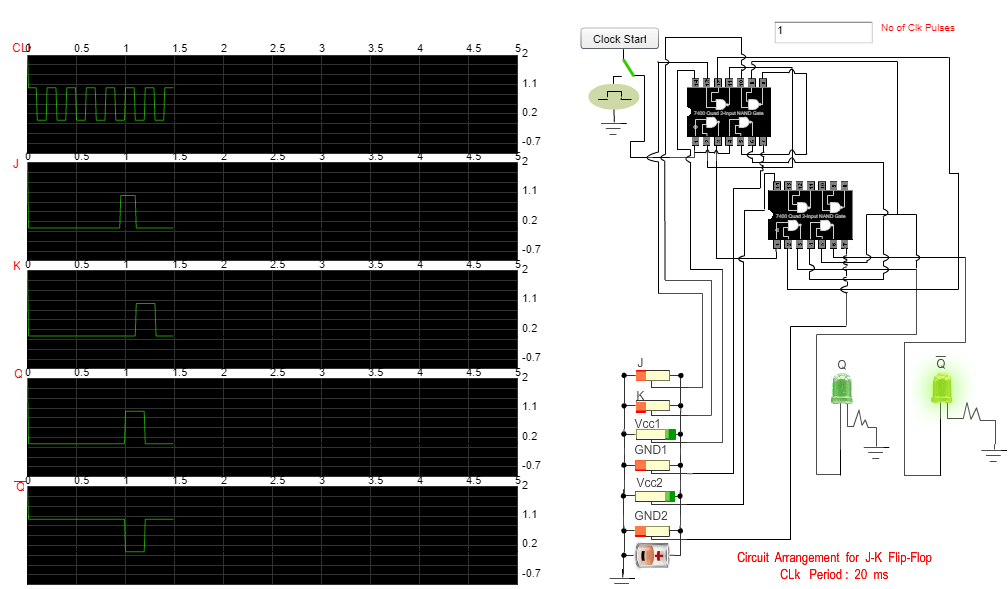
**S=1 , R=0**  **S=0 , R=1** 

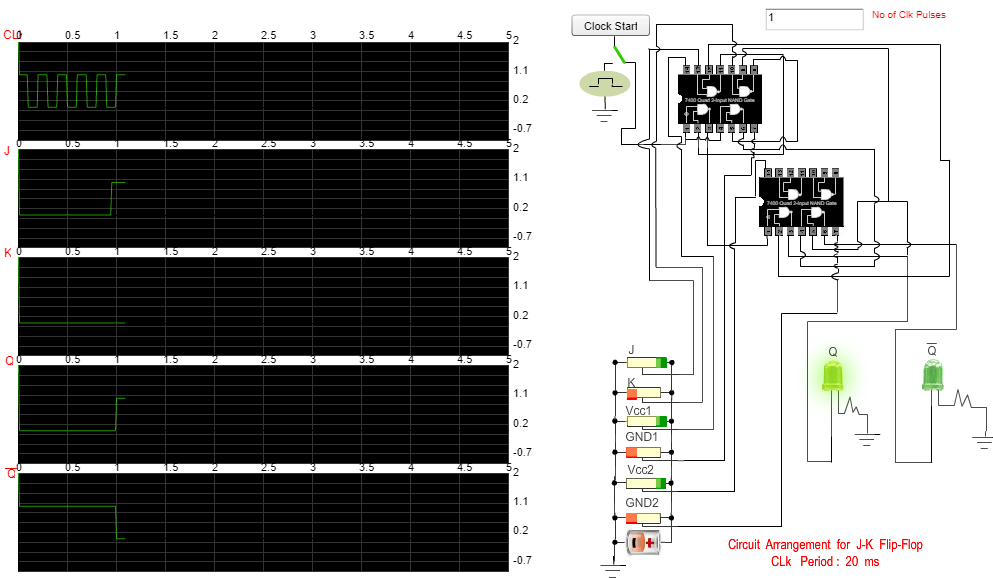
**S=1 , R=1**

**Part 2: NUMBER OF CLOCK PULSES = 1**

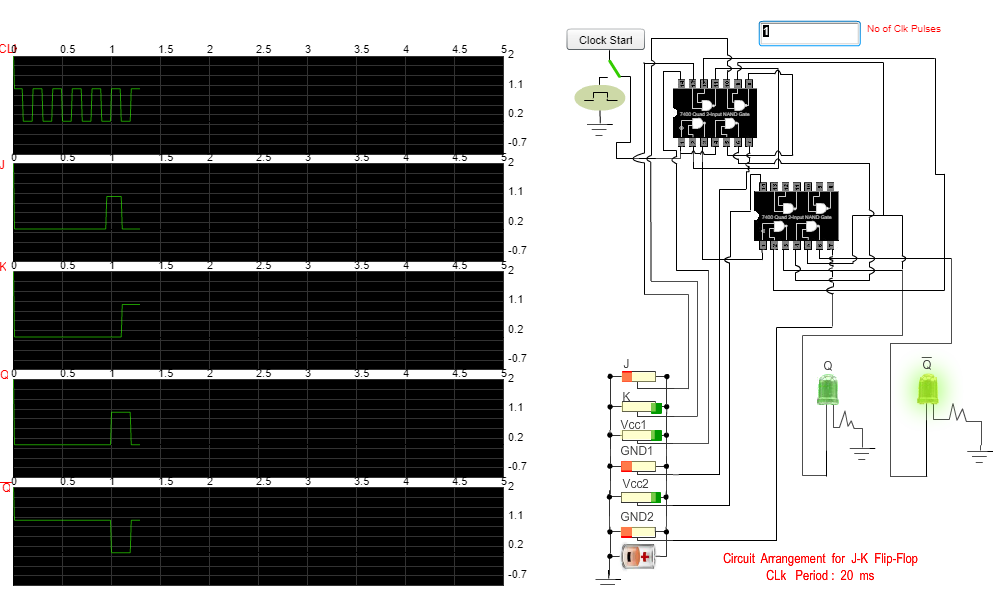
|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **CLOCK PULSE** | **J** | **K** | **Q** | **Q’** |
| **1** | **0** | **0** | **0** | **1** |
| **1** | **1** | **0** | **1** | **0** |
| **1** | **0** | **1** | **0** | **1** |
| **1** | **1** | **1** | **0** | **1** |

**J =0 , K= 0**

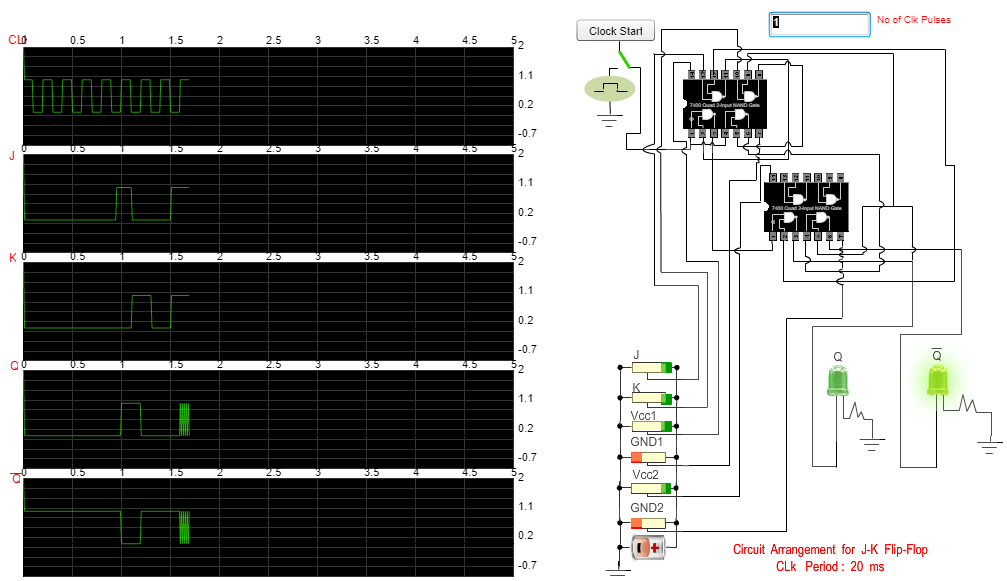




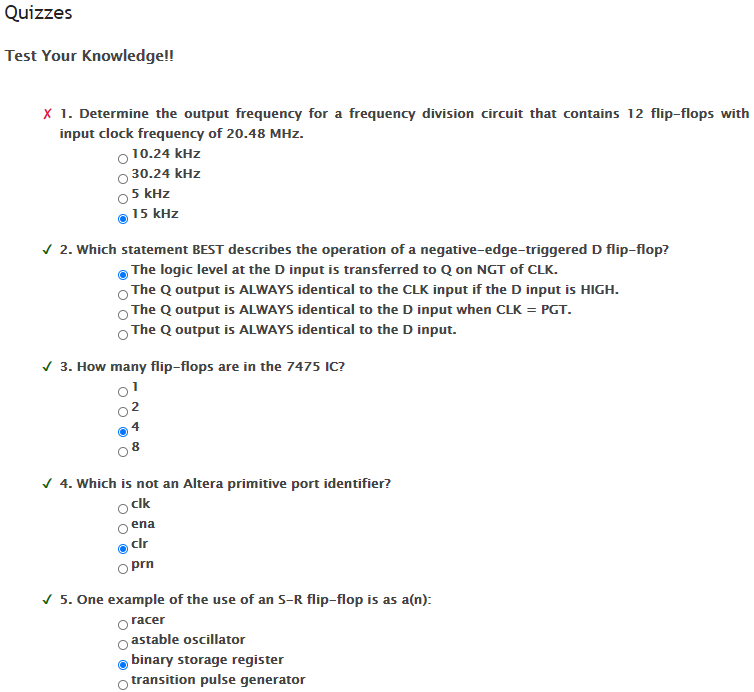
**J =1 , K= 0**



**J = 0 , K = 1**



**J = 1 , K = 1**



**Conclusion:**

**We understood the concept of Flip – Flop & implemented the concept by performing Virtual – Lab ; getting desirable output.**

**Post Lab Descriptive Questions**

1. **How does a JK flip-flop differ from an SR flip-flop in its basic operation?**

The difference between a JK flip-flop & an SR flip-flop is that

* in the J-K flip-flop, both inputs can be HIGH. during this Q output is toggled, that means that the output toggles between HIGH and LOW.
* in R-S flip-flop is that both inputs shouldn’t be HIGH when the clock is triggered. It is considered an invalid input condition, & we cannot predict output during this condition.

1. **What is use of characteristic and excitation table?**

An **excitation table** shows the minimum inputs that are necessary to generate a particular next when the current state is known. They are similar to truth tables & state tables, but rearrange the data so that the current state and next state are next to each other on the left-hand side of the table, and the inputs needed to make that state change happen are shown on the right side of the table.

A characteristic table has the control input (D or T) as the first column, the current state as the middle column, and the next state as the last column. Thus, shows how to the control bit affects the current state to produce the next state.

1. **How many flip flops due you require storing the data 1101?**

We use equation,

2n-1 <= N <= 2n n = no of Flip – Flop needed

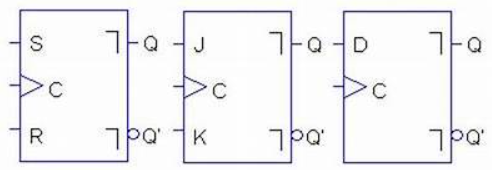
1 Flip Flop stores 1 bit thus 1101 being 4 bit needs 4 Flip – Flop

1. **Describe the basic difference between pulse-triggered and edge-triggered flip-flops.**

**Pulse-Triggered Flip-flops:**

It means that data are entered into the flip- flop on the rising edge of the clock pulse, but the output doesn’t reflect the input state until the falling edge of the clock pulse. As this kind of flip-flops are sensitive to any change of the input levels during the clock pulse being still **HIGH**, the inputs must be set up prior to the clock pulse rising edge and must not be changed before the falling edge ; else, toggling results are obtained.

There are 3 types of **pulse-triggered flip-flops are S-R, J-K and D**.



**Edge-triggered flip-flops:**

It changes states either at the positive edge (rising edge) or at the negative edge (falling edge) of the clock pulse on the control input. The small triangular symbol is called the **dynamic input indicator**, is used to identify an edge-triggered flip-flop.

The three basic types are introduced here: **S-R, J-K and D**. The S-R, J-K and D inputs are called **synchronous inputs** because data on these inputs are transferred to the flip-flops output only on the triggering edge of the clock pulse. pulse. The (SET) & (CLR) inputs are called **asynchronous inputs**, as they are inputs that affect the state of the flip-flop independent of the clock. For the synchronous operations to work properly, both these asynchronous inputs must be LOW.

