Design and Analysis of Operational Trans-conductance Amplifier Using 180nm Technology

Nidhishree
4NI23EC063
Electronics and Communication
NIE ,Mysuru
2023ec_nidhishree_a@nie.ac.in

Kavya G
4NI23EC041
Electronics and Communication
NIE ,Mysuru
2023ec_kavyag_a@nie.ac.in

***Abstract* - This project presents the design and simulation of a high-performance two-stage Operational Trans-conductance Amplifier (OTA) using 180nm CMOS technology in LT-spice. Unlike conventional operational amplifiers, OTAs generate an output current proportional to the differential input voltage, making them highly suitable for voltage-to-current conversion in analog signal processing. The design focuses on achieving high gain, low power dissipation, and improved frequency stability using Miller compensation. The OTA operates with a ±0.9V power supply, achieves an open-loop gain of 60 dB, a phase margin of 60°, and a slew rate of 10.5 V/µs, while consuming less than 3 mW of power. Key design considerations include optimized transistor sizing, consistent channel lengths, and accurate tail current estimation. Simulation results confirm that the OTA meets critical analog performance metrics and is ideal for applications such as analog filters, sensor interfaces, biomedical instrumentation, and low-power mixed-signal systems. Future extensions include scaling to advanced technology nodes and targeting ultra-low voltage operations for energy-constrained environments.**

Keywords—*Operational Transconductance Amplifier, LTspice, Miller Compensation, CMOS, Analog Design*

I. Introduction

Operational Trans-conductance Amplifiers (OTAs) are essential components in analog integrated circuits. This work focuses on the design and simulation of a two-stage OTA using LT-spice under 180nm CMOS technology. The main objective is to achieve high gain, enhanced phase margin, and reduced power dissipation through effective compensation techniques.

II. Miller Compensation for Stability in Op-Amp Circuits

Operational amplifiers (op-amps), particularly those implemented using multiple gain stages such as operational transconductance amplifiers (OTAs), require compensation to ensure closed-loop stability. One of the most widely adopted techniques for compensation is Miller compensation, which introduces a dominant pole to increase the phase margin of the system.

In a typical two-stage op-amp architecture, the first stage is a differential amplifier and the second stage provides additional gain. A compensation capacitor C_c is connected between the output of the second stage and the output of the first stage. This configuration leverages the Miller effect, wherein the capacitor is seen as a much larger effective capacitance due to the gain between its terminals. As a result, the dominant pole is shifted to a lower frequency, enhancing system stability.

The loop gain of the system can be represented as:

$$L(s) = A(s)F(s)$$

where A(s) is the open-loop gain and F(s) is the feedback transfer function. For a stable system, the phase of the loop gain $\angle L(j\omega)$ at the frequency where $|L(j\omega)| = 1$ must be sufficiently greater than −180° to avoid sustained oscillations. The difference between the actual phase and −180° at this frequency is defined as the phase margin (PM):

$$PM = 180° + \angle L(j\omega\_0dB)$$

where ω_0dB is the gain crossover frequency (i.e., the frequency at which the magnitude of the loop gain is unity or 0 dB).

A phase margin of at least 45° is generally considered acceptable, while a margin of 60° is preferred to reduce overshoot and ringing in the transient response. In systems where the uncompensated op-amp has a low phase margin (e.g., <45°), Miller compensation becomes essential.

Thus, Miller compensation ensures that the gain falls to 0 dB before the phase reaches −180°, thereby preventing positive feedback and guaranteeing stable closed-loop operation.

III. TECHNICAL SPECIFICATIONS

A. Software and Tools

1. LT-spice XVII (Simulation and waveform analysis)
2. CMOS 180nm Technology Models
3. Microsoft Word for Documentation
4. 180nm Technology Library File

B. Design Specification

Requirements	***Specifications***
Gain	60dB
VDD	0.9V

Requirements	*Specifications*
VSS	-0.9V
GB	5MHz
CL	10pF
SR	10V/µs
VOUT Range	±5V
ICMR	-0.1V to +0.5V
Power Dissipation	=< 3 mW
Phase Margin	60°
Bandwidth	1.25KHz

C. library and model details

- Library file used: tsmc180nm.lib

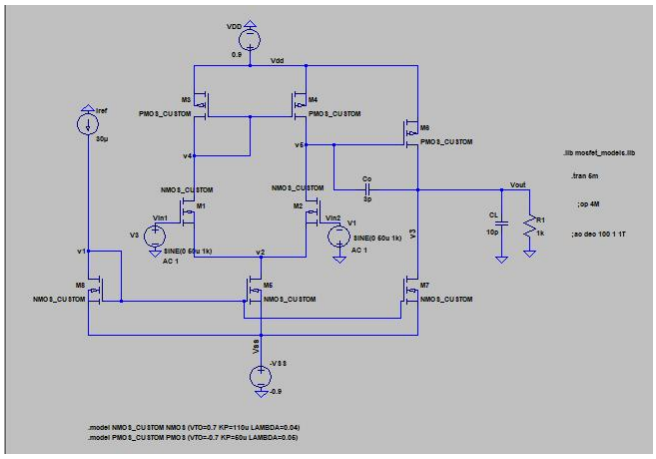
NMOS_CUSTOM NMOS

VTO=0.7 V ; Threshold voltage
KP=110u A/V^{-2} ; µnCox (transconductance parameter)
LAMBDA=0.04 V^{-1} ; Channel length modulation

PMOS_CUSTOM PMOS

VTO=-0.7 V ; Threshold voltage
KP=50u A/V^{-2} ; µpCox (transconductance parameter)
LAMBDA=0.05V^{-1} ; Channel length modulation

D. Schematic View



E. Components List

Sl. No	Mosfet Models & Parameters			
	MOSFET	*WIDTH*	*LENGTH*	*FUNCTION*
1	M1(NMOS)	3µm	1µm	I/P Diff Pair
2	M2(NMOS)	3µm	1µm	I/P Diff Pair
3	M3(PMOS)	60µm	1µm	Active Load
4	M4(PMOS)	60µm	1µm	Active Load
5	M5(NMOS)	2.2µm	1µm	Current Mirror, Tail Current Source
6	M8(NMOS)	2.2µm	1µm	Current Mirror
7	M7(NMOS)	5.49µm	1µm	SS Pull Down Transistor
8	M6(PMOS)	118.5µm	1µm	SS Pull Up Transistor

i. Input differential pair
ii. Second stage driver pull down transistor
iii. Second stage driver pull up transistor

a. Capacitors(Cc and Cl)
   i. Cc (Miller Capacitor) : 3pF
   ii. C_L (Load capacitor) : 10pF

b. Voltage Source (V)
c. Current Source (A)
d. Resistor(R1): 1Kohm

IV. Design Question

To check if all the design specifications are met, we simulate the circuit of OTA. Here, the simulation is done using simulator software called Lt-spice. The schematic of OTA is designed in Lt-spice simulator with V_{DD}= 0.9V and V_{SS}= −0.9V. The bias current of the circuit is 30µA.
The input voltage of ±5V is given to the circuit. The value of compensation capacitor, C_C = 3pF and load capacitor. C_L = 10pF . The schematic of OTA which is drawn in Lt-spice is represented in the figure below.

i. To calculate the value of compensation capacitor Cc which is give as

$$C_C > \frac{2.2}{10} C_L$$

$$C_C > \frac{2.2}{10} (10p)$$

$$C_C > 2.2\ pF$$

$$C_C = 3pF$$

ii. To calculate tail current I_S based on Slew Rate

$$I_S = SR * C_C$$

$$= (10*10^6) * (3pF)$$

$$= 30\mu A$$

iii. Now, determine the aspect ratio of M3

$$S_3 = (W/L)_3 = \frac{I_5}{k_p'[V_{DD} - V_{in(max)} - |V_{To}|_{(max)} + V_{T1(min)}]^2} \geq 1$$

$$= \frac{30 * 10^{-6}}{(50 * 10^{-6})[0.9 - 0.5 - 0.85 + 0.55]^2} = 60$$

Since M3 and M4 are identical, S3 will be equal to S4

$$(W/L)_3 = (W/L)_4 = 60$$

iv. The trans-conductance of the input transistor is determined from the equation that follows

$$g_{m1} = GB * C_c = (5*10^6)(2\pi)(3*10^{-12})$$

$$g_{m1} = 94.25\ \mu s$$

v. From the above equation, the aspect ratio of M1 and M2 can be directly obtained as

$$(W/L)_1 = (W/L)_2 = \frac{g_{m1}^2}{k_2' I_5} = \frac{(94.25\mu)^2}{(110*10^{-6})(30*10^{-6})}$$

$$(W/L)_1 = (W/L)_2 = 2.69 \approx 3$$

vi. The aspect ratio M1 and M2 is determined as

- $S_5 = (W/L)_5 = \frac{2I_5}{k_5'[V_{DS5(sat)}]^2}$

$$V_{DS5(sat)} = V_{in(min)} - V_{SS} - \sqrt{\frac{I_5}{\beta_1}} - V_{T1(max)} \geq 100\text{mV}$$

$$V_{DS5(sat)} = -0.1 + 0.9 - \sqrt{\frac{30 * 10^{-6}}{110 * 10^{-6} * 3}} - 0.3$$

$$V_{DS5(sat)} = 0.499V$$

Now,

$$S_5 = (W/L)_5 = \frac{2I_5}{k_5'[V_{DS5(sat)}]^2} = \frac{2((30*10^{-6})}{110*10^{-6}[0.499]^2}$$

$$(W/L)_5 = 2.19 \approx 2.2$$

- $S_6 = S_4 \frac{g_{m6}}{g_{m4}}$ in which $g_{m6} \geq 10\ g_{m1} \geq 942.5\mu s$

$$S_6 = S_4 \frac{g_{m6}}{g_{m4}} = 60 \frac{942.5\mu}{300\mu}$$

$$S_6 = 118.5$$

vii. Then, determine the value of the current through M6 by the following equation

$$I_6 = \frac{g_{m6}^2}{2k_6' S_6} = \frac{(942.5\mu)^2}{2(50*10^{-6})(118.5)} = 74.96\mu$$

$$I_6 = 74.96\mu A$$

viii. Design S7 to achieve the desired current ratios between I5 and I6

$$(W/L)_7 = \frac{I_6}{I_5} S_5 = 2.2 \frac{74.96\mu}{30\mu}$$

$$(W/L)_7 = 5.49$$

ix. Finally determine the value of gain and power dissipation and check its specification.

- **To determine P_{diss} :-**

$$P_{diss} = (I_5 + I_6)(V_{DD} + |V_{SS}|)$$

$$= (30\mu + 74.96\mu)(0.9 + 0.9)$$

$$= 0.000188$$

$$P_{diss} = 0.188\text{mW}$$

- **To determine A_v:-**

$$A_V = 2 \frac{g_{m2}\, g_{m6}}{I_5(\lambda_2 + \lambda_3) I_6 (\lambda_6 + \lambda_7)}$$

$$= 2 \frac{(94.25\mu)(942.5\mu)}{30*10^{-6}(0.04+0.05)74.96*10^{-6}(0.04+0.05)}$$

$$= 9725.27\text{V/V}$$

$$A_V = 79.74DB$$

A. Hardware Required

Simulation-based study, no external hardware required

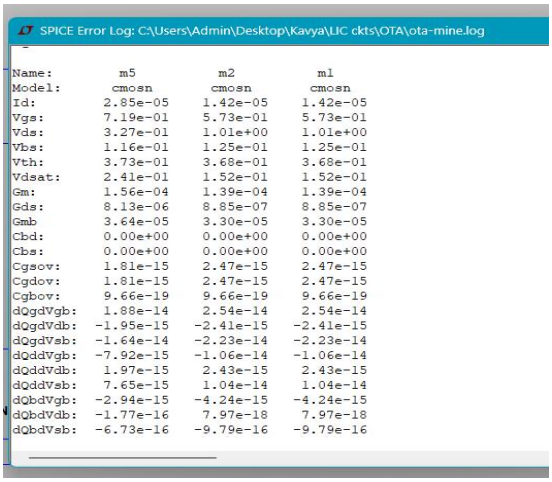
V. Simulation Result

A. DC Characteristics

SPICE Error Log: C:\Users\Admin\Desktop\Kavya\LIC ckts\OTA\ota-mine.log

--- BSIM3 MOSFETS ---

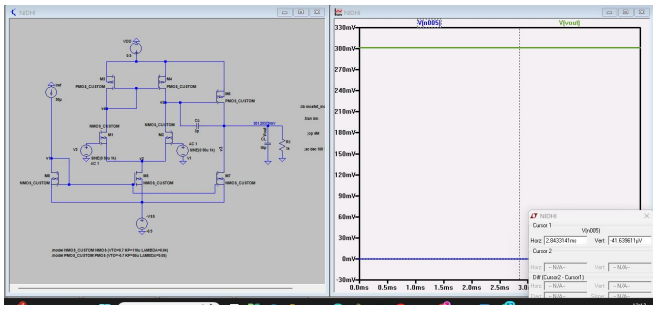
Name:	m3	m4	m6	m7	m8
Model:	cmosp	cmosp	cmosp	cmosn	cmosn
Id:	1.42e-05	1.42e-05	7.79e-05	7.53e-05	3.00e-05
Vgs:	0.00e+00	2.83e-14	4.38e-01	7.19e-01	7.19e-01
Vds:	4.59e-01	4.59e-01	8.97e-01	9.03e-01	7.19e-01
Vbs:	3.40e-01	3.40e-01	7.69e-01	1.28e-01	1.25e-01
Vth:	-3.83e-01	-3.83e-01	-3.79e-01	3.68e-01	3.69e-01
Vdsat:	-8.08e-02	-8.08e-02	-8.25e-02	2.44e-01	2.43e-01
Gm:	2.43e-04	2.43e-04	1.30e-03	4.17e-04	1.67e-04
Gds:	1.77e-06	1.77e-06	8.41e-06	3.26e-06	1.57e-06
Gmb	6.64e-05	6.64e-05	3.53e-04	9.50e-05	3.81e-05
Cbd:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Cbs:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Cgsov:	3.81e-14	3.81e-14	1.90e-13	4.52e-15	1.81e-15
Cgdov:	3.81e-14	3.81e-14	1.90e-13	4.52e-15	1.81e-15
Cgbov:	9.41e-19	9.41e-19	9.41e-19	9.66e-19	9.66e-19
dQgdVgb:	4.39e-13	4.39e-13	2.21e-12	4.66e-14	1.87e-14
dQgdVdb:	-3.75e-14	-3.75e-14	-1.87e-13	-4.42e-15	-1.77e-15
dQgdVsb:	-3.86e-13	-3.86e-13	-1.95e-12	-4.12e-14	-1.65e-14
dQddVgb:	-1.78e-13	-1.78e-13	-8.94e-13	-1.95e-14	-7.79e-15
dQddVdb:	3.78e-14	3.78e-14	1.89e-13	4.47e-15	1.79e-15
dQddVsb:	1.80e-13	1.80e-13	9.07e-13	1.91e-14	7.65e-15
dQbdVgb:	-8.37e-14	-8.37e-14	-4.18e-13	-7.69e-15	-3.08e-15
dQbdVdb:	-2.45e-17	-2.45e-17	3.52e-16	8.17e-18	-1.38e-18
dQbdVsb:	-1.24e-14	-1.24e-14	-5.61e-14	-1.53e-15	-6.26e-16



Name:	m5	m2	m1
Model:	cmosn	cmosn	cmosn
Id:	2.85e-05	1.42e-05	1.42e-05
Vgs:	7.19e-01	5.73e-01	5.73e-01
Vds:	3.27e-01	1.01e+00	1.01e+00
Vbs:	1.16e-01	1.25e-01	1.25e-01
Vth:	3.73e-01	3.68e-01	3.68e-01
Vdsat:	2.41e-01	1.52e-01	1.52e-01
Gm:	1.56e-04	1.39e-04	1.39e-04
Gds:	8.13e-06	8.85e-07	8.85e-07
Gmb	3.64e-05	3.30e-05	3.30e-05
Cbd:	0.00e+00	0.00e+00	0.00e+00
Cbs:	0.00e+00	0.00e+00	0.00e+00
Cgsov:	1.81e-15	2.47e-15	2.47e-15
Cgdov:	1.81e-15	2.47e-15	2.47e-15
Cgbov:	9.66e-19	9.66e-19	9.66e-19
dQgdVgb:	1.88e-14	2.54e-14	2.54e-14
dQgdVdb:	-1.95e-15	-2.41e-15	-2.41e-15
dQgdVsb:	-1.64e-14	-2.23e-14	-2.23e-14
dQddVgb:	-7.92e-15	-1.06e-14	-1.06e-14
dQddVdb:	1.97e-15	2.43e-15	2.43e-15
dQddVsb:	7.65e-15	1.04e-14	1.04e-14
dQbdVgb:	-2.94e-15	-4.24e-15	-4.24e-15
dQbdVdb:	-1.77e-16	7.97e-18	7.97e-18
dQbdVsb:	-6.73e-16	-9.79e-16	-9.79e-16

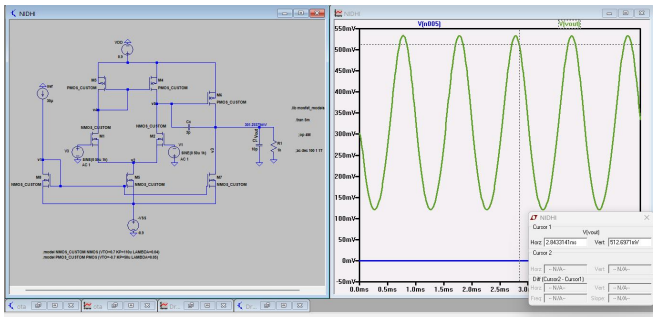
B. *Transfer Characteristics*

1) *Common Mode Analysis*



V_{OUT} = 300mV

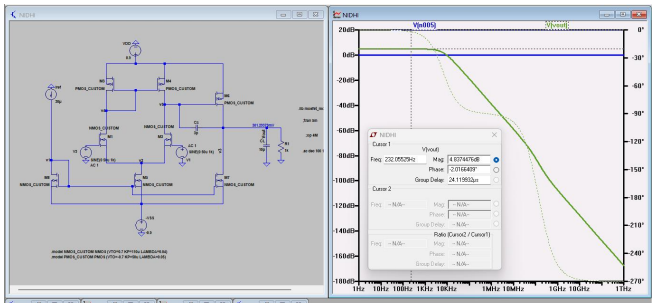
2) *Differential Mode Analysis*



V_{OUT} = 412mV (peak-peak value)
V_{IN} = 100 µV (peak-peak value)

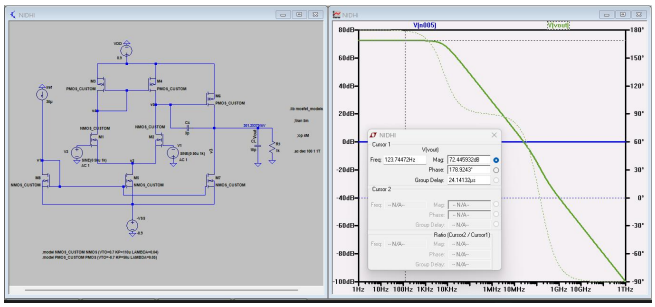
C. *AC Characteristics*

1) *Common Mode Analysis*



Gain = 4dB
Phase = -30°

2) *Differential Mode Analysis*



Gain = 72dB
Cut-off Frequency = 7.3KHz
Phase = 60°

VI. RESULT

Parameters	***Calculated***	***Obtained***
Gain	60dB	72dB
VDD	0.9V	0.9V
VSS	-0.9V	-0.9V
GB	5MHz	26MHz
CL	10pF	10pF
VOUT Range	±5V	520mV to 120mV (for input 50 µV)
ICMR	-0.1V to +0.5V	-0.5V to +0.3V
Power Dissipation	=< 3 mW	1.8mW
Phase Margin	60°	60°
Bandwidth	1.25KHz	6.53KHz

VII. DESIGN METHODOLOGY

The OTA is designed using standard analog design flow starting with length selection (L = 1um), compensation capacitor design, tail current estimation for slew rate, aspect ratio calculations for transistors, and gain-bandwidth tuning. Miller compensation is used to improve stability.

VIII. CONCLUSION

The objective of this work is to design and analyze an Operational Transconductance Amplifier (OTA) using LTspice software based on 180nm CMOS technology. The design incorporates **Miller Compensation**, a widely adopted frequency compensation technique that utilizes the Miller effect by introducing a compensation capacitor across the high-gain stage to ensure stability. The simulation results validate that the designed OTA meets all specified performance metrics, including desired gain and phase margin. **The circuit demonstrates high gain, low power dissipation, and excellent stability, making it well-suited for low-power analog applications.** This analysis highlights the effectiveness of Miller Compensation in achieving robust and power-efficient amplifier performance in deep-submicron CMOS processes.

IX. REFERENCES

[1] Behzad Razavi, Design of Analog CMOS Integrated Circuits, McGraw-Hill.
[2] R. Jacob Baker, CMOS: Circuit Design, Layout, and Simulation, Wiley.