COMP2611 Spring 2022 Homework #1

Note:

- **The deadline of this homework is at 11:55pm on Monday, 14 March 2022 (Hong Kong Time, UTC+8). NO late submissions will be accepted!**
- **Work out the answers of the questions either directly on the hardcopy of this document or on your own paper sheets. Then scan all the answer pages into a single pdf file "homework1_<studID>.pdf", or take photos and zip them into a single zip file "homework1_<stdID>.zip". Make sure every detail of the answers is clearly visible in your submission (verify this on the scanned pages before submitting), otherwise marks may be deducted.**
- **We only accept e-submissions at the Canvas. To submit, first find the Canvas page of COMP2611, homework 1, and then upload the file. You can upload for multiple times, only the last one before the deadline will be marked.**
- **Make sure you keep the original copy of your homework until the homework score is finalized.**

Name : MENG Zeyuan

Student ID : 20761727

Email : zmengaf@connect.ust.hk

Question	Marks
1. Boolean Algebra	/10
2. K-map	/10
3. Combinational Logic	/12
4. Sequential Logic	/8
5. Sequential Logic Circuit Timing Chart	/10
total	/50

Question 1: Boolean Algebra (10 points)

Prove the logic equivalence as stated in the following equation with Boolean Algebra. **Show detailed steps otherwise no points will be given**.

$$ACE + \bar{A}BE + \bar{B}\bar{C}\bar{D} + B\bar{C}E + \bar{C}DE + \bar{A}E = E + \bar{B}\bar{C}\bar{D}$$

$LHS = E(AC + \bar{A}B + B\bar{C} + \bar{C}D + \bar{A}) + \bar{B}\bar{C}\bar{D}(H + E)$

$= E(AC + \bar{A}B + B\bar{C} + \bar{C}D + \bar{B}\bar{C}\bar{D} + \bar{A}) + \bar{B}\bar{C}\bar{D}$

Because that $\bar{B}\bar{C}\bar{D} = \bar{B}\bar{C}\bar{D} + \bar{B}\bar{C}\bar{D}$, we can write the equation above as

$LHS = E(AC + \bar{A} + \bar{C}(B + \bar{B}\bar{D} + D + \bar{B}\bar{D})) + \bar{B}\bar{C}\bar{D}$

we can the expand the above underline part use distributive law

$= E(AC + \bar{A} + \bar{C}((B + \bar{B})(B + \bar{D}) + (D + \bar{B})(D + \bar{D})))) + \bar{B}\bar{C}\bar{D}$

$\because B + \bar{B} = D + \bar{D} = 1$

$\therefore LHS = E(AC + \bar{A} + \bar{C}(B + \bar{B} + D + \bar{D})) + \bar{B}\bar{C}\bar{D}$

$= E(AC + \bar{A} + \bar{C}) + \bar{B}\bar{C}\bar{D}$

De Morgan's Law, $\bar{A} + \bar{C} = \overline{AC}$

$\therefore LHS = E(AC + \overline{AC}) + \bar{B}\bar{C}\bar{D}$

$= E + \bar{B}\bar{C}\bar{D} = RHS$

Question 2: K-map (10 points)

The Boolean expression for the output ***F*** in the inputs ***A, B, C*** and ***D*** is given in **Sum-of-Product (SoP):**

$$F = m_0 + m_1 + m_2 + m_5 + m_8 + m_{10} + m_{11} + m_{12} + m_{13} + m_{14} + m_{15}$$

Assume input ***D*** corresponds to the least significant digit and ***A*** corresponds to the most significant digit in the numbering of the above minterms. **Use the K-map approach to simplify the logic function** and **write its simplest form in Boolean expression**. (Note: You should circle the 1's group(s) clearly in your K-map.)

AB \ *CD*	00	01	11	10
00	1	1	0	1
01	0	1	0	0
11	1	1	1	1
10	1	0	1	1

$AB + AC + \bar{A}\bar{C}D + \bar{B}\bar{D}$

Question 3: Combinational Logic (12 points)

We want to design a circuit that verifies whether a 2-input AND gate works correctly. The combinational logic circuit denoted by the square in the diagram below. The circuit takes the inputs of a 2-input AND gate (i.e. inputs $\mathbf{A_0}$, $\mathbf{A_1}$) and determines whether the output of the AND gate (i.e $\mathbf{A_2}$) is correct (truth table of an AND gate is provided below for quick reference). If the AND gate is outputting correctly, the circuit will output 1 in **F,** otherwise it will output 0 in **F**.

Inputs		Correct AND gate output
A_1	A_0	A_2
0	0	0
0	1	0
1	0	0
1	1	1

a) Construct the truth table for the output ***F*** (be careful about the positions of $\mathbf{A_2}$, $\mathbf{A_1}$, $\mathbf{A_0}$ in the table) (4 points)

Input			**Output**
A_2	A_1	A_0	F
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

b) Derive the Boolean expression for the output ***F*** in the inputs A_2, A_1, and A_0 **<u>in both Sum-of-Product (SoP) and Product-of-Sum (PoS)</u>** formats with minterms and maxterms respectively. (4 points)

SoP : $\bar{A}_0\bar{A}_1\bar{A}_2 + A_0\bar{A}_1\bar{A}_2 + \bar{A}_0A_1\bar{A}_2 + A_0A_1A_2$

PoS : $(A_0 + A_1 + \bar{A}_2)\cdot(\bar{A}_0 + \bar{A}_1 + A_2)\cdot(A_0 + \bar{A}_1 + A_2)\cdot(\bar{A}_0 + A_1 + A_2)$

c) Use K-map to below simplify the **SoP** representation for the circuit by **<u>showing the circled groups clearly</u>**. **<u>Write the expression in its simplest form</u>**. (4 points)

A_2 \ A_1A_0	00	01	11	10
0	1	1	0	1
1	0	0	1	0

$A_0A_1A_2 + \bar{A}_0\bar{A}_2 + \bar{A}_1\bar{A}_2$

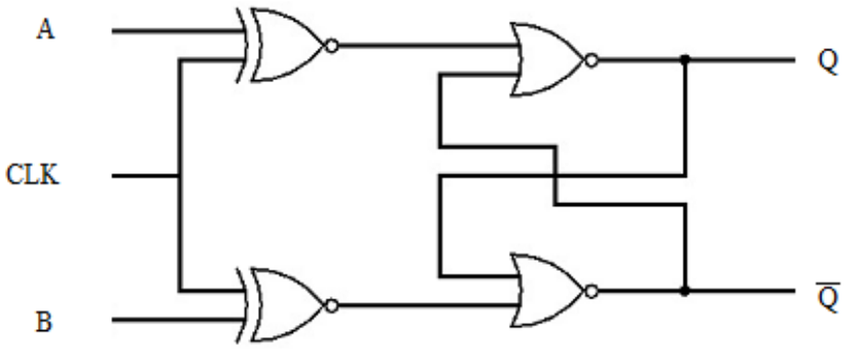
Question 4: Sequential Logic (8 points)

Complete the truth table of the sequential logic circuit given below. Assume $\boldsymbol{Q_{t+1}}$ is the value of the output $\boldsymbol{Q}$ after the corresponding logic gates have been given enough time to produce the output according to the inputs.

If the older value $\boldsymbol{Q_t}$ will be preserved ($\boldsymbol{Q_{t+1} = Q_t}$) by the input combination, put "**Latch**" in the table for the output $\boldsymbol{Q_{t+1}}$.

If the input combination(s) is forbidden, put "**Forbidden**" in the table.

If the new $\boldsymbol{Q_{t+1}}$ value will be stable and there's no relationship between the new value $\boldsymbol{Q_{t+1}}$ and the old value $\boldsymbol{Q_t}$, put the specific new value ("0" or "1") in the table. (7 points)



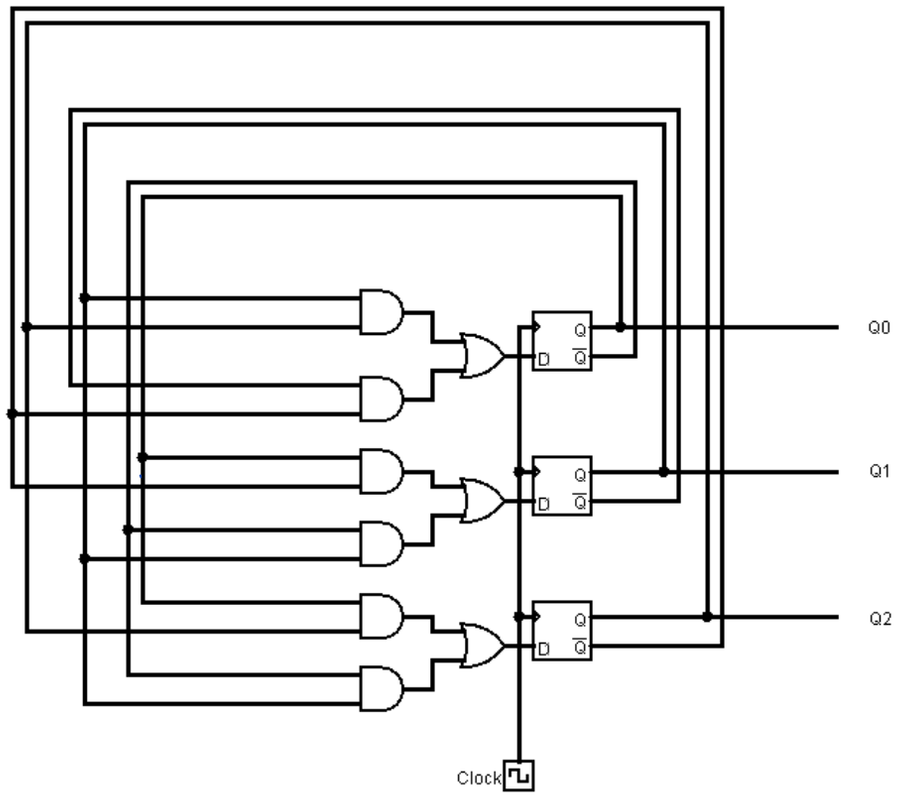
The two gates at the left in the circuit above are XNOR (Exclusive NOR) gates, the truth table is as follows:

Inputs		Output
A	B	A XNOR B
0	0	1
0	1	0
1	0	0
1	1	1

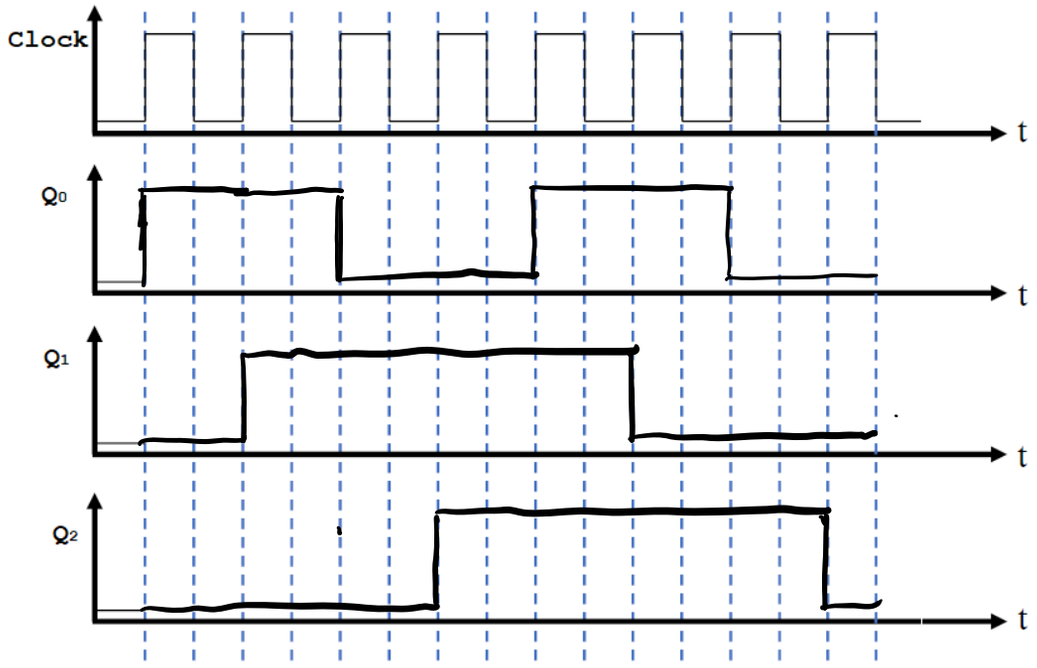
Input			Output
CLK	A	B	Q_{t+1}
0	0	0	Forbidden.
0	0	1	0
0	1	0	1
0	1	1	Latch.
1	0	0	Latch.
1	0	1	1
1	1	0	0
1	1	1	Forbidden.

Question 5: Sequential Logic Circuit Timing Chart (10 points)

A circuit composed of three **rising edge-triggered** D flip-flops is shown below. Ignore propagation delays. Assume the $\mathbf{Q_2}$, $\mathbf{Q_1}$ and $\mathbf{Q_0}$ of the D flip-flops are all **0** initially.



a) Complete the timing diagram below for the outputs of this circuit (8 points).



b) State what the circuit does by referring to the timing diagram (hint: consider $\mathbf{Q_2Q_1Q_0}$ to be a binary value). (2 points)

$Q_2Q_1Q_0 = 001 \rightarrow 011 \rightarrow 010 \rightarrow 110 \rightarrow 111 \rightarrow 101 \rightarrow 100$

so $Q_2Q_1Q_0$ represents the gray code