ECEN405 Lab 6 Report

Niels Clayton : 300437590

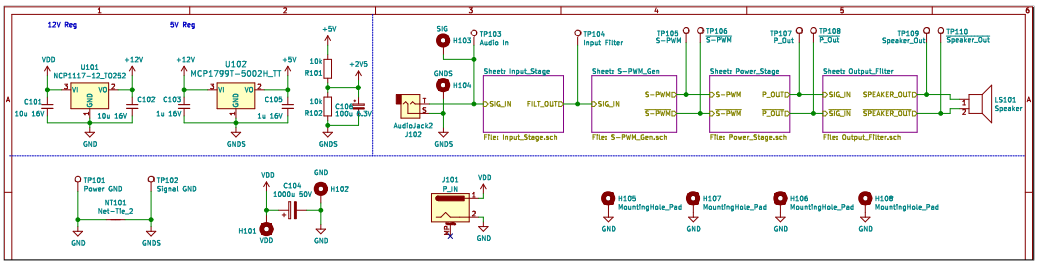

Figure 1: High level design schematic

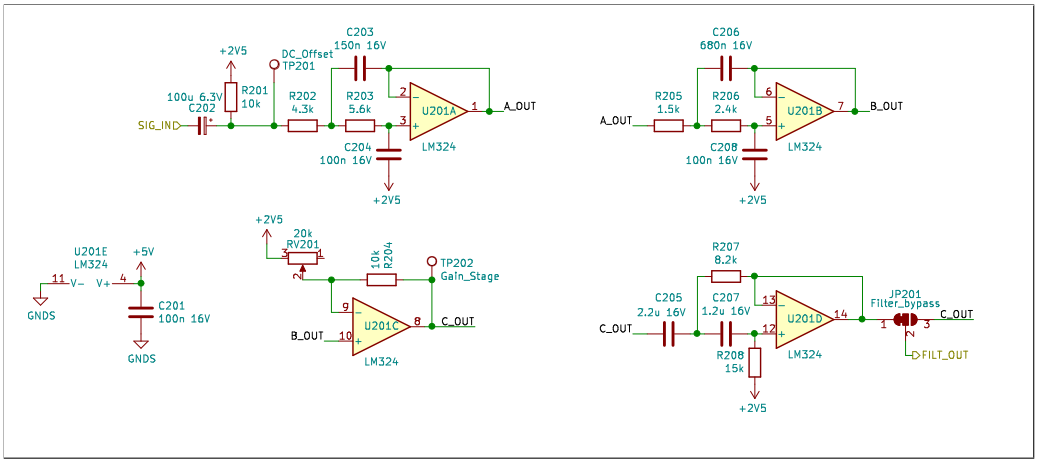

Figure 2: Input filtering schematic

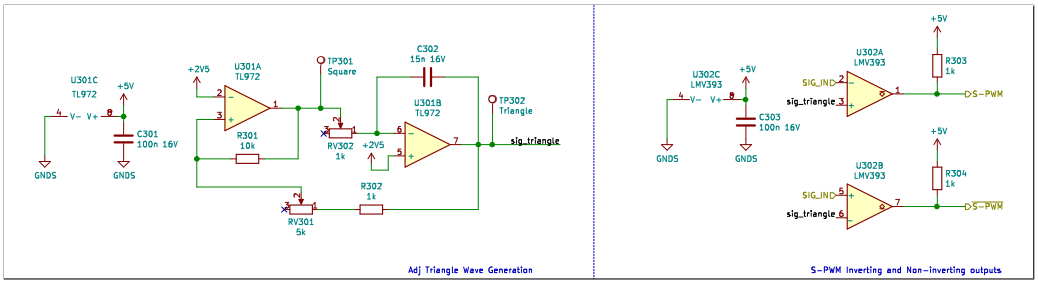

Figure 3: Sampling triangle wave & SPWM generation schematic

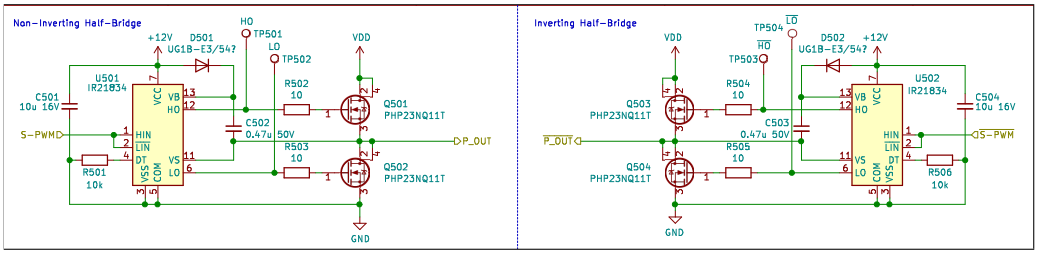

Figure 4: Gate driver schematic

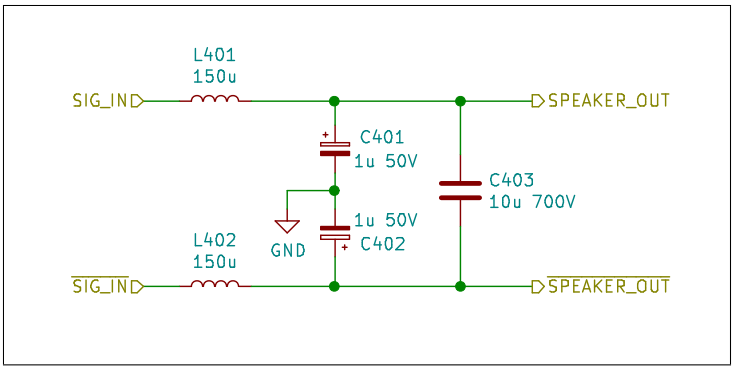

Figure 5: Output filter schematic