ECEN405 Lab 3 Report
Asynchronous Buck Converter

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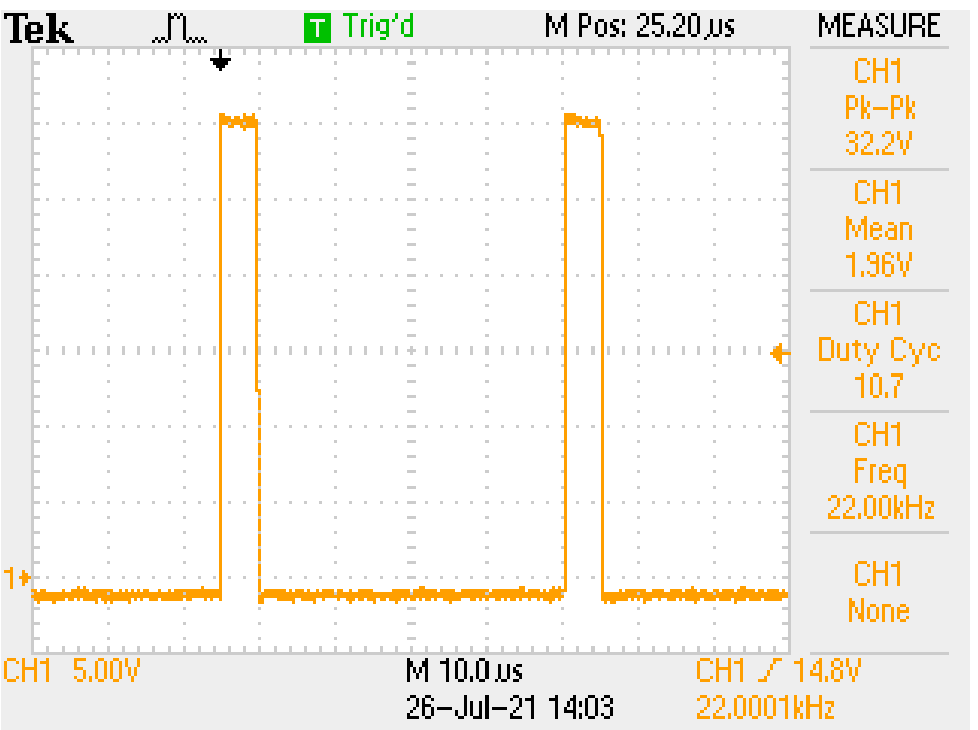
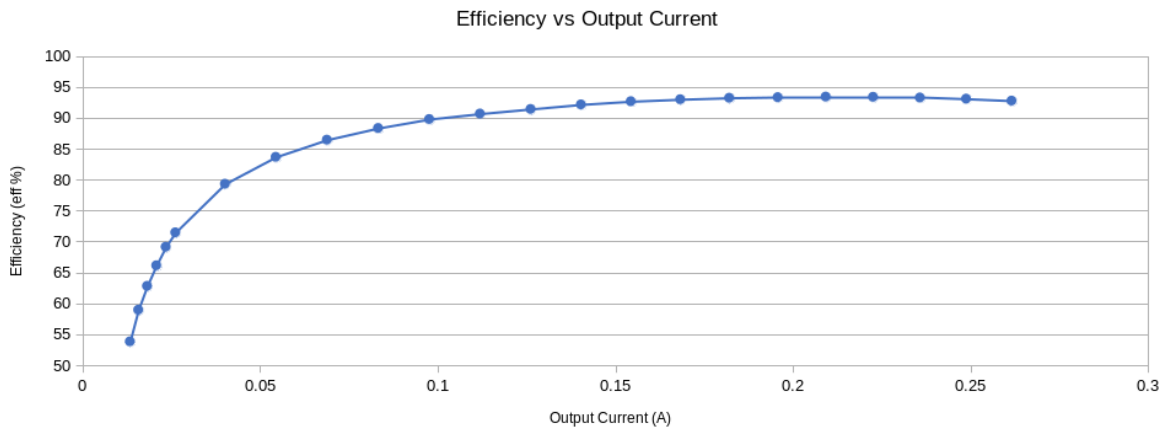
1 MOSFET Source Voltage



High side MOSFET source voltage at 10% duty cycle

The waveform shown above is from the source of the high-side MOSFET. This signal looks mostly the same as the PWM control signal into the gate driver, with a 10% duty cycle, and a 22kHz frequency. The major difference however, is that it now has a peak to peak voltage of 30V, as that is the supply into the drain of the high side MOSFET.

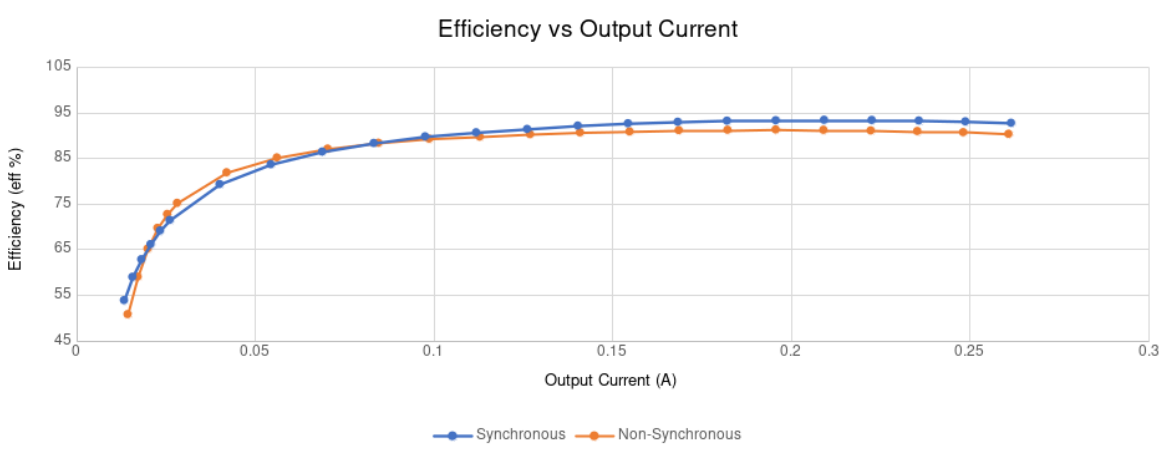
2 Efficiency vs Output Current Plot



Efficiency vs output current plot for a non-synchronous buck converter

From the efficiency vs output current plot above, we can clearly see that as the output current increases the overall efficiency of the converter increases, tapering off at 90% at 150mA. The conduction losses in this system are dependant on the duty cycle of the of the PWM control signal, increasing and decreasing with this duty cycle due to the changing conduction period. The switching losses within the system will remain constant assuming a constant load, since the switching frequency has not changed. From this we know that at low current output the majority of the losses will be due to the switching losses. As the output current increases the conduction losses will will represent a larger portion of the losses.

3 Synchronous vs Non-Synchronous Efficiency

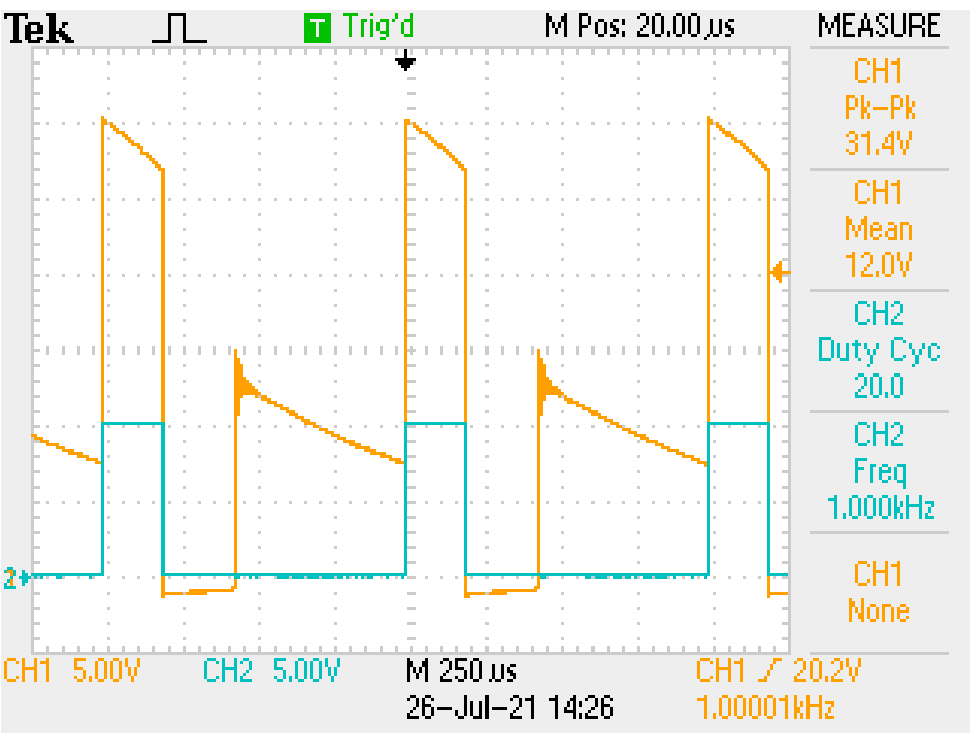


In the plot above we can see the comparison between the efficiency curves of the synchronous and no-synchronous buck converter topologies. From this plot we can see that for our 100Ω load they have very similar efficiency vs output curves. It can however be seen that at higher output currents the synchronous topology has a slightly higher efficiency. This is due to the losses created by the diode drop of the non-synchronous topology, since this diode drop is constant, at high output currents there will be large losses across the diode.

4 Application and Usage

The non-synchronous buck converter topology offers a simpler to implement and often lower cost design compared to the synchronous. This is due to the replacement of a MOSFET with a power diode that is often cheaper to purchase, and the use of a more simple MOSFET gate driver. Because of this, the non-synchronous topology is often used when cost is a driving factor, and efficiency is not required. Due to its simpler design, the non-synchronous topology is also easier to build quickly on a breadboard when a voltage step-down is required.

5 Reduced Switching Frequency (Discontinuous Conduction)



The voltage waveform shown about is produces by causing the non-synchronous converter to operate in discontinuous conduction mode. In discontinuous conduction mode, the inductor will completely discharge, causing the current through it to be zero. when this occurs it will no longer be able to supply the load, causing the load to draw all its current from the capacitor. This can be seen in the image above. The initial high voltage peak that occurs during the on period of the PWM charged the inductor. Once the PWM switches to the off period we see the voltage return to ground until it suddenly spikes again and ramps down towards ground. This secondary spike and ramp correspond with the inductor becoming fully discharged, what we observe is the remaining capacitor voltage being discharged across the load, hence the downwards ramp.