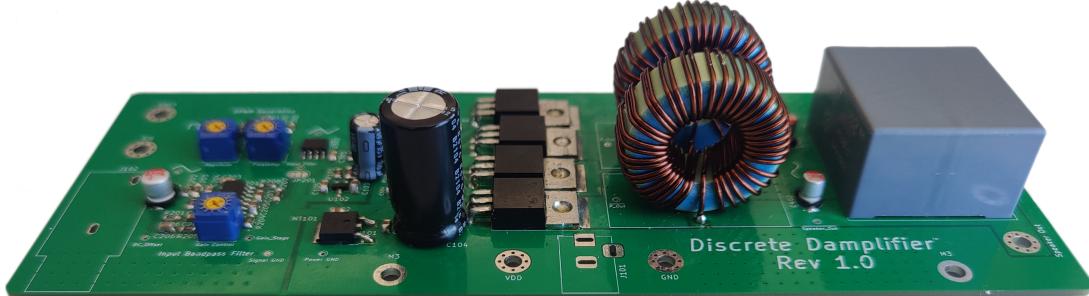


ECEN405 D-Class Amplifier

'What a buck converter would say if it could talk'

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1 Introduction

Audio amplifiers facilitate the driving of high power speakers from small signal audio outputs. Common amplifier types for high fidelity audio are the class A and AB amplifier. These amplifiers provide high power outputs and very little distortion, with the limitation of low power efficiency. The efficiency losses in these topologies are due to the continuous operation of their amplifying elements (usually BJT's) within their saturation region, generating large continuous losses in the form of heat.

In contrast, the class D amplifier is a high efficiency power amplifier. These high efficiencies are achieved through the use of switching elements as amplifiers, allowing for no continuous power loss within the design. This topology can provide efficiencies of up to 90-95%, with the limitation of greatly increased design complexity.

The purpose of this report is to discuss the design and implementation of a class D amplifier for use in driving a sub-woofer speaker to given specifications outlined in Section 1.1. This project was completed in a group of three, where I have taken responsibility for the audio sampling and sinusoidal pulse width modulation (SPWM) generation designs. We have all contributed equally to the final PCB and schematic designs.

1.1 Specifications

- Supply 80W of power into a 4Ω load $\rightarrow P_{out} = 80W$ for $R_L = 4\Omega$.
- Have a 10Hz to 200Hz operating bandwidth.
- Have an input sensitivity of 1V for maximum output.
- Cost a maximum of \$50 per unit.

2 Design

The operation of a class D amplifier can be broken down into discrete sections that are outlined in Figure 1. From this figure we see that the first section is the input audio signal filter, which acts to remove unwanted signal components from the input audio before amplification. In the next stage this filtered audio is sampled at high frequency using a triangle wave and a comparator to produce a high frequency SPWM carrier signal. Finally, this SPWM signal is then amplified to a high power output with a MOSFET before being low pass filtered again to remove the SPWM carrier frequency.

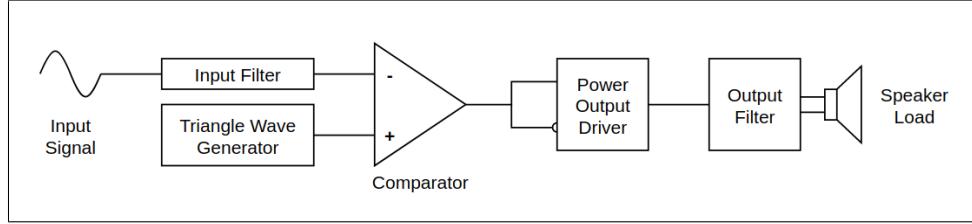


Figure 1: D-Class amplifier high level block diagram

2.1 High Level Design Decisions

The high level design of this class D amplifier consisted of two decision, the selection of amplifier topology, and the selection of the input supply voltage level and supplies.

There exists two topologies for the design of class D amplifiers, half-bridge and full-bridge. The differentiating feature of these topologies is the configuration of their switching elements, with full-bridge requiring four MOSFETS and two gate drivers, while half-bridge requires two MOSFETS and a single gate driver. This has the effect of requiring the half-bridge topology to drive both the positive and negative portions of the output through a single MOSFET bridge, therefore requiring double the input voltage to achieve the same output power as the full-bridge topology. The half-bridge topology can also cause large fluctuations in the supply rail for the amplification, and therefore will often be accompanied by a feedback controller to account for these supply changes. Because of the design complications of the half-bridge topology, our design will implement the full-bridge class D amplifier.

For the selection of the designs power supply, it was decided that a single supply rail should be provided to the amplifier, with all other required voltage levels being generated internally. This was selected to provide a more cohesive and easy to operate final design. Based on this design, the required input voltage (V_{DD}) to achieve the specified output power of 80W has been calculated in the following equation to be 26V. This is then stepped down to both 12V and 5V internally through the use of linear regulators. A $1000\mu\text{F}$ reservoir capacitor was also selected to reduce the strain on the input power supply from the high frequency high power switching elements.

$$V_{DD} = \sqrt{2 \cdot R_L \cdot P_{out}} = \sqrt{2 \cdot 4 \cdot 80} = 25.29 \approx 26$$

In Figure 2 we can see the finalised high-level schematic design of the amplifier. In this schematic the input supply stages can be found, as well as the high level design of the amplifier as discussed in Section 2.

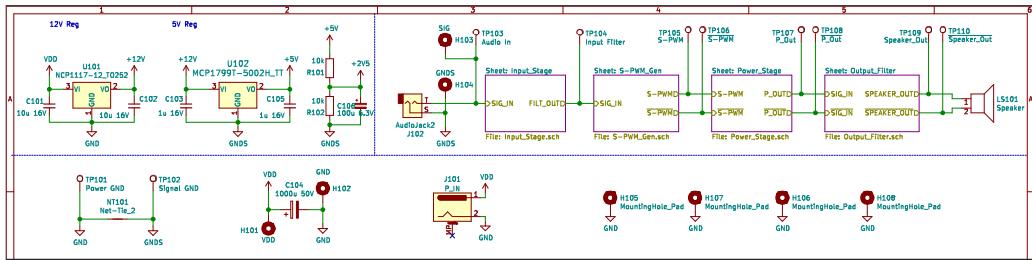


Figure 2: High level design schematic

2.2 Input Filter

The design of the input filter was required to provide a signal passband of 10Hz to 200Hz, and function correctly for input signals of up to 1V amplitude, $2V_{pk-pk}$ as specified in Section 1.1. The design of this section was undertaken by Nickolai Wolfe, and the finalised schematic of this can be seen in Figure 3.

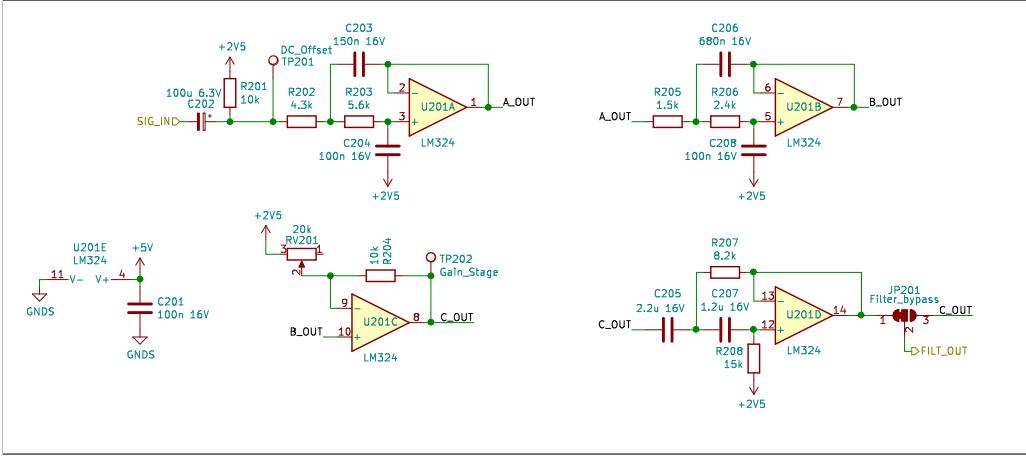


Figure 3: Input filtering schematic

This design consists of a forth order low pass active Butterworth filter with a cut-off frequency of 300Hz, and a second order high pass active Butterworth filter with a cut-off frequency of 10Hz. This provides 40dB per decade gain roll-off for inputs frequencies below 10Hz, as well as a 80dB per decade gain roll-off for inputs frequencies above 300Hz. It should also be noted that the placement of the low pass corner frequency at 300Hz ensures that there is a constant 0dB gain across the full specified bandwidth of the amplifier.

The output signal of the input filter has a DC bias of 2.5V imposed on it. This has been implemented to ‘mid-rail’ the opamps utilised within this design, allowing them to function correctly from a single 5V DC supply.

This input stage also provides an amplifier gain stage to allow for tuning of the filter output amplitude.

2.3 Audio Sampling & SPWM

$$f = \frac{R_2}{4(R_1 \cdot R_2 \cdot C_1)}$$

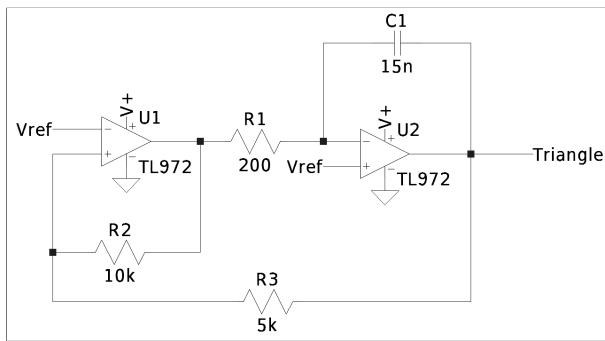


Figure 4: Triangle waveform generation circuit

2.4 Power Stage & Output Filter

3 Implementation

Here you should discuss the assembly of the amplifier and any problems you faced as a team building the amplifier.

Here, the individual components should also be characterised. For example: if you have a filter, what is the response and how does it compare to the calculated? If you have a triangle wave, how does it look? Is it doing what I should? Why? Why not? How do the inputs/outputs of your comparator look? How does the square wave on the gate of the MOSFETs look?

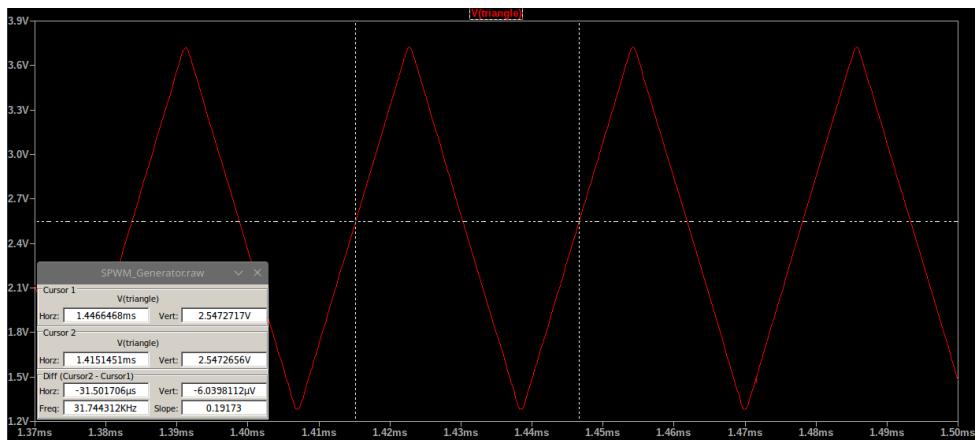


Figure 5: Simulation of the generated 32kHz triangle waveform

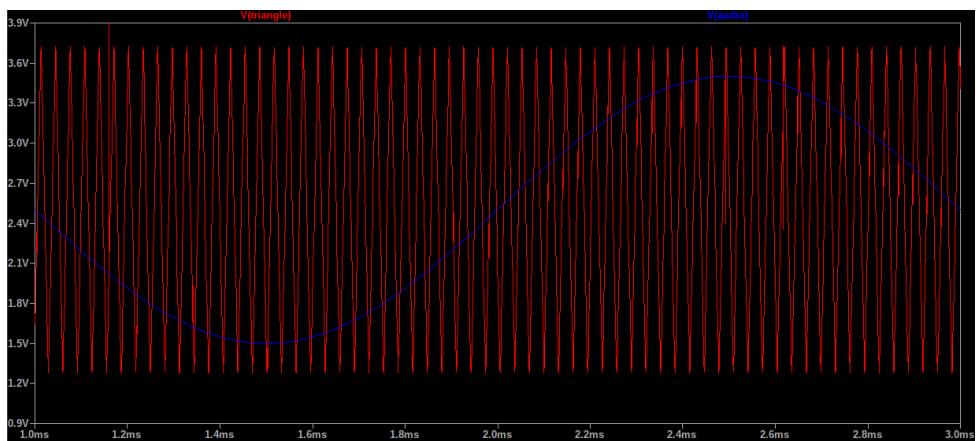


Figure 6: Simulation of a 1V peak to peak input signal sampling

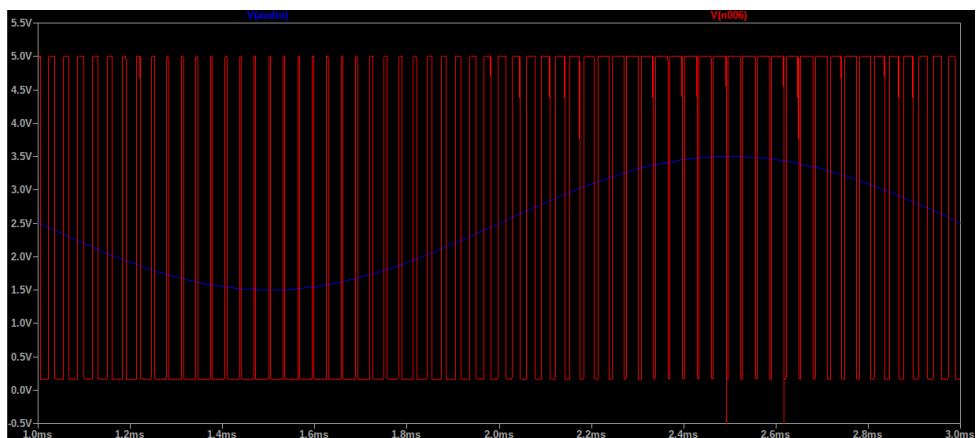


Figure 7: Simulation of the SPWM comparator output

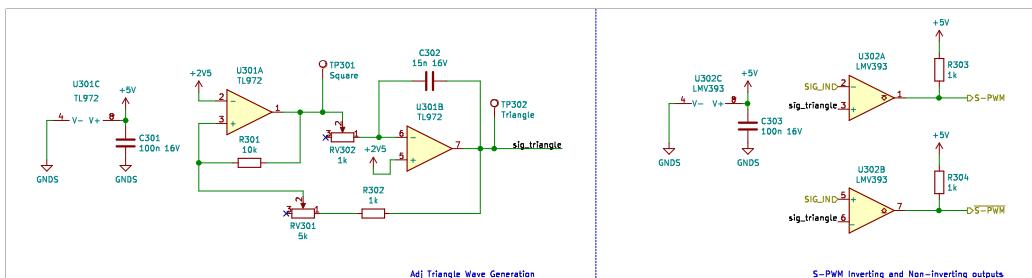


Figure 8: Sampling triangle wave & SPWM generation schematic

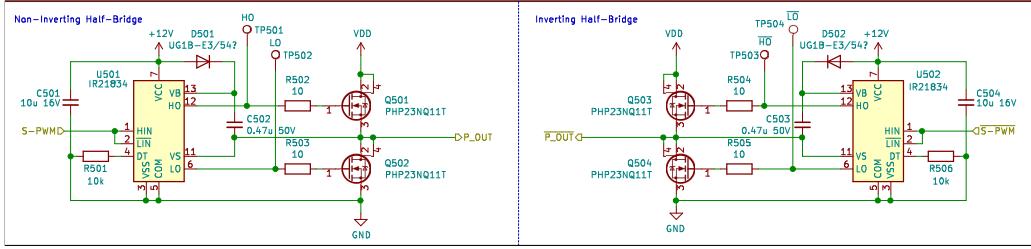


Figure 9: Gate driver schematic

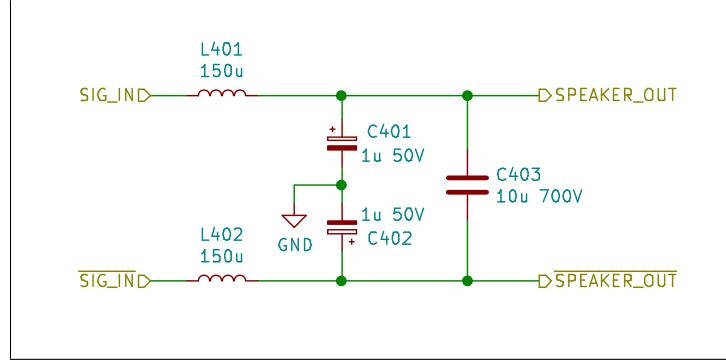


Figure 10: Output filter schematic

3.1 PCB Design and Layout

4 Results

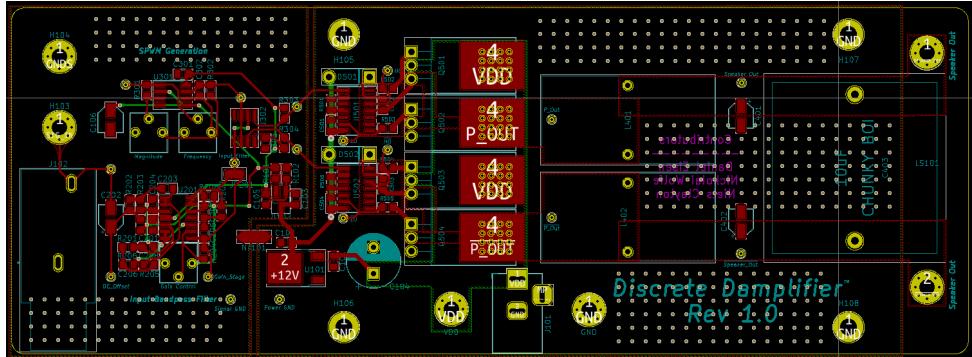
Here I would expect to see the results of the whole amp, for example: an output wave, analysis of the efficiency, discuss maximum power output (which may be frequency dependent), and THD.

Frequency (Hz)	THD (%)
30	1.8
50	2.2
100	3.2
200	3.3
300	3.5
500	3.2

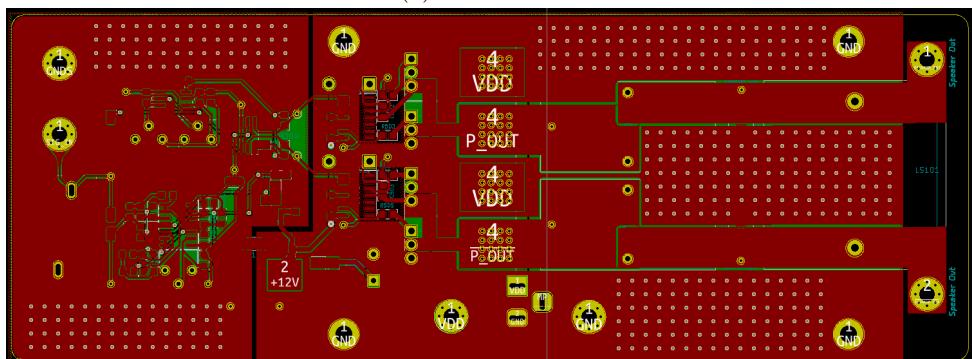
Table 1: Output total harmonic distortion across frequency

5 Conclusions

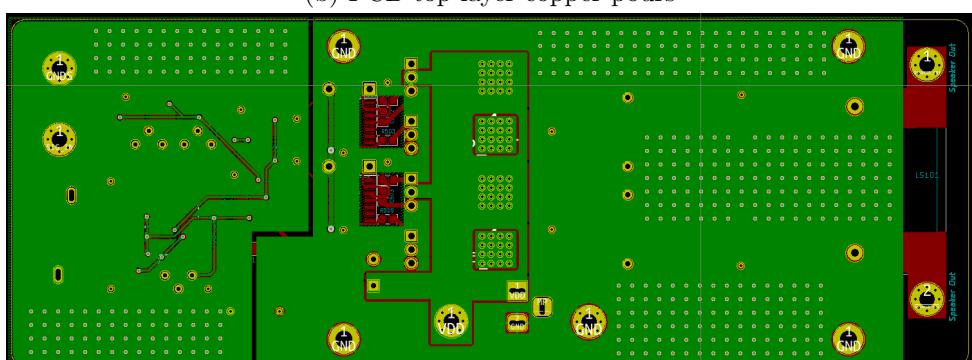
What worked, didn't work? How would you change your approach? Any interesting insights?



(a) PCB Traces

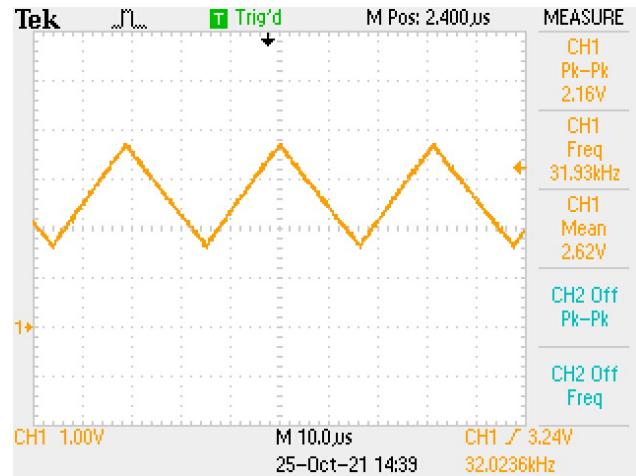


(b) PCB top layer copper pours

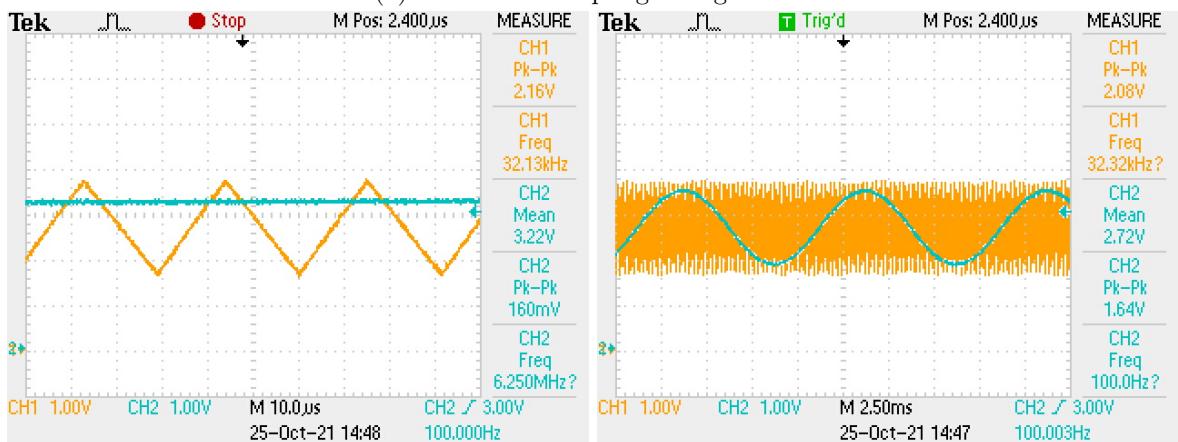


(c) PCB bottom layer copper pours

Figure 11: Design PCB layouts



(a) Generated sampling triangle wave



(b) Triangle wave sampling input signal

(c) Triangle wave sampling envelop of input signal

Figure 12

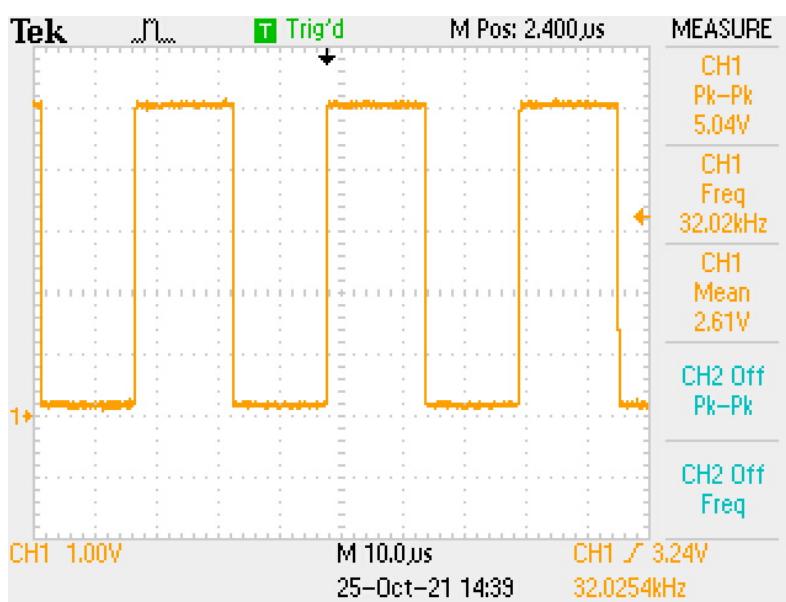


Figure 13: Amplifier output bode plot

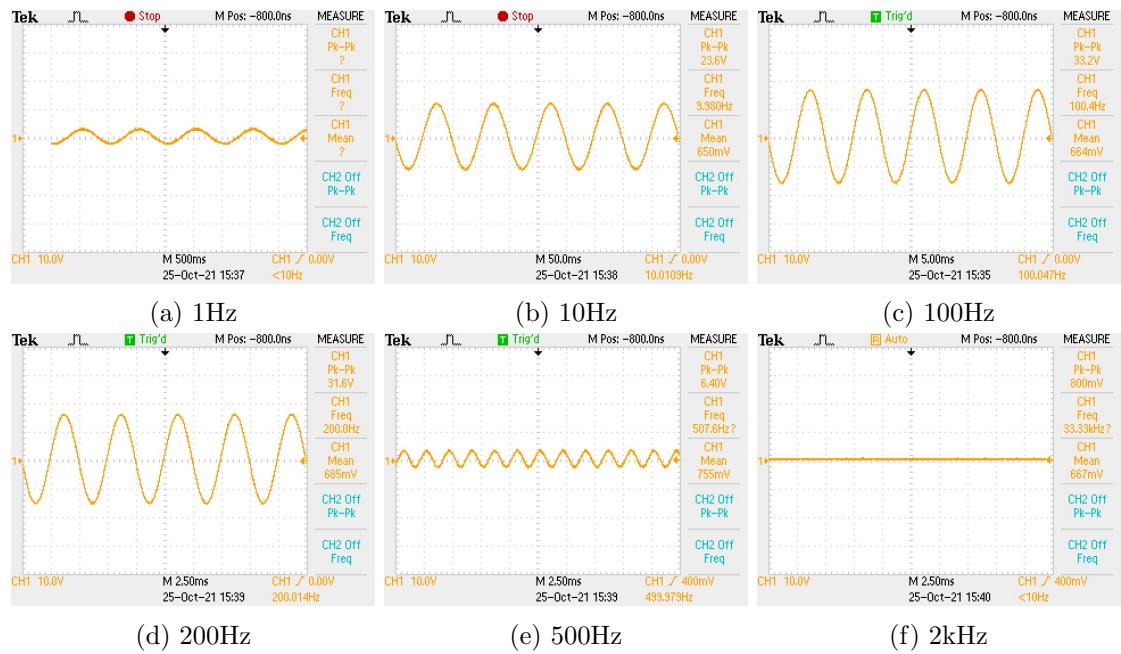


Figure 14: Amplifier output to varying frequency input signal

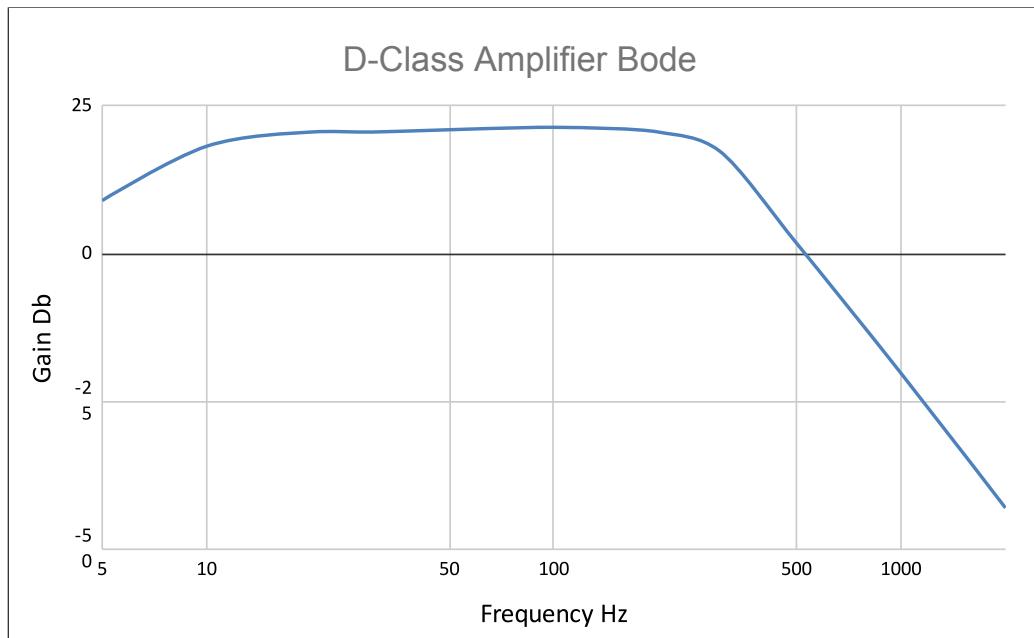


Figure 15: Amplifier output bode plot

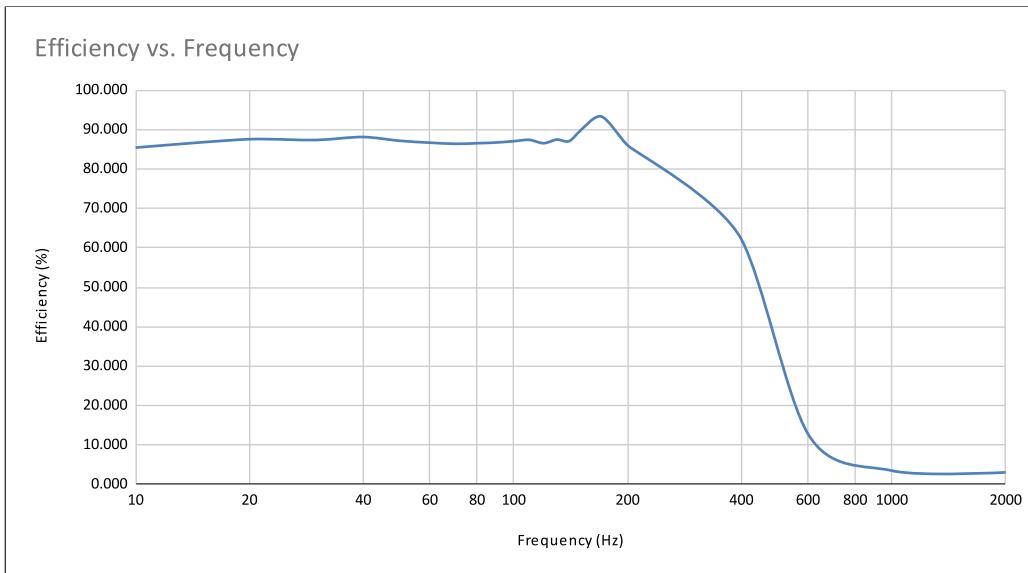


Figure 16: Amplifier output efficiency vs frequency

Appendix

Input Filter

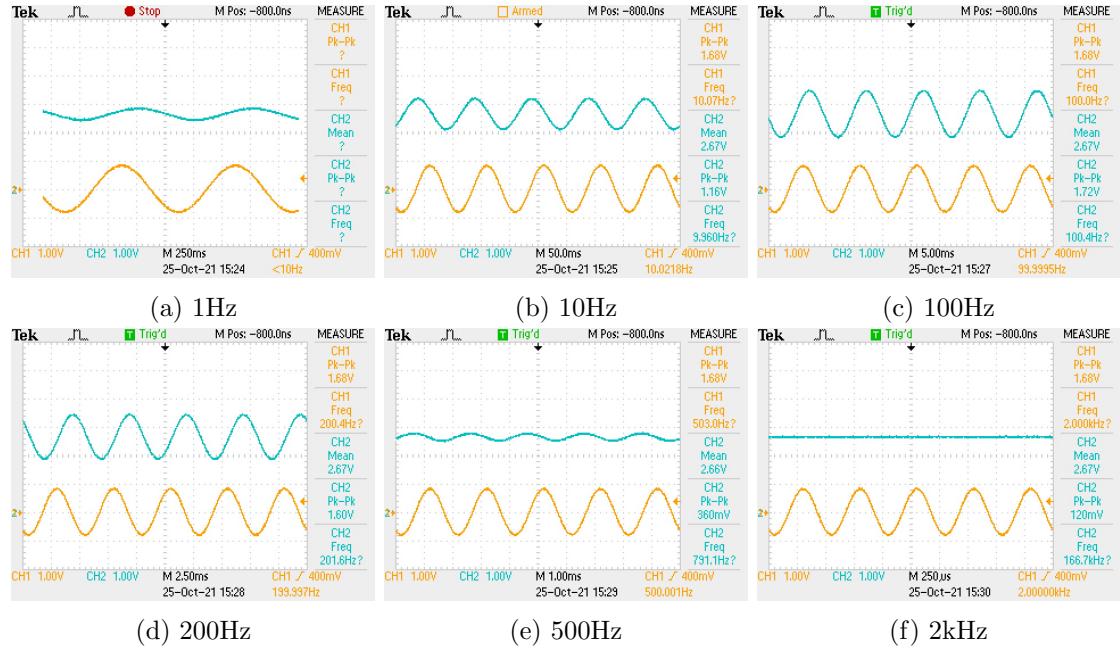


Figure 17: Input filter operation across frequencies, input signal (yellow) vs filter output (blue)