## Power Factor Correction Circuits (PFC)

- Basic Principle with single-phase input
- PFC Controller Design

1

1

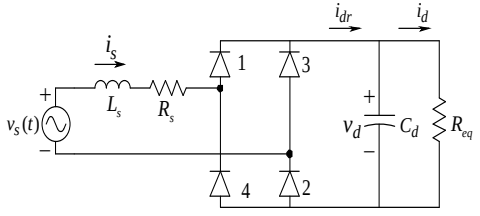
## Why Power Factor Correction?

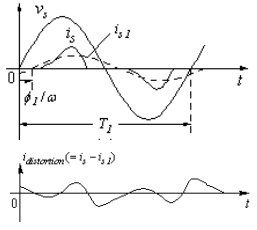
- Reduces RMS input current
- Facilitates power supply hold-up – smaller capacitor
- Improves efficiency of downstream converters
- Improves efficiency of Power Network

2

2

# Diode Rectifier Circuit:



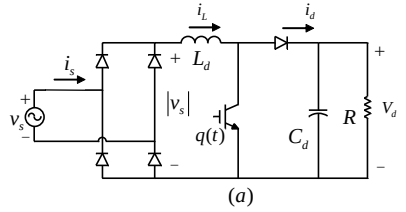



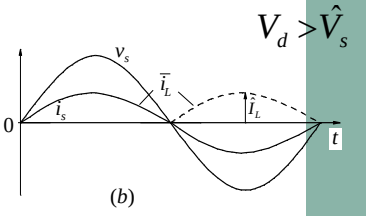


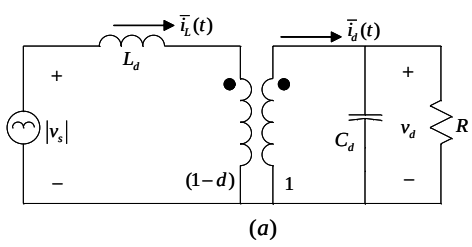

3

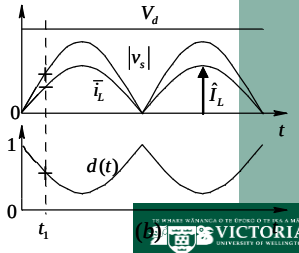
## Implementation of PFC

- Use a boost dc-dc converter to shape the rectified current



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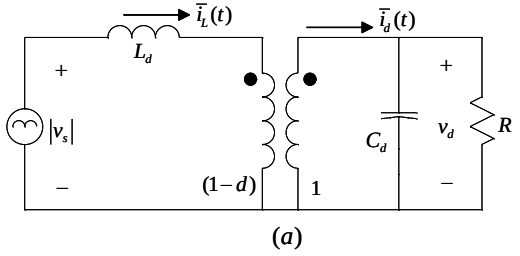


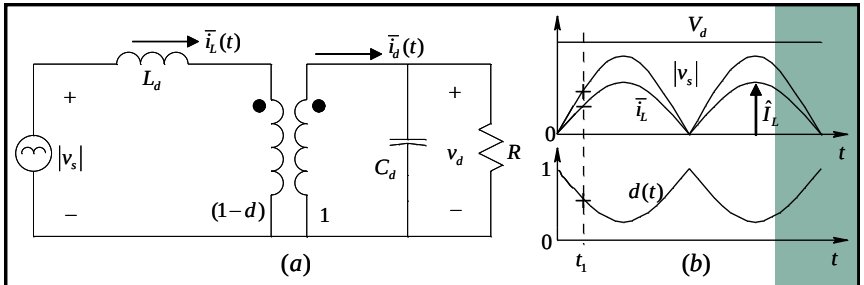

$$\frac{V_d}{|v_s|}=\frac{1}{1-d(t)}$$

$$1-d(t)=\frac{\hat{V}_s|\sin(\omega t)|}{V_d}$$

$$d(t)=1-\frac{\hat{V}_s|\sin(\omega t)|}{V_d}$$

5

5




$$1-d(t)=\frac{\hat{V}_s|\sin(\omega t)|}{V_d} \qquad \bar{i}_L=\hat{I}_L|\sin(\omega t)|$$

$$\bar{i}_d=(1-d(t))\bar{i}_L=\frac{\hat{V}_s|\sin(\omega t)|}{V_d}\hat{I}_L|\sin(\omega t)|=\frac{\hat{V}_s\hat{I}_L}{V_d}|\sin(\omega t)|^2$$

6

$$\bar{i}_d = \frac{\hat{V}_s \hat{I}_L}{V_d}\left|\sin(\omega t)\right|^2$$

$$\bar{i}_d = \frac{\hat{V}_s \hat{I}_L}{V_d}\sin^2(\omega t) = \frac{\hat{V}_s \hat{I}_L}{V_d}\left(\frac{1}{2} - \frac{1}{2}\cos(2\omega t)\right)$$

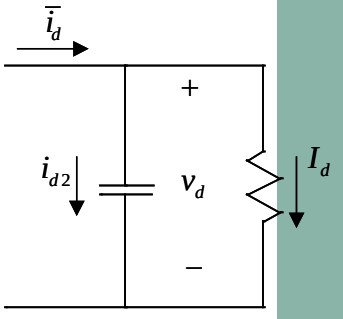
$$\bar{i}_d = \underbrace{\frac{1}{2}\frac{\hat{V}_s}{V_d}\hat{I}_L}_{I_d} - \underbrace{\frac{1}{2}\frac{\hat{V}_s}{V_d}\hat{I}_L \cos 2\omega t}_{i_{d2}(t)}$$

7



# Calculation of $\hat{V}_{d2}$

$$\bar{i}_d = \underbrace{\frac{1}{2}\frac{\hat{V}_s}{V_d}\hat{I}_L}_{I_d} - \underbrace{\frac{1}{2}\frac{\hat{V}_s}{V_d}\hat{I}_L \cos 2\omega t}_{i_{d2}(t)}$$

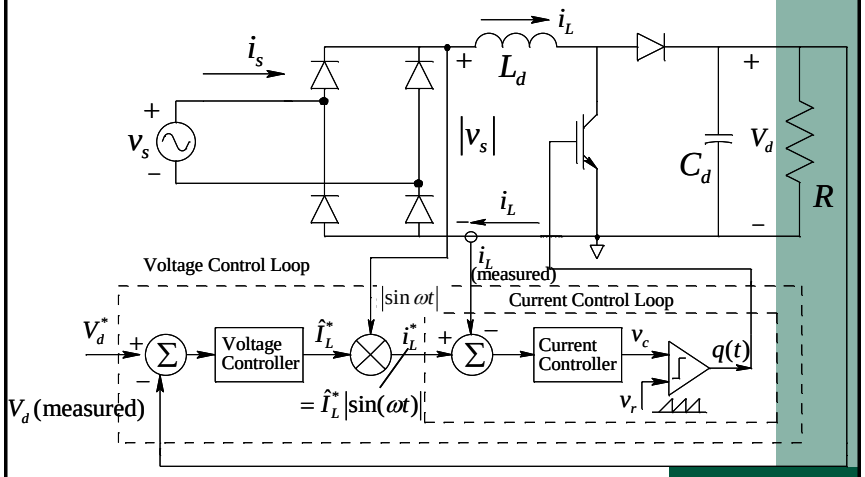



$$\hat{I}_{d2} = \frac{1}{2}\frac{\hat{V}_s}{V_d}\hat{I}_L$$

$$\hat{V}_{d2} = \left(\frac{1}{2\omega C}\right)\hat{I}_{d2} = \frac{\hat{I}_L}{4\omega C}\frac{\hat{V}_s}{V_d}$$

8

## CONTROL OF PFC






9

## Concept Quiz

The Power-Factor-Correction circuit shapes the inductor current to appear as if a purely resistive load was connected at the output of the diode rectifier.

A. True

B. False



10

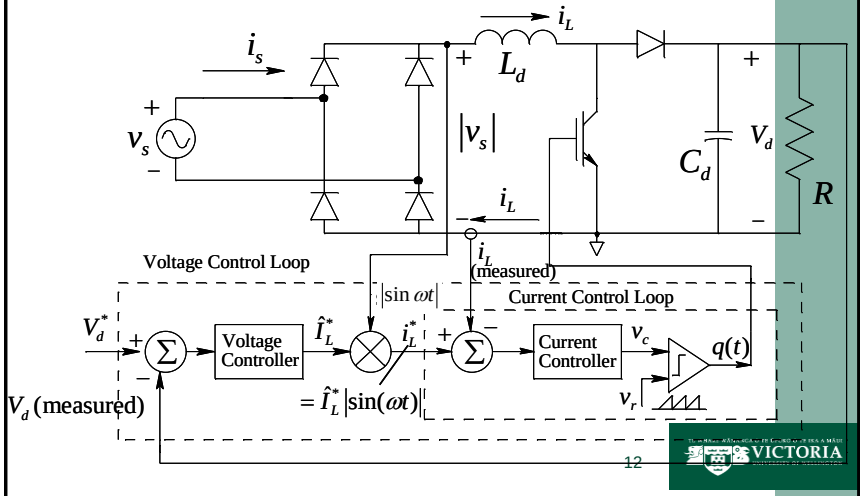
## Quiz

In a PFC, other than the dc component and the switching-frequency related components, the diode current into the output stage contains only of the second-harmonic (of the line-frequency) component.

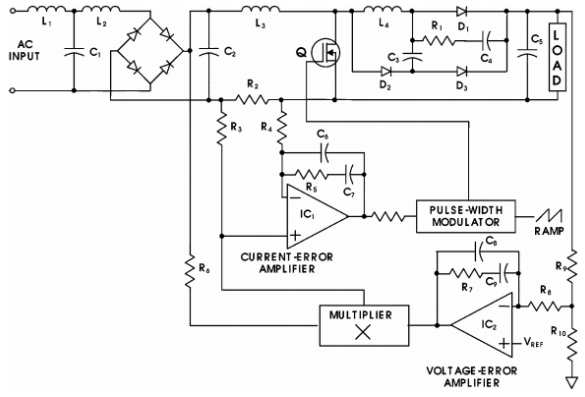
A. Correct
B. Incorrect



## PFC Controller Design



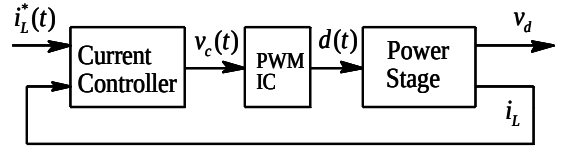
## The circuit



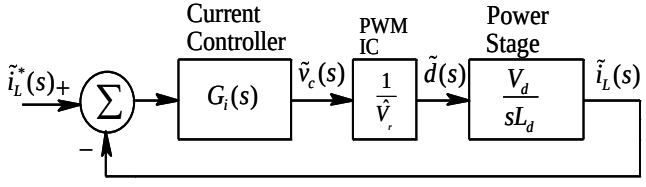

13

13

## DESIGNING INNER AVERAGE-CURRENT-CONTROL LOOP




(a)

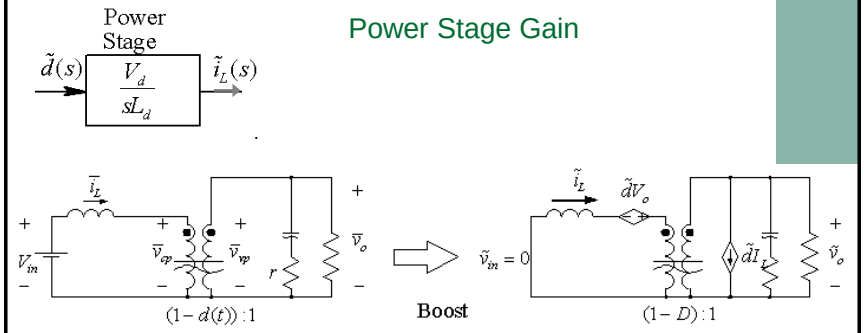



(b)

14

14

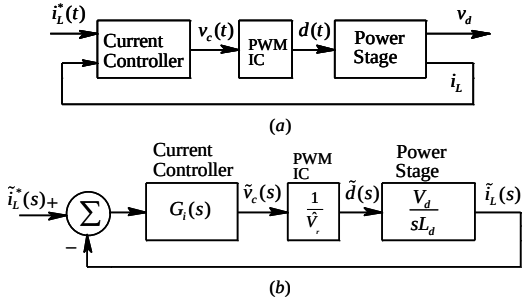
## Power Stage Gain






15

## DESIGNING INNER AVERAGE-CURRENT-CONTROL LOOP




PWM-IC: $\frac{\tilde{d}(s)}{\tilde{v}_c(s)} = \frac{1}{\hat{V}_r}$

Controller: $G_i(s) = \frac{k_c}{s}\underbrace{\frac{1+s/\omega_z}{1+s/\omega_p}}_{\text{phase boost}}$

Power-Stage: $\frac{\tilde{i}_L(s)}{\tilde{d}(s)} = \frac{V_d}{sL_d}$

$K_{boost} = \tan(45^o + \frac{\phi_{boost}}{2})$

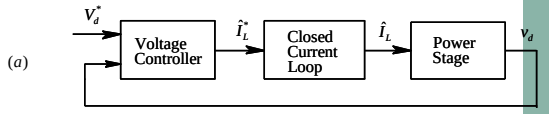
$f_z = \frac{f_{ci}}{K_{boost}}$ $\quad f_p = K_{boost} f_{ci}$ $\quad k_c = \omega_z \left|G_C(s)\right|_{f_c}$



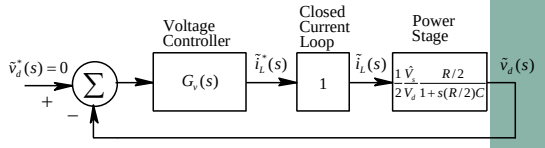
16

## DESIGNING THE OUTER VOLTAGE LOOP

(a)




(b)




$$G_v(s)=\frac{k_v}{1+s/\omega_{cv}}$$

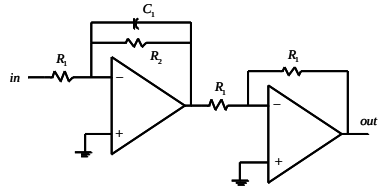
$$\left|\frac{k_v}{1+s/\omega_{cv}}\frac{1}{2}\frac{\hat{V}_s}{V_d}\frac{R/2}{1+s(R/2)C}\right|_{s=j(2\pi\times f_{cv})}=1$$

$$\left|\frac{k_v}{1+s/\omega_{cv}}\right|_{s=j(2\pi\times 120)}=\frac{\hat{I}_{L2}}{\hat{V}_{d2}} \qquad \frac{\hat{I}_{L2}}{\hat{I}_L}=1.5\%$$

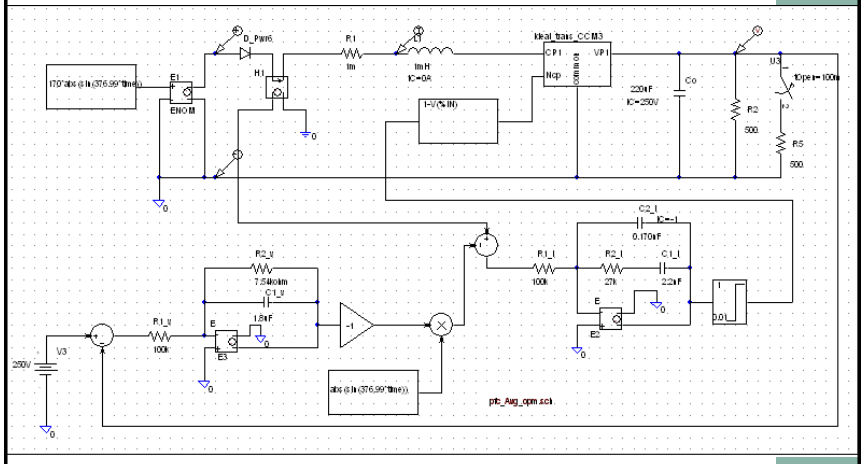




$$G_v(s)=\frac{k_v}{1+s/\omega_{cv}}$$



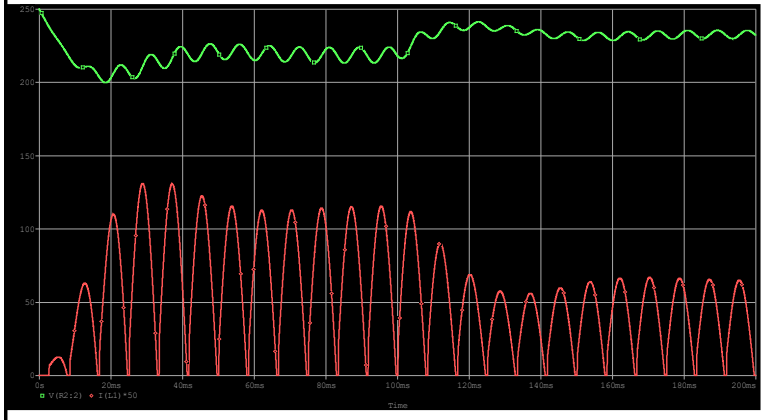
## PSpice Modeling:






19

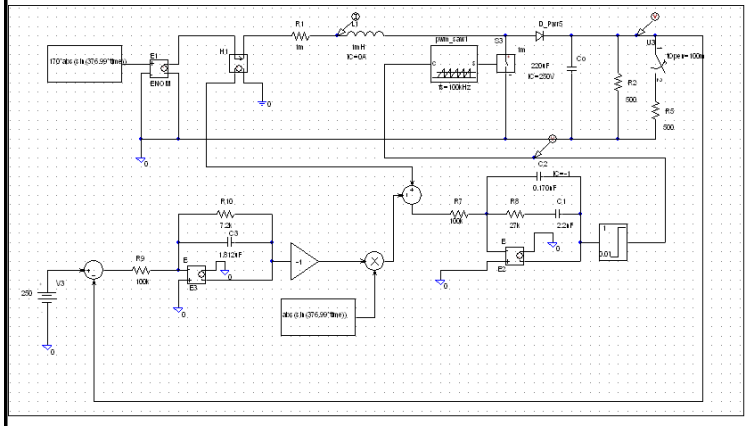
## Simulation Results






20

## PSpice Switching Circuit Modeling:



21



## Simulation Results


22

## Practically

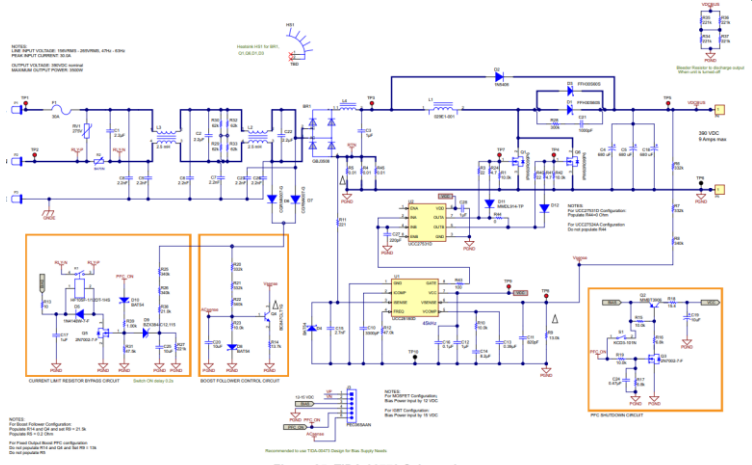
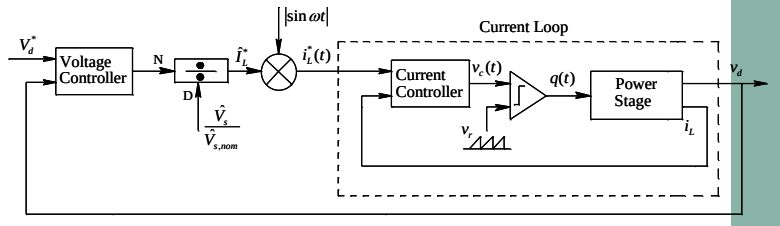


Figure 25. TIDA-00779 Schematics



23

## FEEDFORWARD OF THE INPUT VOLTAGE






24

## Summary

- PFC Basics
- PFC Controller Design

25

25

## Concept Quiz

In the PFC Controller design, the inner current control loop is of the following type:

A. Peak-Current-Mode

B. Average-Current-Mode

26

26