ECEN405 Lab 6 Report

Niels Clayton : 300437590

---

1 Introduction

Cover the motivation for using a class D in the real world and how it relates to content from ECEN405.

2 Design

Here you should describe how your class D amplifier works, giving details of each subsection. In detail, you should describe the section you designed and the design choices you made. If your team broke up the design of the amplifier in a way that doesn't suit individual parts being discussed, you will need to talk about the whole design in a bit more detail but you should also describe how the work was delegated and why.

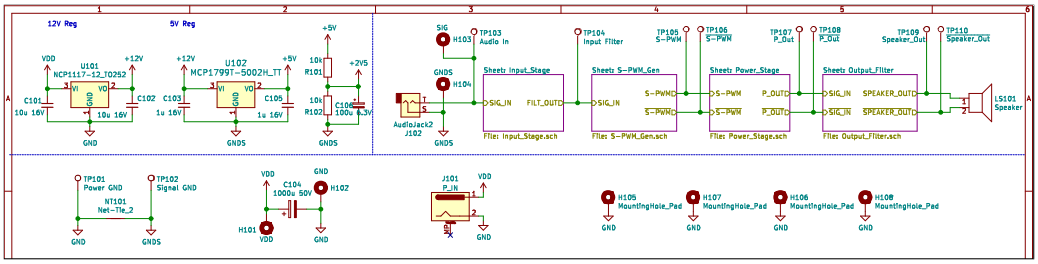


Figure 1: High level design schematic

2.1 Circuit Design and Simulation

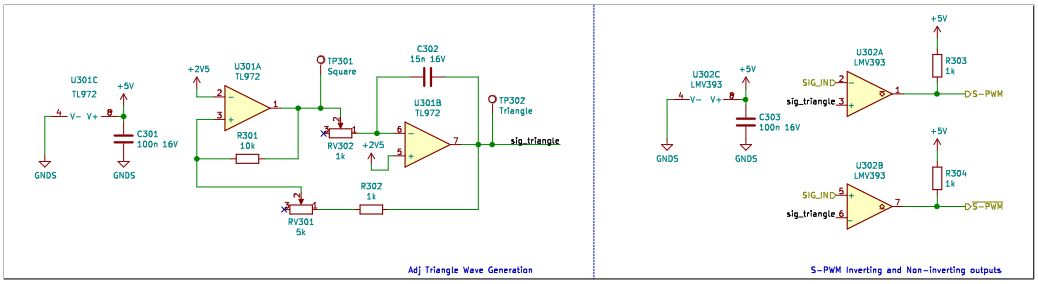


Figure 2: Sampling triangle wave & SPWM generation schematic

2.2 PCB Design and Layout

3 Implementation

Here you should discuss the assembly of the amplifier and any problems you faced as a team building the amplifier.
Here, the individual components should also be characterised. For example: if you have a filter, what is the response and how does it compare to the calculated? If you have a triangle wave, how does it look? Is it doing what I should? Why? Why not? How do the inputs/outputs of your comparator look? How does the square wave on the gate of the MOSFETs look?

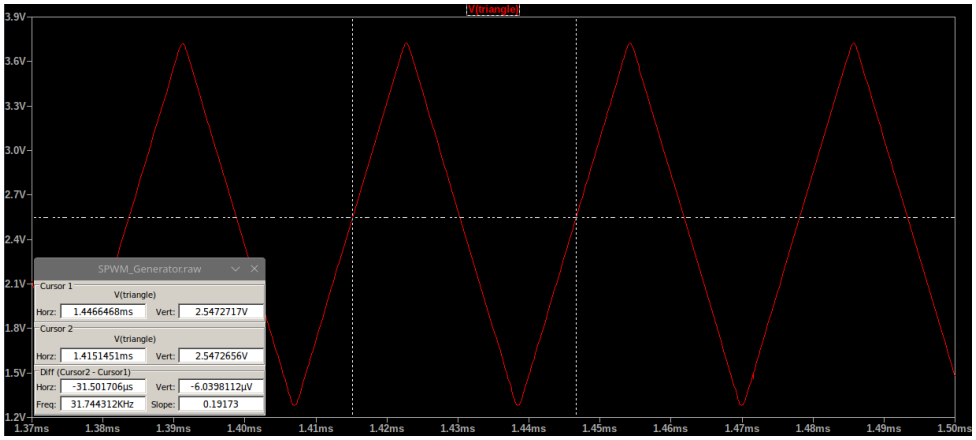


Figure 3: Simulation of the generated 32kHz triangle waveform

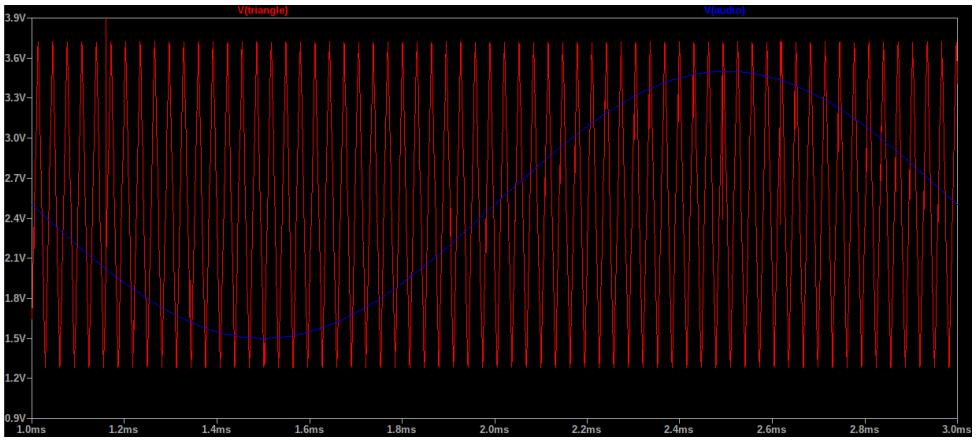


Figure 4: Simulation of a 1V peak to peak input signal sampling

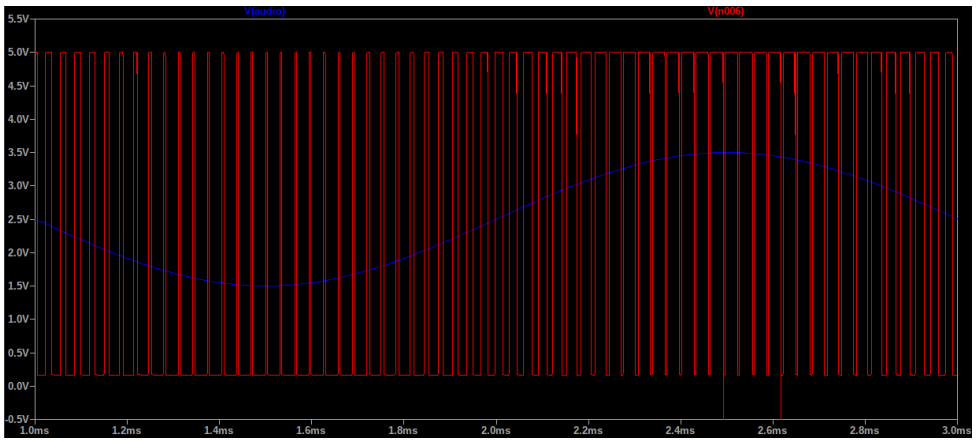


Figure 5: Simulation of the SPWM comparator output

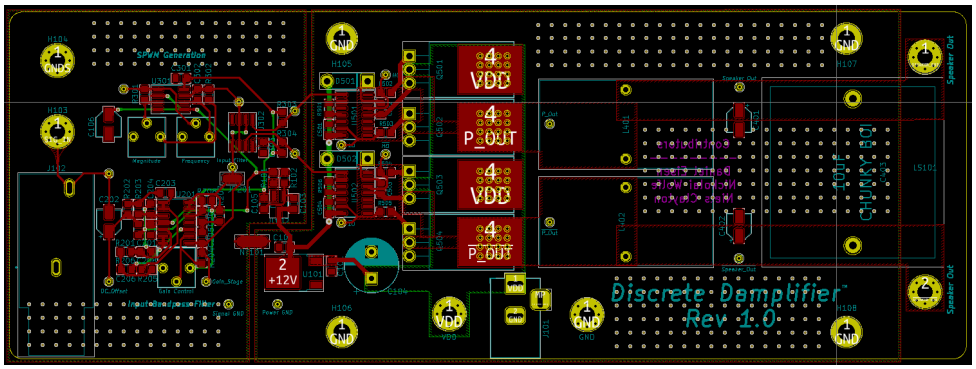
4 Results

Here I would expect to see the results of the whole amp, for example: an output wave, analysis of the efficiency, discuss maximum power output (which may be frequency dependent), and THD.

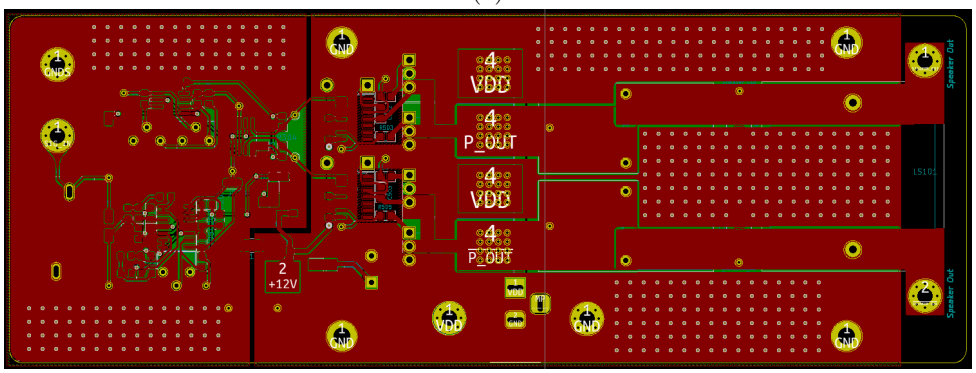
5 Conclusions

What worked, didn't work? How would you change your approach? Any interesting insights?

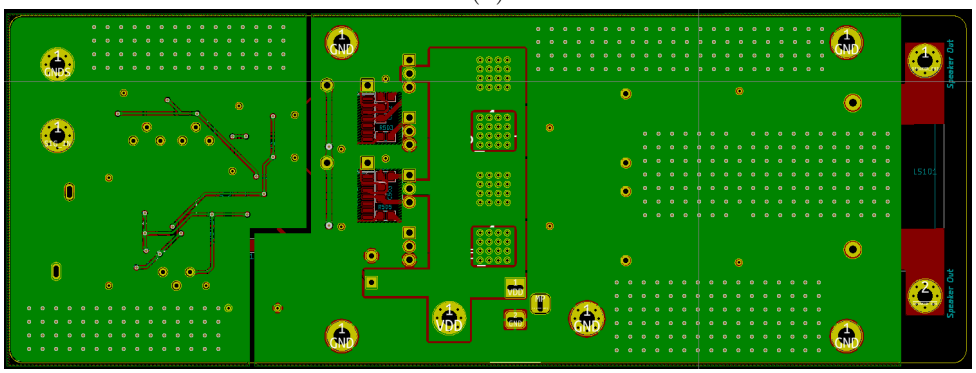
Appendix



(a)



(b)



(c)

Figure 6

Frequency (Hz)	THD (%)
30	1.8
50	2.2
100	3.2
200	3.3
300	3.5
500	3.2

Table 1: Output total harmonic distortion across frequency

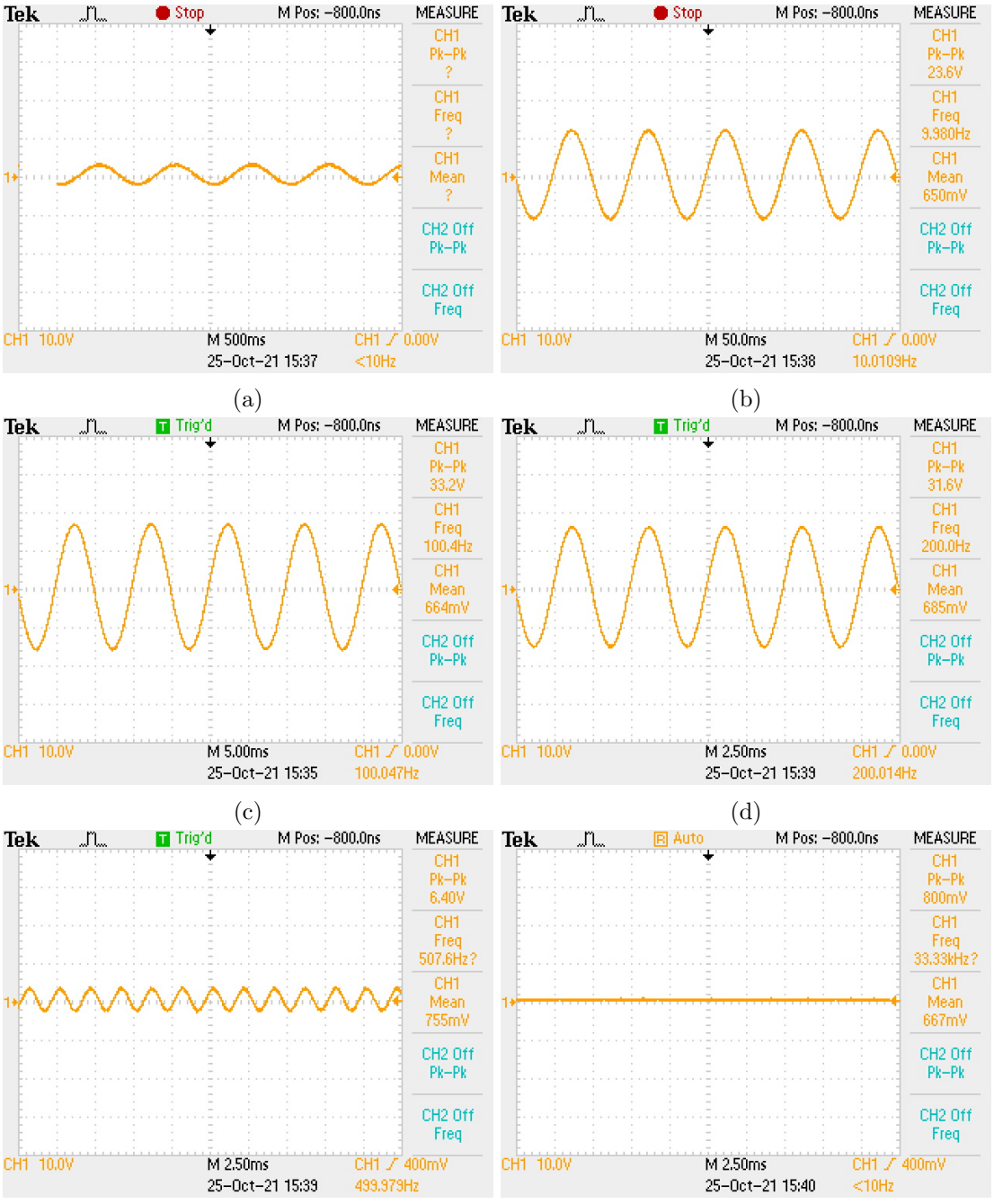

Tek
Stop
M Pos: -800.0ns
MEASURE
CH1 Pk-Pk ?
CH1 Freq ?
CH1 Mean ?
CH2 Off Pk-Pk
CH2 Off Freq
CH1 10.0V
M 500ms
CH1 ∕ 0.00V
25-Oct-21 15:37
<10Hz
(a)
Tek
Stop
M Pos: -800.0ns
MEASURE
CH1 Pk-Pk 23.6V
CH1 Freq 9.980Hz
CH1 Mean 650mV
CH2 Off Pk-Pk
CH2 Off Freq
CH1 10.0V
M 50.0ms
CH1 ∕ 0.00V
25-Oct-21 15:38
10.0109Hz
(b)
Tek
Trig'd
M Pos: -800.0ns
MEASURE
CH1 Pk-Pk 33.2V
CH1 Freq 100.4Hz
CH1 Mean 664mV
CH2 Off Pk-Pk
CH2 Off Freq
CH1 10.0V
M 5.00ms
CH1 ∕ 0.00V
25-Oct-21 15:35
100.047Hz
(c)
Tek
Trig'd
M Pos: -800.0ns
MEASURE
CH1 Pk-Pk 31.6V
CH1 Freq 200.0Hz
CH1 Mean 685mV
CH2 Off Pk-Pk
CH2 Off Freq
CH1 10.0V
M 2.50ms
CH1 ∕ 0.00V
25-Oct-21 15:39
200.014Hz
(d)
Tek
Trig'd
M Pos: -800.0ns
MEASURE
CH1 Pk-Pk 6.40V
CH1 Freq 507.6Hz?
CH1 Mean 755mV
CH2 Off Pk-Pk
CH2 Off Freq
CH1 10.0V
M 2.50ms
CH1 ∕ 400mV
25-Oct-21 15:39
499.979Hz
(e)
Tek
Auto
M Pos: -800.0ns
MEASURE
CH1 Pk-Pk 800mV
CH1 Freq 33.33kHz?
CH1 Mean 667mV
CH2 Off Pk-Pk
CH2 Off Freq
CH1 10.0V
M 2.50ms
CH1 ∕ 400mV
25-Oct-21 15:40
<10Hz
(f)

Figure 7

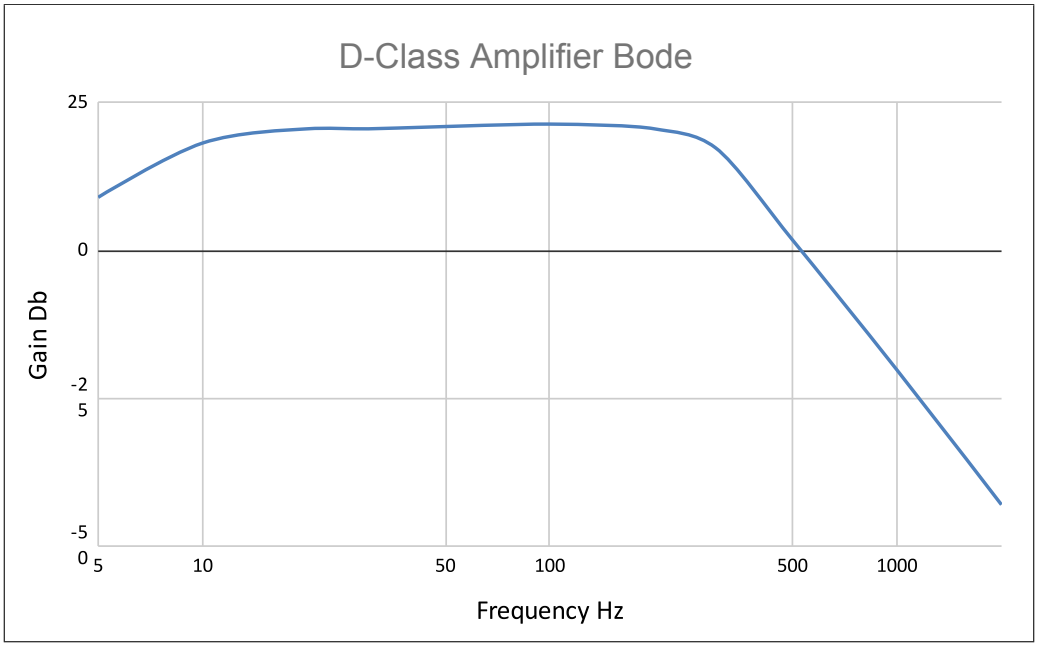


Figure 8: Amplifier output bode plot

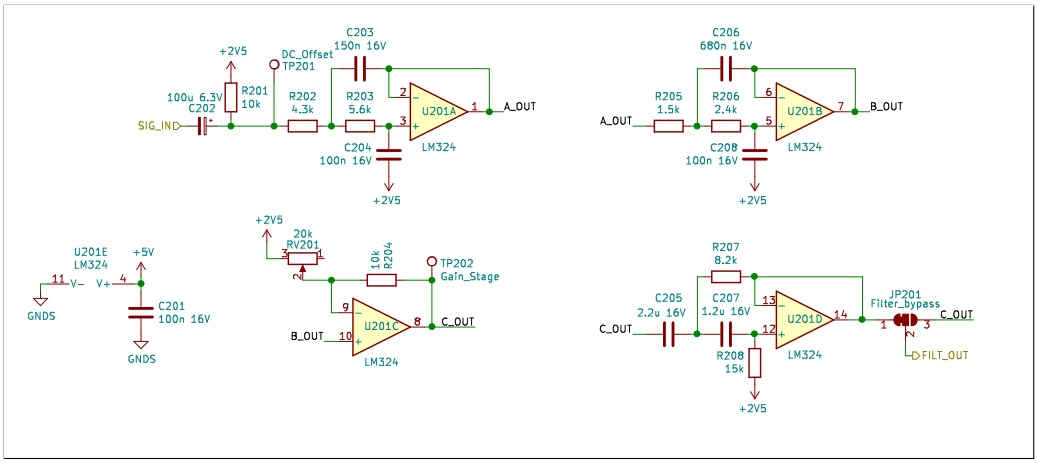


Figure 9: Input filtering schematic

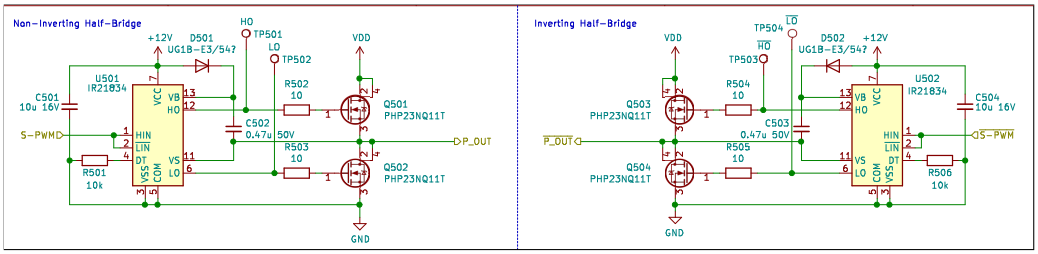


Figure 10: Gate driver schematic

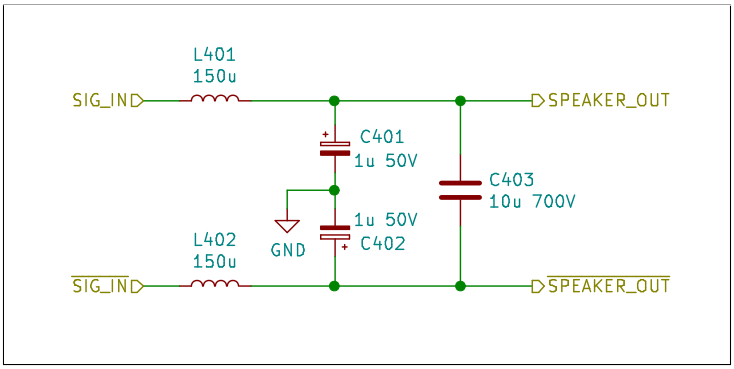


Figure 11: Output filter schematic