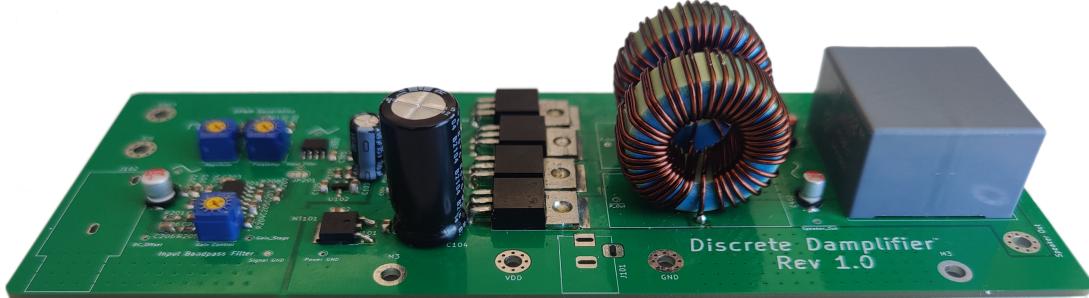


# ECEN405 D-Class Amplifier

*'What a buck converter would say if it could talk'*

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## 1 Introduction

Audio amplifiers facilitate the driving of high power speakers from small signal audio outputs. Common amplifier types for high fidelity audio are the class A and AB amplifier. These amplifiers provide high power outputs and very little distortion, with the limitation of low power efficiency. The efficiency losses in these topologies are due to the continuous operation of their amplifying elements (usually BJT's) within their saturation region, generating large continuous losses in the form of heat.

In contrast, the class D amplifier is a high efficiency power amplifier. These high efficiencies are achieved through the use of switching elements as amplifiers, allowing for no continuous power loss within the design. This topology can provide efficiencies of up to 90-95%, with the limitation of greatly increased design complexity.

The purpose of this report is to discuss the design and implementation of a class D amplifier for use in driving a sub-woofer speaker to given specifications outlined in Section 1.1. This project was completed in a group of three, where I have taken responsibility for the audio sampling and sinusoidal pulse width modulation (SPWM) generation designs. We have all contributed equally to the final PCB and schematic designs.

### 1.1 Specifications

- Supply 80W of power into a  $4\Omega$  load  $\rightarrow P_{out} = 80W$  for  $R_L = 4\Omega$ .
- Have a 10Hz to 200Hz operating bandwidth.
- Have an input sensitivity of 1V for maximum output.
- Cost a maximum of \$50 per unit.

## 2 Design

The operation of a class D amplifier can be broken down into discrete sections that are outlined in Figure 1. From this figure we see that the first section is the input audio signal filter, which acts to remove unwanted signal components from the input audio before amplification. In the next stage this filtered audio is sampled at high frequency using a triangle wave and a comparator to produce a high frequency SPWM carrier signal. Finally, this SPWM signal is then amplified to a high power output with a MOSFET before being low pass filtered again to remove the SPWM carrier frequency.

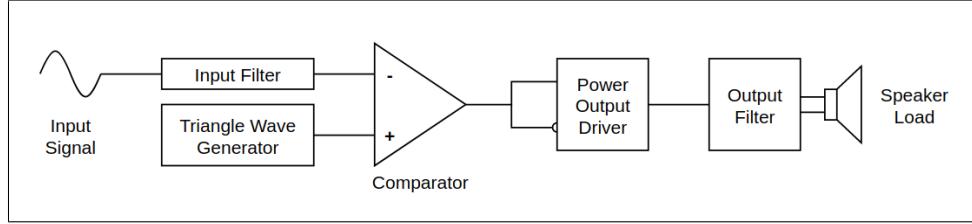


Figure 1: D-Class amplifier high level block diagram

## 2.1 High Level Design Decisions

The high level design of this class D amplifier consisted of two decision, the selection of amplifier topology, and the selection of the input supply voltage level and supplies.

There exists two topologies for the design of class D amplifiers, half-bridge and full-bridge. The differentiating feature of these topologies is the configuration of their switching elements, with full-bridge requiring four MOSFETS and two gate drivers, while half-bridge requires two MOSFETS and a single gate driver. This has the effect of requiring the half-bridge topology to drive both the positive and negative portions of the output through a single MOSFET bridge, therefore requiring double the input voltage to achieve the same output power as the full-bridge topology. The half-bridge topology can also cause large fluctuations in the supply rail for the amplification, and therefore will often be accompanied by a feedback controller to account for these supply changes. Because of the design complications of the half-bridge topology, our design will implement the full-bridge class D amplifier.

For the selection of the designs power supply, it was decided that a single supply rail should be provided to the amplifier, with all other required voltage levels being generated internally. This was selected to provide a more cohesive and easy to operate final design. Based on this design, the required input voltage ( $V_{DD}$ ) to achieve the specified output power of 80W has been calculated in the following equation to be 26V. This is then stepped down to both 12V and 5V internally through the use of linear regulators. A  $1000\mu\text{F}$  reservoir capacitor was also selected to reduce the strain on the input power supply from the high frequency high power switching elements.

$$V_{DD} = \sqrt{2 \cdot R_L \cdot P_{out}} = \sqrt{2 \cdot 4 \cdot 80} = 25.29 \approx 26$$

In Figure 2 we can see the finalised high-level schematic design of the amplifier. In this schematic the input supply stages can be found, as well as the high level design of the amplifier as discussed in Section 2.

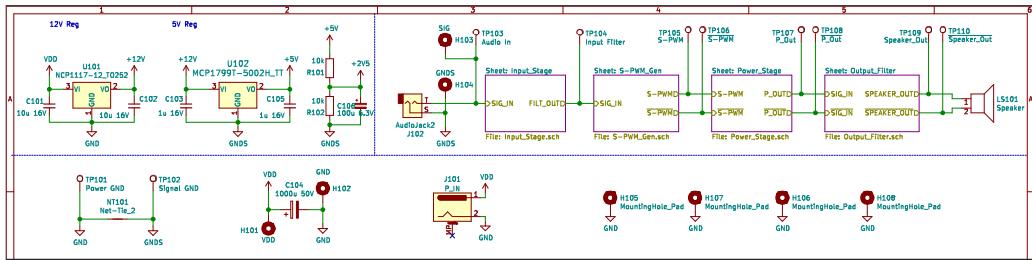


Figure 2: High level design schematic

## 2.2 Input Filter

The design of the input filter was required to provide a signal passband of 10Hz to 200Hz, and function correctly for input signals of up to 1V amplitude,  $2V_{pk-pk}$  as specified in Section 1.1. The design of this section was undertaken by Nickolai Wolfe, and the finalised schematic of this can be seen in Figure 3.

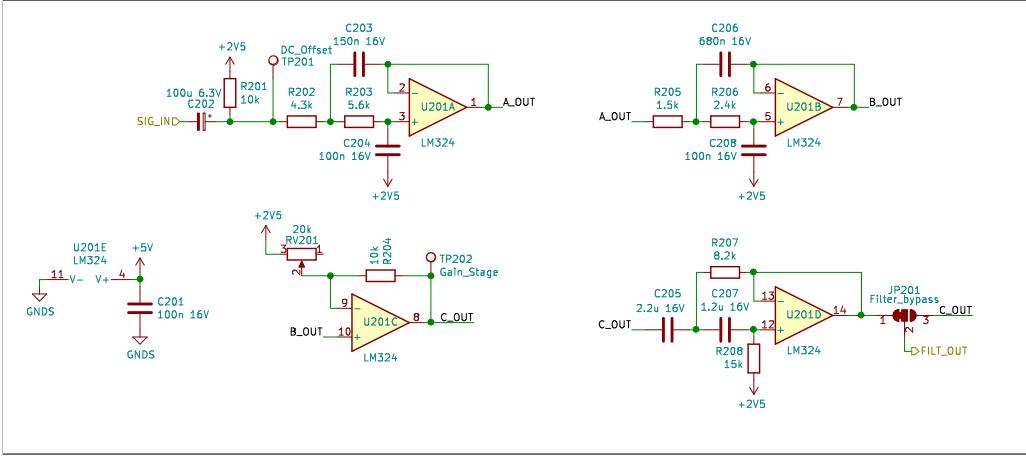


Figure 3: Input filtering schematic

This design consists of a forth order low pass active Butterworth filter with a cut-off frequency of 300Hz, and a second order high pass active Butterworth filter with a cut-off frequency of 10Hz. This provides 40dB per decade gain roll-off for inputs frequencies below 10Hz, as well as a 80dB per decade gain roll-off for inputs frequencies above 300Hz. It should also be noted that the placement of the low pass corner frequency at 300Hz ensures that there is a constant 0dB gain across the full specified bandwidth of the amplifier.

The output signal of the input filter has a DC bias of 2.5V imposed on it. This has been implemented to ‘mid-rail’ the opamps utilised within this design, allowing them to function correctly from a single 5V DC supply.

This input stage also provides an amplifier gain stage to allow for tuning of the filter output amplitude to vary between  $1V_{pk-pk}$  and  $3V_{pk-pk}$ .

### 2.3 Audio Sampling & SPWM

The audio sampling and SPWM generation stage requires the generation of a high quality high frequency triangle waveform. This waveform is compared to the input audio signal with a comparator, facilitating the production of an SPWM carrier signal where the PWM duty cycle encodes the input signal voltage at that given sample.

The design requirements for this section have been selected to ensure that all requirements outlined in Section 1.1 are met, and such that interfacing with both the input filter and the power amplification stage is simple.

With these requirements, the following set of specifications for this design were devised.

- The sampler must produce a triangle wave sampling signal with a switching frequency of at least a decade greater than the highest sampled frequency (200Hz).
- The triangle wave must be imposed on the 2.5V DC offset.
- The sampler must providing the full range of operation for inputs between  $1V_{pk-pk}$  and  $3V_{pk-pk}$  from the input filter.
- The SPWM output must be between 0V and 5V to correctly interface with the selected gate drivers.
- The SPWM output must provide both an inverted and non-inverted output to drive each half bridge.

The sampling triangle wave was generated using an unstable positive feedback opamp oscillator. This circuit design consists of two opamp stages, the first uses positive feedback to cause an opamp to oscillate between its voltage rails and create a square wave, the second integrates this square wave to produce triangle wave. An overview of this circuit can be seen in Figure 4.

Due to this designs reliance on the selected opamps specifications, it becomes difficult to design the exact frequency of the circuits output, however the following equation provides a rough estimate of the output frequency for a given selection of values.

$$f = \frac{R_2}{4(R_1 \cdot R_3 \cdot C_1)}$$

Using this equation, components were calculated that would provide an output triangle wave with a frequency of 30kHz, as this is above the minimum sampling frequency specification of 20kHz.

With these initial components selected, the design was tested within the circuit simulation software LTSpice. A wide assortment of opamp spice models were sourced for the design simulations, with varying slewrates and gain bandwidth products (GBP). Simulations were run across this range of opamps for frequencies between 30kHz and 100kHz, allowing for the comparison and selection of the lowest cost opamp that would be capable of providing the designed switching frequency.

This simulation also allowed for the selection of the triangle wave peak to peak voltage though testing various values for  $R_3$ .

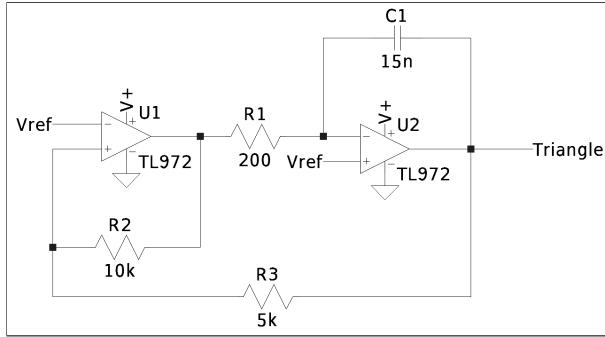


Figure 4: Triangle waveform generation circuit

The final designed circuit can be seen in Figure 8. This circuit utilised the TL972 dual opamp to provide a  $2V_{pk-pk}$  32kHz triangle wave that would also be capable of operating at frequencies of up to 100kHz.

This dual opamp package is capable of implementing the full design. It has also been shown from simulations in Figure 5 show that this opamp is capable of producing a triangle wave with switching frequency and magnitude that meet the given requirements.

In Figure 6 we can see a simulation of a  $2V_{pk-pk}$  input signal within the envelop of the designed triangle. From this we confirm the design is capable of sampling the full input signal range without distortion or clipping. We can also see from both of these figures that the generated triangle wave is imposed on a 2.5V DC offset as specified.

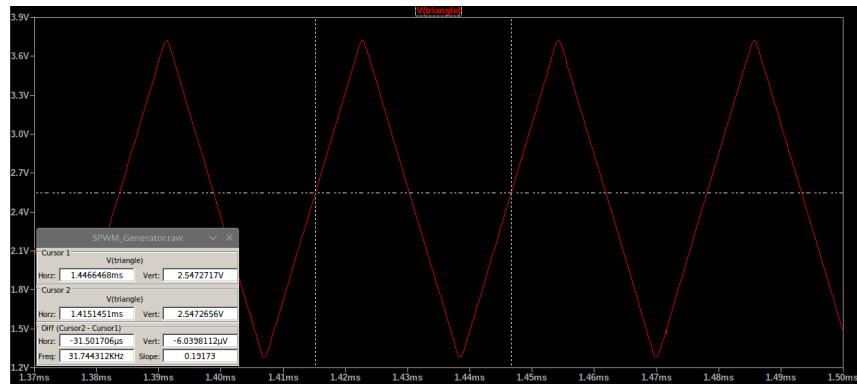


Figure 5: Simulation of the generated 32kHz triangle waveform

Next to design was the SPWM generation circuit. This circuit had the requirement of taking both the audio signal to be sampled, and the sampling triangle waveform, and comparing them

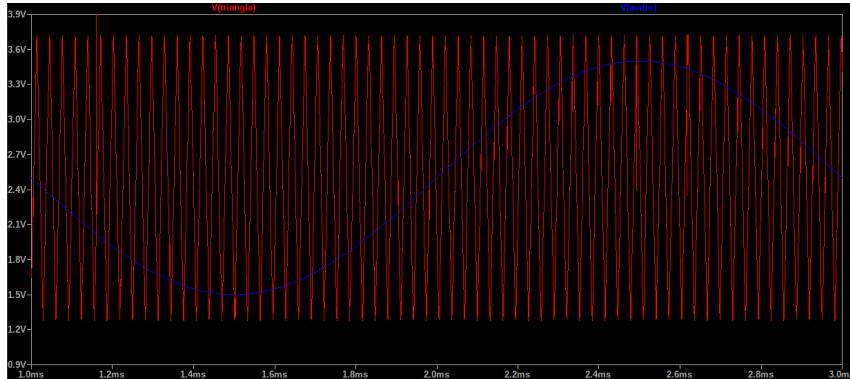


Figure 6: Simulation of a 1V peak to peak input signal sampling

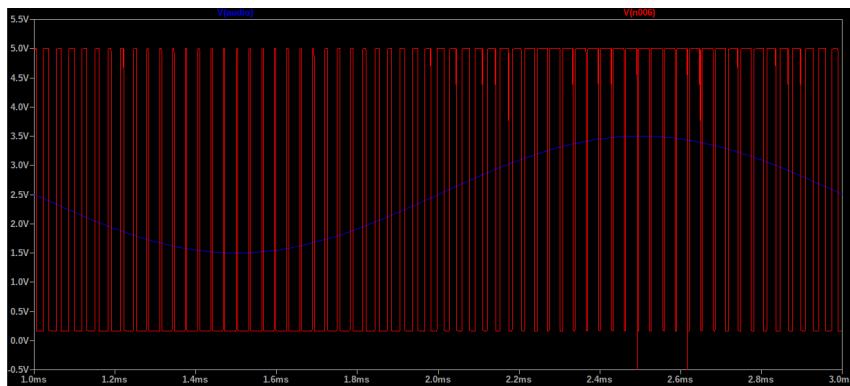


Figure 7: Simulation of the SPWM comparator output

to provide a 5V output. It was also required to provide both an inverted and non-inverted signal output.

To achieve this, a high speed open collector comparator should be used. By selecting an open collector comparator, the output voltage can be defined through the use of a simple voltage pullup resistor. The selected comparator was the LMV393 with a  $1\text{k}\Omega$  pullup resistor. To provide both an inverted and non-inverted output, a dual package comparator was selected, by switching the input terminals of one of the comparators, the signal will be inverted with respect to the other.

Simulations of this SPWM output signal can be found in Figure 7, in which it can be seen that the output signal goes between 0V and 5V, and the duty cycle of the PWM varies depending on the current audio input.

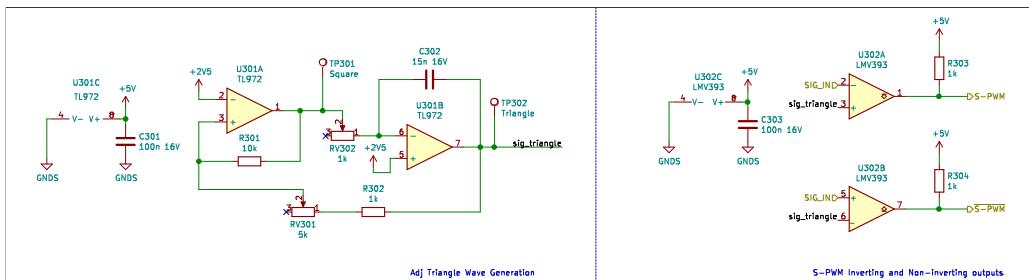


Figure 8: Sampling triangle wave & SPWM generation schematic

The final design and schematic of this section can be seen in Figure 8. In this schematic it can be noted that in the triangle wave generator, resistors  $R_1$  and  $R_3$  have potentiometers in series. This provides the ability to externally tune both the triangle wave frequency between 30kHz and 100kHz, and the scaling between  $1\text{V}_{pk-pk}$  and  $3\text{V}_{pk-pk}$ .

This will allow for the selection of the highest performing switching frequency, as well as the tuning of the sampling to directly match the output of the input filter.

## 2.4 Power Stage & Output Filter

The design of the power stage and output filter was required to amplify the generated SPWM signals from the sampler to  $V_{DD}$  using MOSFET bridges, and then low pass filter this output to remove the SPWM carrier frequency. The design of this section was undertaken by Daniel Eisen.

In Figure 9 the finalised schematic for the MOSFETS and gate drivers can be seen. From this figure it can be seen that this design is split into two symmetrical half-bridge gate drivers, providing the full-bridge topology. This provides the ability to take inputs from both the inverted and non-inverted 5V SPWM signals generated by the sampling stage, and directly step them up to the supply voltage rail.

The gate drivers also provide bootstrapping for the operation of the high-side N-channel MOSFETs, and programmable dead-time.

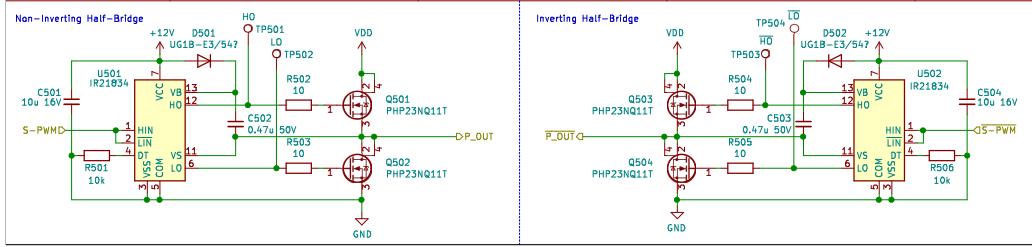


Figure 9: Gate driver schematic

In Figure 10 we can see the the finalised schematic of the output filter. This is a passive second order low pass filter with a cut-off frequency of 3kHz. This cut-off frequency will guarantee a minimum sampling frequency attenuation of 40dB, and has the possibility to provide greater attenuation at increased sampling frequencies.

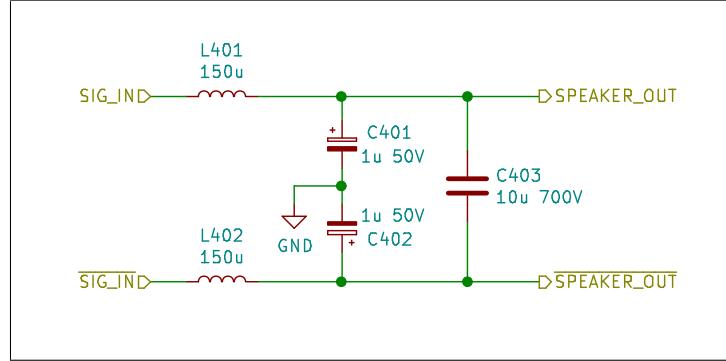


Figure 10: Output filter schematic

## 3 Implementation

This section will discuss the implementation decision made on this project, as well as the issues faces when implementing this project.

### 3.1 PCB Design and Layout

With the final design of the class D amplifier schematic complete, the implementation of the design in the form of a printed circuit board (PCB) began. In Figure 11 we are able to see the final layouts of this designed PCB, including the traces, and both the top and bottom copper pour layers.

As the design of this PCB included both small signal processing at the audio input, and high frequency high power switching at the power output, it was very important to correctly isolate the analog and power ground planes.

To achieve this, a net tie was used to separate the analog and power grounds, and provide a single connection location. This allows for the definition of the current return path of the analog section, ensuring that no high current switching can return underneath sensitive components. These separations can be clearly seen in Figure 11b & Figure 11c

The PCB also features heavy via stitching between the top and bottom copper planes. This is done to both improve the thermal performance of the components, and to ensure there are no potential differences between these two planes.

It can also be noted that all high current paths have been placed using copper pours, providing very low impedance paths.

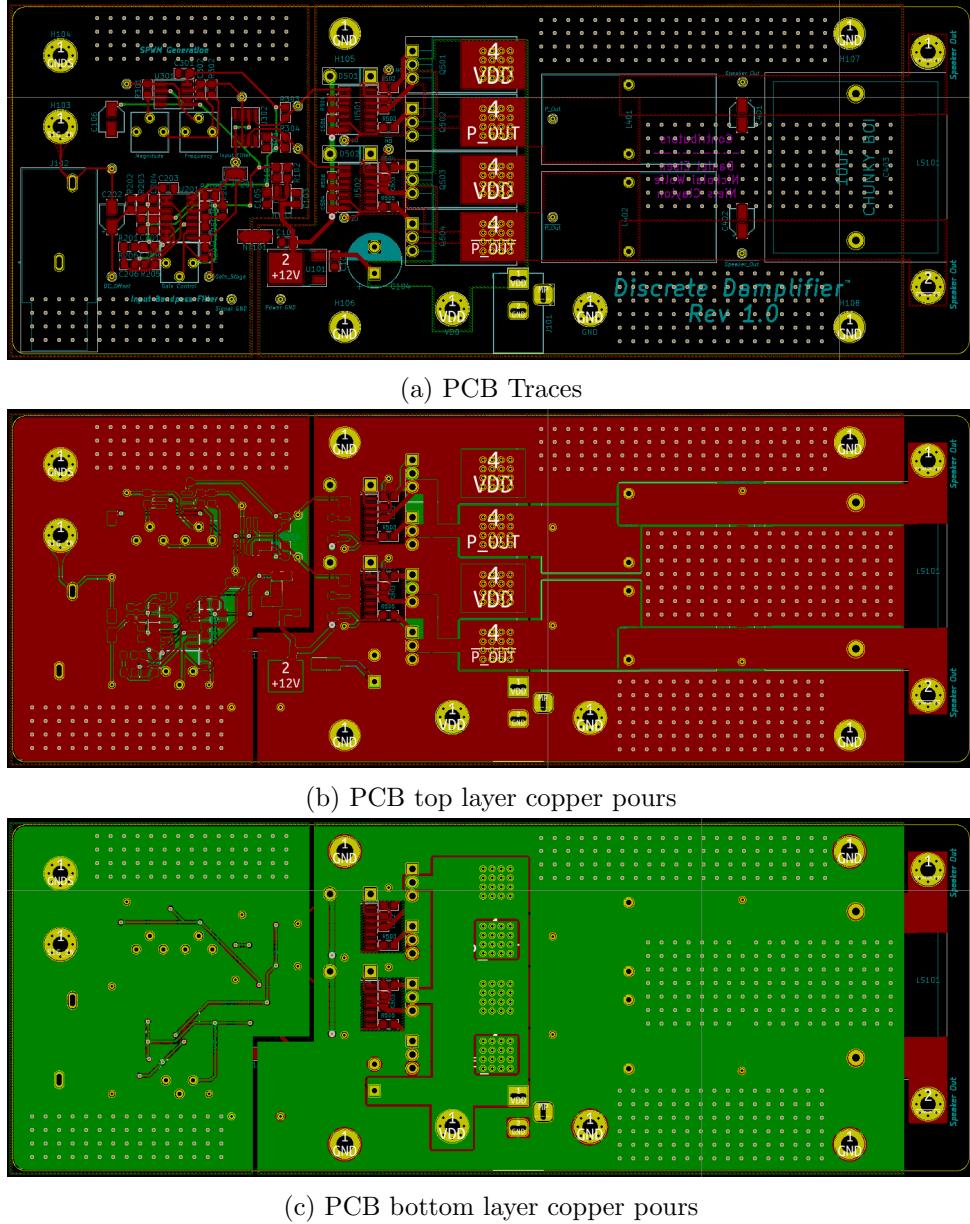


Figure 11: Design PCB layouts

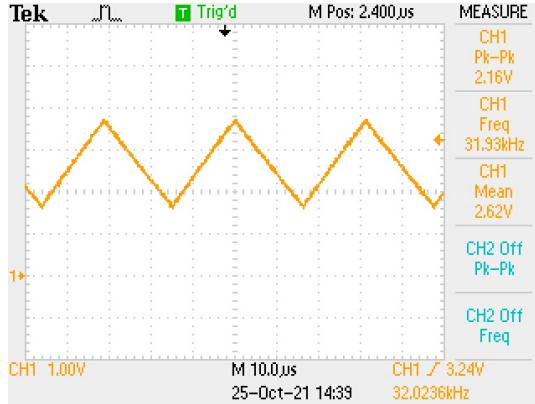
### 3.2 Audio Sampling & SPWM

The initial implementation of the audio sampling triangle wave was unsuccessful. This can be attributed to errors in the manufacturer provided SPICE simulation models of the TL972 opamp, leading to the design being incapable of meeting it's designed requirements. This issue was quickly remedied however as the dual opamp utilised the common SOIC-8 SMD package, this allowed me to easily exchange the opamp for a higher bandwidth LMH6658 opamp.

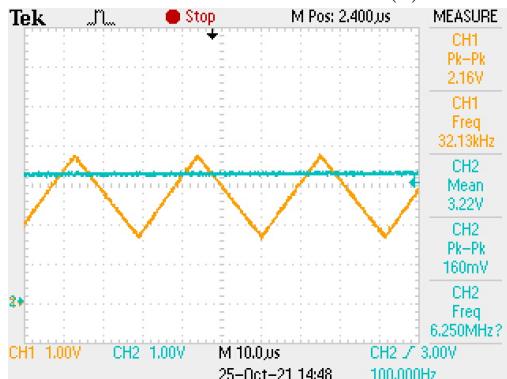
After the replacement opamp was installed, testing was performed to verify the functionality of the audio sampling design.

In Figure 12a the output sampling triangle wave of the implemented circuit can be seen. From this scope image it can be verified that a switching frequency of 32kHz was achieved as designed. It should also be noted that through tuning of the implemented potentiometers it is capable to achieve switching frequencies well beyond 200kHz.

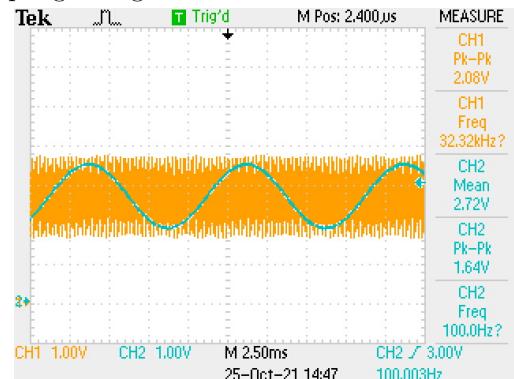
In Figure 12b we can see the triangle waveform directly sampling a 100Hz 2V<sub>pk-pk</sub> input waveform, and in Figure 12c we can see a larger time scale of this sampling. From these two figures we can confirm that the sampling envelop is able to fully sample inputs to the required specifications. It should also be noted that the triangle wave scaling potentiometer is functional, and it is possible to sample inputs ranging between 1V<sub>pk-pk</sub> and 3V<sub>pk-pk</sub> as designed.



(a) Generated sampling triangle wave



(b) Triangle wave sampling input signal



(c) Triangle wave sampling envelop of input signal

Figure 12

Finally, we can confirm the operation of the comparators, and the functionality of the SPWM generation. In Figure 13 we see the comparator output when no input audio is supplied. As expected, this produces a 50% duty cycle PWM output between 0V and 5V.

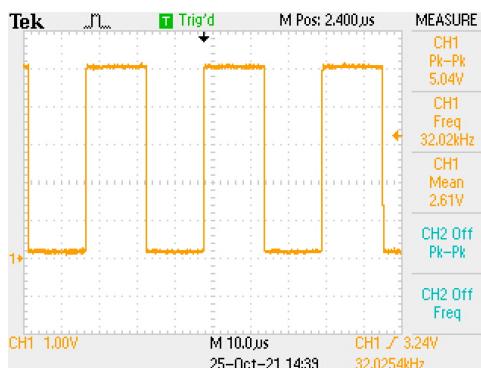


Figure 13: Amplifier output bode plot

## 4 Results

After the successful implementation of the design, a selection of tests were performed to characterise the output of our amplifier, and confirm that we meet all the required specifications.

The first series of test performed were to simply observe the loaded output waveform from the amplifier and a range of frequencies. The outputs of this can be seen in Section 4, in these figures we can visually inspect both the functionality of the input and output filters, as well as observe any distortion on the waveform.

When looking at Figure 14a we can clearly see that there is attenuation of the output caused by the high pass input filter, and we can observe in Figure 14b, that at the 10Hz cut-in frequency this attenuation is mostly gone. Then from Figure 14c & Figure 14d it can be observed that throughout the passband of the filters, there is no attenuation of the output signal, and finally in Figure 14e & Figure 14f we can clearly see the 80dB per decade attenuation of the output.

It can also clearly be seen from these output waveforms that there is little to no noticeable output waveform distortion, and no visible switching from the SPWM carrier frequency.

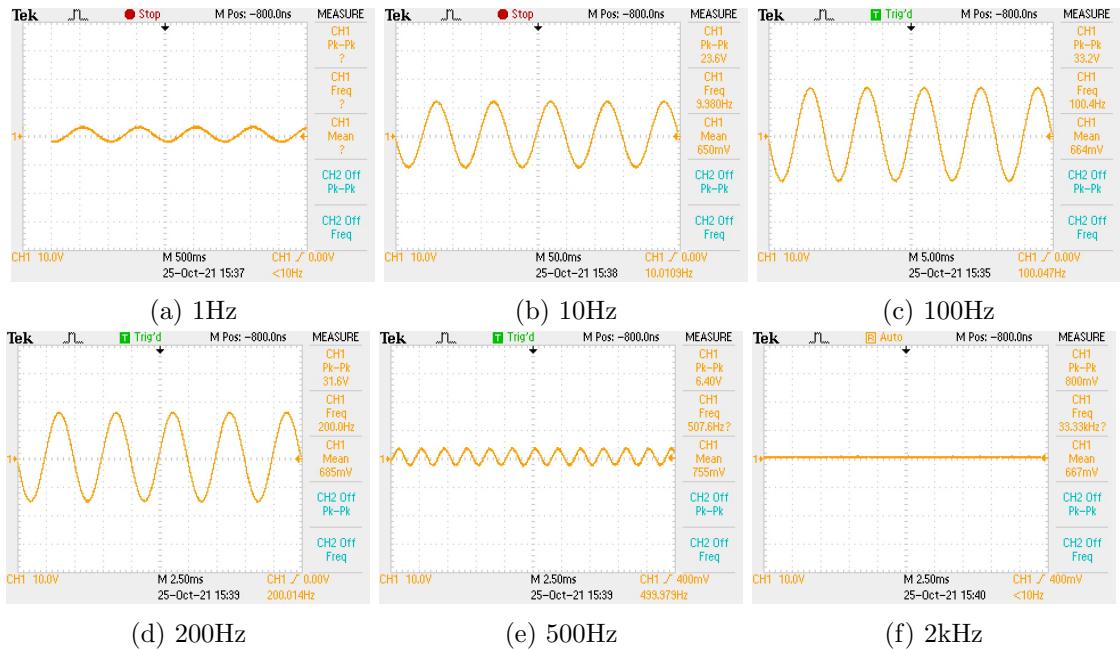


Figure 14: Amplifier output to varying frequency input signal

After observing the outputs waveforms, a bode plot was constructed through the use of the oscilloscope fast Fourier transform (FFT). The bode plot can be seen in Figure 15, and it is exactly as expected.

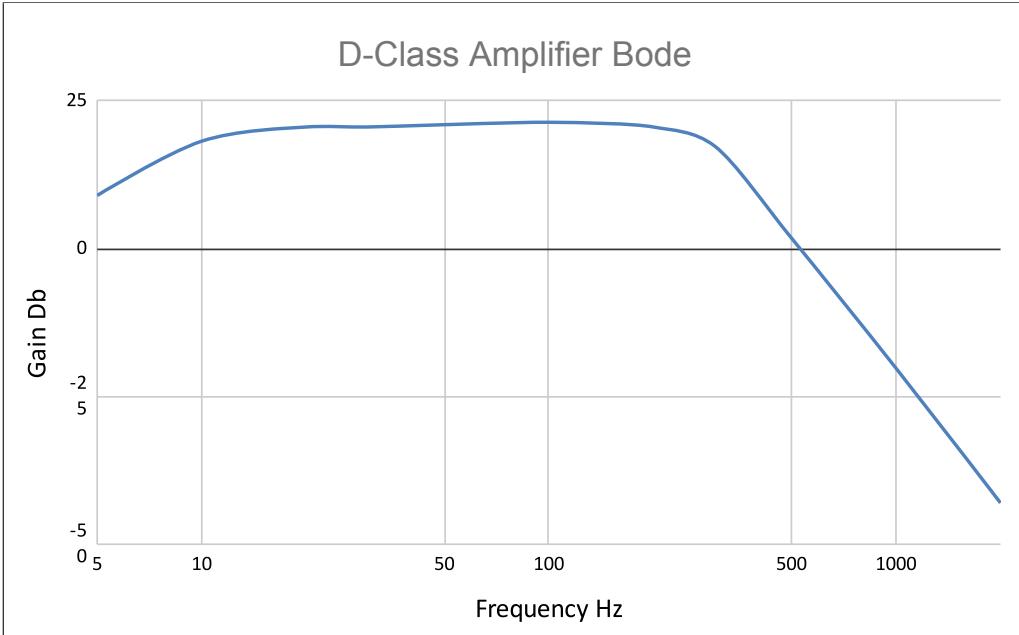


Figure 15: Amplifier output bode plot

Next, an efficiency plot of the amplifiers output was generated, plotting the output efficiency across the amplifiers frequency range, seen in Figure 16. From this figure we can clearly see the the amplifiers efficiency is between 86% and 92% across the amplifiers bandwidth, with the efficiency greatly decreasing as soon as the filters are attenuating the output signal.

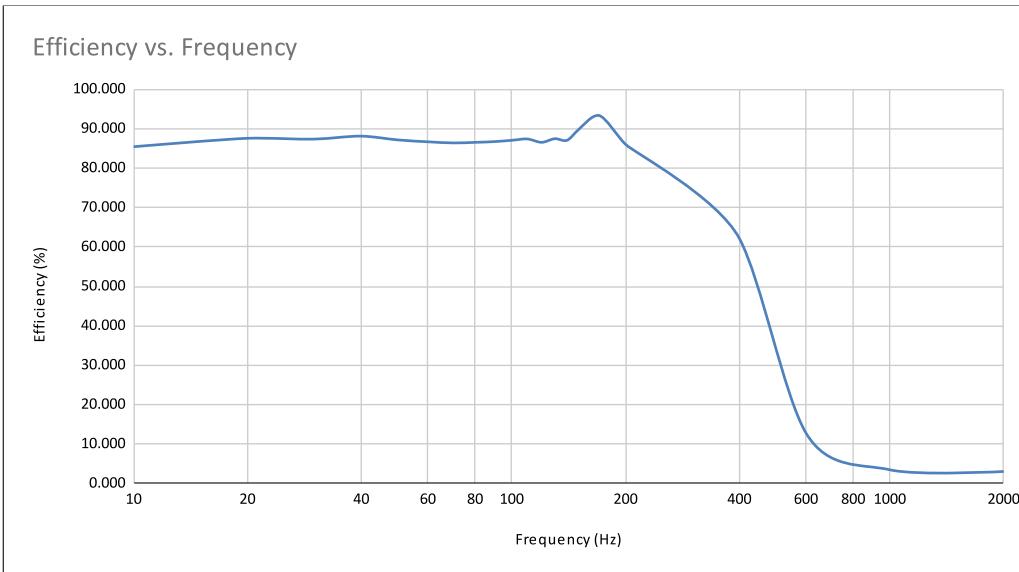


Figure 16: Amplifier output efficiency vs frequency

The final measurements taken of the amplifier were its total harmonic distortion across its frequency range. This can be seen in Table 1.

Frequency (Hz)	THD (%)
30	1.8
50	2.2
100	3.2
200	3.3
300	3.5
500	3.2

Table 1: Output total harmonic distortion across frequency

## 5 Conclusions

Overall, our design and implementation of a class D amplifier was highly successful. We were able to achieve all of the specified requirements outlined in Section 1.1, while also keeping the bill of materials (BOM) for each amplifier to under \$50. This has allowed us to each build our own amplifier that we have been able to take home. The output waveform is undistorted and correctly attenuates all unwanted frequencies, while providing a high efficiency high power audio output.

All designed sections functioned as intended, and all minor changes to the design have been updated within the project to reflect those additions.

In conclusion, I believe that Figure 17 successfully summarises the result of this project.



Figure 17: Me and the ECEN lab crew listening to my class D amplifier OBLITERATE some pop song

# Appendix

## Input Filter

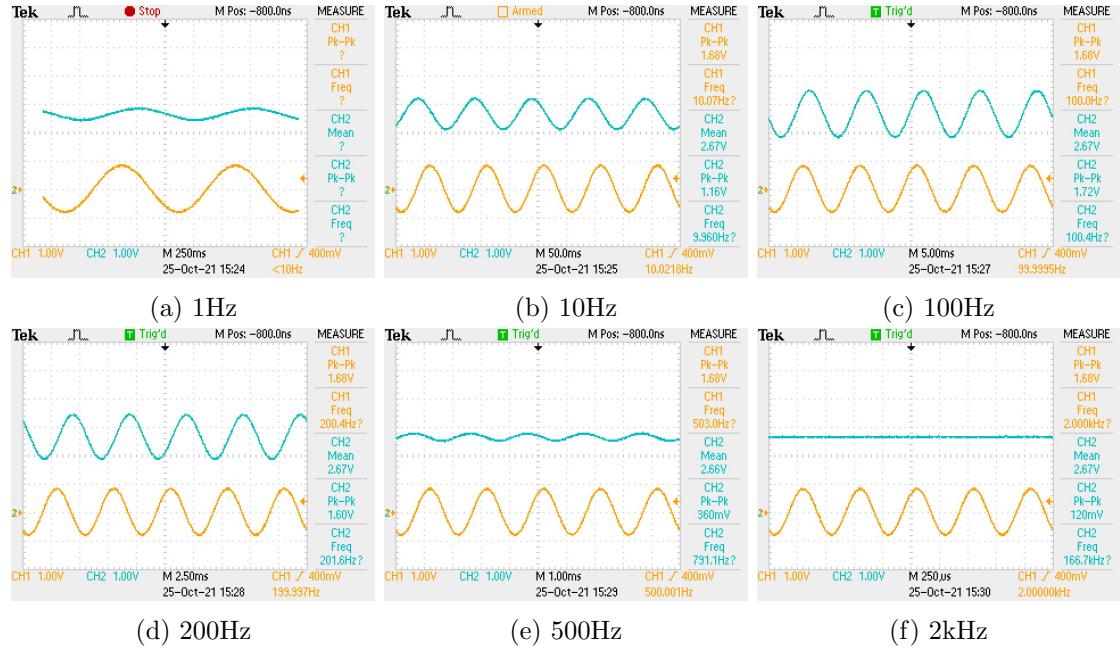


Figure 18: Input filter operation across frequencies, input signal (yellow) vs filter output (blue)