

ECEN405 Lab 6 Report

PI Controlled Buck Converter

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Deliverables

1. Buck Converter Bode Plot

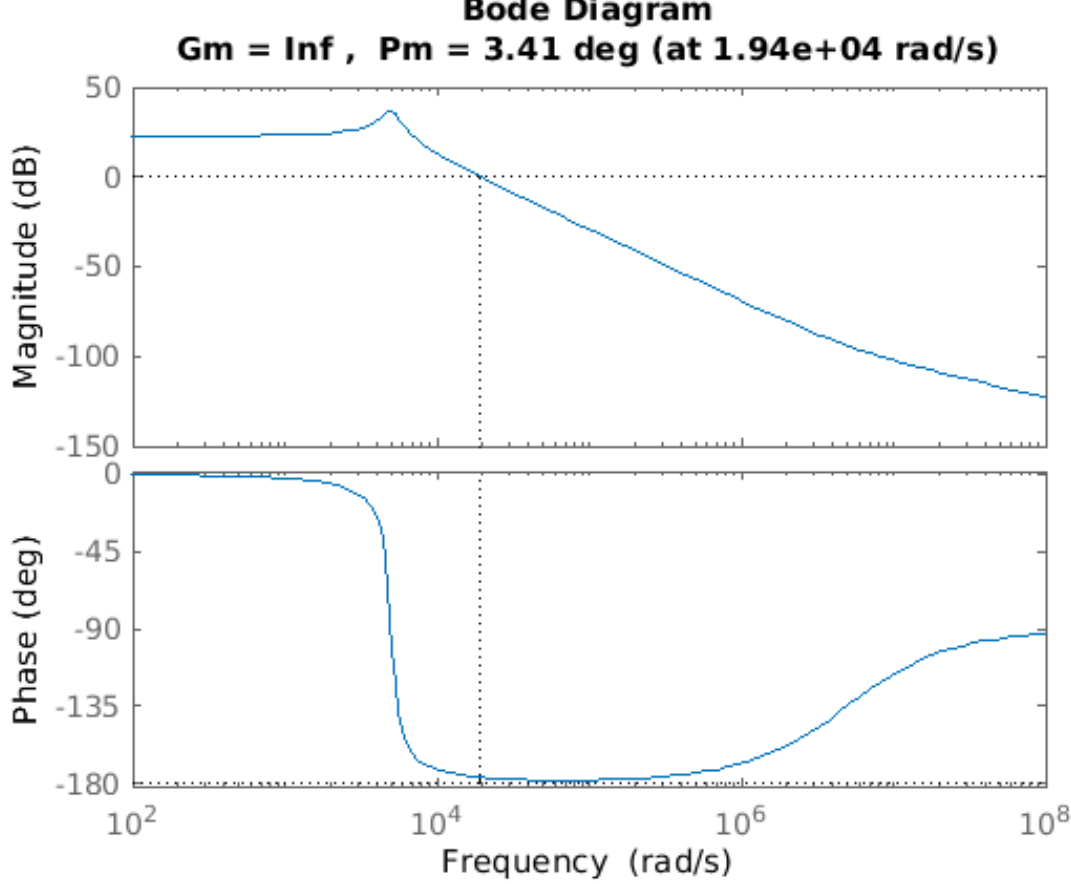


Figure 1: Buck converter Bode plot with gain and phase margin displayed

2. Controller Design

We are looking to design a PI controller, where the unity gain frequency (Phase Margin) of the original buck converter is unaffected. The following values were specified for the design:

- $R_i = 10k\Omega$
- $K_p = 0.1$

From this the value of R_f can be calculated using the following equation:

$$\begin{aligned} R_f &= K_p \cdot R_i \\ &= 0.1 \cdot 10k\Omega \\ &= 1k\Omega \end{aligned}$$

To ensure that the phase margin of the original buck is unaffected, we want the controller to have a phase of 0° at this location. From the transfer function of a PI controller it can be observed that it places a single zero on the S plain. This will cause a 90° phase shift from -90° over one decade, around the location of the integrating zero. By placing this integrating zero two decades below the phase margin of the original system we can guarantee that the phase of the controller will reach zero by this point.

Using this information, we can use the following equation to calculate the capacitor value required to place the zero two decades below the systems phase margin:

$$\begin{aligned} s &= -\frac{1}{R_f \cdot C} \\ \therefore C &= -\frac{1}{R_f \cdot s} \\ &= -\frac{1}{1000 \cdot 1.94 \cdot 10^4} \\ &= -5.17 \cdot 10^{-6} \\ &= 5.17\mu F \end{aligned}$$

The final component values are:

- $R_i = 10k\Omega$
- $R_f = 1k\Omega$
- $C = 5.17\mu F$

3. Controller Bode Plot

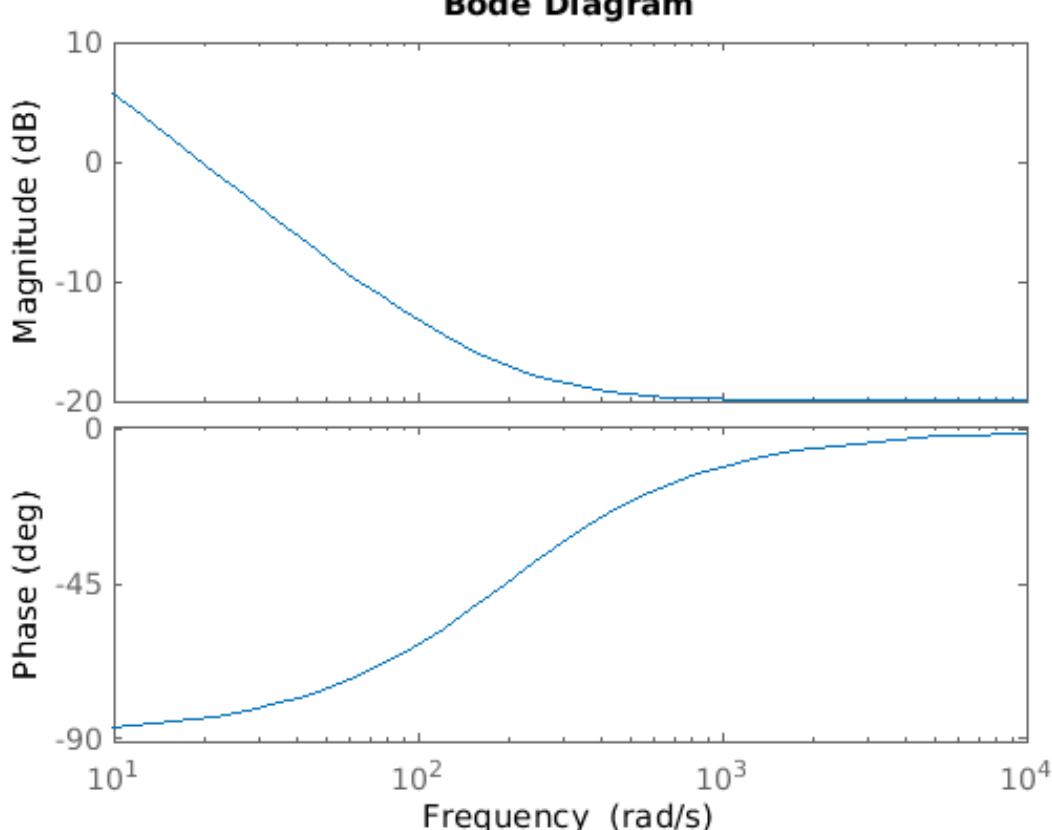


Figure 2: Controller Bode plot

4. Controlled Buck Converter Bode Plot

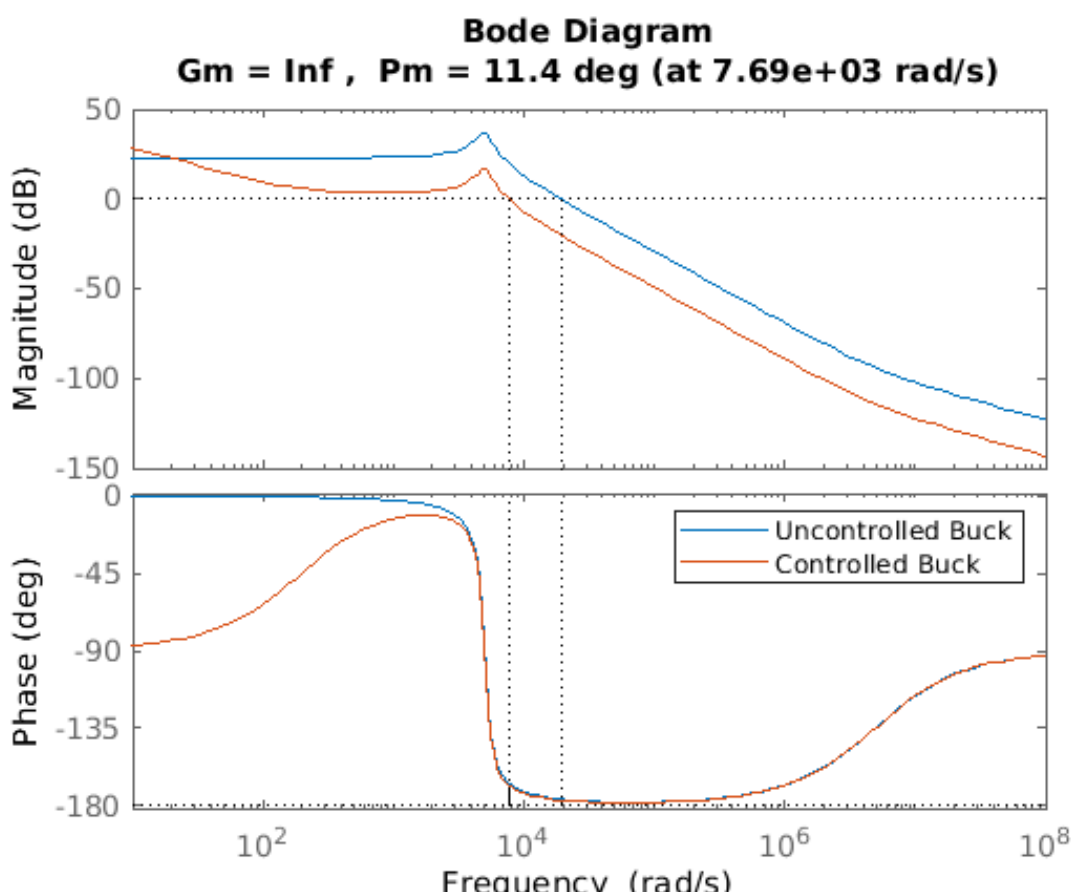


Figure 3: Controlled Buck converter Bode plot with the new gain and phase margin displayed

5. Controlled Buck Converter Simulation

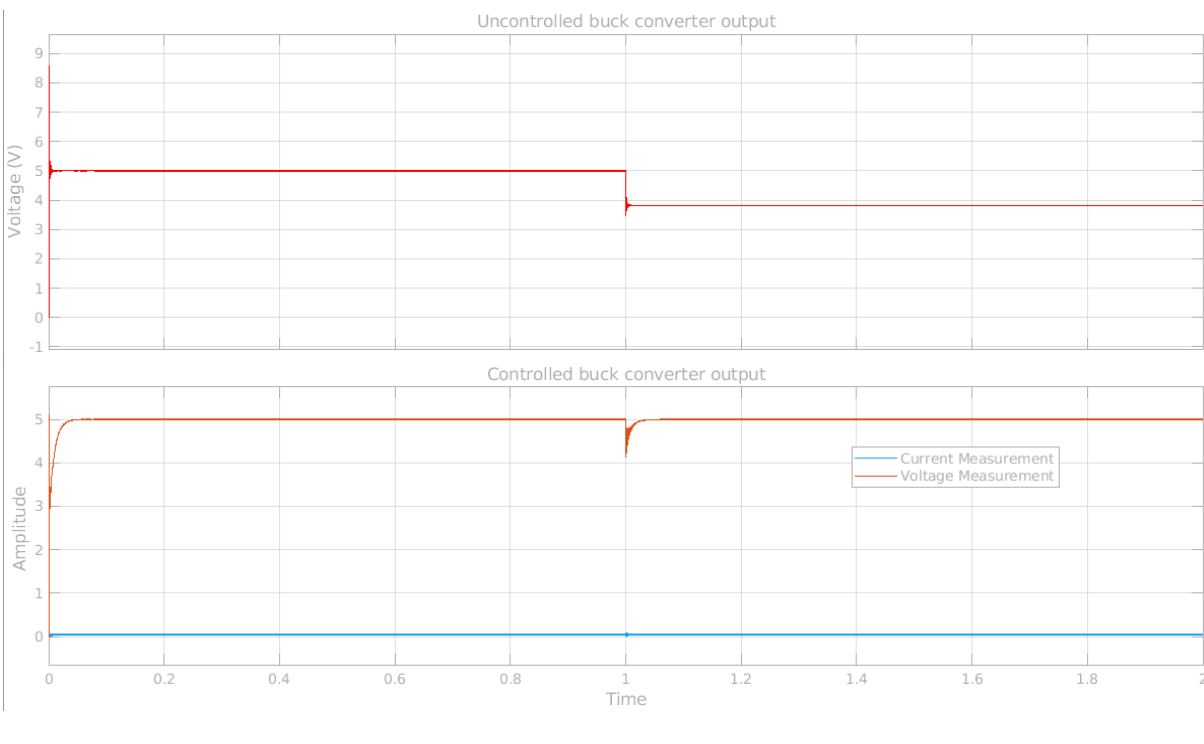


Figure 4: Controlled buck converter vs uncontrolled buck converter simulation

6. Controlled Buck Converter Implementation Schematic

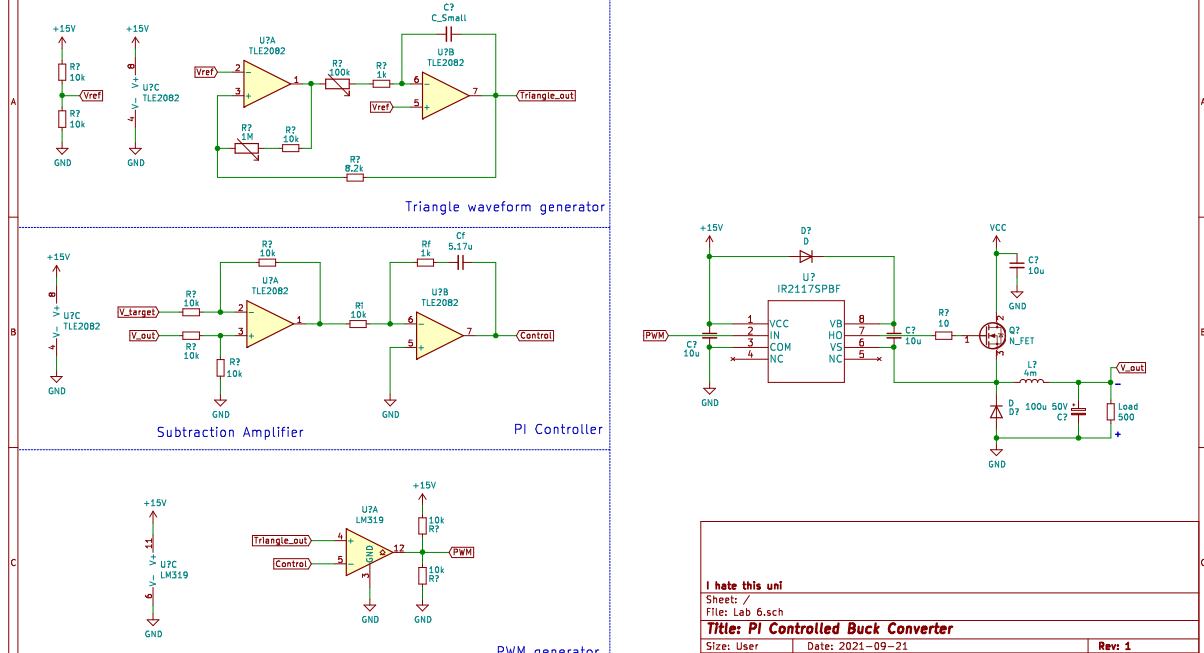


Figure 5: Controlled Buck Converter Implementation Schematic with relevant IC pinouts