

ECEN 204 Lab 4

Bipolar Junction Transistors

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1 Bipolar Junction Transistor (BJT) Measurements

Path Tested	Resistance	Diode Voltage
Base \rightarrow Collector	481k Ω	0.703V
Collector \rightarrow Base	∞	Na
Base \rightarrow Emitter	488k Ω	0.698V
Emitter \rightarrow Base	∞	Na

From these measurements, it can be deduced that a BJT has a similar internal construction to 2 diodes placed in opposite directions as shown in figure 1. Using this model, it would be expected to measure voltage drops of around 0.7V in the forward bias direction's of both diodes (Base \rightarrow Collector & Base \rightarrow Emitter), and for there to be a measurable resistance across the diode. However when placing the diodes in reverse bias (Collector \rightarrow Base & Emitter \rightarrow Base), the resistance should be near infinite. Both of these expected trends can be observed in the above table of measurements:

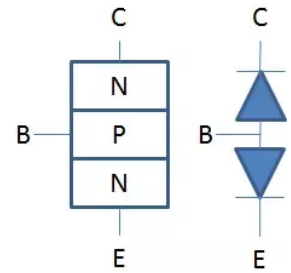


Figure 1: BJT Diode Model

2 Current Limiting Resistors

In our constructed circuit, there were 2 current limiting resistors, one placed between V_{BB} and the base, and the other between V_{CC} and the collector. The purpose of these resistors are to limit the maximum current than can flow from both the base to the emitter, and the collector to the emitter. This is done in order to stop the BJT from exceeding its maximum ratings.

Using 4.7k Ω resistor attached to the base, and a 1k Ω resistor attached to the collector, and assuming an ideal transistor, we can calculate the maximum I_B and I_C .

$$I_B = \frac{V_{BB}}{R} = \frac{5}{4.7k} = 1.06mA$$
$$I_C = \frac{V_{cc}}{R} = \frac{10}{1k} = 10mA$$

3 Current Gain

The current gain of the BJT is defined by the input collector current I_C vs the input base current I_B . This was measured both using a transistor tester, and by measuring the I_C and I_B with different current limiting resistors.

The outputs are as follows:

Using transistor tester: $\beta = 440$

Using lab measurements: $\beta = 391$

It can also be noted from figure 2 that as the base current limiting resistor increases in size, the gain of the transistor increases, meaning that for the highest gain value, a large resistor must be used.



Figure 2: Transistor gain vs Base limiting transistor

4 Base current vs Collector current

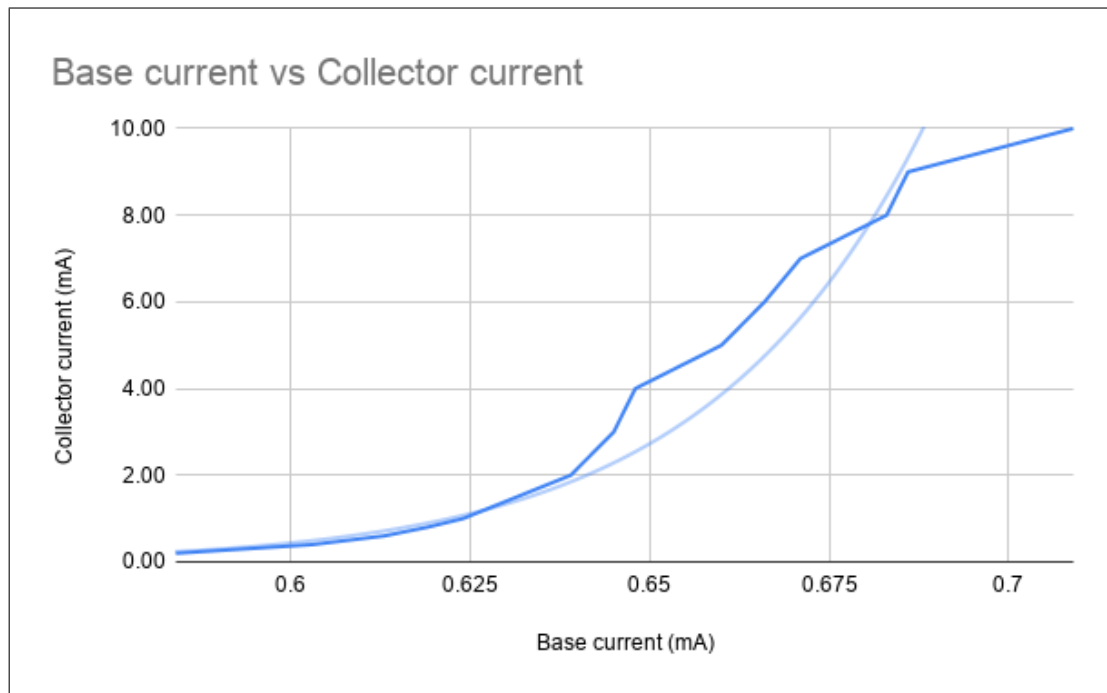


Figure 3: Base current vs Collector current

It can be observed in figure 3 that as the base current (I_B) increases, the collector current (I_C) will increase at an exponential rate. This means that with a relatively low base current, a large collector current can be allowed to flow. This is the basis of the amplification properties of transistors.

5 Collector Emitter Current vs Collector-Emitter Voltage

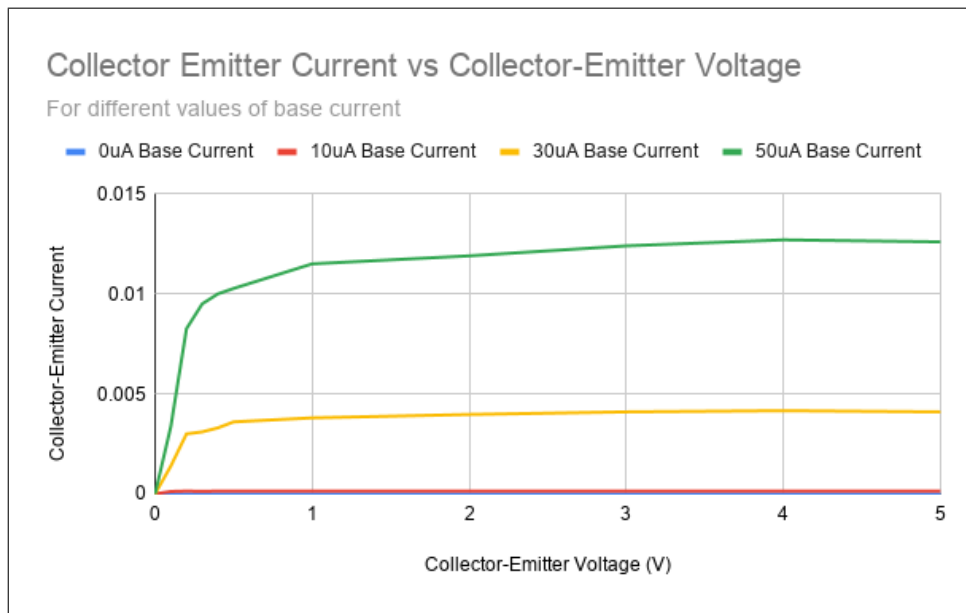


Figure 4: Collector Emitter Current vs Collector-Emitter Voltage

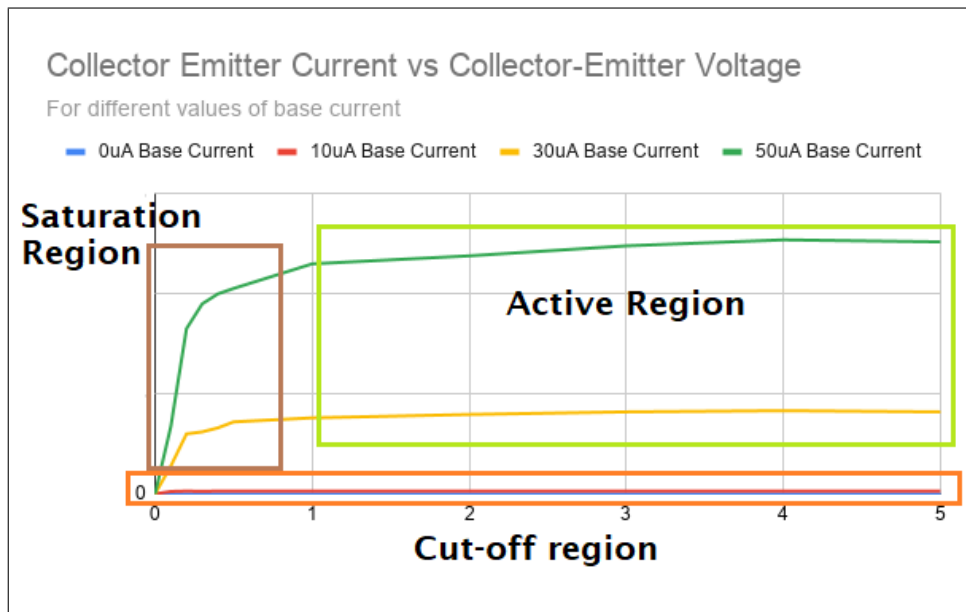


Figure 5: Transistor Regions

In figure 4, the collector current I_C vs collector-emitter voltage V_{CE} at different base currents I_B can be seen, and in figure 5, the 3 defined regions of a transistor curve can be seen.

In the cut-off region I_B will be 0A, therefore I_C will also be 0A and the transistor will be off.

In the saturation region $V_{BE} = 0.7V$ meaning that the base-emitter junction will be forward biased, however V_{CE} will be very small, leading to a very small collector-emitter current that is not yet saturated.

In the active region collector-emitter current is saturated, and the greatest transistor gain can be observed. Because of this, currents within the active region are chosen to calculate the gain of the transistor.

Base current = 10uA: $\beta = 14$

Base current = 30uA: $\beta = 136.7$

Base current = 50uA: $\beta = 252$

6 Using a transistor as a logical NOT

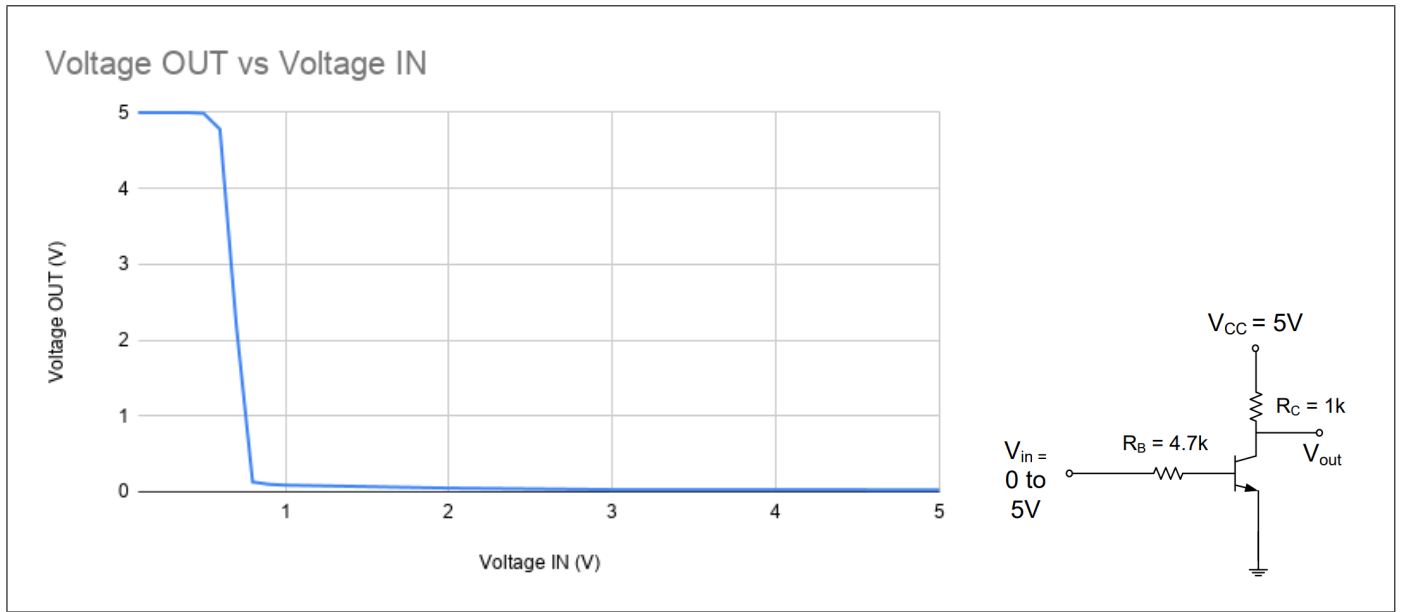


Figure 6: Transistor used as a logical NOT

When the voltage into the base of the transistor is below 0.7V, the two hypothetical diodes within the transistor are reverse biased, because of this the voltage difference between V_{OUT} and GND will be 5V. However once the threshold voltage of the diodes is reached (0.7V), the transistor will be considered to be on and have negligible resistance, meaning that 0V will be dropped across V_{OUT} and GND. This behaviour can be seen in figure 6.

A practical use of this circuit is as a rudimentary logical NOT gate. When the input is larger than 0.7V the output will be 0V, and when the input is 0V, the output will be 5V.