Self Tuning Buck Converter Design

---

1 PWM Generation

Based on our evaluation criteria, the generated PWM signal will need to be capable of outputting frequencies between 1kHz and 100kHz.

This PWM signal will also need to facilitate the required output voltage accuracy of ±5% of the target output voltage, for target voltages between 3V and 10V. The relationship between the input and output voltage of a buck converter is given by $V_{out} = D \times V_{in}$. It should be noted that the output voltage is a function of the PWM duty cycle, therefore we must design the duty cycle such that it can provide the required output voltage accuracy. The workings of this design can be seen in the following.

Assuming $V_{min} = 3V$

$$V_{error} = 5\% \text{ of } V_{min} = 0.15V$$
$$D_{steps} \geq \frac{V_{in}}{V_{error}} \geq 80$$

By designing the PWM duty cycle based on the buck converter minimum output voltage, we design the system to achieve the smallest tolerable error. This design guarantees that the required output voltage accuracy will always be achievable by our system if our PWM duty cycle has more than 80 steps.

1.1 Analogue

1.2 Microcontroller

1.3 FPGA

2 Current Ripple Sensing