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Self Tuning Buck Converter

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Submitted in partial fulfilment of the requirements for
Bachelor of Engineering with Honours.

Abstract

Switch-mode power supplies are commonly used in a wide variety of consumer and professional appliances to transform DC voltages with high efficiency. One such switch-mode supply is the buck converter, which steps down a DC voltage. The current buck converter design process requires that a specific output filter be designed around the switching frequency of the converter, the required output voltage, and the desired inductor ripple. This filter design process often results in the selection of non-standard components that are difficult to purchase or manufacture, increasing costs and leading to design compromises. This project will develop a platform that allows for observation and control of the inductor current ripple by modulating the switching frequency of the converter. This will allow engineers to design buck converters directly for the specified inductor current ripple their application can tolerate, eliminating the issues of designing this output filter.

Contents

Chapter 1: Introduction

Historically power distribution has been primarily in the form of AC (Alternating current). This is credited to the fact that AC power is simple to produce, and made it easy to step up and down the voltages efficiently with transformers [1]. However, with the invention of solid-state electronics such as the metal–oxide–semiconductor field-effect transistor or MOSFET for short, it has become possible to efficiently step up and step down direct current (DC) voltages. This has been achieved by the invention of the switch-mode power supply, which has facilitated the continued reduction of size and increase in efficiency of electronics [2].
Today, switch-mode power supplies can be found in a wide variety of consumer and professional electronics, with some examples being laptops, phones, and any form of DC charger. Their widespread usage when compared to other DC-DC converters such as linear regulators can be attributed to their far greater efficiency. One such switch-mode power supply is the buck converter, which will step down a DC input voltage to a lower DC output voltage.

1.1 Project Motivation

Although buck converters are a widespread technology, they are not without their limitations and drawbacks. The current buck converter design process requires that a specific output filter be designed around the switching frequency of the converter, and the desired inductor ripple current. This filter design process will often result in the converter requiring discrete passive components that are non-standard and hard to source. This will usually result in the designer having to make compromises in their design for either the cost or the performance of the converter.
Another drawback of this design process is the static nature of both the filter and the switching components once they have been selected. This results in the buck converters desired inductor current ripple only being achieved at a very specific designed output voltage or load. This means that with current buck converter designs varying the desired output voltage or varying the output load will cause the inductor current ripple to vary. This is an issue, as very few loads are static and will not change during their operation.

1.2 Project Goals

The goal of this project is to develop a testing platform through which the effects of variable buck converter switching frequency on inductor current ripple can be observed and controlled. The aim of this is to eliminate the need to design the output stage of the buck converter by implementing a control system to maintain a specified inductor current ripple, and output voltage.

To achieve this goal, a proof of concept buck converter will be designed to operate as the testing platform. This converter will require a variable frequency pulse width modulated

(PWM) signal generator, and inductor current ripple sensing. This will allow for direct manipulation and control of inductor current ripple. The converter will also need to implement the full functionality of existing buck converter designs, including controlled output voltage regulation.
It is also important to note that as this project aims to produce a testing platform to be used as a proof of concept, there will be continued work undertaken after the projects conclusion. Because of this, it is important that the design and implementation undertaken in this project considers the ease of use and future expansion of the project.

The following list of specifications outlines the requirements the designed test platform will meet:

1. Operate with a 12V DC input supply voltage
2. Provide a selectable DC output voltage between 3V and 10V
3. Provide an output voltage precision of at least $\pm 5\%$ of the targeted output voltage
4. Provide a selectable inductor current ripple between 20% and 50% of the total output current
5. Provide a variable converter switching frequency between $1k$Hz and $100k$Hz
6. Provide an inductor current ripple precision of at least $\pm 5\%$ of the target inductor current ripple
7. Operate with variable load sizes between 10Ω and $20\ \Omega$

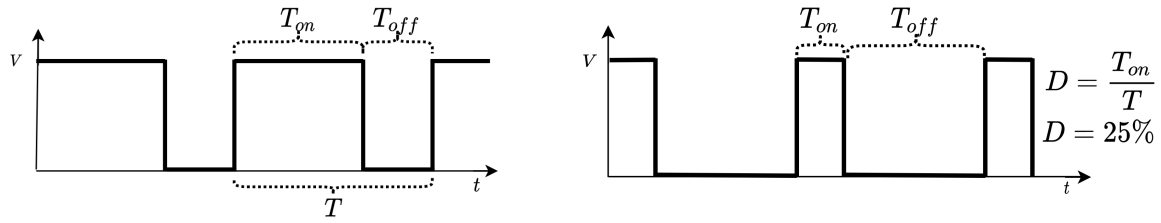
Chapter 2: Background

A literature research was performed to inform design decision made in this project, and to evaluate any existing research. This chapter will discuss buck converter design factors and topologies, as well as the various different methods of PWM generation, current sensing, and control implementation. In performing this literature research, we searched Google Scholar, Engineering Village, and Te Waharoa to find designs that utilised variable frequency PWM.
These searches returned no research relevant to the designs of this project, with the only related work focusing on the electromagnetic noise reduction using randomised frequency modulation [3, 4]. Because of this, research was instead performed to inform the design of the buck converter and the generation of PWM signals.

2.1 Pulse Width Modulated Signal Generation

Pulse width modulation (PWM) is a digital signal generation technique shown in Figure 2.1a, in which the Period T of the signal is held constant, while the ratio of its logic high period T_{on} to logic low period T_{off} is modulated. This ratio of high period to the low period is referred to as the duty cycle of the PWM signal and is often expressed as a percentage, this can be seen in Figure 2.1b.

PWM signals are used in a wide variety of applications for both digital and analogue electronics. PWM is often used to generate analogue signals from digital components by varying the average voltage of the digital PWM signal over time [5]. PWM is also used to control the switching elements contained within switch mode power supplies using this same principle, as discussed in Section 2.2. With regard to this project, we will be looking to generate a PWM signal that can be modulated in both duty cycle and frequency.



(a) Pulse width modulated signal

(b) Duty cycle calculation

Figure 2.1: Pulse width modulated signal characteristics

2.1.1 Analogue PWM Signal Generation

Designing a PWM signal generator using analogue components has three distinct stages required to generate the signal. These stages can be seen in Figure 2.2, and include clock

generation, triangle wave generation, and signal comparator stages [6].

The clock generation stage generates a square wave clock signal at a set frequency. This is usually done using a quartz crystal oscillator, or another form of resonating oscillator circuit. The triangle wave generating state must take the clock signal from the previous stage, and produce a triangle wave of the same frequency. This stage is most often done using a standard op-amp integrating circuit with unity gain at the resonating frequency of the clock source. The final signal comparator stage will convert this triangle wave into a PWM signal. Using a comparator, a reference voltage can be applied to the non-inverting input, and then the triangle wave can be applied to the inverting input. This will produce a pulse train with the same frequency as the clock source, where the period of T_{on} and T_{off} is set by the reference voltage.

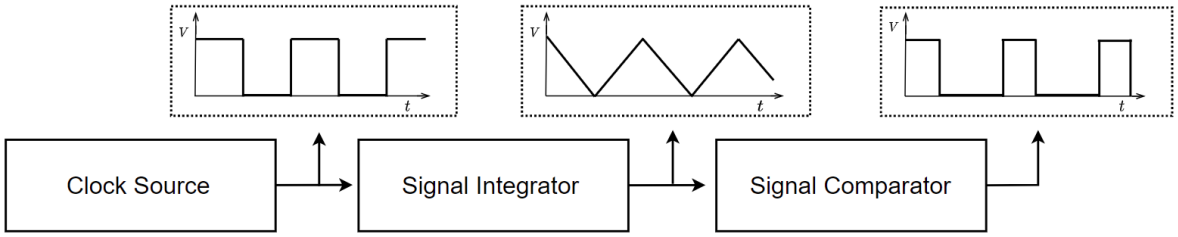


Figure 2.2: Stages of analogue PWM generation

2.1.2 Digital PWM Signal Generation

Designing a PWM signal generator with digital components is less complex than the method described in Section 2.1.1, and can be done using either a microcontroller or a Field Programmable Gate Array (FPGA). By using an internal timing register that is continually incrementing at a known period we can set a period for our PWM. It is possible to vary the period of the PWM by simply increasing or decreasing the timing registers clock. Next, by toggling a digital I/O when a compare variable is equal to the current value of the timer, we are able to generate a PWM signal with a variable duty cycle [7]. This timing architecture can be simply implemented within an FPGA, but it can also commonly be found within the hardware of most microcontrollers.It should be noted however, that the range of achievable frequencies and duty cycle accuracy will be dependant on an individual microcontrollers clock speed and internal register sizes.

2.2 Buck Converters

The buck converters is a variant of a switch mode power supply that steps down a DC input voltage to a DC output voltage. They are commonly used in a wide variety of consumer and professional appliances such as laptops, phones, and chargers due to their high efficiency compared to other DC-to-DC step down converters such as linear regulators [8].

The basic operational components of a buck converter can be seen below in Figure 2.3. From this we see that a buck converter has three main elements, the input voltage source, two switching components, and an output filter across the load. In the case of Figure 2.3, the first switching component is an actively controlled switch such as a MOSFET or transistor, and the second a passive switching diode. This configuration of an active and a passive switch is known as the non-synchronous buck converter topology, if the passive diode

were to be replaced with a second active switch the topology would be considered synchronous. Although both topologies function under the same fundamental principles, the non-synchronous topology is easier to implement with the drawback of higher losses and therefore lower efficiency.

It can also be seen from Figure 2.3 that a buck converter has two operating states that are controlled through the activation of these switching components. By toggling these switching components at high speed though the use of PWM, we can control the current flowing through the inductor of the output filter. By controlling this current we are also able to directly control the current through, and voltage across the output load of the converter. Using this, buck converters will often have a feedback control system in their design to be able to actively control and regulate the output voltage during usage. This controller will vary the duty cycle of the the switching PWM signal, thereby varying the output voltage of the buck converter as shown in Equation (2.1).

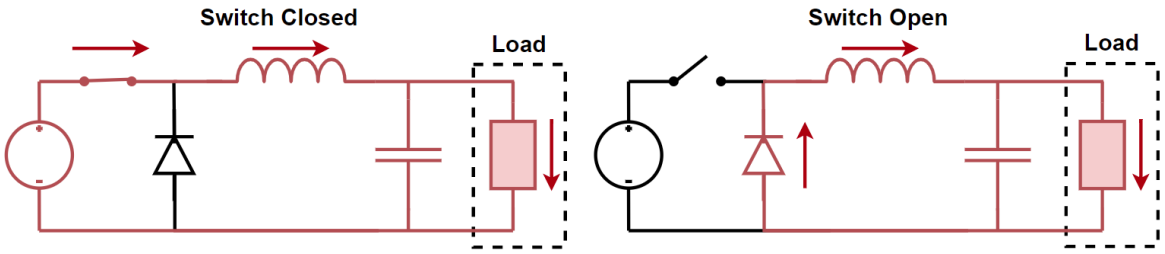


Figure 2.3: Operating states of a buck converter

2.2.1 Buck Converter Design

The design of a common buck converter has two primary considerations, the output voltage of the converter V_0, and the inductor current ripple of the converter Δi_L. These considerations can be specified by designing the buck converter using Equation (2.1) & Equation (2.2) [9, 10].

When designing a buck converter the first design specification that must be met is the output voltage. In Equation (2.1) the output voltage can be directly related to the input voltage V_{in} and the switching duty cycle D. Using this equation it is possible to directly set the output voltage of the buck converter by varying this duty cycle.

$$V_o = D \cdot V_{in} \tag{2.1}$$

Once the output voltage has been specified, the inductor current ripple can be calculated and specified with Equation (2.2). This equation allows for the inductor current ripple to be directly related to the inductor size L, and the PWM switching frequency f_s. This allows the the specification of the inductor current ripple through the varying of these two values.

$$\Delta i_L = \frac{V_o \cdot (1 - D)}{L \cdot f_s} \tag{2.2}$$

These two equations will be used to inform the designs and specifications of this project, and will be discussed in detail in Section 3.1.

2.3 Current Sensing

Current sensors are transducers that converter an input current to an easily measured output voltage that is proportional to the current through the sensor. Current sensors operate on one of two principles, Ohm's law, Faraday's and Ampere's law [11]. Ohm's law describes how when current flows through a resistive element a voltage drop will occur. Sensors operating under this principle will measure the voltage drop across a known resistance, and are referred too as direct sensors as they directly effect the circuit. Faraday's and Ampere's law describes how a changing electric flux will induce a changing magnetic field, and a changing magnetic field will induce a changing magnetic flux. Sensors operating under this principle will use the magnetic field induced by the current through the sensor to produce a voltage proportional to that current, and are referred to as indirect sensors as they make no direct contact with the circuit being sensed.

2.3.1 Current Sense Amplification

Current sense voltage amplification sensors are a form of direct sensor, working on the principle of Ohm's law $I = \frac{V}{R}$. By sensing the voltage dropped across a known value resistive element (Often called the current shunt), it is possible to calculate the current that is flowing through the element. This form of current sensing is very simple to implement in theory, however it has the effect of altering the system being sensed by adding a resistive load, and thereby increasing the losses of the system.
To mitigate the effects of this sensing on a circuit, a smaller resistive load can be used. However, this will also decrease the measurable voltage across the load, and therefore decrease the precision of a taken measurement. Because of this, shunt based current sensors are often paired with an operational amplifier of known gain. This combination allows for accurate amplification of the shunts voltage drop, increasing the precision of measurements, and allowing for drastically smaller shunt resistors.

2.3.2 Hall Effect Sensors

Hall effect sensors are a form of indirect sensor, working on the principles of Faraday's and Ampere's law as discussed above. They function by measuring the magnetic flux density, meaning that they are commonly used to sense the presence of a magnets or magnetic fields. However since a current flowing though a wire will produce a magnetic flux, they can also be used to measure current flow.
Due to this operation, they are able to sense a current without contacting or altering the circuit. This means that they are commonly used in the measurement of high voltage or high current circuits, as they will remain completely isolated from the circuit being sensed. This provides large safety advantages, eliminates sensing power losses, and can often decrease the complexity of the sensing circuit.
Hall affect sensors do however suffer from a lack of precision. Due to their operation, their measurements will constantly be offset by any ambient magnetic flux within the surrounding environment. This means that they are not commonly used for the sensing of small signal currents, as the noise floor of the Earth's own magnetic field can often be larger than the signal being sensed [12].

2.4 Control Systems

Control systems are integral to the operation of any system for which you wish to achieve a desired outcome. In their simplest, a control systems has the purpose of obtaining a desired output from a system, with a desired performance, when a given input is provided.

There are two main topologies of control system, open loop and closed loop. An open loop control system requires no feedback of the output, and therefore no sensing. Because of this, open loop controllers are often very easy and fast to implement within a system because of this, however they have no knowledge of the systems state and are therefore unable to correct for errors such as external disturbances.
On the other hand, closed loop controllers require feedback from the current output of a system, and therefore will require sensing to be implemented. This added sensing requirement will add complexity to the system, however a closed loop controller provides the ability to compensate for errors in the systems output.

The performance of a specific control system is often discussed in terms of it's steady state settling time, and it's stead state error. The steady state settling time of a controller describes the time it takes for a controller to reach it's final value ('steady state') when provided with a given input. The slower the steady settling time of a controller, the slower it will react to a given input, and vice versa. The steady state error of a controller describes the error between the desired output and the final output of the system once it's steady state has been achieved.

Chapter 3: Design

The design processes outlined within this report will draw heavily on the background research discussed in Chapter 2. These designs aim to effectively implement the outlined system requirements discussed by Section 1.2 in a robust and repeatable manner.

3.1 System Specifications and Architecture

Section 1.2 outlines a list of specifications that this project must achieve. For each item in this list, design specifications can be derived to ensure that our designs are capable of meeting the outlined requirements. This list of specifications will also help to shape the architectural approach taken on this project.

Requirement 1: Operate with a 12V DC input supply voltage

To meet this requirement, the buck converter must be designed to be 12V DC compatible. this will require all designed hardware, including additional digital and analog circuity to be capable of operating with this supply.

Requirement 2: Provide a selectable DC output voltage between 3V and 10V

To meet this requirement, the designed buck converter must have the ability to change the duty cycle of it's PWM switching signal. This will allow for variation of the output voltage based on Equation (2.1).

Requirement 3: Provide an output voltage precision of at least $\pm 5\%$ of the targeted output voltage

To meet this requirement, the designed buck converter must have a control system to regulate the output voltage. To achieve a steady state error of less than $\pm 5\%$, feedback should be implemented, requiring output voltage sensing. We can also specify that a minimum duty cycle resolution of 1.25% will be required to achieve this. For the derivation of these values, please see **??**.

Requirement 4: Provide a selectable inductor current ripple between 20% and 50% of the total output current

To meet this requirement, the designed buck converter must have the ability to change the frequency of it's PWM switching signal. This will allow for variation of the inductor peak to peak current ripple based on equation Equation (2.2).

Requirement 5: Provide a variable converter switching frequency between 1kHz and 100kHz

To meet this requirement, the PWM switching frequency must be selectable across the specified range. This, in tandem with requirement 4, allow for the specification of the inductor range for which these requirements can be met. For the derivation of these values, please see **??**.

Requirement 6: Provide an inductor current ripple precision of at least $\pm$5% of the target inductor current ripple

To meet this requirement, the designed buck converter must have a control system to regulate the inductor current ripple. To achieve a steady state error of $\pm$5%, feedback should be implemented, requiring inductor current ripple sensing. We can also specify that a minimum frequency selection resolution of 200Hz, as well as a minimum current ripple measurement resolution of a resolution of 15mA will be required to achieve this. For the derivation of these values, please see **??**.

Requirement 7: Operate with variable load sizes between 10Ω and 20Ω

To meet this requirement, all components of the buck converter must be designed to handle the maximum output current of 1A that will occur with a 10Ω load at 10V. It will also be important that any current sensing is designed to operate within the range defined by these loads. Finally it is required that control systems are implemented to maintain requirements 3, & 6 as the load varies.

3.1.1 System Architecture

Based on the specifications outlined in the above section, an architecture that outlines the system design has been developed. This architecture has been divided into three subsystems that must each be developed. This architecture system can be seen in Figure 3.1.

Subsystem one implements a PWM generator. From requirements 2, & 5 it has been identified that a PWM generator capable of varying both the duty cycle and the frequency of it's output signal independently must be designed. This system can be seen in Figure 3.1 outlined in green.

Subsystem two implements system state sensing. From requirement 3 & 6 it has been identified that an output voltage sensor, and an inductor current ripple sensor must be designed. This system can be seen in Figure 3.1 outlined in blue.

Subsystem three implements two control systems. From requirements 3, 4, 6, & 7 it has been identified that control systems should be designed to ensure that the specified steady state errors of the output voltage and inductor current ripple are met.
One control system will take the output load voltage measurement, and control the PWM duty cycle. The other control system will take the inductor current ripple, and control the PWM frequency. This system can be seen in Figure 3.1 outlined in red.

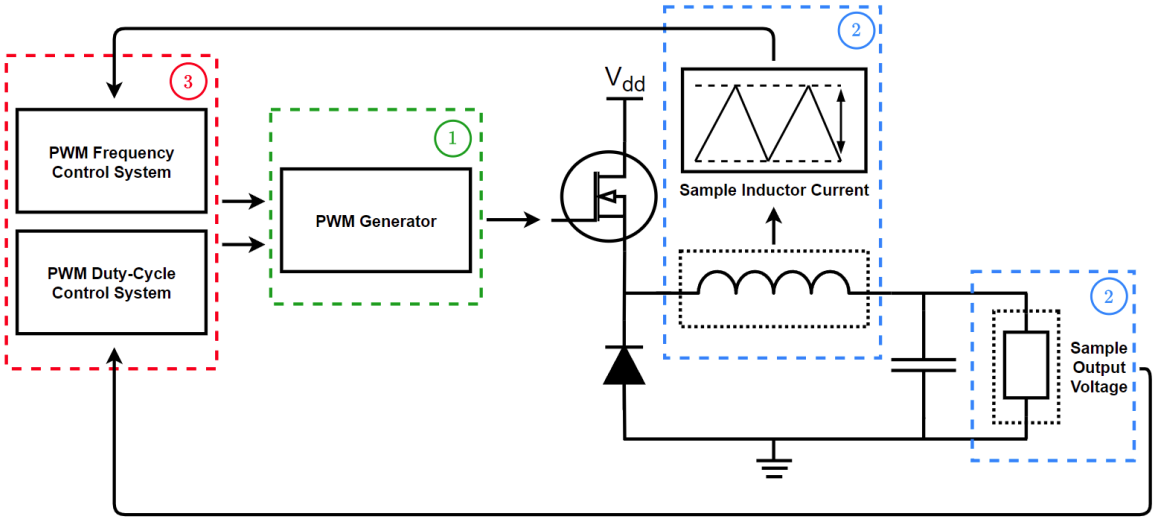


Figure 3.1: System architecture design, with three internal subsystems

3.2 PWM Signal Generator

In the design of the PWM generator, both the analogue and digital topologies discussed in Section 2.1 were considered, and designed for. Each of these designs presented pros and cons that would affect the overall design. This section will discuss these design choices, and finalise the design of the PWM signal generator.
A successful design will meet all of the requirements outlined by Section 3.1. Therefore the design must be capable of duty cycle variation with a resolution of 1.25%, as specified by requirements 2 & 3, as well as switching frequency variation between 1kHz & 100kHz with a resolution of 200Hz, as specified by requirements 4, 5, & 6. A successful design will also adhere to the ease of use and future expansion goal specified in Section 1.2.

3.2.1 Analogue PWM Generator Design

It has been discussed in Section 2.1.1 that the design of an analogue PWM signal generator requires three distinct stages. These stages are signal clock generation, signal integration, and signal comparison, as shown in Figure 2.2.
Designs for these sections were implemented within the circuit simulation software LTSpice, see **??**. From these simulations it was identified that the signal integration stage of the design functions as a first order low pass filter, where integration occurs beyond the filter's cut-off frequency. This causes a 40dB attenuation of the output signal across the required frequency range. Due to this, the design was identified to be unsuitable for this system as it was unable to meet requirements 4, 5, & 6.

3.2.2 Digital PWM Generator Design

As discussed in Section 2.1.2, The design of a digital PWM signal generator is based on the toggling an output when a timer reaches a given comparison value. This design can be achieved with either discrete logic designed within an FPGA, or using existing hardware within a microcontroller.

FPGA PWM Generator

The operation of an FPGA allows for the design and implementation of customised logic. Because of this, designs utilising FPGA's would easily be able to meet the specified requirements for the PWM signal generator.
However the designs integration into the system architecture described in Figure 3.1 must also be considered. A PWM generator implemented in an FPGA will be required to either implement or provide an interface with the control subsystem, as well as the state sensing subsystem. These interfaces must also be designed, greatly increasing the complexity of this specific subsystem. Due to this added complexity, it was identified that this design was not suitable for an initial proof of concept, and would not adhere to the ease of use goal.

Microcontroller PWM Generator

The selection of the microcontroller is highly dependant on the clock frequency and internal PWM peripheral architecture. Since these vary greatly between different processors, a selection of microcontroller data-sheets were reviewed to identify their specifications.
The microcontrollers reviewed were selected based on the ease of use of their available development environments. This included AVR, STM8, Espressif, and teensy based microcontroller development boards.
From this review it was identified that the ESP32 microcontroller [13] would be best suited to this project. This microcontroller is capable of outputting a maximum PWM frequency of $125kHz$ when a duty cycle resolution of 9 bits is selected. This will provide a total of 512 selectable duty cycle values, for a resolution of 0.2%, while providing a selectable duty cycle frequency between 1Hz, & 125kHz.
Based on these specifications, it is clear that this design meets the duty cycle requirements of 2 & 3, as well as the frequency requirements of 4, 5, & 6, and is therefore suitable.

3.3 System State Sensing

The design of the state sensing system will include the output voltage sensor and the inductor current ripple sensor. These sensors will be responsible for providing the feedback data for the control systems, illustrated in Figure 3.1. To provide a peak to peak inductor current measurement as a percentage of the output current, both the average and peak inductor currents must be measured. Based on these measurements, the inductor current ripple percentage can be calculated.
A successful design will meet all the requirements outlined by Section 3.1. Therefore the output voltage sensor must be capable of measuring voltages between 3V & 10V with a resolution of 150mV, as specified by requirements 2 & 3. It is also required that the average inductor current, and the peak inductor current ripple measurements achieve a resolution of 15mA, for frequencies between 1kHz & 100kHz, as specified by requirement 4, 5, 6, & 7.

3.3.1 Output Voltage Sensing

The output voltage of the buck converter will be a DC voltage between 3V & 10V. As there are no high frequency components to this signal, there are no bandwidth requirements on it's sampling. Due to this the internal analog to digital converter (ADC) of the ESP32 microcontroller will be used for sampling. This 12 bit ADC can measure an input voltage range of 0V to 3V [13], therefore the output voltage will have to be measured through a voltage divider. This divider will provide an output ratio of $\frac{10}{3.33}$, allowing for maximal use of the ADC's input range. This will provide a theoretical measurement resolution of 2.5mV.

Based on these specifications, this design is capable of measuring output voltages between 3V and 10V, with a resolution of 2.5mV, meeting the outlines requirements 2 & 3.

3.3.2 Current Sensor Selection

To maintain design simplicity, both the average inductor current, and the peak inductor current ripple will be measured from the same sensor. Due to this, a hall effect based current sensor is not suitable for this application. It was discussed in Section 2.3.2 that they lack precision due to a high noise floor, and would be unable to meet requirements 4 & 6.
Because of this, a current shunt based sensor with a defined gain and selectable shunt resistance has been designed, specifically the LT1999-50 with a 60mΩ shunt. This current sense amplifier has a specified gain of 50V/V, a typical gain error of 0.2%, and a bandwidth of 2MHz [14]. This sensing solution will provide a voltage output between 0.67V & 3.72V across the total current sensing range, with a resolution defined by the gain error of 50μA at the output. Please see **??** for the calculation of these values. The datasheet also specifies that there will be no attenuation of the output gain for frequencies of 100kHz or below.
Based on these specifications, this design is capable of measuring the full current input range specified in requirements 4 & 7, while surpassing the resolution and frequency specifications of requirements 5, & 6.

3.3.3 Average Inductor Current Sensing

To obtain the average inductor current ripple, the output of the previously designed current sense amplifier can be low pass filtered. By designing a first order passive low pass filter with a cut-off frequency of 10Hz, we can be sure to attenuate any selectable switching frequency by at least 40dB. This will provide a simple to measure DC voltage between 0.45V and 3V. This can be measured using the internal ADC of the ESP32 providing a theoretical resolution of 5mV, or 117μA. Please see **??** for the calculation of these values.

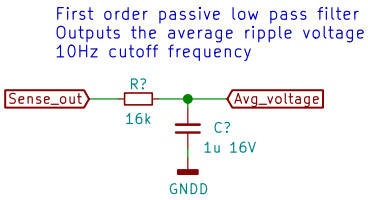


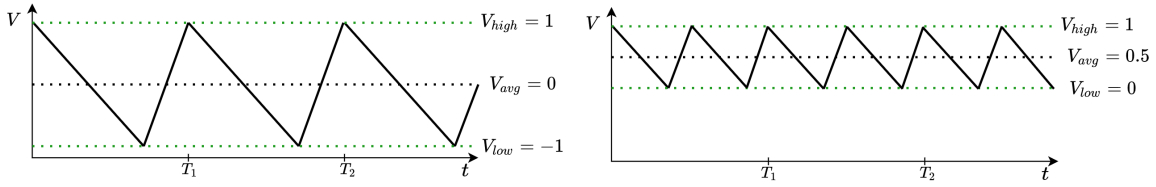
Figure 3.2: Average current 10Hz cut-off low pass filter

3.3.4 Peak Inductor Current Sensing

Based on the bandwidth requirement of 1kHz to 100kHz, it was identified that sampling the output signal of the current sensors to identify the peaks would be impractical. To achieve this a sampling rate of at least twice the highest frequency component would be specified by the Nyquist theorem, and a recommended minimum of one decade above is considered common practice, requiring a sampling rate of 1Mhz.
Due to this, designs were undertaken to simplify the sampling requirements. The following designs will take direct input from the current sensor, and aim to output a DC voltage that is representative of the input current peak values.

Precision Rectifier Peak Voltage Detection

This design is based around the operation of a signal precision rectifier, and the knowledge that the inductor current ripple will be symmetrical and triangular in shape [9]. Due to this symmetry, we know that the average inductor ripple current over a period will be zero, shown in Figure 3.3 (a). After rectification of the signal, the the ripple peak to peak value will halve, the frequency will double, and the new signal average will be half the new ripple peak to peak, shown in Figure 3.3 (b).



(a) Pre-rectification current sense output of 1V pk to pk, average voltage of 0V

(b) Post-rectification current sense output of 1V pk to pk, average voltage of 0.5V

Figure 3.3: Average voltage output of a symmetrical signal, before and after rectification

From here, we can obtain the signal average by applying a passive a low pass filter with a cut off of 10Hz to the output, producing a sampleable DC voltage. To obtain the full original signal peak to peak value, this signal can then amplified with a gain of 4. The full design can be seen in Figure 3.4.

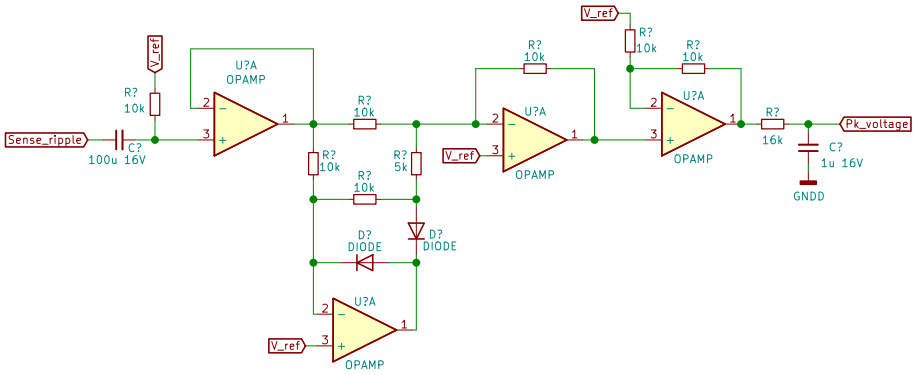


Figure 3.4: Precision rectifier peak detector designed circuit schematic

Sample and Hold Peak Voltage Detection

This design is based on existing voltage peak detection designs [15, 16]. The design operates on a similar principle to a sample and hold unit, charging a signal capturing capacitor through a diode such that it will not discharge. In order to remove the voltage drop across the charging diode, it is placed within the forward path of an operational amplifier buffer. The output voltage is then buffered again to allow for sampling. The full design can be seen in Figure 3.5.

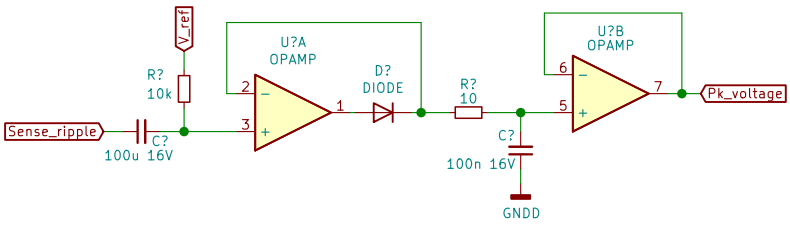


Figure 3.5: Sample & hold peak detector designed circuit schematic

Both of the discussed designs have been simulated in LTSpice, and have had their operation confirmed, please see **??** for output plots. From this it was identified that both designs would

be able to meet the resolution specification of 10mA, and bandwidth specification of 1kHz to 100kHz outlined in requirement 4, 5, 6, & 7.
It should also be noted however that the design of the precision rectifier based peak detector is much more complex than that of the sample and hold peak detector. Because of this, it was decided that the sample and hold based peak detector would be most suitable for this project, as it meets all required specifications, and best adheres to the ease of use goal.

Current sensing digitisation

Due to the operation of the design discussed in Section 3.3.4, the output DC voltage will be imposed on a DC refrence voltage. To eliminate this DC bias from the output, a dedicated external ADC with a differential input can be employed. This will allow for the removal of the bias at the digitisation of the signal. The selected ADC is the MAX11644, which provides a 12bit resolution, an internal reference of 4.096V, and the required differential input. Based on these specifications, this design is capable of measuring input voltages between 0V and 4.096V, with a resolution of 8mV. This will give a current sensing resolution of 2.6mA, meeting the specifications of requirement 6.

3.4 Control System

When designing the output voltage and inductor current ripple control systems, a successful design will meet all the requirements outlined by Section 3.1. From this we can identify that both controllers must provide a steady state error that is less $\pm 5\%$ of the targeted value, as specified in requirements 3 & 6.

3.4.1 Output Load Voltage Controller

To achieve the desired output voltage steady state error, a feedback controller with an integrating term should be used. To provide this, the design will implement a proportional, integral, & differential (PID) controller. This controller will be provided with the buck converter output voltage as an input, this will then be converted to the theoretical PWM duty cycle required to produce that output based on Equation (2.1). This will then be used to calculate the controller error and output the new PWM duty cycle.
To design this, a mathematical model of a buck converter [17] was found and simulated in Matlab. This model was then discretised such that it could be implemented on a microcontroller, and a PID controller was then designed with the '`PIDTune()`' function. A step response simulation of this model can be found in **??**.
Due to the control topology used in this design, this design will be able to provide an output voltage steady state error of less than $\pm 5\%$, as specified in requirement 3.

3.4.2 Inductor Current Ripple Controller

To achieve the desired inductor current ripple steady state error, the same topology implemented for the output voltage controller will be implemented. This PID controller will take the system's inductor current ripple as a percentage of the average current, and then calculate the error between it and the target value. From here it will then output the new PWM switching frequency.
Due to the control topology used in this design, this design will be able to provide an inductor current ripple steady state error of less than $\pm 5\%$, as specified in requirement 6.

Chapter 4: Implementation

4.1 PWM Signal Generation

The PWM signal generator subsystem was designed around the Espressif ESP32 microcontroller. For ease of development around this microcontroller, a pre-built breadboard compatible development board was purchased for the implementation.

Using this development board, a PWM hardware driver was developed to facilitate the implementation of this subsystems core functionality as specified in Section 3.1. This driver implements three core functions, '`PWM_setup()`' to initialise the PWM hardware, '`PWM_set_duty()`' to select a new duty cycle, and '`PWM_set_frequency`' to select a new frequency. The full driver implementation can be found in **??**.

After the software implementation had been completed, it was identified that the 3.3V digital output of the microcontroller would be incapable of driving the buck converters switching power MOSFET. To resolve this, the IR2125 high side N-channel gate driver IC was purchased to drive the MOSFET from the PWM generators output signal. This final circuit was then implemented and it's functionality was tested on a breadboard. Please see **??** for the designed schematic, and **??** for the implemented breadboard circuit.

4.2 System State Sensing

4.2.1 Output Voltage Sensing

The output voltage sensing design discussed in Section 3.3.1 was implemented on a prototyping breadboard. Please see **??** for the designed schematic, and **??** for the implemented breadboard circuit.
Using the ESP32 development board, an ADC hardware driver was developed to facilitate the measurement of the sensor output. This driver implements the core functionality of the ADC though two functions, '`init_adc()`' to assign the input IO and measurement resolution, and '`read_adc()`' to take an ADC measurement. Using these two functions this driver then also facilitates the computation of a rolling average with the '`rolling_average()`' function, and voltage conversion with the '`adc_conversion()`' function. The full driver implementation can be found in **??**.

When initially implementing the ADC conversion function, it was assumed that that the output conversion of the ADC was linear. Once this had been implemented, it was observed that there were large inaccuracies in the voltage conversion.
From this it was identified that the internal ADC was non-linear, and would require calibration before meeting the required specifications. To achieve this, ADC measurements were taken for a selection of known input voltages ranging from 100mV to 3V in 500mV

steps. These ADC measurements were then plotted against their respective input voltages using Matlab, and a forth order polynomial was fit to the data, shown in Figure 4.1. This polynomial was then used for the conversion of the raw ADC reading to a voltage, greatly improving the ADC's accuracy.

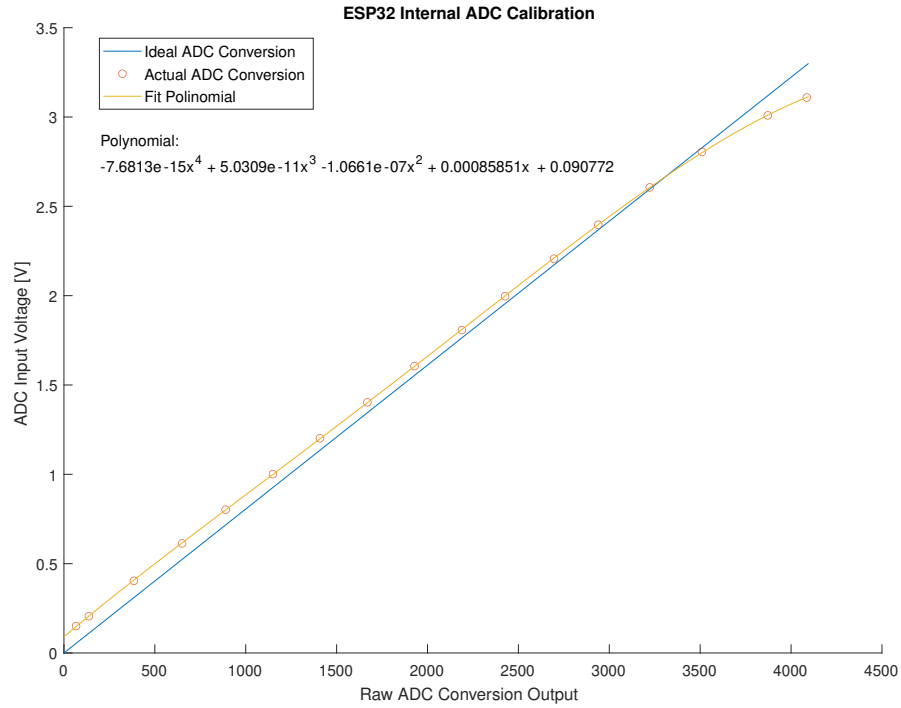


Figure 4.1: ESP32 internal ADC calibration data with forth order polynomial fit

4.2.2 Inductor Current Sensing

Average Inductor Current Sensing

The average inductor current sensing design discussed in Section 3.3.3 was implemented on a prototyping breadboard. Please see Figure 4.2 for the designed schematic, and **??** for the implemented breadboard circuit.
This design also utilises the ESP32 internal ADC, which was previously implemented in Section 4.2.1. Therefore no further implementation was required for the functionality of this design.

Peak Inductor Current Sensing

The peak inductor current sensing design discussed in Section 3.3.4 was initially implemented on a prototyping breadboard, using an LT084CN operational amplifier (op amp) provided by the lab technicians.
On implementation it was observed that the functional principles of the design held true, as the design maintained a DC output voltage that was dependant in the input peak to peak ripple. However it was observed that the accuracy of the design was much lower than expected when compared to the design simulations. The operation of this original design can be seen in **??**.

It was identified that the limiting factor within the design was the bandwidth and slew-rate of the input stage op amp seen in Figure 3.5. This op amp is responsible for charging the sampling capacitor and negating the forward bias diode drop, and therefore it's bandwidth and slew-rate will dictate the bandwidth of the design.
Based on this, the input op amp was replaced with the OPA2830, as it provided a greatly improved bandwidth of 230MHz and a slew rate of 500V/μs. The original design was also altered to place a potentiometer in series with the sampling capacitor, as well as adding a high impedance resistor in parallel with this capacitor. This allows for the final designs performance to be tuned through the potentiometer, and any overshoot to be quickly dissipated by the parallel discharge resistor. This final design of the schematic can be seen in Figure 4.2, and the implemented breadboard circuit can be found in **??**.

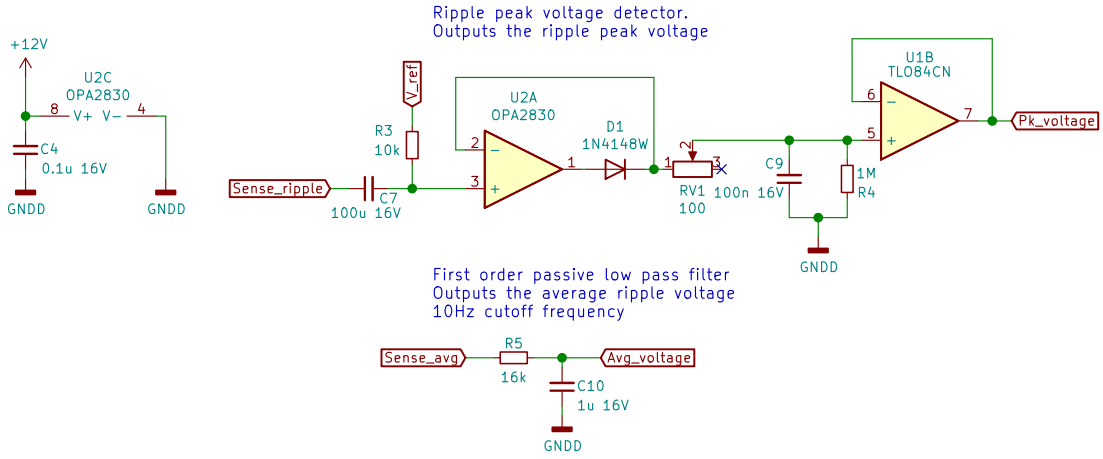


Figure 4.2: Finalised peak detector schematic, with updated op amp selection and performance improvements

4.3 Control System

The control system design discussed in Section 3.4 has been implemented in the form of a generic PID based control system library. This control system implementation provides a structure in which all of the controller variables and states are stored. This simplifies the initialisation of the controller, as the proportional, integral, derivative, and time period constants can all be specified at the structure initialisation. This implementation also allows for the creation and management of multiple controllers simultaneously, meeting requirements 2 & 4.
This control library also provides more advanced safety features for the system, including selectable minimum and maximum output limits, and selectable integrator windup limits.

This library implements two core functions which provide the full functionality of a digital PID control loop. '`PID_init()`' initialises and sets up the controller, and '`PID_update()`' calculates the new output of the controller. The full driver implementation can be found in **??**.

4.4 Full system implementation

Software implementation

The full system software implementation is built upon the ESP-IDF framework, and utilises a FreeRTOS to provide tasks and scheduling.
The ESP-IDF Framework was chosen over other supported frameworks due to it's increased control of the ESP32 available hardware peripherals, which was required for the designs system to meet it's specified requirements from Figure 3.1.
The use of the ESP-IDF framework also facilitated the use of FreeRTOS, providing access to a task scheduler that would greatly decrease the structural complexity of this system. This scheduler allows each subsystem within the design to operate from within a task, independent of all others. therefore, this implementation reduces the complexity of further developments within this project, without limiting the functionality of the microcontroller platform. The full system software implementation can be found in **??**.

Hardware implementation

To facilitate the ease of use of the fully designed system, a printed circuit board (PCB) was designed and implemented using the KiCAD software platform. This PCB implements all finalised designed elements discussed in Chapter 3, and provides multiple footprints for the buck converter output filter to allow for expedited testing and varying filters. For the full system schematic, please refer to **??**.

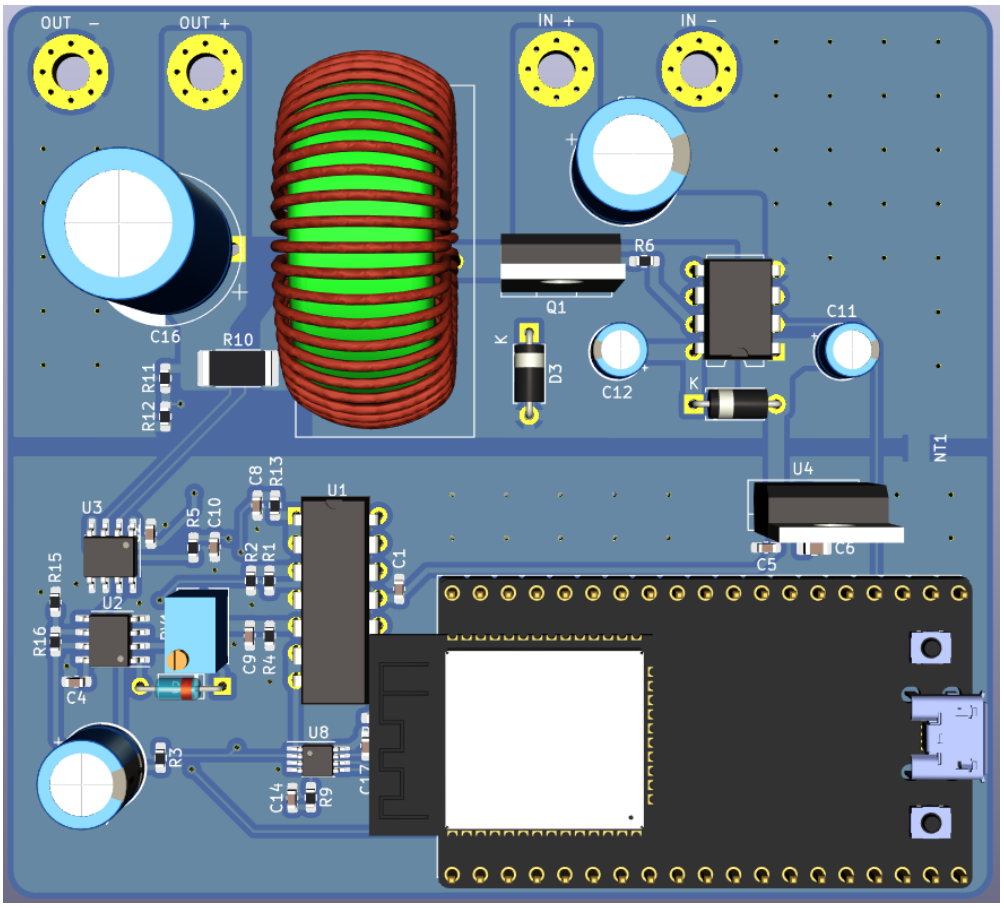


Figure 4.3: Full system printed circuit board implementation

Chapter 5: Evaluation

This evaluation will look to evaluate the the success of the designed and implemented components, in achieving their specified requirements as outlined in Chapter 3.

5.1 PWM Generation

Duty Cycle Variation

Switching Frequency Variation

5.2 System State Sensing

5.2.1 Output Voltage Sensing

5.2.2 Inductor Current Sensing

Average Inductor Current Sensing

Peak Inductor Current Sensing

5.3 Control System

Output Voltage Control

Chapter 6: Conclusions & Future Work

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