

# 8 PIN DIP HIGH SPEED 10MBit/s LOGIC GATE PHOTOCOUPLER

**6N137**

## Features:

- High speed 10Mbit/s
- Guaranteed performance from -40 to 85°C
- Logic gate output
- High isolation voltage between input and output (Viso=5000 V rms )
- Pb free and RoHS compliant.
- UL approved (No. 214129)
- VDE approved (No. 132249)
- SEMKO approved
- NEMKO approved
- DEMKO approved
- FIMKO approved
- CSA approved (No. 2037145)

## Description

The 6N137 consists of an infrared emitting diode optically coupled to a high speed integrated photo detector logic gate with a strobable output.

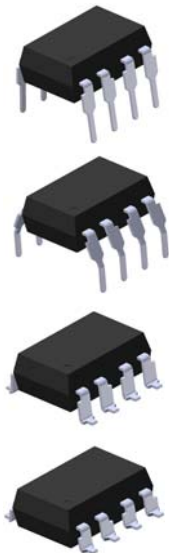
It is packaged in a 8-pin DIP package and available in wide-lead spacing and SMD options.

## Applications

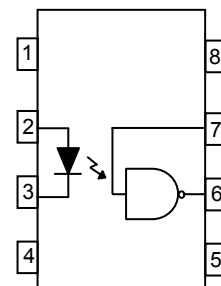
- Ground loop elimination
- LSTTL to TTL, LSTTL or 5 volt CMOS
- Line receiver, data transmission
- Data multiplexing
- Switching power supplies
- Pulse transformer replacement
- Computer peripheral interface

## Truth Table (Positive Logic)

Input	Enable	Output
H	H	L
L	H	H
H	L	H
L	L	H
H	NC	L
L	NC	H



## Schematic



A 0.1μF bypass capacitor must be connected between pins 8 and 5<sup>\*3</sup>

## Pin Configuration

- 1, No Connection
- 2, Anode
- 3, Cathode
- 4, No Connection
- 5, Gnd
- 6, Vout
- 7, V<sub>E</sub>
- 8, V<sub>CC</sub>

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**6N137**

## Absolute Maximum Ratings ( $T_a=25^{\circ}\text{C}$ )

Parameter		Symbol	Rating	Unit
Input	Forward current	$I_F$	50	mA
	Enable input voltage Not exceed $V_{CC}$ by more than 500mV	$V_E$	5.5	V
	Reverse voltage	$V_R$	5	V
	Power dissipation No derating needed	$P_D$	100	mW
Output	Power dissipation No derating needed	$P_C$	85	mW
	Output current	$I_O$	50	mA
	Output voltage	$V_O$	7.0	V
	Supply voltage	$V_{CC}$	7.0	V
Output Power Dissipation		$P_O$	100	mW
Isolation voltage <sup>*1</sup>		$V_{ISO}$	5000	V rms
Operating temperature		$T_{OPR}$	-40 ~ +85	$^{\circ}\text{C}$
Storage temperature		$T_{STG}$	-55 ~ +125	$^{\circ}\text{C}$
Soldering temperature <sup>*2</sup>		$T_{SOL}$	260	$^{\circ}\text{C}$

### Notes

\*1 AC for 1 minute, R.H.= 40 ~ 60% R.H. In this test, pins 1 & 2 are shorted together, and pins 3 & 4 are shorted together.

\*2 For 10 seconds.

# 8 PIN DIP HIGH SPEED 10MBit/s LOGIC GATE PHOTOCOUPLER

**6N137**

## Electrical Characteristics ( $T_a = -40$ to $85^\circ\text{C}$ unless specified otherwise)

### Input

Parameter	Symbol	Min.	Typ.*	Max.	Unit	Condition
Forward voltage	$V_F$	-	1.4	1.8	V	$I_F = 10\text{mA}$
Reverse voltage	$V_R$	5.0	-	-	V	$I_R = 10\mu\text{A}$
Temperature coefficient of forward voltage	$\Delta V_F / \Delta T_A$	-	-1.8	-	mV/ $^\circ\text{C}$	$I_F = 10\text{mA}$
Input capacitance	$C_{IN}$	-	60	-	pF	$V_F = 0$ , $f = 1\text{MHz}$

### Output

Parameter	Symbol	Min.	Typ.*	Max.	Unit	Condition
High level supply current	$I_{CCH}$	-	7	10	mA	$I_F = 10\text{mA}$ , $V_E = 0.5\text{V}$ , $V_{CC} = 5.5\text{V}$
Low level supply current	$I_{CCL}$	-	9	13	mA	$I_F = 0\text{mA}$ , $V_E = 0.5\text{V}$ , $V_{CC} = 5.5\text{V}$
High level enable current	$I_{EH}$	-	-0.6	-1.6	mA	$V_E = 0.5\text{V}$ , $V_{CC} = 5.5\text{V}$
Low level enable current	$I_{EL}$	-	-0.8	-1.6	mA	$V_E = 2.0\text{V}$ , $V_{CC} = 5.5\text{V}$
High level enable voltage	$V_{EH}$	2.0	-	-	V	$I_F = 10\text{mA}$ , $V_{CC} = 5.5\text{V}$
Low level enable voltage	$V_{EL}$	-	-	0.8	V	$I_F = 10\text{mA}$ , $V_{CC} = 5.5\text{V}$

## Transfer Characteristics ( $T_a = -40$ to $85^\circ\text{C}$ unless specified otherwise)

Parameter	Symbol	Min.	Typ.*	Max.	Unit	Condition
HIGH Level Output Current	$I_{OH}$	-	2.1	100	$\mu\text{A}$	$V_{CC} = 5.5\text{V}$ , $V_O = 5.5\text{V}$ , $I_F = 250\mu\text{A}$ , $V_E = 2.0\text{V}$
LOW Level Output Voltage	$V_{OL}$	-	0.35	0.6	V	$V_{CC} = 5.5\text{V}$ , $I_F = 5\text{mA}$ , $V_E = 2.0\text{V}$ , $I_{OL} = 13\text{mA}$
Input Threshold Current	$I_{FT}$	-	2.5	5	mA	$V_{CC} = 5.5\text{V}$ , $V_O = 0.6\text{V}$ , $V_E = 2.0\text{V}$ , $I_{OL} = 13\text{mA}$

# 8 PIN DIP HIGH SPEED 10MBit/s LOGIC GATE PHOTOCOUPLER

**6N137**

## Switching Characteristics (T<sub>a</sub>=-40 to 85°C, V<sub>CC</sub>=5V, I<sub>F</sub>=7.5mA unless specified otherwise)

Parameter	Symbol	Min.	Typ.*	Max.	Unit	Condition
Propagation delay time to output High level (Fig.12)	T <sub>PHL</sub>	-	35	75	ns	C <sub>L</sub> = 15pF, R <sub>L</sub> =350Ω, TA=25°C
Propagation delay time to output Low level (Fig.12)	T <sub>PLH</sub>	-	40	75	ns	C <sub>L</sub> = 15pF, R <sub>L</sub> =350Ω, TA=25°C
Pulse width distortion	T <sub>phl</sub> – T <sub>plh</sub>	-	5	35	ns	C <sub>L</sub> = 15pF, R <sub>L</sub> =350Ω
Output rise time (Fig.12)	t <sub>r</sub>	-	40	-	ns	C <sub>L</sub> = 15pF, R <sub>L</sub> =350Ω
Output fall time (Fig.12)	t <sub>f</sub>	-	10	-	ns	C <sub>L</sub> = 15pF, R <sub>L</sub> =350Ω

## Switching Characteristics (T<sub>a</sub>=-40 to 85°C, V<sub>CC</sub>=5V, I<sub>F</sub>=7.5mA unless specified otherwise)

Enable Propagation Delay Time to Output High Level (Fig.13)	t <sub>ELH</sub>	-	15	-	ns	I <sub>F</sub> = 7.5mA, V <sub>EH</sub> =3.5V, C <sub>L</sub> = 15pF, R <sub>L</sub> =350Ω
Enable Propagation Delay Time to Output Low Level (Fig.13)	t <sub>EHL</sub>	-	15	-	ns	I <sub>F</sub> = 7.5mA, V <sub>EH</sub> =3.5V, C <sub>L</sub> = 15pF, R <sub>L</sub> =350Ω
Common Mode Transient Immunity at Logic High *4	CM <sub>H</sub>	5000	-	-	V/μS	I <sub>F</sub> = 0mA, V <sub>CM</sub> =50Vp-p, V <sub>OH</sub> =2.0V, R <sub>L</sub> =350Ω, TA=25°C
Common Mode Transient Immunity at Logic Low *5	CM <sub>L</sub>	5000	-	-	V/μS	I <sub>F</sub> = 7.5mA, V <sub>CM</sub> =50Vp-p, V <sub>OL</sub> =0.8V, R <sub>L</sub> =350Ω, TA=25°C

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**6N137**

## Typical Performance Curves

Fig.1 Input Diode Forward Voltage vs. Forward Current

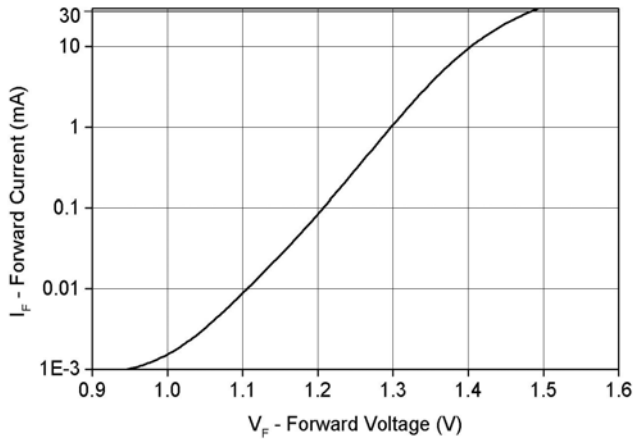


Fig.2 Low Level Output Voltage vs. Ambient Temperature

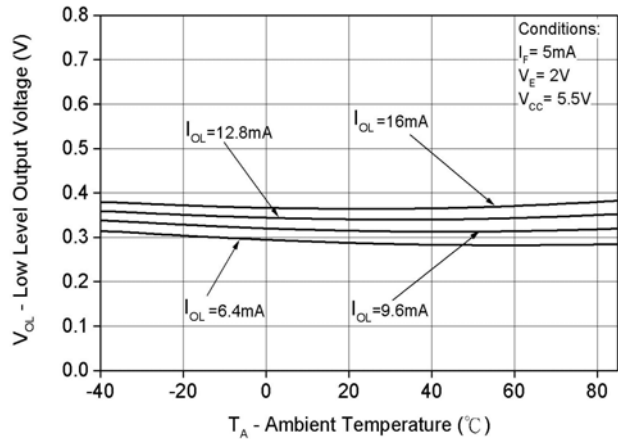


Fig.3 Low Level Output Current vs. Ambient Temperature

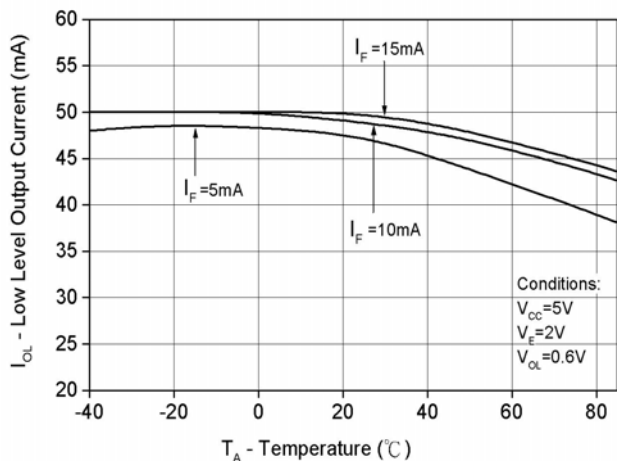


Fig.4 Input Threshold Current vs. Ambient Temperature

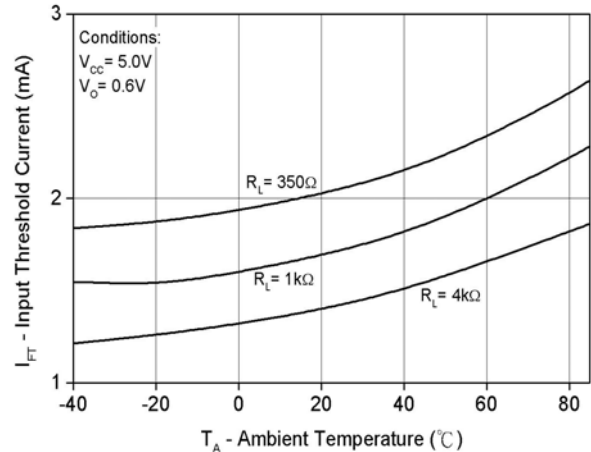


Fig.5 Output Voltage vs. Input Forward Current

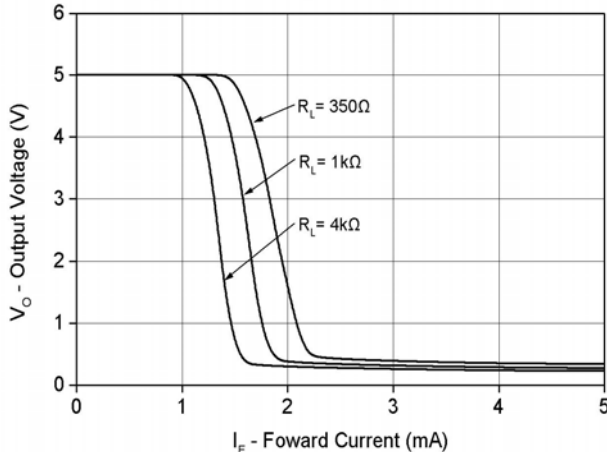
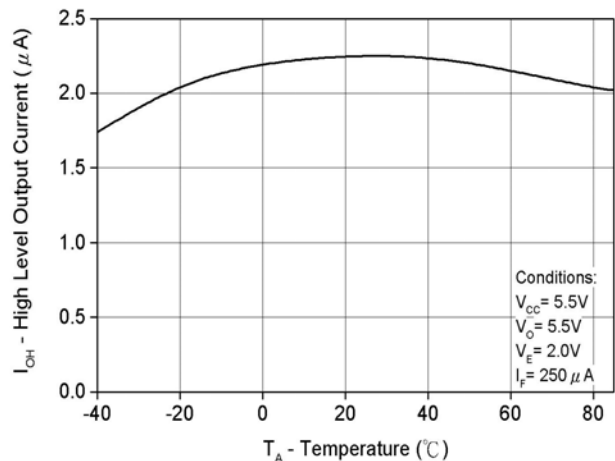


Fig.6 High Level Output Current vs. Temperature



# 8 PIN DIP HIGH SPEED 10MBit/s LOGIC GATE PHOTOCOUPLER

**6N137**

Fig.7 Switching Time vs. Forward Current

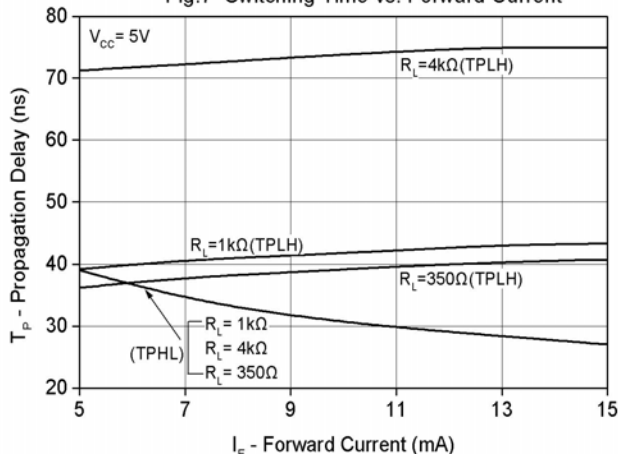


Fig.8 Switching Time vs. Temperature

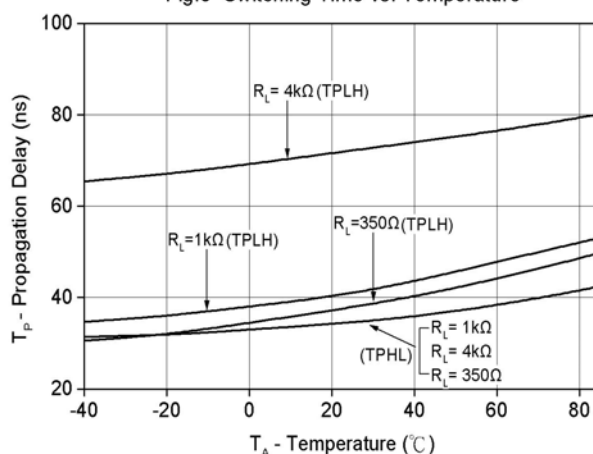


Fig.9 Pulse Width Distortion vs. Temperature

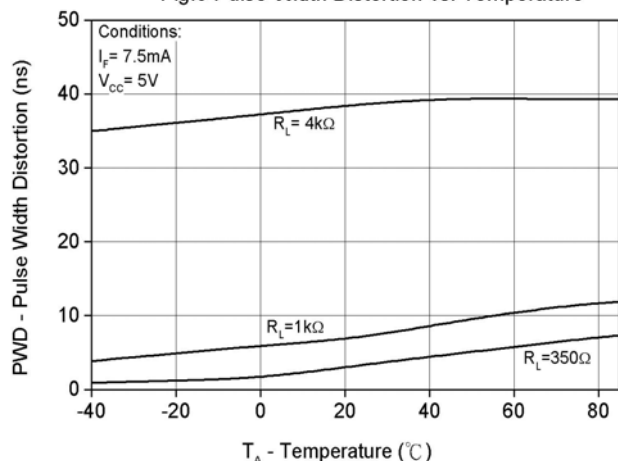


Fig.10 Rise and Fall Time vs. Temperature

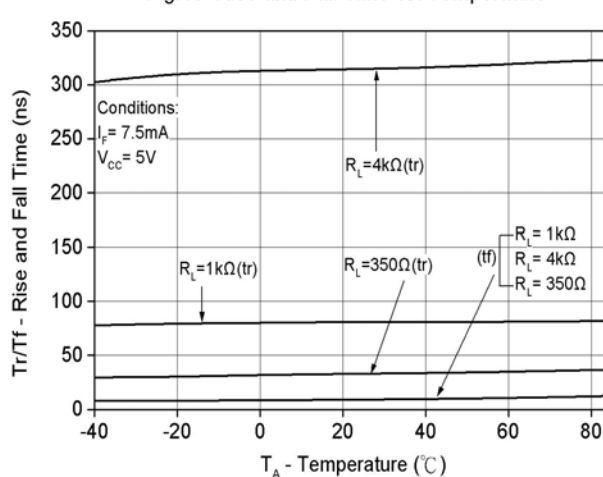
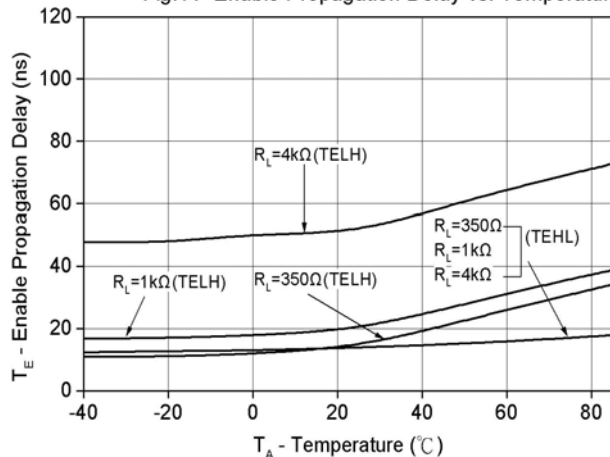
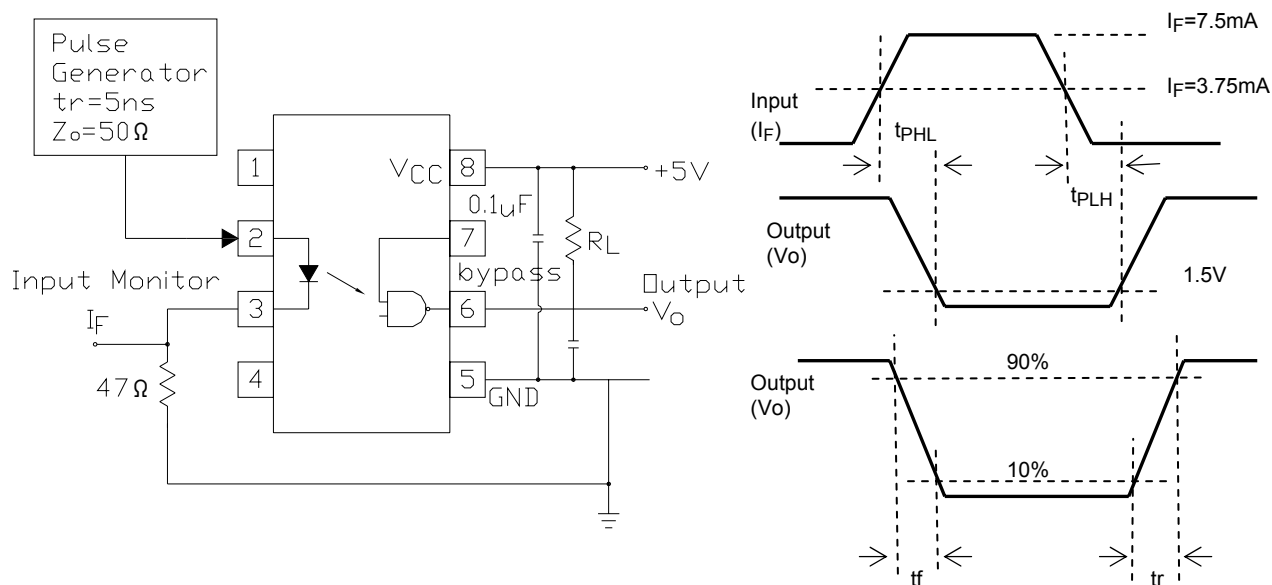


Fig.11 Enable Propagation Delay vs. Temperature

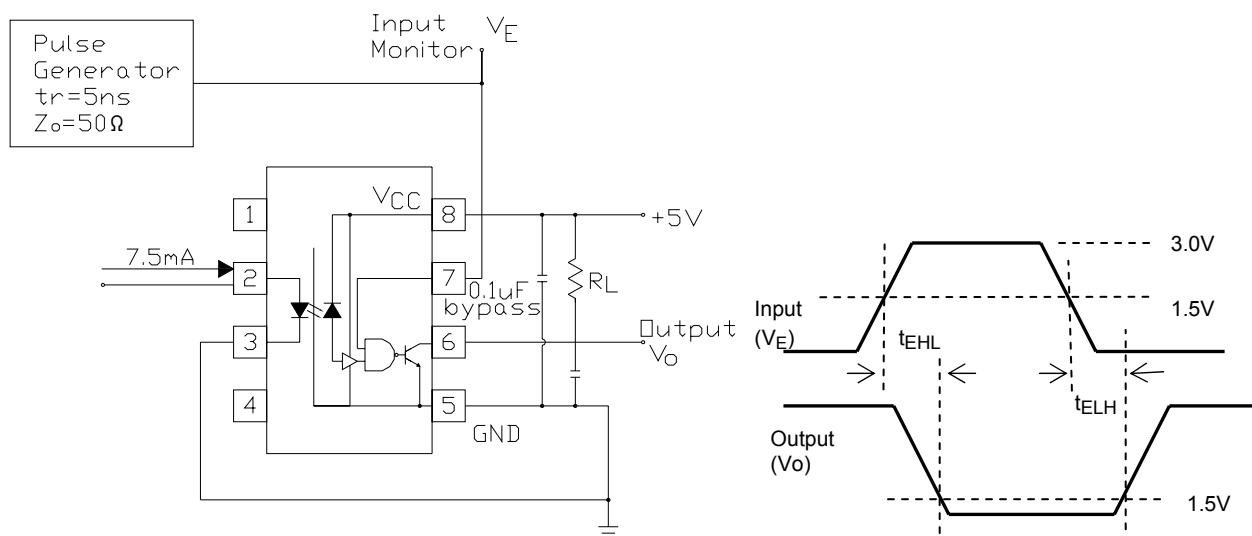


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**6N137**



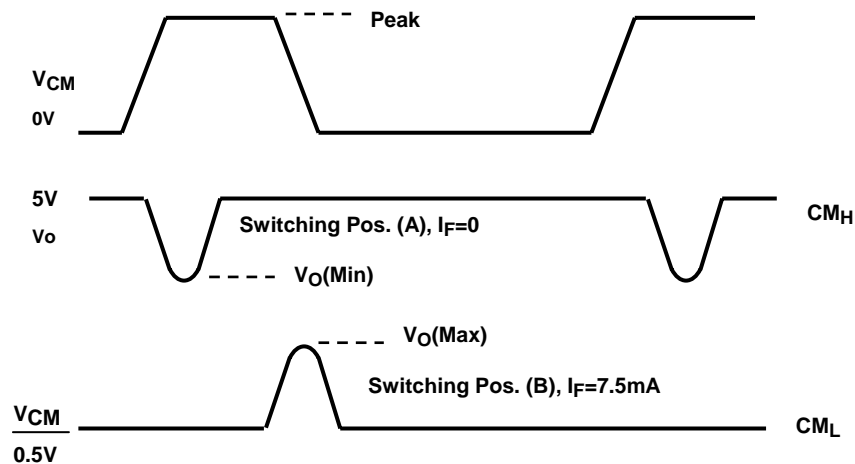
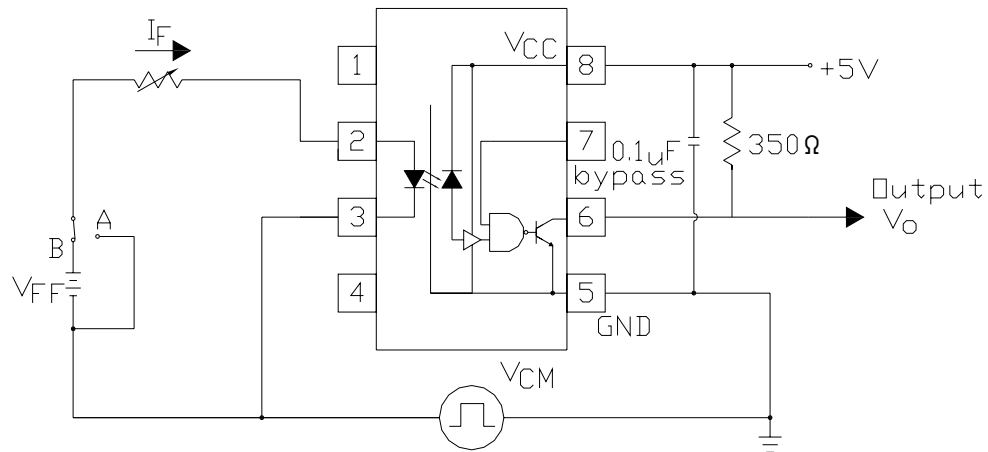
**Fig. 12 Test circuit and waveforms for  $t_{PHL}$ ,  $t_{PLH}$ ,  $t_r$ , and  $t_f$**



**Fig. 13 Test circuit and waveform for  $t_{EHL}$  and  $t_{ELH}$**

## 8 PIN DIP HIGH SPEED 10MBit/s LOGIC GATE PHOTOCOUPLER

**6N137**



**Fig. 14 Test circuit Common mode Transient Immunity**

**Notes:**

- \*3 The VCC supply must be bypassed by a 0.1μF capacitor or larger. This can be either a ceramic or solid tantalum capacitor with good high frequency characteristic and should be connected as close as possible to the package VCC and GND pins
- \*4 CMH– The maximum tolerable rate of rise of the common mode voltage to ensure the output will remain in the HIGH state (i.e., VOUT > 2.0V).
- \*5 CML– The maximum tolerable rate of rise of the common mode voltage to ensure the output will remain in the LOW output state (i.e., VOUT < 0.8V).





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## 8 PIN DIP HIGH SPEED 10MBit/s LOGIC GATE PHOTOCOUPLER

**6N137**

### Order Information

#### Part Number

**6N137Y(Z)-V**

#### Note

- Y = Lead form option (S, S1, M or none)  
Z = Tape and reel option (TA, TB or none).  
V = VDE (optional)

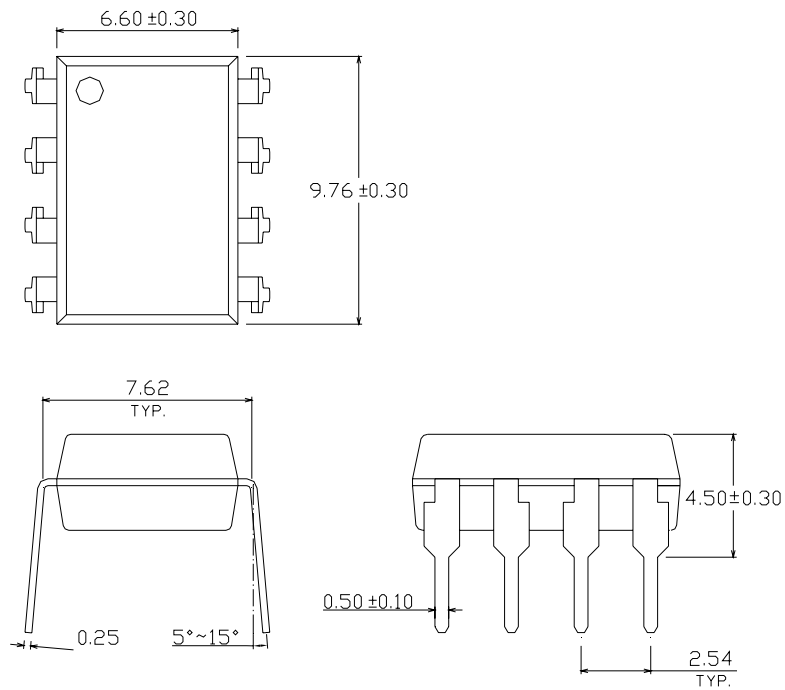
Option	Description	Packing quantity
None	Standard DIP-8	45 units per tube
M	Wide lead bend (0.4 inch spacing)	45 units per tube
S (TA)	Surface mount lead form + TA tape & reel option	1000 units per reel
S (TB)	Surface mount lead form + TB tape & reel option	1000 units per reel
S1 (TA)	Surface mount lead form (low profile) + TA tape & reel option	1000 units per reel
S1 (TB)	Surface mount lead form (low profile) + TB tape & reel option	1000 units per reel

# 8 PIN DIP HIGH SPEED 10MBit/s LOGIC GATE PHOTOCOUPLER

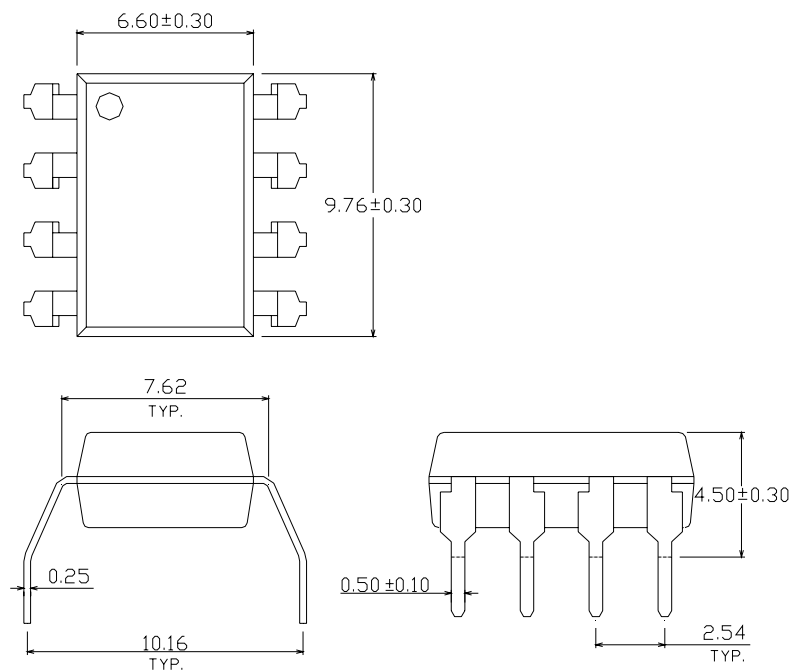
**6N137**

## Package Drawing (Dimensions in mm)

### Standard DIP Type



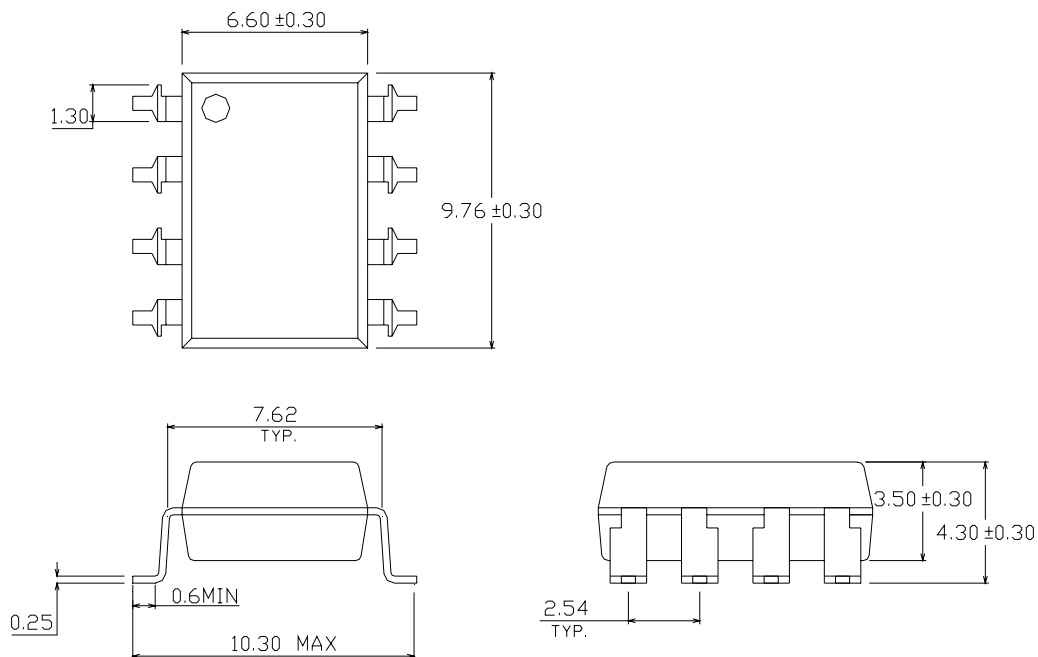
### Option M Type



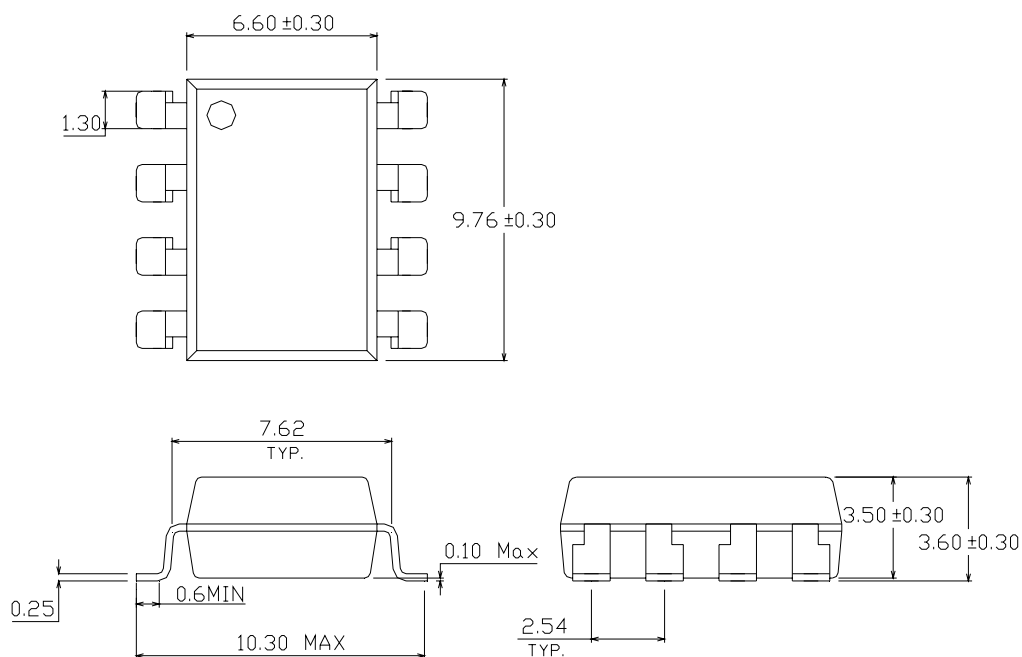
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**6N137**

## Option S Type



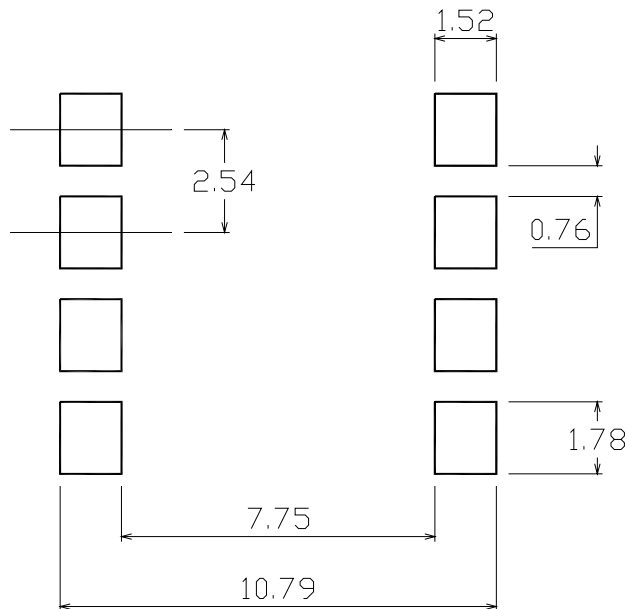
## Option S1 Type



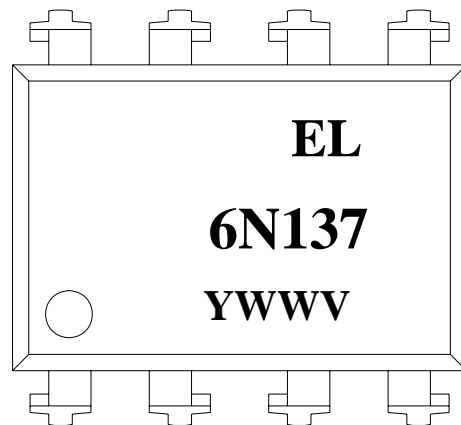
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**6N137**

## Recommended pad layout for surface mount leadform



## Device Marking



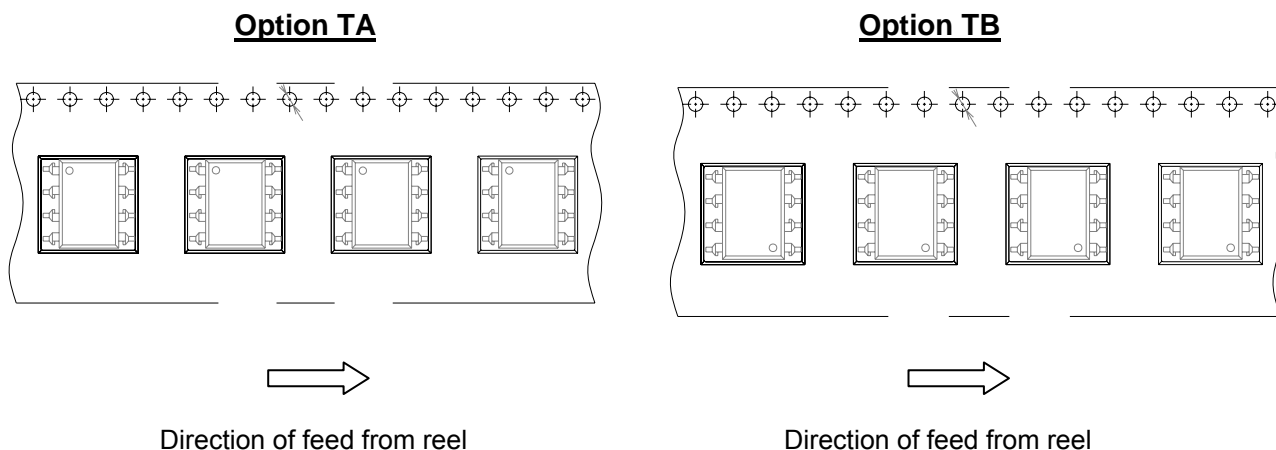
## Notes

- 6N137 denotes Device Number
- Y denotes 1 digit Year code
- WW denotes 2 digit Week code
- V denotes VDE (optional)

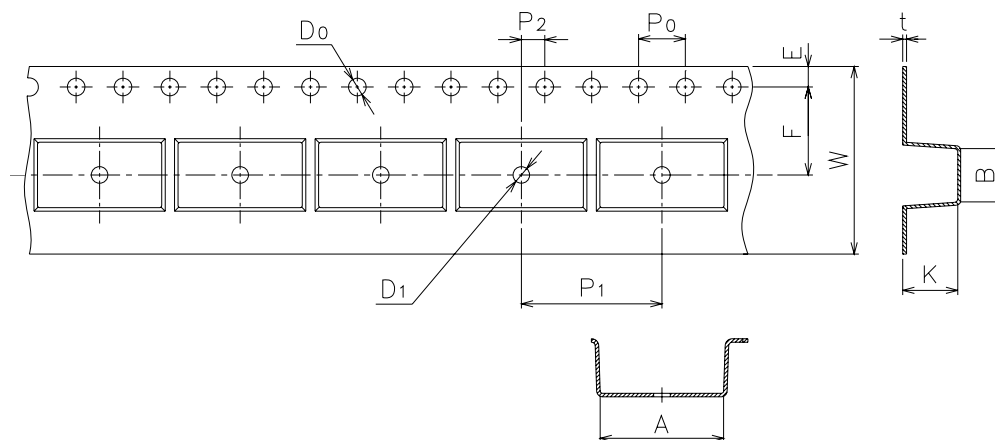
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**6N137**

## Tape & Reel Packing Specifications



## Tape dimensions



Dimension No.	A	B	Do	D1	E	F
Dimension(mm)	10.4±0.1	10.0±0.1	1.5±0.1	1.5±0.1	1.75±0.1	7.5±0.1
Dimension No.	Po	P1	P2	t	W	K
Dimension(mm)	4.0±0.1	12.0±0.1	2.0±0.1	0.4±0.1	16.0+0.3/ -0.1	4.5±0.1

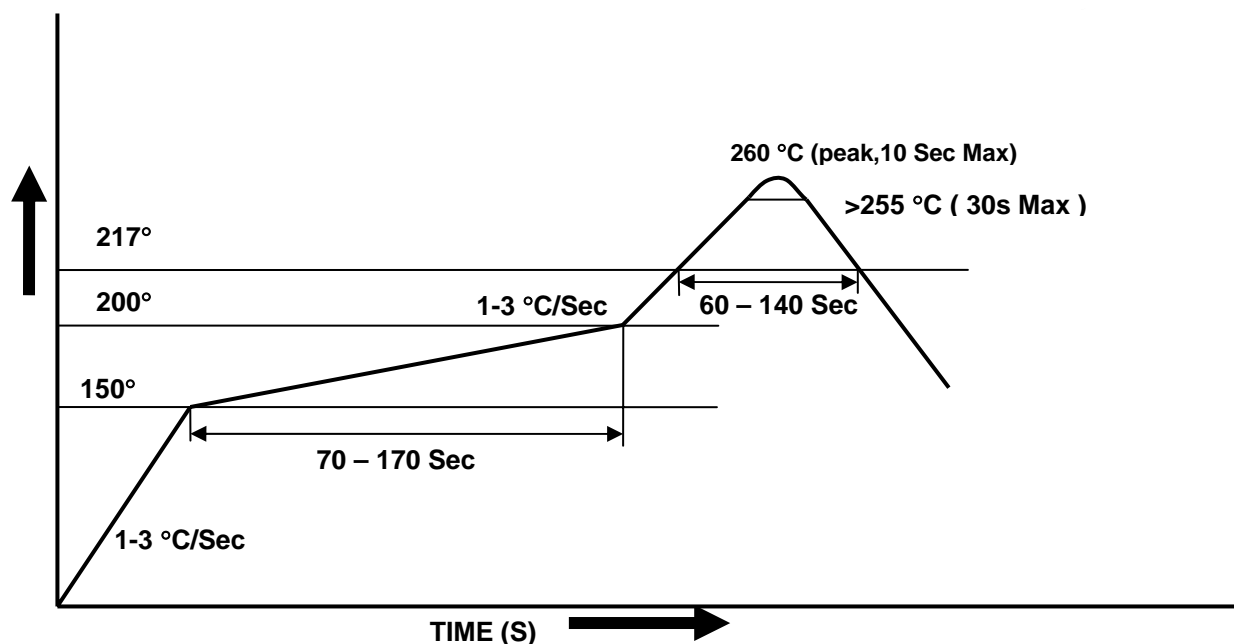


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6N137

### Solder Reflow Temperature Profile



## **8 PIN DIP HIGH SPEED 10MBit/s LOGIC GATE PHOTOCOUPLER**

**6N137**

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