2Pai Semi

3.0 kV rms/4.0 kV rms 双通道数字隔离器

Data Sheet

π120/π121/π122

产品特性

超低功耗: 0.35mA/通道
数据速率: π12xA: 600Mbps
π12xM: 10Mbps
π12xU: 150kbps
高共模瞬变抗扰度: 100 kV/μs （典型值）
对辐射和传导噪声的高抗干扰能力
低传输延迟:
3.6 ns （最大值，5 V 工作电压）
4.4 ns （最大值，3.3 V 工作电压）
隔离电压:
π12xx3: AC 3000Vrms, DC 5000V, Surge 5000V
π12xx4: AC 4000Vrms, DC 6000V, Surge 6000V
安全和法规认证(申请中)
UL 认证:
3000Vrms/4000Vrms 测试 1 分钟 符合 UL1577
CSA 元件验收通知 5A
VDE 合格证书
DIN V VDE V 0884-10 (VDE V 0884-10):2006-12
V_{IORM} = 565V peak/753 V peak
CQC 认证，符合 GB4943.1-2011
3 V to 5.5 V 电平转换
宽工作温度范围: -40~125°C
8 引脚 SOIC 封装，符合 RoHS 标准
未用的输入信号引脚需要连接到默认状态

应用

通用多通道隔离
工业现场总线隔离

概述

π120/π121/π122 双通道数字隔离器是基于荣湃半导体公司的隔离技术,利用高速、互补金属氧化物半导体（CMOS）技术设计而成。具有优于光耦合器件和其它集成式耦合器等替代器件的出色性能特征。在 5V 的工作条件下，这些器件的最大传播延迟为 3.6ns，脉冲宽度失真小于 0.3ns，最大的通道匹配为 0.4ns。π120/π121/π122 数据通道属于独立式通道，可提供多种配置选择，可承受 3 KV rms 或 4.0 KV rms 的隔离电压(参见"订购指南)。

功能框图

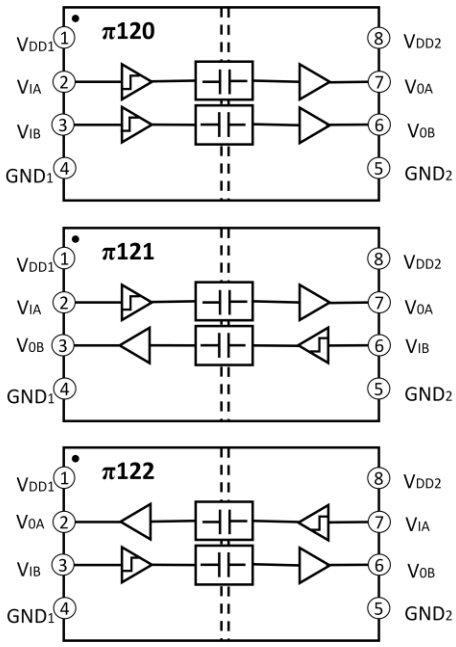


图 1. π120/π121/π122 功能模块框图

这些器件均可采用3.0V至5.5V电源电压工作，与低压系统兼容，并且能够跨越隔离栅实现电平转换功能。与其它光耦合器不同，这些器件可确保在没有输入时能正确输出。它们提供两种不同的故障安全选项，输入电源未用或输入禁用时，输出转换到预定状态。

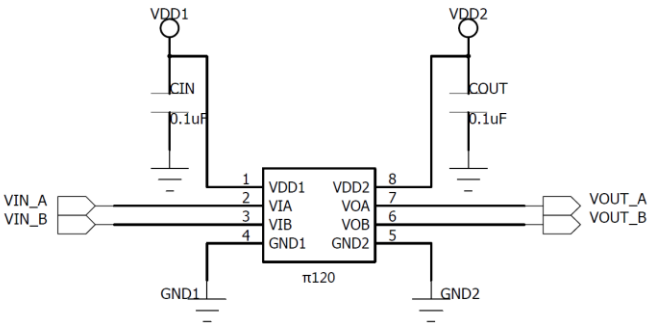


图 2. π120 典型应用电路

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—5 V OPERATION

All typical specifications are at T_A = 25 ℃, V_{DD1} = V_{DD2} = 5 V. Minimum/maximum specifications apply over the entire recommended operation range of 4.5 V ≤ V_{DD1} ≤ 5.5 V, 4.5 V ≤ V_{DD2} ≤ 5.5 V, and −40°C ≤ T_A ≤ +125°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted. Supply currents are specified with 50% duty cycle signals and C_L = 0 pF.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SWITCHING SPECIFICATIONS						
π12xA						
Pulse Width	PW			1.5	ns	Within pulse width distortion (PWD) limit
Max Data Rate		600			Mbps	Within PWD limit
π12xM						
Pulse Width	PW			100	ns	Within pulse width distortion (PWD) limit
Max Data Rate		10			Mbps	Within PWD limit
π12xU						
Pulse Width	PW			6.6	µs	Within pulse width distortion (PWD) limit
Max Data Rate		150			Kbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}	3.2	3.6	4.0	ns	50% input to 50% output
Pulse Width Distortion	PWD	0	0.3	0.4	ns	|tPLH − tPHL|
Change vs. Temperature			1.5		ps/°C	
Propagation Delay Skew	t_{PSK}			0.5	ns	Between any two units at the same temperature, voltage, and load
Channel Matching						
Codirectional	t_{PSKCD}		0	0.4	ns	
Opposing Direction	t_{PSKOD}		0	0.4	ns	
Jitter		40	50	60	ps p-p	See the Jitter Measurement section
		7	8	9	ps rms	See the Jitter Measurement section
DC SPECIFICATIONS						
Input Threshold Voltage						
Logic High	V_{IH}	2.41	3.02	3.63	V	
Logic Low	V_{IL}	1.41	1.77	2.13	V	
Output Voltage						
Logic High	V_{OH}	V_{DDx} − 0.1	V_{DDx}		V	I_{Ox}[1] = −20 µA, V_{Ix} = V_{IxH}[2]
		V_{DDx} − 0.2	V_{DDx}		V	I_{Ox}[1] = −4 mA, V_{Ix} = V_{IxH}[2]
Logic Low	V_{OL}		0.0	0.1	V	I_{Ox}[1] = 20 µA, V_{Ix} = V_{IxL}[3]
			0.1	0.2	V	I_{Ox}[1] = 4 mA, V_{Ix} = V_{IxL}[3]
Input Current per Channel	I_I	−10	+0.01	+10	µA	0 V ≤ V_{Ix} ≤ V_{DDx}
Quiescent Supply Current						C_L = 0 pF
π120	$I_{DD1 (Q)}$	68	85	102	µA	V_I[4] = 0 (N0), 1 (N1)[5]
	$I_{DD2 (Q)}$	472	590	708	µA	V_I[4] = 0 (N0), 1 (N1)[5]
	$I_{DD1 (Q)}$	68	85	102	µA	V_I[4] = 1 (N0), 0 (N1)[5]

	$I_{DD2 (Q)}$	477	597	717	µA	V_I[4] = 1 (N0), 0 (N1)[5]
π121	$I_{DD1 (Q)}$	269	337	405	µA	V_I[4] = 0 (N0), 1 (N1)[5]
	$I_{DD2 (Q)}$	280	351	422	µA	V_I[4] = 0 (N0), 1 (N1)[5]
	$I_{DD1 (Q)}$	265	332	399	µA	V_I[4] = 1 (N0), 0 (N1)[5]
	$I_{DD2 (Q)}$	269	337	405	µA	V_I[4] = 1 (N0), 0 (N1)[5]
π122	$I_{DD1 (Q)}$	269	337	405	µA	V_I[4] = 0 (N0), 1 (N1)[5]
	$I_{DD2 (Q)}$	280	351	422	µA	V_I[4] = 0 (N0), 1 (N1)[5]
	$I_{DD1 (Q)}$	265	332	399	µA	V_I[4] = 1 (N0), 0 (N1)[5]
	$I_{DD2 (Q)}$	269	337	405	µA	V_I[4] = 1 (N0), 0 (N1)[5]
Dynamic Supply Current						C_L = 0 pF
Dynamic Input	$I_{DDI (D)}$	10	13	16	µA /Mbps	Inputs switching, 50% duty cycle
Dynamic Output	$I_{DDO (D)}$	117	147	177	µA /Mbps	Inputs switching, 50% duty cycle
Under voltage Lockout	UVLO					
Positive V_{DDx} Threshold	V_{DDxUV+}	2.09	2.62	3.15	V	
Negative V_{DDx} Threshold	V_{DDxUV-}	1.93	2.42	2.91	V	
V_{DDx} Hysteresis	V_{DDxUVH}	0.15	0.19	0.23	V	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
AC SPECIFICATIONS						
Output Rise/Fall Time	t_R/t_F	0.4	0.6	0.8	ns	10% to 90%
Common-Mode Transient Immunity[6]	$\|CM_H\|$	75	100		kV/µs	V_{Ix} = V_{DDx}, V_{CM} = 1000 V, transient magnitude = 800 V
	$\|CM_L\|$	75	100		kV/µs	V_{Ix} = 0 V, V_{CM} = 1000 V, transient magnitude = 800 V

Notes:
[1] I_{Ox} is the Channel x output current, where x = A or B.
[2] V_{IxH} is the input side logic high voltage.
[3] V_{IxL} is the input side logic low voltage.
[4] V_I is the input voltage.
[5] N0 is the π120xx0/π121xx0/π122xx0 models, and N1 is the π120xx1/π121xx1/π122xx1 models. See the Ordering Guide.
[6] $|CM_H|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining the voltage output (V_O) > 0.8 V_{DDx}. $|CM_L|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O > 0.8 V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

Table 2. Total Supply Current vs. Data Throughput (C_L = 0 pF)

		2 Kbps			20 Mbps			80Mbps			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
SUPPLY CURRENT											
π120A											
Supply Current Side 1	I_{DD1}	0.07	0.09	0.11	0.24	0.31	0.38	0.76	0.95	1.14	mA
Supply Current Side 2	I_{DD2}	0.47	0.59	0.71	1.72	2.16	2.60	5.03	6.29	7.55	mA
π121A											
Supply Current Side 1	I_{DD1}	0.27	0.34	0.41	0.99	1.24	1.49	3.15	3.94	4.73	mA
Supply Current Side 2	I_{DD2}	0.27	0.34	0.41	1.02	1.28	1.54	3.29	4.12	4.95	mA
π122A											
Supply Current Side 1	I_{DD1}	0.27	0.34	0.41	0.99	1.24	1.49	3.15	3.94	4.73	mA
Supply Current Side 2	I_{DD2}	0.27	0.34	0.41	1.02	1.28	1.54	3.29	4.12	4.95	mA

Parameter	Symbol	2 Kbps			1 Mbps			10Mbps			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
SUPPLY CURRENT											
π120M											
Supply Current Side 1	I_{DD1}	0.07	0.09	0.11	0.08	0.10	0.12	0.16	0.20	0.24	mA
Supply Current Side 2	I_{DD2}	0.47	0.59	0.71	0.53	0.67	0.81	1.10	1.38	1.66	mA
π121M											
Supply Current Side 1	I_{DD1}	0.27	0.34	0.41	0.30	0.38	0.46	0.64	0.80	0.96	mA
Supply Current Side 2	I_{DD2}	0.27	0.34	0.41	0.31	0.39	0.47	0.61	0.77	0.93	mA
π122M											
Supply Current Side 1	I_{DD1}	0.27	0.34	0.41	0.30	0.38	0.46	0.64	0.80	0.96	mA
Supply Current Side 2	I_{DD2}	0.27	0.34	0.41	0.31	0.39	0.47	0.61	0.77	0.93	mA

Parameter	Symbol	2 Kbps			50 Kbps			150 Kbps			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
SUPPLY CURRENT											
π120U											
Supply Current Side 1	I_{DD1}	68	85	102	68	86	104	69	87	105	µA
Supply Current Side 2	I_{DD2}	473	592	711	476	596	716	483	604	725	µA
π121U											
Supply Current Side 1	I_{DD1}	268	335	402	269	337	405	273	342	411	µA
Supply Current Side 2	I_{DD2}	274	343	412	276	345	414	280	350	420	µA
π122U											
Supply Current Side 1	I_{DD1}	268	335	402	269	337	405	273	342	411	µA
Supply Current Side 2	I_{DD2}	274	343	412	276	345	414	280	350	420	µA

ELECTRICAL CHARACTERISTICS—3.3 V OPERATION.

All typical specifications are at T_A = 25 ℃, V_{DD1} = V_{DD2} = 3.3 V. Minimum/maximum specifications apply over the entire recommended operation range: 3.0 V ≤ V_{DD1} ≤ 3.6 V, 3.0 V ≤ V_{DD2} ≤ 3.6 V, and −40°C ≤ T_A ≤ +125°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted. Supply currents are specified with 50% duty cycle signals and C_L = 0 pF.

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SWITCHING SPECIFICATIONS						
π12xA						
Pulse Width	PW			1.5	ns	Within pulse width distortion (PWD) limit
Max Data Rate		600			Mbps	Within PWD limit
π12xM						
Pulse Width	PW			100	ns	Within pulse width distortion (PWD) limit
Max Data Rate		10			Mbps	Within PWD limit
π12xU						
Pulse Width	PW			6.6	µs	Within pulse width distortion (PWD) limit
Max Data Rate		150			Kbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}	3.5	4.4	5.3	ns	50% input to 50% output
Pulse Width Distortion	PWD	0.25	0.32	0.39	ns	|tPLH − tPHL|
Change vs. Temperature			1.5		ps/°C	
Propagation Delay Skew	t_{PSK}			0.5	ns	Between any two units at the same temperature, voltage, and load
Channel Matching						
Codirectional	t_{PSKCD}		0	0.4	ns	
Opposing Direction	t_{PSKOD}		0	0.4	ns	
Jitter		59	66	73	ps p-p	See the Jitter Measurement section
		10	11	12	ps rms	See the Jitter Measurement section
DC SPECIFICATIONS						
Input Threshold Voltage						
Logic High	V_{IH}	1.6	2.0	2.4	V	
Logic Low	V_{IL}	0.92	1.15	1.38	V	
Output Voltage						
Logic High	V_{OH}	V_{DDx} − 0.1	V_{DDx}		V	I_{Ox}[1] = −20 µA, V_{Ix} = V_{IxH}[2]
		V_{DDx} − 0.2	V_{DDx}		V	I_{Ox}[1] = −2 mA, V_{Ix} = V_{IxH}[2]
Logic Low	V_{OL}		0.0	0.01	V	I_{Ox}[1] = 20 µA, V_{Ix} = V_{IxL}[3]
			0.1	0.2	V	I_{Ox}[1] = 2 mA, V_{Ix} = V_{IxL}[3]
Input Current per Channel	I_I	−10	+0.01	+10	µA	0 V ≤ V_{Ix} ≤ V_{DDx}
Quiescent Supply Current						C_L = 0 pF
π120	$I_{DD1 (Q)}$	67	84	101	µA	V_I[4] = 0 (N0), 1 (N1)[5]
	$I_{DD2 (Q)}$	484	605	726	µA	V_I[4] = 0 (N0), 1 (N1)[5]
	$I_{DD1 (Q)}$	67	84	101	µA	V_I[4] = 1 (N0), 0 (N1)[5]

	$I_{DD2 (Q)}$	488	610	732	µA	V_I[4] = 1 (N0), 0 (N1)[5]
π121	$I_{DD1 (Q)}$	274	343	412	µA	V_I[4] = 0 (N0), 1 (N1)[5]
	$I_{DD2 (Q)}$	284	355	426	µA	V_I[4] = 0 (N0), 1 (N1)[5]
	$I_{DD1 (Q)}$	272	340	408	µA	V_I[4] = 1 (N0), 0 (N1)[5]
	$I_{DD2 (Q)}$	276	346	416	µA	V_I[4] = 1 (N0), 0 (N1)[5]
π122	$I_{DD1 (Q)}$	274	343	412	µA	V_I[4] = 0 (N0), 1 (N1)[5]
	$I_{DD2 (Q)}$	284	355	426	µA	V_I[4] = 0 (N0), 1 (N1)[5]
	$I_{DD1 (Q)}$	272	340	408	µA	V_I[4] = 1 (N0), 0 (N1)[5]
	$I_{DD2 (Q)}$	276	346	416	µA	V_I[4] = 1 (N0), 0 (N1)[5]
Dynamic Supply Current						C_L = 0 pF
Dynamic Input	$I_{DDI (D)}$	6.4	8	9.6	µA /Mbps	Inputs switching, 50% duty cycle
Dynamic Output	$I_{DDO (D)}$	42	53	64	µA /Mbps	Inputs switching, 50% duty cycle
Undervoltage Lockout	UVLO					
Positive V_{DDx} Threshold	V_{DDxUV+}	2.10	2.62	3.15	V	
Negative V_{DDx} Threshold	V_{DDxUV-}	1.94	2.42	2.91	V	
V_{DDx} Hysteresis	V_{DDxUVH}	0.15	0.19	0.23	V	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
AC SPECIFICATIONS Output						
Rise/Fall Time	t_R/t_F	0.4	0.6	0.8	ns	10% to 90%
Common-Mode Transient Immunity[6]	$\|CM_H\|$	75	100		kV/µs	$V_{Ix} = V_{DDx}$, V_{CM} = 1000 V, transient magnitude = 800 V
	$\|CM_L\|$	75	100		kV/µs	V_{Ix} = 0 V, V_{CM} = 1000 V, transient magnitude = 800 V

Notes:
[1] I_{Ox} is the Channel x output current, where x = A or B.
[2] V_{IxH} is the input side logic high voltage.
[3] V_{IxL} is the input side logic low voltage.
[4] V_I is the input voltage.
[5] N0 is the π120xx0/π121xx0/π122xx0 models, and N1 is the π120xx1/π121xx1/π122xx1 models. See the Ordering Guide.
[6] $|CM_H|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O > 0.8\ V_{DDx}$. $|CM_L|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O > 0.8$ V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

Table 4. Total Supply Current vs. Data Throughput (C_L = 0 pF)

		2 Kbps			20 Mbps			80 Mbps			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
SUPPLY CURRENT											
π120A											
Supply Current Side 1	I_{DD1}	0.06	0.08	0.10	0.18	0.23	0.28	0.52	0.66	0.80	mA
Supply Current Side 2	I_{DD2}	0.48	0.61	0.74	1.28	1.60	1.92	3.42	4.28	4.14	mA
π121A											
Supply Current Side 1	I_{DD1}	0.27	0.34	0.41	0.70	0.88	1.06	2.07	2.59	3.11	mA
Supply Current Side 2	I_{DD2}	0.28	0.35	0.42	0.75	0.94	1.13	2.23	2.79	3.35	mA
π122A											

Supply Current Side 1	I_{DD1}	0.27	0.34	0.41	0.70	0.88	1.06	2.07	2.59	3.11	mA
Supply Current Side 2	I_{DD2}	0.28	0.35	0.42	0.75	0.94	1.13	2.23	2.79	3.35	mA

		2 Kbps			1 Mbps			10 Mbps			
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
SUPPLY CURRENT											
π120M											
Supply Current Side 1	I_{DD1}	0.06	0.08	0.10	0.07	0.09	0.11	0.12	0.16	0.20	mA
Supply Current Side 2	I_{DD2}	0.48	0.61	0.74	0.52	0.66	0.8	0.87	1.09	1.31	mA
π121M											
Supply Current Side 1	I_{DD1}	0.27	0.34	0.41	0.29	0.37	0.45	0.51	0.64	0.77	mA
Supply Current Side 2	I_{DD2}	0.28	0.35	0.42	0.30	0.38	0.46	0.51	0.64	0.77	mA
π122M											
Supply Current Side 1	I_{DD1}	0.27	0.34	0.41	0.29	0.37	0.45	0.51	0.64	0.77	mA
Supply Current Side 2	I_{DD2}	0.28	0.35	0.42	0.30	0.38	0.46	0.51	0.64	0.77	mA

		2 Kbps			50 Kbps			150 Kbps			
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
SUPPLY CURRENT											
π120U											
Supply Current Side 1	I_{DD1}	67	84	101	67	84	101	68	85	102	µA
Supply Current Side 2	I_{DD2}	485	607	729	487	609	731	491	614	737	µA
π121U											
Supply Current Side 1	I_{DD1}	272	341	410	274	343	412	276	345	414	µA
Supply Current Side 2	I_{DD2}	280	351	422	282	353	424	284	356	428	µA
π122U											
Supply Current Side 1	I_{DD1}	272	341	410	274	343	412	276	345	414	µA
Supply Current Side 2	I_{DD2}	280	351	422	282	353	424	284	356	428	µA

INSULATION AND SAFETY RELATED SPECIFICATIONS

Table 5. π12xx3

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		3000	V rms	1-minute duration
Minimum External Air Gap (Clearance)	L (I01)	4.0	mm min	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L (I02)	4.0	mm min	Measured from input terminals to output terminals, shortest distance path along body
Minimum Clearance in the Plane of the Printed Circuit Board (PCB Clearance)	L (PCB)	4.5	mm min	Measured from input terminals to output terminals, shortest distance through air, line of sight, in the PCB mounting plane
Minimum Internal Gap (Internal Clearance)		7	µm min	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>400	V	DIN IEC 112/VDE 0303 Part 1

Material Group		II		Material Group (DIN VDE 0110, 1/89, Table 1)

π12xx4

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		4000	V rms	1-minute duration
Minimum External Air Gap (Clearance)	L (I01)	4.0	mm min	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L (I02)	4.0	mm min	Measured from input terminals to output terminals, shortest distance path along body
Minimum Clearance in the Plane of the Printed Circuit Board (PCB Clearance)	L (PCB)	4.5	mm min	Measured from input terminals to output terminals, shortest distance through air, line of sight, in the PCB mounting plane
Minimum Internal Gap (Internal Clearance)		7	µm min	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>400	V	DIN IEC 112/VDE 0303 Part 1
Material Group		II		Material Group (DIN VDE 0110, 1/89, Table 1)

PACKAGE CHARACTERISTICS

Table 6.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Resistance (Input to Output)[1]	R_{I-O}		10^{13}		Ω	
Capacitance (Input to Output)[1]	C_{I-O}		0.6		pF	f = 400Hz
Input Capacitance[2]	C_I		3.0		pF	
IC Junction to Ambient Thermal Resistance	θ_{JA}		80		°C/W	Thermocouple located at center of package underside

Notes:
[1]The device is considered a 2-terminal device: Pin 1 through Pin 4 are shorted together, and Pin 5 through Pin 8 are shorted together.
[2]Input capacitance is from any input data pin to ground.

REGULATORY INFORMATION

See Table 10 and the Insulation Lifetime section for details regarding recommended maximum working voltages for specific cross isolation waveforms and insulation levels.

Table7. π12xx3

UL (Pending)	CSA (Pending)	VDE (Pending)	CQC (Pending)
Recognized under UL 1577 Component Recognition Program[1]	Approved under CSA Component Acceptance Notice 5A	DIN V VDE V 0884-10 (VDE V 0884-10):2006-12[2]	Certified under CQC11-471543-2012
Single Protection, 3000 V rms Isolation Voltage	CSA 60950-1-07+A1+A2 and IEC 60950-1, second edition, +A1+A2:	Reinforced insulation, 565 V peak, V_{IOSM} = 5000 V peak	GB4943.1-2011
	Basic insulation at 400 V rms (565 V peak)		Basic insulation at 770 V rms (1089 V peak) working voltage

	Reinforced insulation at 200 V rms (283 V peak) IEC 60601-1 Edition 3.1: Basic insulation (1 MOPP), 250 V rms (354 V peak) CSA 61010-1-12 and IEC 61010-1 third edition Basic insulation at 300 V rms mains, 400 V rms (565 V peak) Reinforced insulation at 300 V rms mains, 200 V secondary (283 V peak)		Reinforced insulation at 385 V rms (545 V peak)
File (pending)	File (pending)	File (pending)	File (pending)

Notes:
[1] In accordance with UL 1577, each π120x3/π121x3/π122x3 is proof tested by applying an insulation test voltage ≥ 4500 V rms for 1 sec.
[2] In accordance with DIN V VDE V 0884-10, each π120x3/π121x3/π122x3 is proof tested by applying an insulation test voltage ≥ 1059 V peak for 1 sec (partial discharge detection limit = 5 pC). The * marking branded on the component designates DIN V VDE V 0884-10 approval.

π12xx4

UL (Pending)	CSA (Pending)	VDE (Pending)	CQC (Pending)
Recognized under UL 1577 Component Recognition Program[1]	Approved under CSA Component Acceptance Notice 5A	DIN V VDE V 0884-10 (VDE V 0884-10):2006-12[2]	Certified under CQC11-471543-2012
Single Protection, 3750 V rms Isolation Voltage	CSA 60950-1-07+A1+A2 and IEC 60950-1, second edition, +A1+A2: Basic insulation at 400 V rms (565 V peak) Reinforced insulation at 200 V rms (283 V peak) IEC 60601-1 Edition 3.1: Basic insulation (1 MOPP), 250 V rms (354 V peak) CSA 61010-1-12 and IEC 61010-1 third edition Basic insulation at 300 V rms mains, 400 V rms (565 V peak) Reinforced insulation at 300 V rms mains, 200 V secondary (283 V peak)	Reinforced insulation, 630 V peak, V_{IOSM} = 6000 V peak	GB4943.1-2011 Basic insulation at 770 V rms (1089 V peak) working voltage Reinforced insulation at 385 V rms (545 V peak)
File (pending)	File (pending)	File (pending)	File (pending)

Notes:
[3] In accordance with UL 1577, each π120x4/π121x4/π122x4 is proof tested by applying an insulation test voltage ≥ 4500 V rms for 1 sec.
[4] In accordance with DIN V VDE V 0884-10, each π120x4/π121x4/π122x4 is proof tested by applying an insulation test voltage ≥ 1059 V peak for 1 sec (partial discharge detection limit = 5 pC). The * marking branded on the component designates DIN V VDE V 0884-10 approval.

DIN V VDE V 0884-10 (VDE V 0884-10) INSULATION CHARACTERISTICS

These isolators are suitable for reinforced electrical isolation only within the safety limit data. Protective circuits ensure the maintenance of the safety data. The * marking on packages denotes DIN V VDE V 0884-10 approval.

Table 8.
π12xx3

Description	Test Conditions/Comments	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110 For				
Rated Mains Voltage ≤ 150 V rms			I to IV	
For Rated Mains Voltage ≤ 300 V rms			I to III	
For Rated Mains Voltage ≤ 400 V rms			I to III	
Climatic Classification			40/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Working Insulation Voltage		V_{IORM}	565	V peak
Input to Output Test Voltage, Method B1	$V_{IORM} \times 1.875 = V_{pd\,(m)}$, 100% production test, $t_{ini} = t_m = 1$ sec, partial discharge < 5 pC	$V_{pd\,(m)}$	1059	V peak
Input to Output Test Voltage, Method A After				
Environmental Tests Subgroup 1	$V_{IORM} \times 1.5 = V_{pd\,(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC	Vpd (m)	848	V peak
After Input and/or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{pd\,(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC		678	V peak
Highest Allowable Overvoltage		V_{IOTM}	5000	V peak
Surge Isolation Voltage Reinforced	V peak = 10 kV, 1.2 µs rise time, 50 µs, 50% fall time	V_{IOSM}	5000	V peak
Safety Limiting Values	Maximum value allowed in the event of a failure (see Figure 3)			
Maximum Junction Temperature		T_S	150	°C
Total Power Dissipation at 25°C		P_S	1.56	W
Insulation Resistance at T_S	V_{IO} = 800 V	R_S	$>10^9$	Ω

π12xx4

Description	Test Conditions/Comments	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110 For				
Rated Mains Voltage ≤ 150 V rms			I to IV	
For Rated Mains Voltage ≤ 300 V rms			I to III	
For Rated Mains Voltage ≤ 400 V rms			I to III	
Climatic Classification			40/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Working Insulation Voltage		V_{IORM}	753	V peak
Input to Output Test Voltage, Method B1	$V_{IORM} \times 1.875 = V_{pd\,(m)}$, 100% production test, $t_{ini} = t_m = 1$ sec, partial discharge < 5 pC	$V_{pd\,(m)}$	1412	V peak
Input to Output Test Voltage, Method A After				
Environmental Tests Subgroup 1	$V_{IORM} \times 1.5 = V_{pd\,(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC	Vpd (m)	1130	V peak
After Input and/or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{pd\,(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC		904	V peak
Highest Allowable Overvoltage		V_{IOTM}	6000	V peak
Surge Isolation Voltage Reinforced	V peak = 10 kV, 1.2 µs rise time, 50 µs, 50% fall time	V_{IOSM}	6000	V peak
Safety Limiting Values	Maximum value allowed in the event of a failure (see Figure 3)			
Maximum Junction Temperature		T_S	150	°C

Total Power Dissipation at 25°C		P_S	1.56	W
Insulation Resistance at T_S	V_{IO} = 800 V	R_S	$>10^9$	Ω

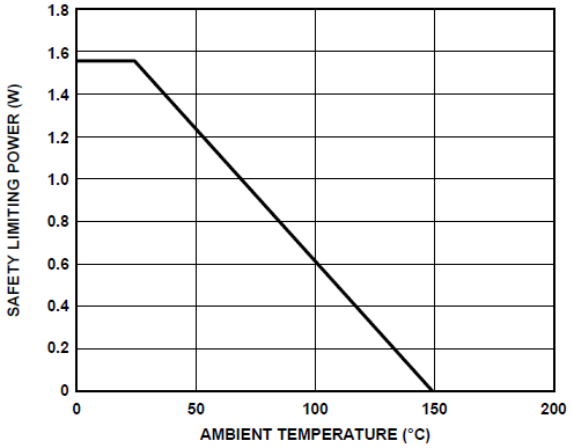


Figure3. Thermal Derating Curve, Dependence of Safety Limiting Values with Ambient Temperature per DIN V VDE V 0884-10

ABSOLUTE MAXIMUM RATINGS

T_A = 25 ℃, unless otherwise noted.

Table 9.

Parameter	Rating
Supply Voltages (V_{DD1}, V_{DD2})	−0.5 V to +7.0 V
Input Voltages (V_{IA}, V_{IB})[1]	−0.5 V to V_{DDI} + 0.5 V
Output Voltages (V_{OA}, V_{OB})[2]	−0.5 V to V_{DDO} + 0.5 V
Average Output Current per Pin[3]	
Side 1 Output Current (I_{O1})	−10 mA to +10 mA
Side 2 Output Current (I_{O2})	−10 mA to +10 mA
Common-Mode Transients[4]	−150 kV/µs to +150 kV/µs
Storage Temperature (T_{ST}) Range	−65°C to +150°C
Ambient Operating Temperature (T_A) Range	−40°C to +125°C

Notes:
[1] V_{DDI} is the input side supply voltage.
[2] V_{DDO} is the output side supply voltage.
[3] See Figure 3 for the maximum rated current values for various temperatures.
[4] Common-mode transients refer to the common-mode transients across the insulation barrier. Common-mode transients exceeding the absolute maximum ratings may cause latch-up or permanent damage.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Table 10. Maximum Continuous Working Voltage[1]

π12xx3

Parameter	Rating	Constraint[2]
AC VOLTAGE		Lifetime limited by package creepage maximum approved working voltage per IEC 60950-1
Bipolar Waveform		
Basic Insulation	789 V peak	
Reinforced Insulation	403 V peak	
Unipolar Waveform		
Basic Insulation	909 V peak	
Reinforced Insulation	469 V peak	
DC VOLTAGE		Lifetime limited by package creepage maximum approved working voltage per IEC 60950-1
Basic Insulation	800 V peak	
Reinforced Insulation	400 V peak	

π12xx4

Parameter	Rating	Constraint[2]
AC VOLTAGE		Lifetime limited by package creepage maximum approved working voltage per IEC 60950-1
Bipolar Waveform		
Basic Insulation	789 V peak	
Reinforced Insulation	403 V peak	
Unipolar Waveform		
Basic Insulation	909 V peak	
Reinforced Insulation	469 V peak	
DC VOLTAGE		Lifetime limited by package creepage maximum approved working voltage per IEC 60950-1
Basic Insulation	800 V peak	
Reinforced Insulation	400 V peak	

Notes:

[1] Maximum continuous working voltage refers to the continuous voltage magnitude imposed across the isolation barrier. See the Insulation Lifetime section for more details.

[2] Insulation lifetime for the specified test condition is greater than 50 years.

Truth Tables

Table 11. π120/π121/π122 Truth Table (Positive Logic)

V_{Ix} Input[1]	V_{DDI} State[1]	V_{DDO} State[1]	Default Low (N0), V_{Ox} Output[1,2]	Default High (N1), V_{Ox} Output[1,2]	Test Conditions/Comments
Low	Powered	Powered	Low	Low	Normal operation
High	Powered	Powered	High	High	Normal operation

Don't Care[3]	Unpowered	Powered	Low	High	Fail-safe output
Don't Care[3]	Powered	Unpowered	Indeterminate	Indeterminate	

Notes:
[1] V_{Ix} and V_{Ox} refer to the input and output signals of a given channel (A or B). V_{DDI} and V_{DDO} refer to the supply voltages on the input and output sides of the given channel, respectively.
[2] N0 is the π120xx0/π121xx0/π122xx0 models; N1 is the π120xx1/π121xx1/π122xx1 models. See the Ordering Guide.
[3] Input pins (V_{Ix}) on the same side as an unpowered supply must be in a low state to avoid powering the device through its ESD protection circuitry.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

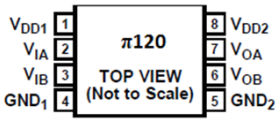


Figure4. π120 Pin Configuration

π120 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1}	Supply Voltage for Isolator Side 1.
2	V_{IA}	Logic Input A.
3	V_{IB}	Logic Input B.
4	GND_1	Ground 1. This pin is the ground reference for Isolator Side 1.
5	GND_2	Ground 2. This pin is the ground reference for Isolator Side 2.
6	V_{OB}	Logic Output B.
7	V_{OA}	Logic Output A.
8	V_{DD2}	Supply Voltage for Isolator Side 2.

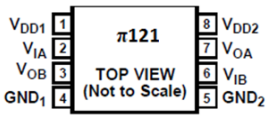


Figure5. π121 Pin Configuration

π121 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1}	Supply Voltage for Isolator Side 1.
2	V_{IA}	Logic Input A.
3	V_{OB}	Logic Output B.
4	GND_1	Ground 1. This pin is the ground reference for Isolator Side 1.
5	GND_2	Ground 2. This pin is the ground reference for Isolator Side 2.
6	V_{IB}	Logic Input B.
7	V_{OA}	Logic Output A.
8	V_{DD2}	Supply Voltage for Isolator Side 2.

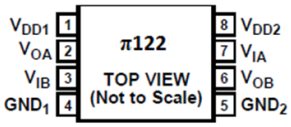


Figure6. π122 Pin Configuration

π122 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1}	Supply Voltage for Isolator Side 1.
2	V_{OA}	Logic Output A.
3	V_{IB}	Logic Input B.
4	GND_1	Ground 1. This pin is the ground reference for Isolator Side 1.
5	GND_2	Ground 2. This pin is the ground reference for Isolator Side 2.
6	V_{OB}	Logic Output B.
7	V_{IA}	Logic Input A.
8	V_{DD2}	Supply Voltage for Isolator Side 2.

APPLICATIONS INFORMATION

OVERVIEW

The π120/π121/π122 transmit data across an isolation barrier by layers of silicon oxide isolation.

The π120/π121/π122 have very low propagation delay and high speed. The input/output design techniques allow logic and supply voltages over a wide range from 3.0 V to 5.5 V, offering voltage translation of 3.3 V, and 5 V logic. The architecture is designed for high common-mode transient immunity and high immunity to electrical noise and magnetic interference.

See the Ordering Guide for the model numbers that have the fail-safe output state of low or the fail-safe output state of high.

PCB LAYOUT

The π120/π121/π122 digital isolators require no external interface circuitry for the logic interfaces. Power supply bypassing is strongly recommended at the input and output supply pins (see Figure 7). Bypass capacitors are most conveniently connected between Pin 1 and Pin 4 for V_{DD1} and between Pin 5 and Pin 8 for V_{DD2}. The recommended bypass capacitor value is between 0.01 µF and 0.1 µF. The total lead length between both ends of the capacitor and the input power supply pin must not exceed 10 mm.

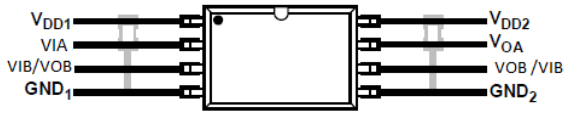


Figure7.Recommended Printed Circuit Board Layout

In applications involving high common-mode transients, ensure that board coupling across the isolation barrier is minimized. Furthermore, design the board layout such that any coupling that does occur equally affects all pins on a given component side. Failure to ensure this can cause voltage differentials between pins exceeding the Absolute Maximum Ratings of the device, thereby leading to latch-up or permanent damage.

PROPAGATION DELAY RELATED PARAMETERS

Propagation delay is a parameter that describes the time it takes a logic signal to propagate through a component. The propagation delay to a Logic 0 output may differ from the propagation delay to a Logic 1 output.

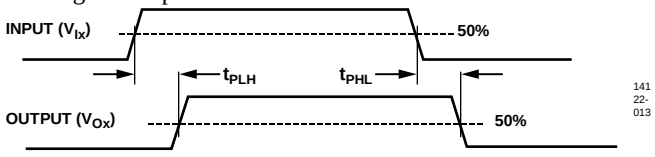


Figure 8. Propagation Delay Parameters

Pulse width distortion is the maximum difference between these two propagation delay values and is an indication of how accurately the timing of the input signal is preserved.

Channel matching is the maximum amount the propagation delay differs between channels within a single π120/π121/π122 component.

Propagation delay skew is the maximum amount the propagation delay differs between multiple π120/π121/π122 components operating under the same conditions.

JITTER MEASUREMENT

Figure 9 shows the eye diagram for the π120/π121/π122. The measurement was taken using an Keysight 81160A pulse pattern generator at 150 Mbps with pseudorandom bit sequences (PRBS) 2(n − 1), n = 14, for 5 V supplies. Jitter was measured with the Keysight DSOS104A oscilloscope, 1 GHz, 20 GS/s with the DPOJET jitter and eye diagram analysis tools. The result shows a typical measurement on the π120/π121/π122 with 47 ps p-p jitter.

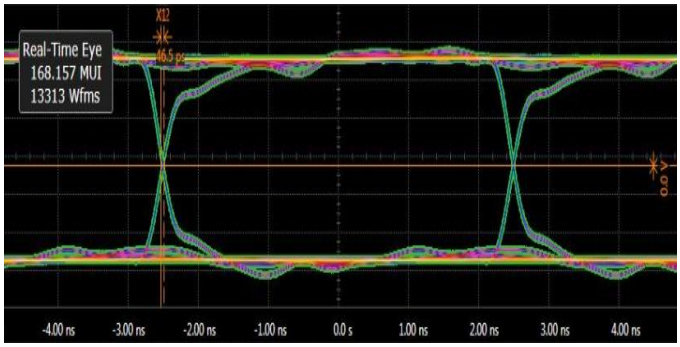


Figure9. π120/π121/π122 Eye Diagram

INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation as well as on the materials and material interfaces.

The two types of insulation degradation of primary interest are breakdown along surfaces exposed to the air and insulation wear out. Surface breakdown is the phenomenon of surface tracking and the primary determinant of surface creepage requirements in system level standards. Insulation wear out is the phenomenon where charge injection or displacement currents inside the insulation material cause long-term insulation degradation.

Surface Tracking

Surface tracking is addressed in electrical safety standards by setting a minimum surface creepage based on the working voltage, the environmental conditions, and the properties of the insulation material. Safety agencies perform characterization testing on the surface insulation of components that allows the components to be categorized in different material groups. Lower material group ratings are more resistant to surface tracking and,

therefore, can provide adequate lifetime with smaller creepage. The minimum creepage for a given working voltage and material group is in each system level standard and is based on the total rms voltage across the isolation, pollution degree, and material group. The material group and creepage for the π120/π121/π122 isolators are presented in Table 5.

Insulation Wear Out

The lifetime of insulation caused by wear out is determined by its thickness, material properties, and the voltage stress applied. It is important to verify that the product lifetime is adequate at the application working voltage. The working voltage supported by an isolator for wear out may not be the same as the working voltage supported for tracking. It is the working voltage applicable to tracking that is specified in most standards.

Testing and modeling show that the primary driver of long term degradation is displacement current in the silicon oxide insulation causing incremental damage. The stress on the insulation can be broken down into broad categories, such as dc stress, which causes very little wear out because there is no displacement current, and an ac component time varying voltage stress, which causes wear out.

The ratings in certification documents are usually based on 60 Hz sinusoidal stress because this reflects isolation from line voltage. However, many practical applications have combintions of 60 Hz ac and dc across the barrier as shown in Equation 1. Because only the ac portion of the stress causes wear out, the equation can be rearranged to solve for the ac rms voltage, as is shown in Equation 2. For insulation wear out with the silicon oxide materials used in these products, the ac rms voltage determines the product lifetime.

$$V_{RMS} = \sqrt{V_{AC\ RMS}{}^2 + V_{DC}{}^2} \quad (1)$$

or

$$V_{AC\ RMS} = \sqrt{V_{RMS}{}^2 - V_{DC}{}^2} \quad (2)$$

where:

V_{RMS} is the total rms working voltage.

$V_{AC\ RMS}$ is the time varying portion of the working voltage.

V_{DC} is the dc offset of the working voltage.

Calculation and Use of Parameters Example

The following example frequently arises in power conversion applications. Assume that the line voltage on one side of the isolation is 240 $V_{AC\ RMS}$ and a 400 V_{DC} bus voltage is present on the other side of the isolation barrier. The isolator material is polyimide. To establish the critical voltages in determining the creepage, clearance, and lifetime of a device, see Figure 10 and the following equations.

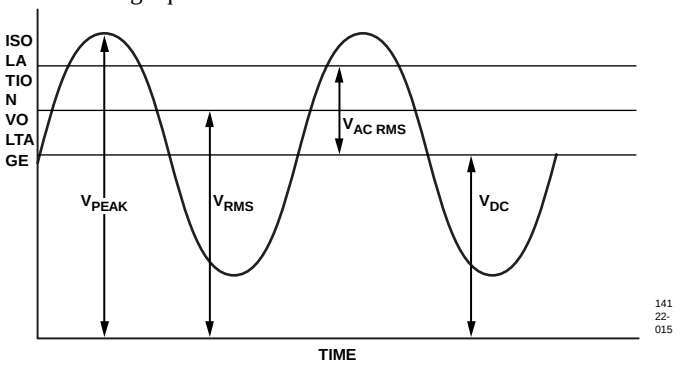


Figure10. Critical Voltage Example

The working voltage across the barrier from Equation 1 is

$$V_{RMS} = \sqrt{V_{AC\ RMS}{}^2 + V_{DC}{}^2}$$

$$V_{RMS} = \sqrt{240^2 + 400^2}$$

$$V_{RMS} = 466\ \text{V}$$

This is the working voltage used together with the material group and pollution degree when looking up the creepage required by a system standard.

To determine if the lifetime is adequate, obtain the time varying portion of the working voltage. To obtain the ac rms voltage, use Equation 2.

$$V_{AC\ RMS} = \sqrt{V_{RMS}{}^2 - V_{DC}{}^2}$$

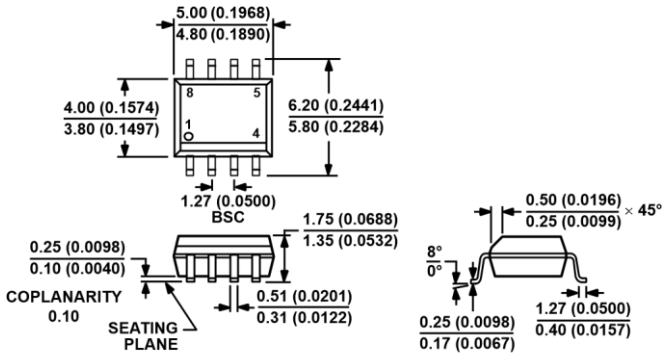
$$V_{AC\ RMS} = \sqrt{466^2 - 400^2}$$

$$V_{AC\ RMS} = 240\ \text{V rms}$$

In this case, the ac rms voltage is simply the line voltage of 240 V rms. This calculation is more relevant when the waveform is not sinusoidal. The value is compared to the limits for working voltage in Table 10 for the expected lifetime, less than a 60 Hz sine wave, and it is well within the limit for a 50-year service life.

Note that the dc working voltage limit in Table 10 is set by the creepage of the package as specified in IEC 60664-1. This value can differ for specific system level standards.

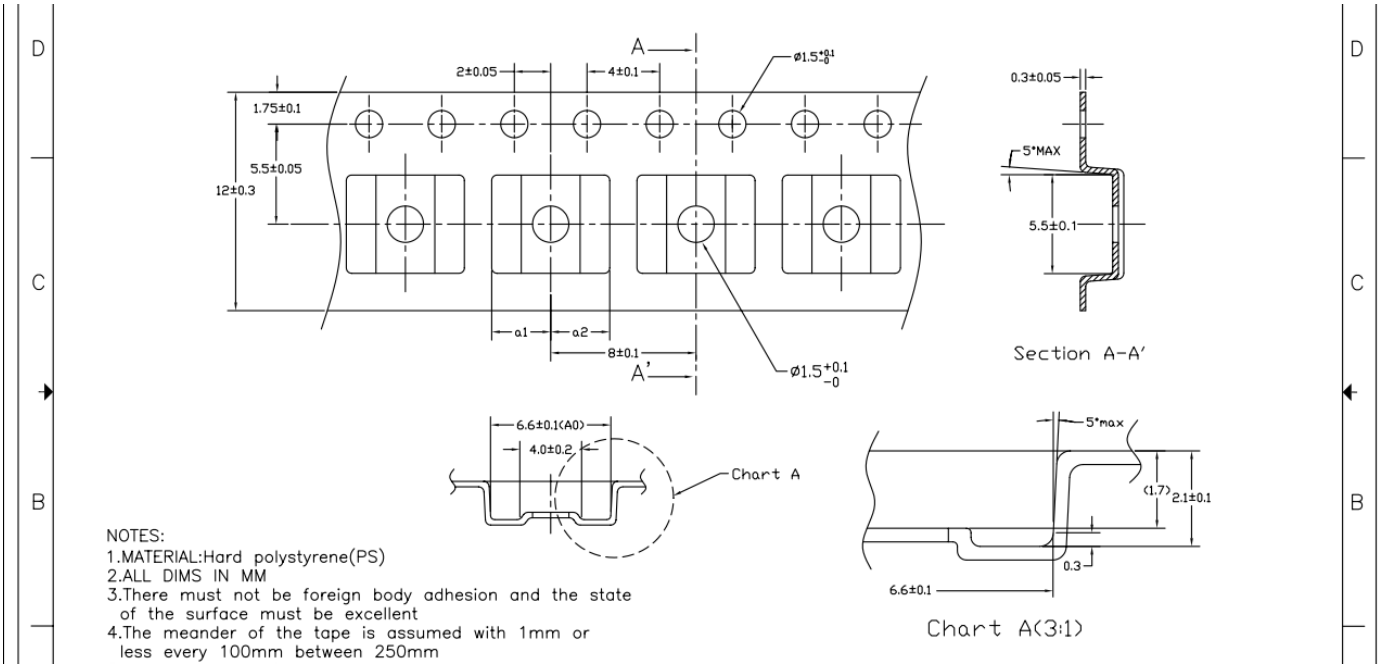
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure11. 8-Lead Standard Small Outline Package [SOIC_N]
N/Arrow Body (S-8-N)
Dimensions shown in millimeters and (inches)

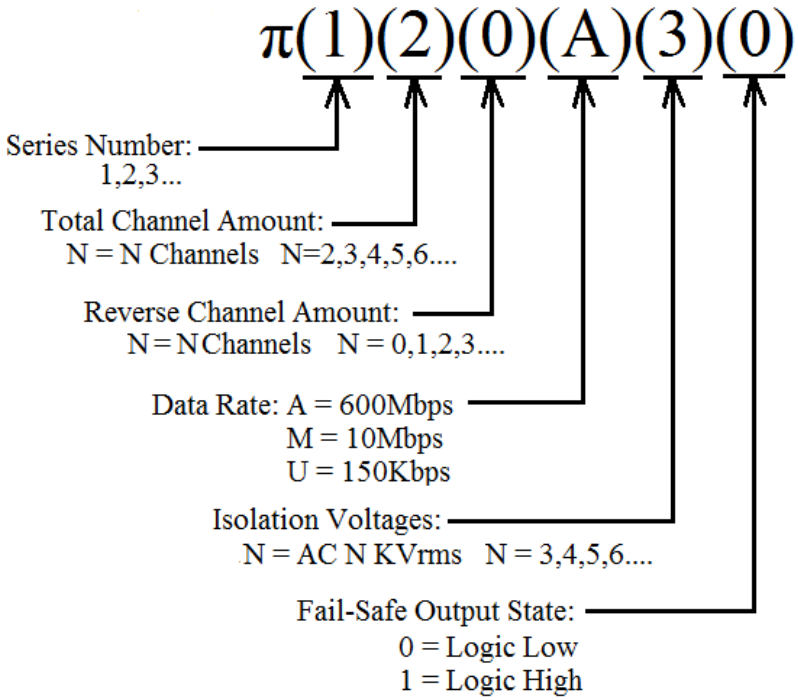
REEL INFORMATION



ORDERING GUIDE

Model	Temperature Range	No. of Inputs, V_{DD1} Side	No. of Inputs, V_{DD2} Side	Withstand Voltage Rating (kV rms)	Fail-Safe Output State	Package Description	Package Option	Quantity
π120A41	−40°C to +125°C	2	0	3.75	High	8-Lead SOIC_N	S-8-N	2500 per reel
π120A40	−40°C to +125°C	2	0	3.75	Low	8-Lead SOIC_N	S-8-N	2500 per reel
π121A41	−40°C to +125°C	1	1	3.75	High	8-Lead SOIC_N	S-8-N	2500 per reel
π121A40	−40°C to +125°C	1	1	3.75	Low	8-Lead SOIC_N	S-8-N	2500 per reel
π122A41	−40°C to +125°C	1	1	3.75	High	8-Lead SOIC_N	S-8-N	2500 per reel
π122A40	−40°C to +125°C	1	1	3.75	Low	8-Lead SOIC_N	S-8-N	2500 per reel

Part number named rule:



For product information and a complete list of distributors, please contact us:

2Pai Semiconductor Co., Limited
Telephone：021-50850681
Mobile phone：13925282158
Room 307, Building No 19, No.498, GuoShouJin Road, Pudong New District, Shanghai, China