

TPS74401 具有可编程软启动功能的 3.0A Ultra-LDO

1 特性

- 输入电压范围：1.1V 至 5.5V
- 软启动 (SS) 引脚可借助由外部电容器设置的斜坡时间实现线性启动
- 线路、负载和温度上精度 1%
- 借助外部偏置电源可支持低至 0.9V 的输入电压
- 可调节输出电压范围：0.8V 至 3.6V
- 超低压降：3.0A 时为 115mV（典型值）
- 搭配使用任意输出电容或不使用输出电容时均可保持稳定
- 出色的瞬态响应
- 漏极开路电源正常输出（仅限 VQFN）
- 封装：5mm × 5mm × 1mm VQFN (RGW)，3.5mm × 3.5mm VQFN (RGR) 和 DDPK

2 应用

- FPGA 应用
- DSP 内核以及 I/O 电压
- 后置稳压 应用
- 具有特殊的 启动时间或排序要求的应用
- 热插拔和浪涌控制

3 说明

TPS74401 低压降 (LDO) 线性稳压器提供了一套面向多种应用的易用稳健型电源管理 解决方案。用户可编程的软启动功能可降低器件启动时的电容浪涌电流，从而以最大限度减小输入电源的应力。软启动具有单调性，非常适合为各类处理器和专用集成电路 (ASIC) 供电。借助使能输入和电源正常输出，可通过外部稳压器轻松实现上电排序。凭借全方位的灵活性，用户可为现场可编程门阵列 (FPGA)、数字信号处理器 (DSP) 等具有特殊启动要求的应用配置出一套可满足其 排序要求的 解决方案。

该器件还具有高精度的参考电压电路和误差放大器，可在整个负载、线路、温度和过程范围内提供 1% 精度。TPS74401 系列 LDO 在不使用输出电容或搭配使用陶瓷输出电容时都可以稳定运行。该器件系列的额定工作温度范围为 $T_J = -40^{\circ}\text{C}$ 至 125°C 。TPS74401 可提供两种 20 引脚小型 VQFN 封装（一个 5mm × 5mm RGW 和一个

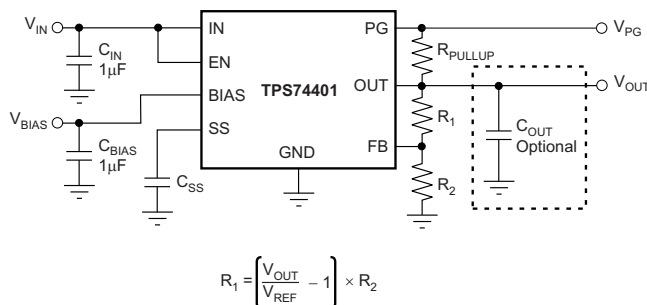
3.5mm × 3.5mm RGR 封装），因此总体解决方案尺寸高度紧凑。对于 要求 额外功率耗散的应用，还提供了 DDPK (KTV) 封装。

器件信息⁽¹⁾

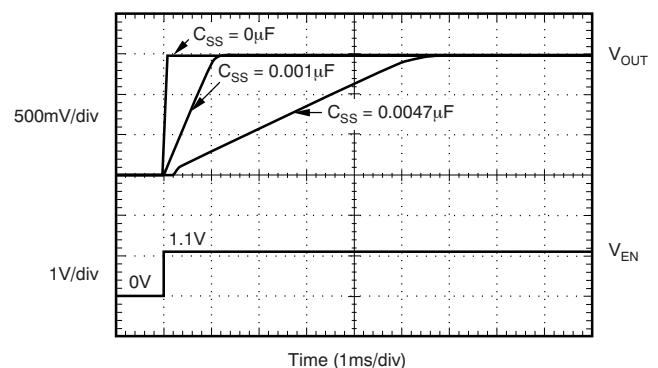
器件型号	封装	封装尺寸（标称值）
TPS74401	TO-263 (7)	10.10mm x 8.89mm
	VQFN, RGW (20)	5.00mm x 5.00mm
	VQFN, RGR (20)	3.50mm x 3.50mm

(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。

典型应用电路



导通响应



目录

1	特性	1	8	Application and Implementation	18
2	应用	1	8.1	Application Information	18
3	说明	1	8.2	Typical Applications	20
4	修订历史记录	2	9	Power Supply Recommendations	24
5	Pin Configuration and Functions	5	10	Layout	25
6	Specifications	6	10.1	Layout Guidelines	25
6.1	Absolute Maximum Ratings	6	10.2	Layout Example	25
6.2	ESD Ratings	6	10.3	Power Dissipation	25
6.3	Recommended Operating Conditions	6	10.4	Thermal Considerations	26
6.4	Thermal Information	7	11	器件和文档支持	29
6.5	Electrical Characteristics	7	11.1	器件支持	29
6.6	Timing Requirements	8	11.2	文档支持	29
6.7	Typical Characteristics	9	11.3	接收文档更新通知	29
7	Detailed Description	14	11.4	社区资源	29
7.1	Overview	14	11.5	商标	29
7.2	Functional Block Diagram	14	11.6	静电放电警告	29
7.3	Feature Description	14	11.7	Glossary	29
7.4	Device Functional Modes	15	12	机械、封装和可订购信息	30
7.5	Programming	16			

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision Q (April 2015) to Revision R	Page
• 已添加 在文档中增加了 RGR 封装	1
• 已更改 通篇将 TPS744xx 更改为 TPS74401	1
• 已更改 封装 特性 要点	1
• 已更改 对 说明 部分的第二段进行了更改：增加了 RGR 封装，更改了第二句到最后一句	1
• 已删除 典型应用电路方框图的固定电压版本	1
• Added RGR package to <i>Pin Configuration and Functions</i> section	5
• Changed FB/SNS to FB in both pin out drawings, deleted TPS744xx from VQFN package	5
• Changed <i>Surface Mount</i> to <i>Top View</i> in KTW pin out drawing	5
• Changed <i>input capacitor</i> to <i>bias capacitor</i> in BIAS pin description	5
• Deleted (<i>adjustable version only</i>) from description of FB pin in <i>Pin Functions</i> table	5
• Changed I/O column value to — from O for NC pins of <i>Pin Functions</i> table	5
• Deleted SNS pin from <i>Pin Functions</i> table	5
• Added RGR package to <i>Thermal Information</i> table	7
• Deleted (<i>adjustable version</i>) from V_{REF} parameter name in <i>Electrical Characteristics</i> table	7
• Deleted SNS pin reference from I_{FB} , I_{SNS} parameter: changed symbol from I_{FB} , I_{SNS} to I_{FB} , deleted <i>sense</i> from parameter name	7
• Deleted <i>adjustable</i> from footnote 1 and deleted I_{SNS} from footnote 4 of <i>Electrical Characteristics</i> table	7
• Changed conditions of R_1 , R_2 in <i>Noise Spectral Density</i> figure	11
• Deleted <i>Fixed Voltage Versions</i> figure from <i>Functional Block Diagram</i> section	14
• Changed first paragraph of <i>Application Information</i> section: deleted <i>and tracking capabilities</i> from first sentence and changed <i>very low input and output voltages</i> to <i>very low output voltages with low V_{IN} to V_{OUT} headroom</i> in last sentence	18
• Changed title of first typical application from <i>Adjustable Voltage Part and Setting</i> to <i>Setting the TPS74401</i>	20
• Deleted reference to adjustable version in first sentence and <i>Typical Application Circuit for the TPS74401</i> figure in first typical application section	20
• Changed <i>Because $V_{IN} \geq V_{OUT} + 1.62\text{ V}$</i> to <i>Because V_{IN} is less than V_{OUT} plus the V_{BIAS} dropout and $V_{BIAS} = V_{IN}$</i> to	

修订历史记录 (接下页)

$V_{BIAS} = V_{OUT}$ in last paragraph of <i>Detailed Design Procedure</i> in first typical application section	21
• Deleted <i>Fixed Voltage and Sense Pin</i> section	23
• Deleted BIAS recommendation from <i>Layout Guidelines</i> section.....	25
• Changed <i>RGW Package</i> to <i>VQFN Packages</i> in caption of <i>Layout Schematic</i> figure.....	25
• Added RGR package to VQFN description in <i>Power Dissipation</i> section.....	26
• Added RGR package to <i>Thermal Considerations</i> section	27

Changes from Revision P (January 2015) to Revision Q	Page
• 通篇将 QFN 更改为 VQFN	1
• 通篇将 TPS744xx 更改为 TPS74401	1
• 删除了固定输出电压 特性 要点	1
• Changed V_{BIAS} minimum value in <i>Recommended Operating Conditions</i> table.....	6
• Changed footnote 1 for <i>Recommended Operating Conditions</i> table.....	6
• Added second row to V_{OUT} accuracy parameter	7
• Added last four rows to V_{DO} , V_{BIAS} dropout voltage parameter	7
• Added <i>Timing Requirements</i> table	8
• Added <i>Device Functional Modes</i> section	15
• Changed third paragraph of <i>Dropout Voltage</i>	19
• Changed first sentence of <i>Without an Auxiliary Bias</i> section	24
• Changed <i>Power Dissipation</i> section location; moved to after <i>Layout Example</i> section.....	25
• 已添加 开发支持 部分	29
• 已添加 相关文档部分增加了有关参考设计 TIDU421 和用户指南 SLVU143 的信息	29

Changes from Revision O (March 2013) to Revision P	Page
• 已删除 特性列表中的高电平有效使能项目	1
• Added <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section	6
• Changed footnote 3c for <i>Thermal Information</i> table	7
• Changed y-axis in Figure 1 , Figure 2 , Figure 4 , and Figure 7 from abbreviation (I_{OUT}) to text (Output Current)	9
• Added "V" to $V_{IN} = 1.8$ V condition in Figure 9 , Figure 10 , and Figure 11	9
• y-axis and graph title in Figure 15 from abbreviation (I_{OUT}) to text (Output Current)	10
• Changed Figure 25 ; made V_{OUT} trace red to show data trend separation	12
• Changed <i>Overview</i> section text.....	14
• Changed second paragraph of <i>Dropout Voltage</i>	19
• Changed Figure 27 ; updated equation in figure	20

Changes from Revision N (December 2012) to Revision O	Page
• Changed RGW and KTW values in Thermal Information table.....	7

Changes from Revision M (November 2010) to Revision N	Page
• Changed T_J max value from 125 to 150 in Absolute Maximum Ratings table	6

Changes from Revision L (August, 2010) to Revision M
Page

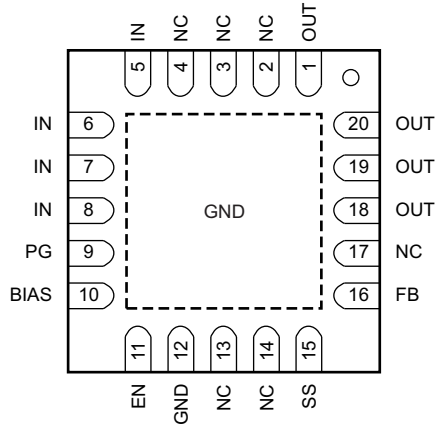
-
- Corrected equation for [Table 2](#) [17](#)
-

Changes from Revision K (December, 2009) to Revision L
Page

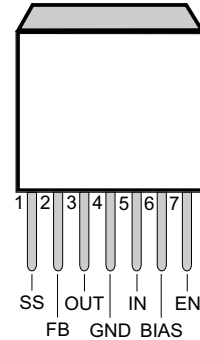
-
- Replaced the *Dissipation Ratings* table with the *Thermal Information* table [7](#)
 - Revised *Layout Recommendations and Power Dissipation* section [25](#)
 - Revised [Thermal Considerations](#) section [26](#)
-

5 Pin Configuration and Functions

RGW, RGR Package
5-mm × 5-mm and 3.5-mm × 3.5-mm, 20-Pin VQFN
Top View



KTW Package
7-Pin DDPAK
Top View



Pin Functions

NAME	PIN		I/O	DESCRIPTION
	KTW	RGW, RGR		
BIAS	6	10	I	Bias input voltage for error amplifier, reference, and internal control circuits. A 1- μ F or larger bias capacitor is recommended for optimal performance. If IN is connected to BIAS, use a 4.7 μ F or larger capacitor.
EN	7	11	I	Enable pin. Driving this pin high enables the regulator. Driving this pin low puts the regulator into shutdown mode. This pin must not be left floating.
FB	2	16	I	This pin is the feedback connection to the center tap of an external resistor divider network that sets the output voltage. This pin must not be left floating.
GND	4	12	—	Ground
IN	5	5–8	I	Unregulated input to the device. An input capacitor of 1 μ F or greater is recommended for optimal performance.
NC	N/A	2–4, 13, 14, 17	—	No connection. This pin can be left floating or connected to GND to allow better thermal contact to the top-side plane.
OUT	3	1, 18–20	O	Regulated output voltage. No capacitor is required on this pin for stability, but is recommended for optimal performance.
PAD/TAB	—	—	—	Must be soldered to the ground plane for increased thermal performance. Internally connected to ground.
PG	N/A	9	O	Power-good (PG) is an open-drain, active-high output that indicates the status of V_{OUT} . When V_{OUT} exceeds the PG trip threshold, the PG pin goes into a high-impedance state. When V_{OUT} is below this threshold, the pin is driven to a low-impedance state. Connect a pullup resistor from 10 k Ω to 1 M Ω from this pin to a supply up to 5.5 V. The supply can be higher than the input voltage. Alternatively, the PG pin can be left floating if output monitoring is not necessary.
SS	1	15	—	Soft-start pin. A capacitor connected on this pin to ground sets the start-up time. If this pin is left floating, the regulator output soft-start ramp time is typically 100 μ s.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V_{IN}, V_{BIAS}	Input voltage	-0.3	6	V
V_{EN}	Enable voltage	-0.3	6	V
V_{PG}	Power-good voltage	-0.3	6	V
I_{PG}	PG sink current	0	1.5	mA
V_{SS}	SS pin voltage	-0.3	6	V
V_{FB}	Feedback pin voltage	-0.3	6	V
V_{OUT}	Output voltage	-0.3	$V_{IN} + 0.3$	V
I_{OUT}	Maximum output current	Internally limited		
	Output short-circuit duration	Indefinite		
P_{DISS}	Continuous total power dissipation	See Thermal Information		
T_J	Operating junction temperature	-40	150	°C
T_{stg}	Storage temperature	-55	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000
		Charged device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±500

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input supply voltage range	1.1		5.5	V
V_{EN}	Enable supply voltage range	0		5.5	V
$V_{BIAS}^{(1)}$	BIAS supply voltage range	$V_{OUT} + V_{DO} (V_{BIAS})$		5.5	V
I_{OUT}	Output current	0		3	A
C_{OUT}	Output capacitor	0			μF
$C_{IN}^{(2)}$	Input capacitor	1			μF
C_{BIAS}	Bias capacitor	1			μF
T_J	Operating junction temperature	-40		125	°C

- (1) BIAS supply is required when V_{IN} is below $V_{OUT} + V_{DO} (V_{BIAS})$.

- (2) If V_{IN} and V_{BIAS} are connected to the same supply, the recommended minimum capacitor for the supply is 4.7 μF.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾⁽²⁾		TPS74401 ⁽³⁾			UNIT
		RGW (VQFN)	RGR (VQFN)	KTW (DDPAK)	
		20 PINS	20 PINS	7 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	35.4	39.1	26.6	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	32.4	29.3	41.7	°C/W
R _{θJB}	Junction-to-board thermal resistance	14.7	10.2	12.5	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	0.4	0.4	4.0	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	14.8	10.1	7.3	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	3.9	2.0	0.3	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.
- (2) For thermal estimates of this device based on PCB copper area, see the [TI PCB Thermal Calculator](#).
- (3) Thermal data for the RGW, RGR, and KTW packages are derived by thermal simulations based on JEDEC-standard methodology as specified in the JESD51 series. The following assumptions are used in the simulations:
 - (a) i. RGW and RGR: The exposed pad is connected to the PCB ground layer through a 4x4 thermal via array.
 - ii. KTW: The exposed pad is connected to the PCB ground layer through a 6x6 thermal via array.
 - (b) Each of top and bottom copper layers has a dedicated pattern for 20% copper coverage.
 - (c) These data were generated with only a single device at the center of a JEDEC high-K (2s2p) board with 3in x 3in copper area. To understand the effects of the copper area on thermal performance, refer to the [Thermal Considerations](#) section.

6.5 Electrical Characteristics

At $V_{EN} = 1.1\text{ V}$, $V_{IN} = V_{OUT} + 0.3\text{ V}$, $C_{IN} = C_{BIAS} = 0.1\text{ }\mu\text{F}$, $C_{OUT} = 10\text{ }\mu\text{F}$, $I_{OUT} = 50\text{ mA}$, $V_{BIAS} = 5.0\text{ V}$, and $T_J = -40^\circ\text{C}$ to 125°C , unless otherwise noted. Typical values are at $T_J = 25^\circ\text{C}$.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range		$V_{OUT} + V_{DO}$		5.5	V
V_{BIAS}	Bias pin voltage range		2.375		5.25	V
V_{REF}	Internal reference	$T_J = 25^\circ\text{C}$	0.796	0.8	0.804	V
V_{OUT}	Output voltage range	$V_{IN} = 5\text{ V}$, $I_{OUT} = 1.5\text{ A}$, $V_{BIAS} = 5\text{ V}$	V_{REF}		3.6	V
	Accuracy	$2.97\text{ V} \leq V_{BIAS} \leq 5.25\text{ V}$, $V_{OUT} + 1.62\text{ V} \leq V_{BIAS}$, $50\text{ mA} \leq I_{OUT} \leq 3.0\text{ A}$ ⁽¹⁾	-1%	±0.2%	1%	
		$V_{OUT} + V_{DO}$, $BIAS \leq V_{BIAS} \leq 5.25\text{ V}$, $100\text{ mA} \leq I_{OUT} \leq I_{VDO, BIAS}$, VQFN ⁽²⁾	-1%	±0.2%	1%	
$\Delta V_{OUT(\Delta V_{IN})}$		Line regulation				% / V
		$V_{OUT(nom)} + 0.3 \leq V_{IN} \leq 5.5\text{ V}$, VQFN		0.0005	0.05	
		$V_{OUT(nom)} + 0.3 \leq V_{IN} \leq 5.5\text{ V}$, DDPAK		0.0005	0.06	
$\Delta V_{OUT(\Delta I_{OUT})}$		Load regulation				% / mA
		$0\text{ mA} \leq I_{OUT} \leq 50\text{ mA}$		0.013		
		$50\text{ mA} \leq I_{OUT} \leq 3.0\text{ A}$		0.03		% / A
V_{DO}	V_{IN} dropout voltage ⁽³⁾	$I_{OUT} = 3.0\text{ A}$, $V_{BIAS} - V_{OUT(nom)} \geq 1.62\text{ V}$, VQFN		115	195	mV
		$I_{OUT} = 3.0\text{ A}$, $V_{BIAS} - V_{OUT(nom)} \geq 1.62\text{ V}$, DDPAK		120	240	
	V_{BIAS} dropout voltage ⁽³⁾	$I_{OUT} = 3.0\text{ A}$, $V_{IN} = V_{BIAS}$			1.62	V
		$I_{OUT} = 3.0\text{ A}$			1.62	
		$I_{OUT} = 1.0\text{ A}$			1.35	
		$I_{OUT} = 500\text{ mA}$			1.27	
		$I_{OUT} = 100\text{ mA}$			1.16	
I_{CL}	Current limit	$V_{OUT} = 80\% \times V_{OUT(nom)}$, VQFN	3.8		6.0	A
		$V_{OUT} = 80\% \times V_{OUT(nom)}$, DDPAK	3.5		6.0	
I_{BIAS}	Bias pin current	$I_{OUT} = 0\text{ mA}$ to 3.0 A		2	4	mA
I_{SHDN}	Shutdown supply current (V_{IN})	$V_{EN} \leq 0.4\text{ V}$		1	100	μA
I_{FB}	Feedback pin current ⁽⁴⁾	$I_{OUT} = 50\text{ mA}$ to 3.0 A	-250	95	250	nA

- (1) Devices tested at 0.8 V; external resistor tolerance is not taken into account.
- (2) V_{OUT} is set to 1.5 V to avoid minimum V_{BIAS} restrictions.
- (3) Dropout is defined as the voltage from the input to V_{OUT} when V_{OUT} is 2% below nominal.
- (4) I_{FB} current flow is out of the device.

Electrical Characteristics (continued)

At $V_{EN} = 1.1\text{ V}$, $V_{IN} = V_{OUT} + 0.3\text{ V}$, $C_{IN} = C_{BIAS} = 0.1\text{ }\mu\text{F}$, $C_{OUT} = 10\text{ }\mu\text{F}$, $I_{OUT} = 50\text{ mA}$, $V_{BIAS} = 5.0\text{ V}$, and $T_J = -40^\circ\text{C}$ to 125°C , unless otherwise noted. Typical values are at $T_J = 25^\circ\text{C}$.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PSRR ⁽⁵⁾	Power-supply rejection (V_{IN} to V_{OUT})	1 kHz, $I_{OUT} = 1.5\text{ A}$, $V_{IN} = 1.8\text{ V}$, $V_{OUT} = 1.5\text{ V}$		73		dB
		800 kHz, $I_{OUT} = 1.5\text{ A}$, $V_{IN} = 1.8\text{ V}$, $V_{OUT} = 1.5\text{ V}$		42		
	Power-supply rejection (V_{BIAS} to V_{OUT})	1 kHz, $I_{OUT} = 1.5\text{ A}$, $V_{IN} = 1.8\text{ V}$, $V_{OUT} = 1.5\text{ V}$		62		dB
		800 kHz, $I_{OUT} = 1.5\text{ A}$, $V_{IN} = 1.8\text{ V}$, $V_{OUT} = 1.5\text{ V}$		50		
V_n	Output noise voltage	100 Hz to 100 kHz, $I_{OUT} = 1.5\text{ A}$, $C_{SS} = 0.001\text{ }\mu\text{F}$		$16 \times V_{OUT}$		μV_{RMS}
V_{TRAN}	% V_{OUT} droop during load transient	$I_{OUT} = 100\text{ mA}$ to 3.0 A at $1\text{ A}/\mu\text{s}$, $C_{OUT} = 0\text{ }\mu\text{F}$		4		% V_{OUT}
I_{SS}	Soft-start charging current	$V_{SS} = 0.4\text{ V}$	0.5	0.73	1	μA
$V_{EN(high)}$	Enable input high level		1.1		5.5	V
$V_{EN(low)}$	Enable input low level		0		0.4	V
$V_{EN(hys)}$	Enable pin hysteresis			50		mV
I_{EN}	Enable pin current	$V_{EN} = 5\text{ V}$		0.1	1	μA
V_{IT}	PG trip threshold	V_{OUT} decreasing	86.5	90	93.5	% V_{OUT}
V_{HYS}	PG trip hysteresis			3		% V_{OUT}
$V_{PG(low)}$	PG output low voltage	$I_{PG} = 1\text{ mA}$ (sinking), $V_{OUT} < V_{IT}$			0.3	V
$I_{PG(lkg)}$	PG leakage current	$V_{PG} = 5.25\text{ V}$, $V_{OUT} > V_{IT}$		0.03	1	μA
T_J	Operating junction temperature		-40		125	$^\circ\text{C}$
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing		155		$^\circ\text{C}$
		Reset, temperature decreasing		140		

(5) See Figure 8 to Figure 11 for PSRR at different conditions.

6.6 Timing Requirements

At $V_{EN} = 1.1\text{ V}$, $V_{IN} = V_{OUT} + 0.3\text{ V}$, $C_{IN} = C_{BIAS} = 0.1\text{ }\mu\text{F}$, $C_{OUT} = 10\text{ }\mu\text{F}$, $I_{OUT} = 50\text{ mA}$, $V_{BIAS} = 5.0\text{ V}$, and $T_J = -40^\circ\text{C}$ to 125°C , unless otherwise noted. Typical values are at $T_J = 25^\circ\text{C}$.

		MIN	NOM	MAX	UNIT
t_{STR}	Minimum startup time ($I_{OUT} = 1.5\text{ A}$, $C_{SS} = \text{open}$)		100		μs
$V_{EN(dg)}$	Enable pin de-glitch time		20		μs

6.7 Typical Characteristics

At $T_J = 25^\circ\text{C}$, $V_{OUT} = 1.5\text{ V}$, $V_{IN} = V_{OUT(nom)} + 0.3\text{ V}$, $V_{BIAS} = 3.3\text{ V}$, $I_{OUT} = 50\text{ mA}$, $C_{IN} = 1\text{ }\mu\text{F}$, $C_{BIAS} = 1\text{ }\mu\text{F}$, $C_{SS} = 0.01\text{ }\mu\text{F}$, and $C_{OUT} = 10\text{ }\mu\text{F}$, unless otherwise noted.

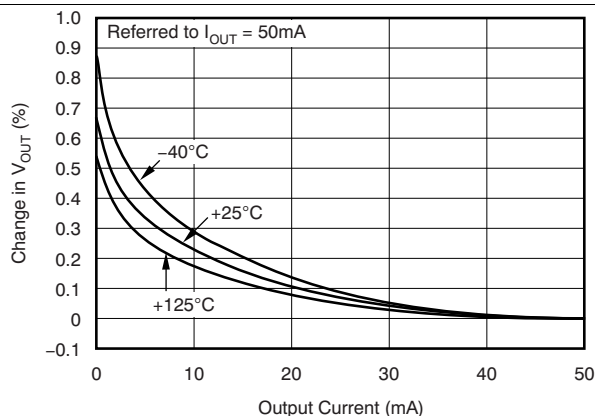


Figure 1. Load Regulation

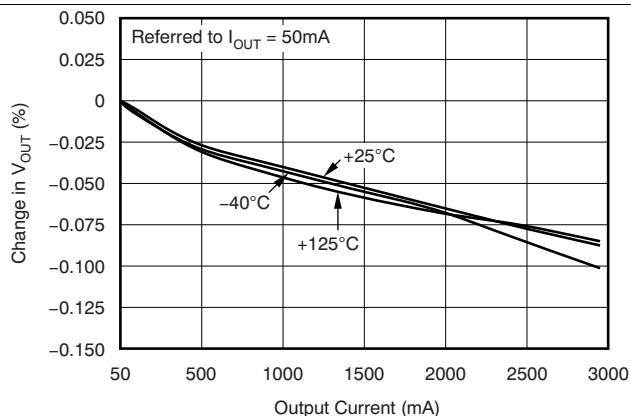


Figure 2. Load Regulation

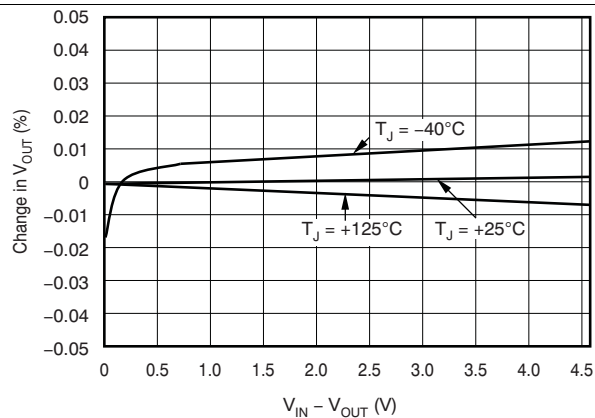


Figure 3. Line Regulation

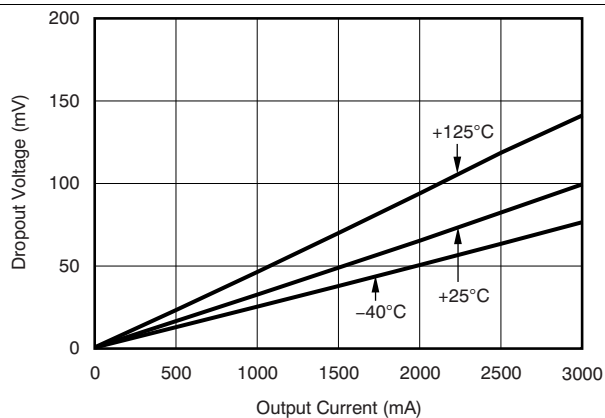


Figure 4. V_{IN} Dropout Voltage vs I_{OUT} and Temperature (T_J)

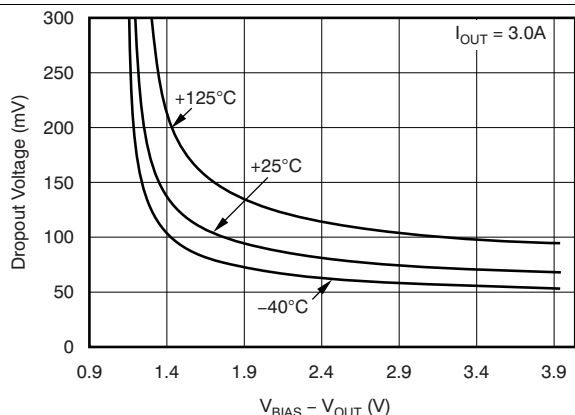


Figure 5. V_{IN} Dropout Voltage vs $V_{BIAS} - V_{OUT}$ and Temperature (T_J)

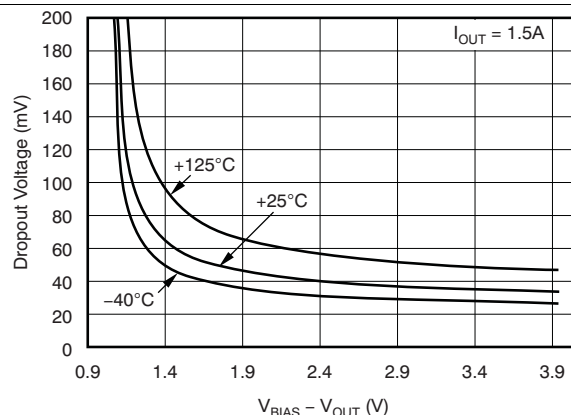


Figure 6. V_{IN} Dropout Voltage vs $V_{BIAS} - V_{OUT}$ and Temperature (T_J)

Typical Characteristics (continued)

At $T_J = 25^\circ\text{C}$, $V_{OUT} = 1.5\text{ V}$, $V_{IN} = V_{OUT(nom)} + 0.3\text{ V}$, $V_{BIAS} = 3.3\text{ V}$, $I_{OUT} = 50\text{ mA}$, $C_{IN} = 1\text{ }\mu\text{F}$, $C_{BIAS} = 1\text{ }\mu\text{F}$, $C_{SS} = 0.01\text{ }\mu\text{F}$, and $C_{OUT} = 10\text{ }\mu\text{F}$, unless otherwise noted.

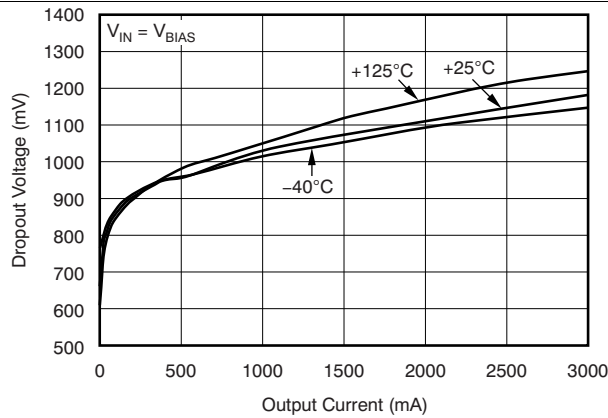


Figure 7. V_{BIAS} Dropout Voltage vs I_{OUT} and Temperature (T_J)

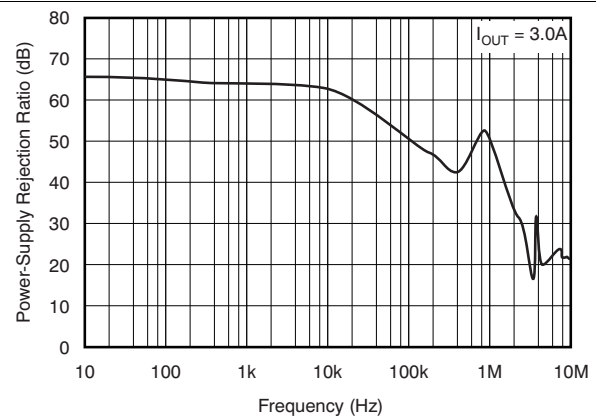


Figure 8. V_{BIAS} PSRR vs Frequency

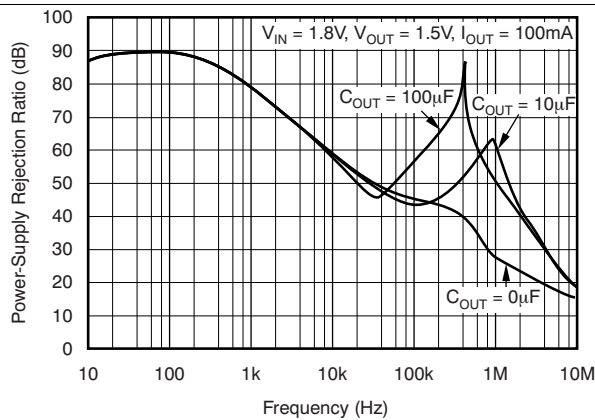


Figure 9. V_{IN} PSRR vs Frequency

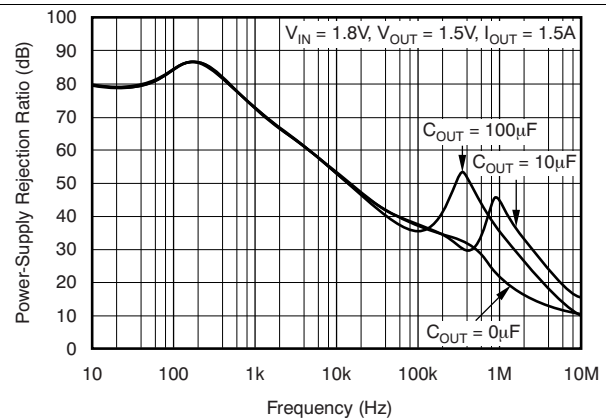


Figure 10. V_{IN} PSRR vs Frequency

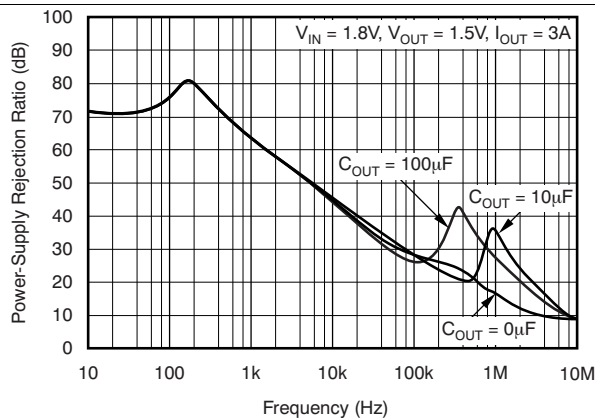


Figure 11. V_{IN} PSRR vs Frequency

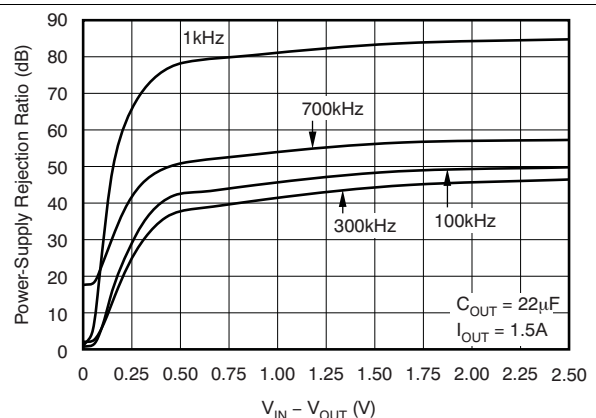


Figure 12. V_{IN} PSRR vs $V_{IN} - V_{OUT}$

Typical Characteristics (continued)

At $T_J = 25^\circ\text{C}$, $V_{OUT} = 1.5\text{ V}$, $V_{IN} = V_{OUT(nom)} + 0.3\text{ V}$, $V_{BIAS} = 3.3\text{ V}$, $I_{OUT} = 50\text{ mA}$, $C_{IN} = 1\text{ }\mu\text{F}$, $C_{BIAS} = 1\text{ }\mu\text{F}$, $C_{SS} = 0.01\text{ }\mu\text{F}$, and $C_{OUT} = 10\text{ }\mu\text{F}$, unless otherwise noted.

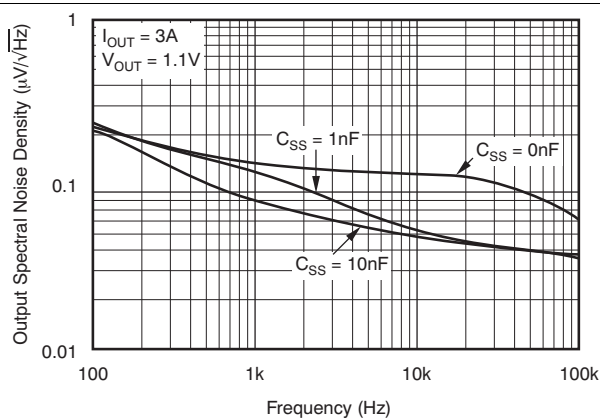


Figure 13. Noise Spectral Density

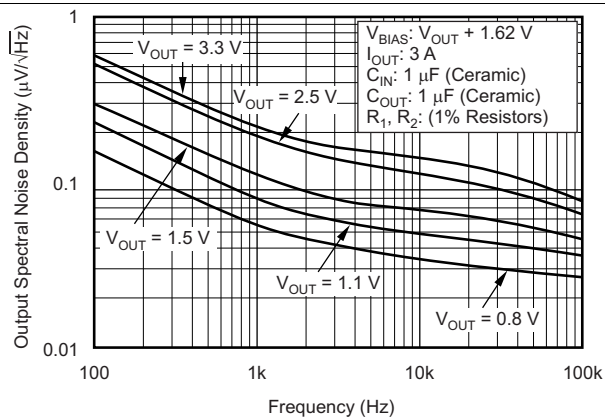


Figure 14. Noise Spectral Density

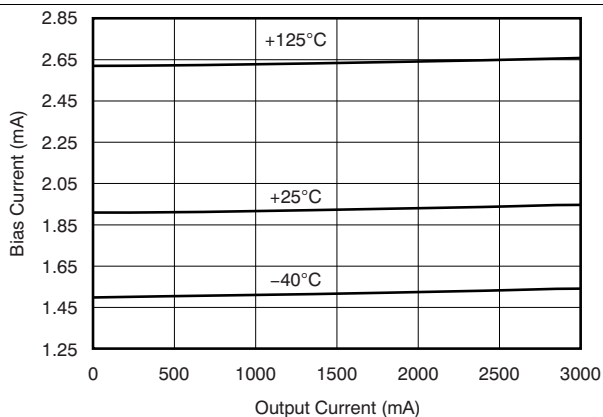


Figure 15. I_{BIAS} vs Output Current and Temperature

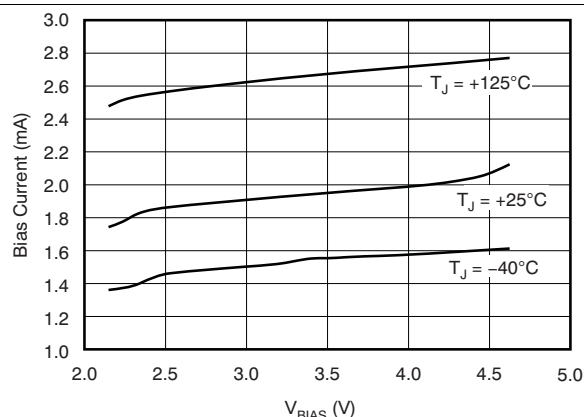


Figure 16. I_{BIAS} vs V_{BIAS} and V_{OUT}

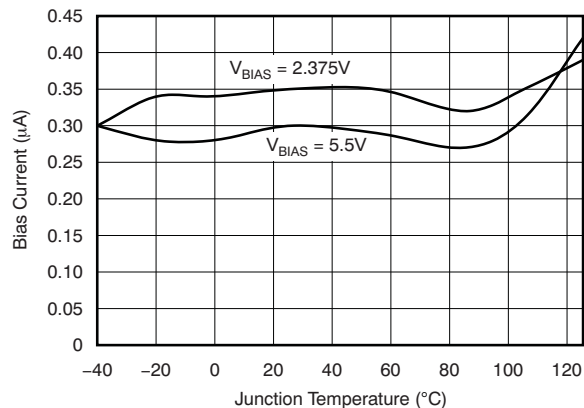


Figure 17. I_{BIAS} Shutdown vs Temperature

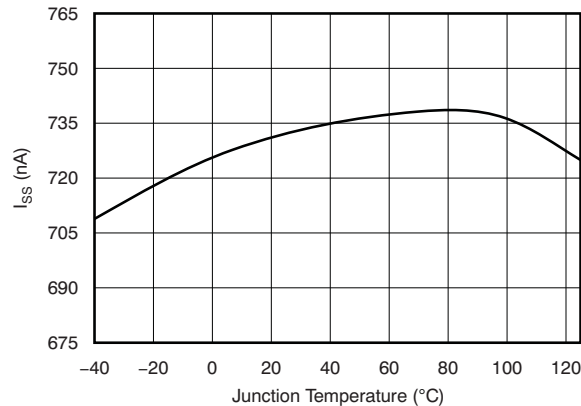
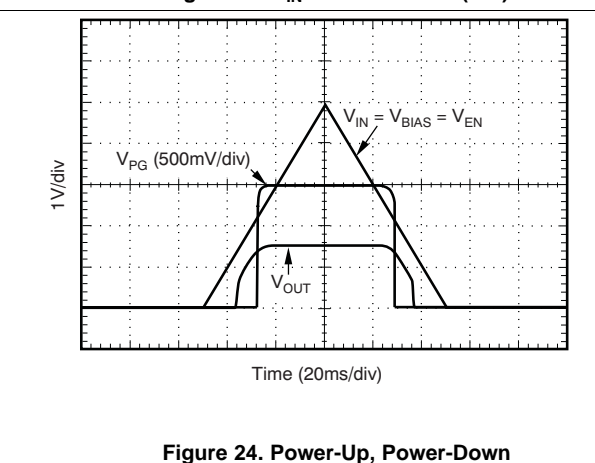
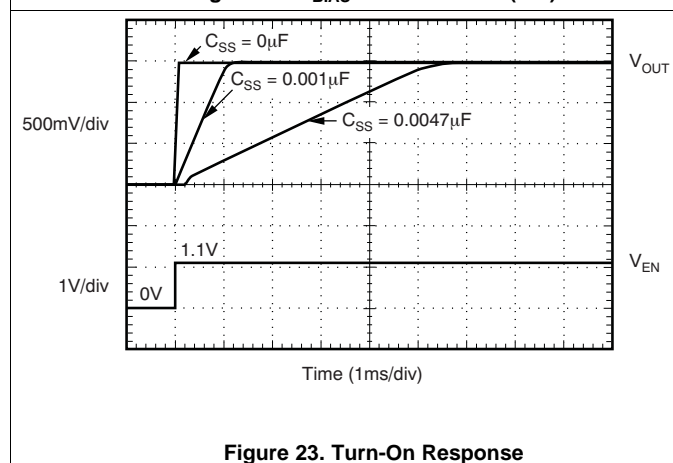
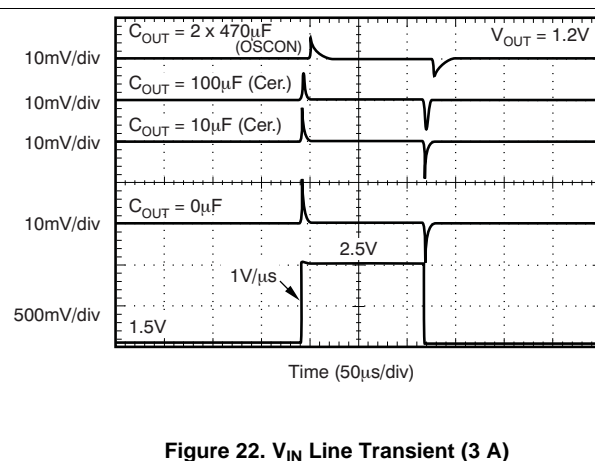
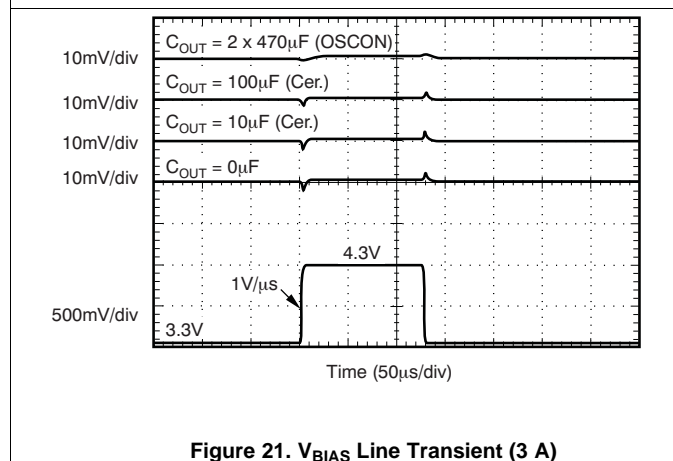
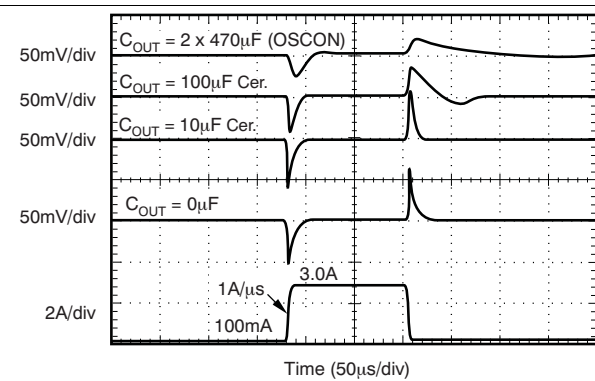
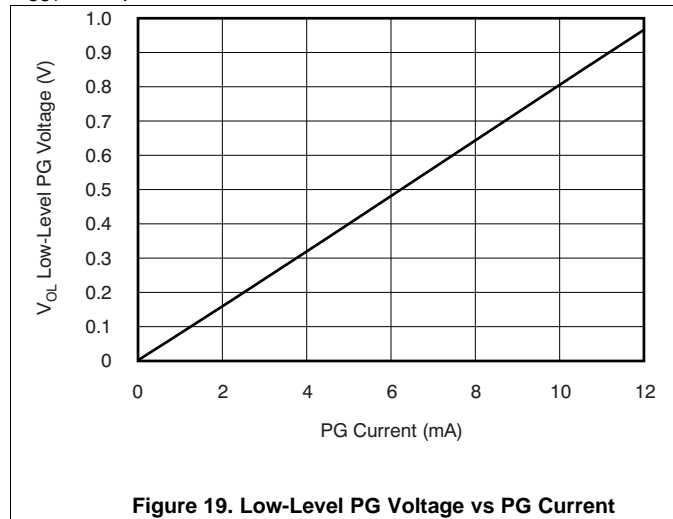


Figure 18. Soft-Start Charging Current (I_{SS}) vs Temperature

Typical Characteristics (continued)

At $T_J = 25^\circ\text{C}$, $V_{OUT} = 1.5\text{ V}$, $V_{IN} = V_{OUT(\text{nom})} + 0.3\text{ V}$, $V_{BIAS} = 3.3\text{ V}$, $I_{OUT} = 50\text{ mA}$, $C_{IN} = 1\text{ }\mu\text{F}$, $C_{BIAS} = 1\text{ }\mu\text{F}$, $C_{SS} = 0.01\text{ }\mu\text{F}$, and $C_{OUT} = 10\text{ }\mu\text{F}$, unless otherwise noted.



Typical Characteristics (continued)

At $T_J = 25^\circ\text{C}$, $V_{OUT} = 1.5\text{ V}$, $V_{IN} = V_{OUT(nom)} + 0.3\text{ V}$, $V_{BIAS} = 3.3\text{ V}$, $I_{OUT} = 50\text{ mA}$, $C_{IN} = 1\text{ }\mu\text{F}$, $C_{BIAS} = 1\text{ }\mu\text{F}$, $C_{SS} = 0.01\text{ }\mu\text{F}$, and $C_{OUT} = 10\text{ }\mu\text{F}$, unless otherwise noted.

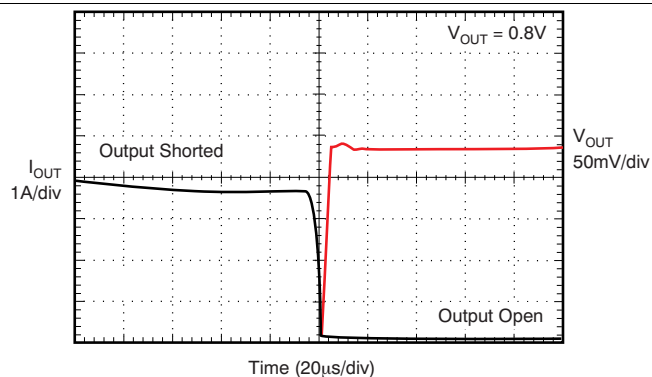


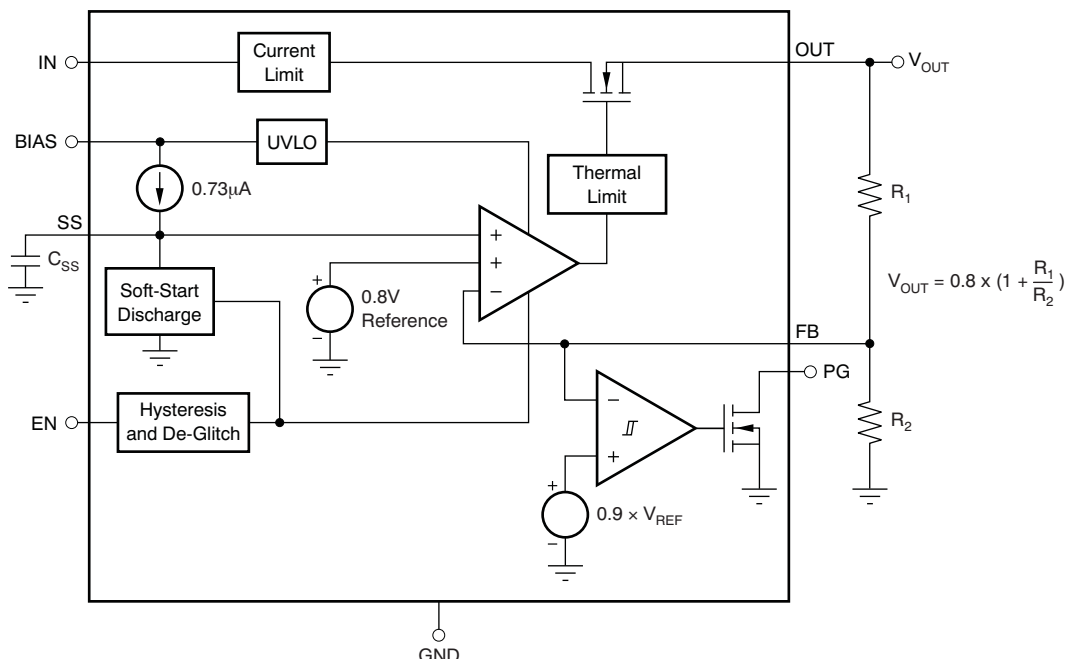
Figure 25. Output Short-Circuit Recovery

7 Detailed Description

7.1 Overview

The TPS74401 family of low-dropout regulators (LDOs) incorporates many features to ensure a wide range of uses. Hysteresis and de-glitch on the EN input improve the ability to sequence multiple devices without worrying about false start-up. The soft-start is fully programmable and allows the user to control the startup time of the LDO output. Hysteresis is also available on the PG comparator to ensure no false PG signals. The TPS74401 family of LDOs is ideal for FPGAs, DSPs, and any other device that requires linear supply and sequencing.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Enable, Shutdown

The enable (EN) pin is active high and compatible with standard digital signaling levels. V_{EN} lower than 0.4 V turns the regulator off, whereas V_{EN} above 1.1 V turns the regulator on. Unlike many regulators, the enable circuitry has hysteresis and de-glitching for use with relatively slow-ramping analog signals. This configuration allows the TPS74401 to be enabled by connecting the output of another supply to the EN pin. The enable circuitry typically has 50 mV of hysteresis and a de-glitch circuit to help avoid on-off cycling resulting from small glitches in the V_{EN} signal.

The enable threshold is typically 0.8 V and varies with temperature and process variations. Temperature variation is approximately $-1 \text{ mV}/^\circ\text{C}$; therefore, process variation accounts for most of the variation in the enable threshold. If precise turn-on timing is required, use a fast rise-time signal to enable the TPS74401.

If not used, EN can be connected to either IN or BIAS. If EN is connected to IN, connect EN as close as possible to the largest capacitance on the input to prevent voltage droops on that line from triggering the enable circuit.

Feature Description (continued)

7.3.2 Power-Good (VQFN Package Only)

The power-good (PG) pin is an open-drain output and can be connected to any 5.5 V or lower rail through an external pullup resistor. This pin requires at least 1.1 V on V_{BIAS} in order to have a valid output. The PG output is high-impedance when V_{OUT} is greater than $(V_{IT} + V_{HYS})$. If V_{OUT} drops below V_{IT} or if V_{BIAS} drops below 1.9 V, the open-drain output turns on and pulls the PG output low. The PG pin also asserts when the device is disabled. The recommended operating condition of the PG pin sink current is up to 1 mA, thus the pullup resistor for PG must be in the range of 10 k Ω to 1 M Ω . PG is only provided on the VQFN package. If output voltage monitoring is not needed, the PG pin can be left floating.

7.3.3 Internal Current Limit

The TPS74401 features a factory-trimmed, accurate current limit that is flat over temperature and supply voltage. The current limit allows the device to supply surges of up to 3.5 A and maintain regulation. The current limit responds in approximately 10 μ s to reduce the current during a short-circuit fault. Recovery from a short-circuit condition is well-controlled and results in very little output overshoot when the load is removed. See [Figure 25](#) in the [Typical Characteristics](#) section for short-circuit recovery performance.

The internal current limit protection circuitry of the TPS74401 is designed to protect against overload conditions. This circuitry is not intended to allow operation above the rated current of the device. Continuously running the TPS74401 above the rated current degrades device reliability.

7.3.4 Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 155°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is enabled. Depending on power dissipation, thermal resistance, and ambient temperature the thermal protection circuit can cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Activation of the thermal protection circuit indicates excessive power dissipation or inadequate heatsinking. For reliable operation, limit junction temperature to 125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, trigger thermal protection at least 30°C above the maximum expected ambient condition of the application. This condition produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS74401 is designed to protect against overload conditions. This circuitry is not intended to replace proper heatsinking. Continuously running the TPS74401 into thermal shutdown degrades device reliability.

7.4 Device Functional Modes

7.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage and bias voltage are both at least at the respective minimum specifications.
- The enable voltage has previously exceeded the enable rising threshold voltage and has not decreased below the enable falling threshold.
- The output current is less than the current limit.
- The device junction temperature is less than the maximum specified junction temperature.
- The device is not operating in dropout.

7.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this condition, the output voltage is the same as the input voltage minus the dropout voltage. The transient performance of the device is significantly degraded because the pass device is in a triode state and no longer controls the current through the LDO. Line or load transients in dropout can result in large output voltage deviations.

Device Functional Modes (continued)

7.4.3 Disabled

The device is disabled under the following conditions:

- The input or bias voltages are below the respective minimum specifications.
- The enable voltage is less than the enable falling threshold voltage or has not yet exceeded the enable rising threshold.
- The device junction temperature is greater than the thermal shutdown temperature.

Table 1 shows the conditions that lead to the different modes of operation.

Table 1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER				
	V _{IN}	V _{EN}	V _{BIAS}	I _{OUT}	T _J
Normal mode	V _{IN} > V _{OUT(nom)} + V _{DO} (V _{IN})	V _{EN} > V _{EN(high)}	V _{BIAS} ≥ V _{OUT} + 1.62 V	I _{OUT} < I _{CL}	T _J < 125°C
Dropout mode	V _{IN} < V _{OUT(nom)} + V _{DO} (V _{IN})	V _{EN} > V _{EN(high)}	V _{BIAS} < V _{OUT} + 1.62 V	—	T _J < 125°C
Disabled mode (any true condition disables the device)	V _{IN} < V _{IN(min)}	V _{EN} < V _{EN(low)}	V _{BIAS} < V _{BIAS(min)}	—	T _J > 155°C

7.5 Programming

7.5.1 Programmable Soft-Start

The TPS74401 features a programmable, monotonic, voltage-controlled soft-start that is set with an external capacitor (C_{SS}). This feature is important for many applications to eliminate power-up initialization problems when powering FPGAs, DSPs, or other processors. The controlled voltage ramp of the output also reduces peak inrush current during start-up, minimizing start-up transients to the input power bus.

To achieve a linear and monotonic soft-start, the TPS74401 error amplifier tracks the voltage ramp of the external soft-start capacitor until the voltage exceeds the internal reference. The soft-start ramp time depends on the soft-start charging current (I_{SS}), the soft-start capacitance (C_{SS}), and the internal reference voltage (V_{REF}), and can be calculated using Equation 1:

$$t_{SS} = \frac{(V_{REF} \times C_{SS})}{I_{SS}} \quad (1)$$

If large output capacitors are used, the device current limit (I_{CL}) and the output capacitor can set the start-up time. In this case, the start-up time is given by Equation 2:

$$t_{SSCL} = \frac{(V_{OUT(nom)} \times C_{OUT})}{I_{CL(min)}} \quad (2)$$

where

- V_{OUT(nom)} is the nominal set output voltage as set by the user,
- C_{OUT} is the output capacitance,
- and I_{CL(min)} is the minimum current limit for the device.

In applications where monotonic startup is required, the soft-start time given by Equation 1 must be set to be greater than Equation 2.

Programming (continued)

The maximum recommended soft-start capacitor is 0.015 μF . Larger soft-start capacitors can be used and do not damage the device; however, the soft-start capacitor discharge circuit may not be able to fully discharge the soft-start capacitor when re-enabled. Soft-start capacitors larger than 0.015 μF can be a problem in applications where the user must rapidly pulse the enable pin and also require the device to soft-start from ground. C_{SS} must be low-leakage; X7R, X5R, or C0G dielectric materials are preferred. Table 2 lists suggested soft-start capacitor values.

Table 2. Standard Capacitor Values for Programming the Soft-Start Time⁽¹⁾

C_{SS}	SOFT-START TIME
Open	0.1 ms
470 pF	0.5 ms
1000 pF	1 ms
4700 pF	5 ms
0.01 μF	10 ms
0.015 μF	16 ms

$$(1) \quad t_{\text{SS}}(\text{s}) = \frac{V_{\text{REF}} \times C_{\text{SS}}}{I_{\text{SS}}} = \frac{0.8\text{V} \times C_{\text{SS}}(\text{F})}{0.73\mu\text{A}} \quad \text{where } t_{\text{SS}}(\text{s}) = \text{soft-start time in seconds.}$$

7.5.2 Sequencing Requirements

The device can have V_{IN} , V_{BIAS} , and V_{EN} sequenced in any order without causing damage to the device. However, for the soft-start function to work as intended, certain sequencing rules must be applied. Enabling the device after V_{IN} and V_{BIAS} are present is preferred, and can be accomplished using a digital output from a processor or supply supervisor. An analog signal from an external RC circuit, as shown in Figure 26, can also be used as long as the delay time is long enough for V_{IN} and V_{BIAS} to be present.

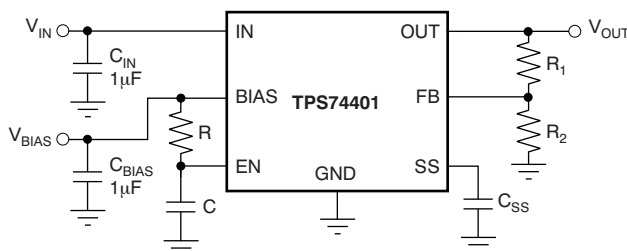


Figure 26. Soft-Start Delay Using an RC Circuit on Enable

If a signal is not available to enable the device after V_{IN} and V_{BIAS} , simply connecting EN to IN is acceptable for most applications as long as V_{IN} is greater than 1.1 V and the ramp rate of V_{IN} and V_{BIAS} is faster than the set soft-start ramp rate. If the ramp rate of the input sources is slower than the set soft-start time, the output tracks the slower supply less the dropout voltage until the set output voltage is reached. If EN is connected to BIAS , the device soft-starts as programmed, provided that V_{IN} is present before V_{BIAS} . If V_{BIAS} and V_{EN} are present before V_{IN} is applied and the set soft-start time has expired, then V_{OUT} tracks V_{IN} .

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS74401 belongs to a family of ultra-low dropout regulators that feature soft-start. These regulators use a low current bias input to power all internal control circuitry, allowing the NMOS pass transistor to regulate very low output voltages with low V_{IN} to V_{OUT} headroom.

The use of an NMOS-pass FET offers several critical advantages for many applications. Unlike a PMOS topology device, the output capacitor has little effect on loop stability. This architecture allows the TPS74401 to be stable with any or even no output capacitor. Transient response is also superior to PMOS topologies, particularly for low V_{IN} applications.

The TPS74401 features a programmable, voltage-controlled soft-start circuit that provides a smooth, monotonic start-up and limits startup inrush currents that can be caused by large capacitive loads. A power-good (PG) output is available to allow supply monitoring and sequencing of other supplies. An enable (EN) pin with hysteresis and de-glitch allows slow-ramping signals to be used for sequencing the device. The low V_{IN} and V_{OUT} capability allows for inexpensive, easy-to-design, and efficient linear regulation between the multiple supply voltages often present in processor intensive systems.

8.1.1 Input, Output, and Bias Capacitor Requirements

The TPS74401 does not require any output capacitor for stability. If an output capacitor is needed, the device is designed to be stable for all available types and values of output capacitance. The device is also stable with multiple capacitors in parallel, of any type or value. This flexibility is a result of an innovative control loop that ensures the device is stable independent of the output capacitance.

The capacitance required on the IN and BIAS pins strongly depends on the input supply source impedance. To counteract any inductance in the input, the minimum recommended capacitor for V_{IN} and V_{BIAS} is 1 μF . If V_{IN} and V_{BIAS} are connected to the same supply, the recommended minimum capacitor for V_{BIAS} is 4.7 μF . Use good quality, low-ESR capacitors on the input; ceramic X5R and X7R capacitors are preferred. Place these capacitors as close to the pins as possible for optimum performance and to help ensure stability.

8.1.2 Transient Response

The TPS74401 is designed to have transient response within 5% for most applications without an output capacitor. In some cases, the transient response can be limited by the transient response of the input supply. This limitation is especially true in applications where the difference between the input and output is less than 300 mV. In this case, adding additional input capacitance improves the transient response much more than just adding additional output capacitance. With a solid input supply, adding additional output capacitance reduces undershoot and overshoot during a transient at the expense of a slightly longer V_{OUT} recovery time; see [Figure 20](#) in the [Typical Characteristics](#) section. Because the TPS74401 is stable without an output capacitor, many applications can allow for little or no capacitance at the LDO output. For these applications, local bypass capacitance for the device under power can be sufficient to meet the transient requirements of the application. This design reduces the total solution cost by avoiding the need to use expensive, high-value capacitors at the LDO output.

Application Information (continued)

8.1.3 Dropout Voltage

The TPS74401 offers industry-leading dropout performance, making the device well-suited for high-current, low V_{IN} and low V_{OUT} applications. The extremely low dropout of the TPS74401 also allows the device to be used in place of a dc/dc converter and also achieve good efficiencies. Equation 3 provides a quick estimate of the efficiencies.

$$\text{Efficiency} \approx \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times (I_{IN} + I_Q)} \approx \frac{V_{OUT}}{V_{IN}} \text{ at } I_{OUT} \gg I_Q \quad (3)$$

This efficiency allows users to redesign the power architecture for their applications to achieve the smallest, simplest, and lowest cost solution.

There are two different specifications for dropout voltage with the TPS74401. The first specification (see Figure 38) is referred to as V_{IN} Dropout and is for users who wish to apply an external bias voltage to achieve low dropout. This specification assumes that V_{BIAS} is at least 1.62 V above V_{OUT} ; for example, when V_{BIAS} is powered by a 3.3-V rail with 5% tolerance and with $V_{OUT} = 1.5$ V. If V_{BIAS} is higher than ($3.3 \text{ V} \times 0.95$) or V_{OUT} is less than 1.5 V, V_{IN} dropout is less than specified.

The second specification (see Figure 39) is referred to as V_{BIAS} Dropout and is for users who wish to have $V_{BIAS} < V_{IN} + 1.62$ V. This option allows the device to be used in applications where an auxiliary bias voltage is not available or low dropout is not required. Dropout is limited by BIAS in these applications because V_{BIAS} provides the gate drive to the pass FET and therefore must be greater than $V_{OUT} + V_{DO} (V_{BIAS})$. Because of this usage, IN and BIAS tied together easily consume excessive power. Pay attention and do not exceed the power rating of the IC package.

8.1.4 Output Noise

The TPS74401 provides low output noise when a soft-start capacitor is used. When the device reaches the end of the soft-start cycle, the soft-start capacitor serves as a filter for the internal reference. By using a 0.001-μF soft-start capacitor, the output noise is reduced by half and is typically 19 μV_{RMS} for a 1.2-V output (100 Hz to 100 kHz). Noise is a function of the set output voltage because most of the output noise is generated by the internal reference. The RMS noise with a 0.001-μF soft-start capacitor is given in Equation 4.

$$V_N (\mu V_{RMS}) = 16 \left(\frac{\mu V_{RMS}}{V} \right) \times V_{OUT} (V) \quad (4)$$

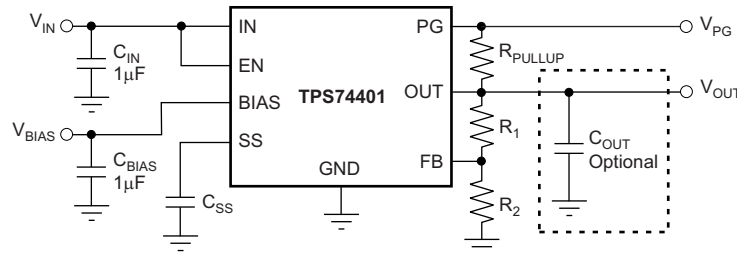
The low output noise of the TPS74401 makes the device a good choice for powering transceivers, PLLs, or other noise-sensitive circuitry.

8.2 Typical Applications

8.2.1 Setting the TPS74401

Figure 27 shows a typical application circuit for the TPS74401.

R_1 and R_2 can be calculated for any output voltage using the formula shown in Figure 27. Table 3 lists sample resistor values of common output voltages. In order to achieve the maximum accuracy specifications, R_2 must be $\leq 4.99\text{ k}\Omega$.



$$R_1 = \left[\frac{V_{OUT}}{V_{REF}} - 1 \right] \times R_2$$

Figure 27. Typical Application Circuit for the TPS74401

Table 3. Standard 1% Resistor Values for Programming the Output Voltage⁽¹⁾

R_1 (k Ω)	R_2 (k Ω)	V_{OUT} (V)
Short	Open	0.8
0.619	4.99	0.9
1.13	4.53	1.0
1.37	4.42	1.05
1.87	4.99	1.1
2.49	4.99	1.2
4.12	4.75	1.5
3.57	2.87	1.8
3.57	1.69	2.5
3.57	1.15	3.3

(1) $V_{OUT} = 0.8 \times (1 + R_1 / R_2)$.

NOTE

When V_{BIAS} and V_{EN} are present and V_{IN} is not supplied, this device outputs approximately 50 μA of current from OUT. Although this condition does not cause any damage to the device, the output current can charge up the OUT node if total resistance between OUT and GND (including external feedback resistors) is greater than 10 k Ω .

8.2.1.1 Design Requirements

The design goals are $V_{IN} = 1.8\text{ V}$, $V_{OUT} = 1.5\text{ V}$, and $I_{OUT} = 2\text{ A}$ max. The design optimizes transient response while meeting a 1-ms startup time with a startup dominated by the soft-start feature. The input supply comes from a supply on the same circuit board. The available system rails for V_{BIAS} are 2.7 V, 3.3 V, and 5 V.

The design space consists of C_{IN} , C_{OUT} , C_{BIAS} , C_{SS} , V_{BIAS} , R_1 , R_2 , and R_3 , and the circuit is from [Figure 27](#).

This example uses a V_{IN} of 1.8 V, with a V_{BIAS} of 2.5 V.

8.2.1.2 Detailed Design Procedure

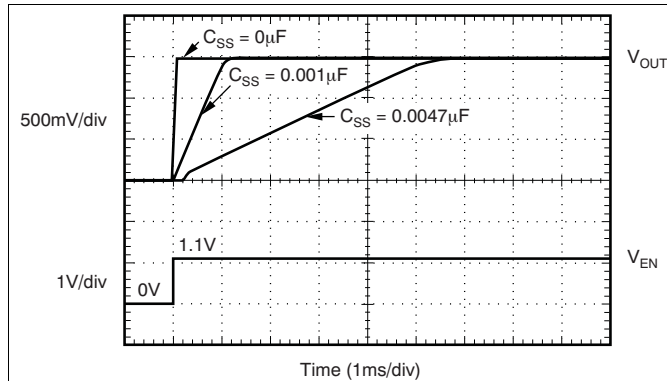
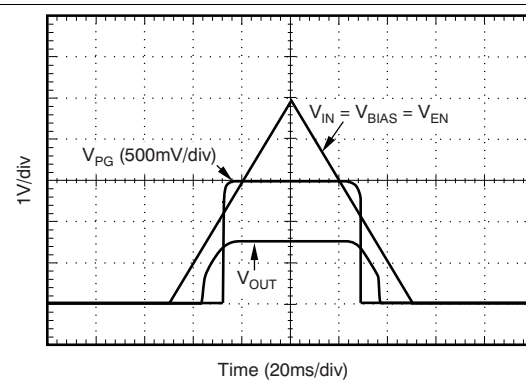
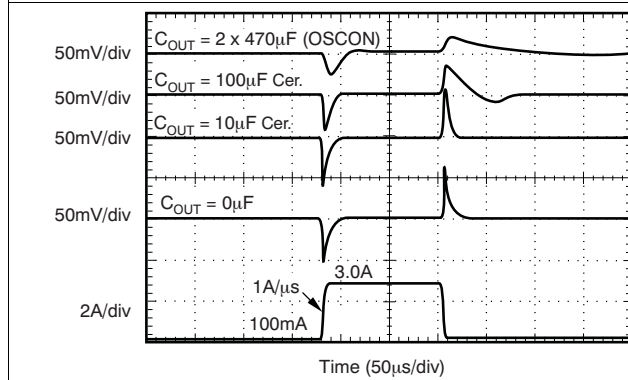
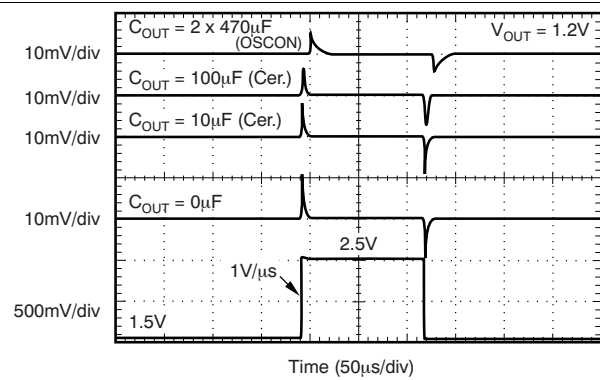
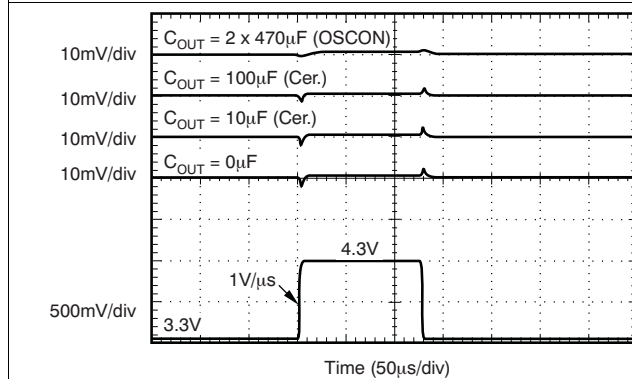
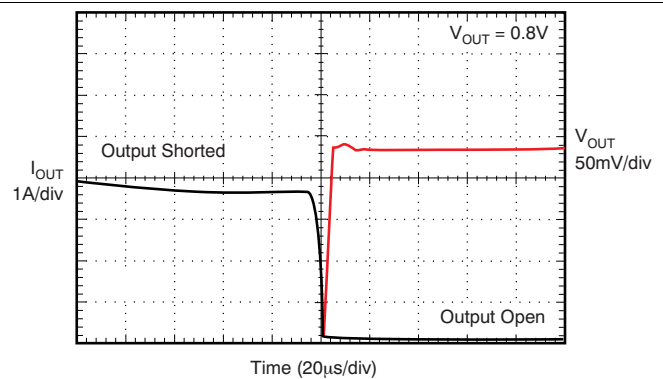
The first step for this design is to examine the maximum load current along with the input and output voltage requirements, to determine if the device thermal and dropout voltage requirements can be met. At 3 A, the input dropout voltage of the TPS74401 family is a maximum of 240 mV over temperature. As a result, the dropout headroom is sufficient for operation over both input and output voltage accuracy.

The maximum power dissipated in the linear regulator is the maximum voltage dropped across the pass element from the input to the output multiplied by the maximum load current. In this example, the maximum voltage drop across in the pass element is $(1.8\text{ V} - 1.5\text{ V})$, giving a $V_{DROP} = 300\text{ mV}$. The power dissipated can then be estimated by the equation $P_{DISS} = I_{L(max)} \times V_{DROP} = \sim 600\text{ mW}$. This calculation gives an efficiency of nearly 83.3% by using [Equation 3](#).

When the power dissipated in the linear regulator is known, the corresponding junction temperature increase can be calculated. To estimate the junction temperature increase above ambient, the power dissipated must be multiplied by the junction-to-ambient thermal resistance. For thermal resistance information, refer to the [Thermal Information](#) table. For this example, using the KTW package, the junction temperature rise is calculated to be 21.2°C. The maximum junction temperature increase is calculated by adding the junction temperature rise to the maximum ambient temperature. In this example, the maximum junction temperature is 46.2°C. Keep in mind that the junction temperature must be less than 125°C for reliable operation. Additional ground planes, added thermal vias, and air flow all help to improve the thermal transfer characteristics of the system.

The next step is to determine the bias voltage or if a separate source is needed for the bias voltage. Because V_{IN} is less than V_{OUT} plus the V_{BIAS} dropout, V_{BIAS} must be an independent supply. $V_{BIAS} = V_{OUT} + 1.62\text{ V} = 3.12\text{ V}$; the system has a 3.3-V rail to use for this supply and also to provide some limited headroom for V_{BIAS} . The 5-V rail is a better choice to improve the performance of the LDO, so the 5-V rail is used.

8.2.1.3 Application Curves


Figure 28. Turn-On Response

Figure 29. Power-Up, Power-Down

Figure 30. Load Transient Response

Figure 31. V_{IN} Line Transient (3 A)

Figure 32. V_{BIAS} Line Transient (3 A)

Figure 33. Output Short-Circuit Recovery

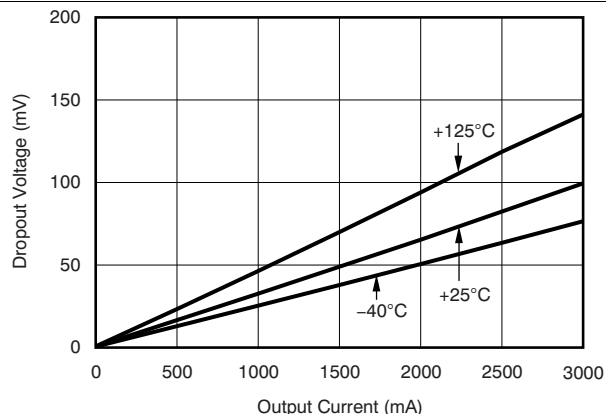


Figure 34. V_{IN} Dropout Voltage vs I_{OUT} and Temperature (T_J)

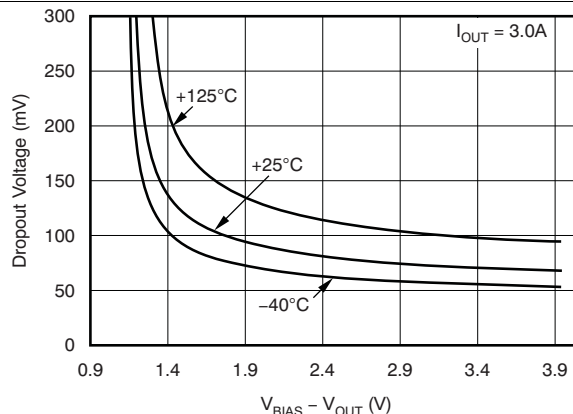


Figure 35. V_{IN} Dropout Voltage vs $V_{BIAS} - V_{OUT}$ and Temperature (T_J)

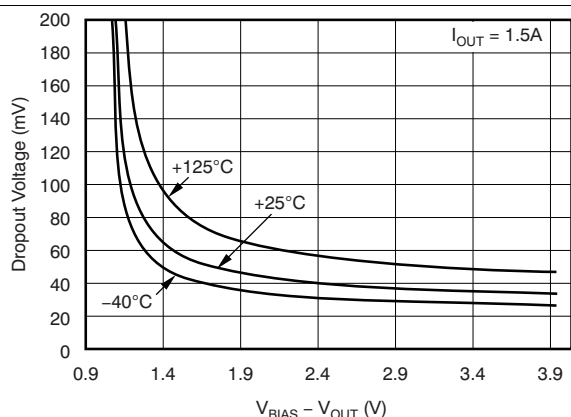


Figure 36. V_{IN} Dropout Voltage vs $V_{BIAS} - V_{OUT}$ and Temperature (T_J)

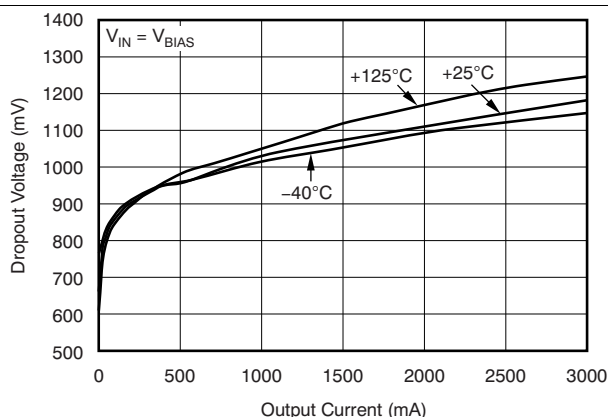


Figure 37. V_{BIAS} Dropout Voltage vs I_{OUT} and Temperature (T_J)

8.2.2 Using an Auxiliary Bias Rail

Figure 38 shows a typical application of the TPS74401 using an auxiliary bias rail. The auxiliary bias rail allows for the designer to specify the system to have a low V_{DO} . The bias rail supplies the error amplifier with a higher supply voltage, increasing the voltage that can be applied to the gate of the pass device.

V_{BIAS} must be at least $V_{OUT} + 1.62$ V.

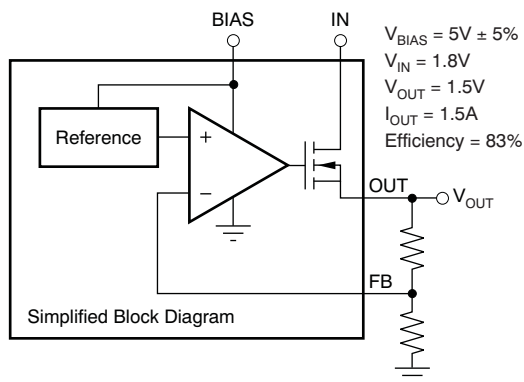


Figure 38. Typical Application of the TPS74401 Using an Auxiliary Bias Rail

8.2.3 Without an Auxiliary Bias

The TPS74401 family is capable of operating without a bias rail if $V_{IN} \geq V_{OUT} + V_{DO}$ (V_{BIAS}). Additional capacitance is advised for this scenario, with at least 4.7 μF of capacitance near the input pin. [Figure 39](#) shows a typical application of the TPS74401 without an auxiliary bias.

If using the TPS74401 in this situation and under high load conditions, ensure that the printed circuit board (PCB) provides adequate thermal handling capabilities to keep the device in its recommended operating range. See the [Power Supply Recommendations](#) section for more information.

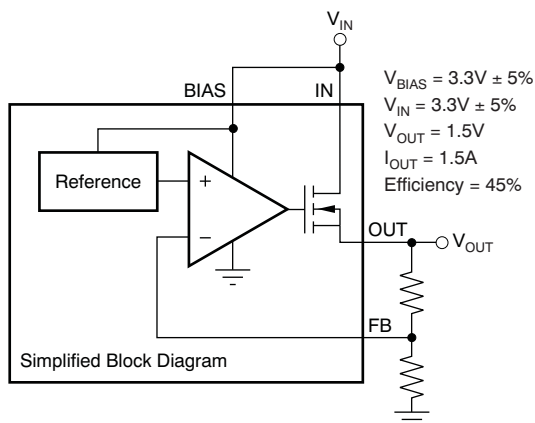


Figure 39. Typical Application of the TPS74401 Without an Auxiliary Bias

9 Power Supply Recommendations

The TPS74401 is designed to operate from an input voltage between 1.1 V to 5.5 V, provided the bias rail is at least 1.62 V higher than the input supply. The bias rail and the input supply must both provide adequate headroom and current for the device to operate normally.

Connect a low output impedance power supply directly to the IN pin of the TPS74401. This supply must have at least 1 μF of capacitance near the IN pin for stability. A supply with similar requirements must also be connected directly to the bias rail with a separate 1 μF or larger capacitor.

If the IN pin is tied to the bias pin, a minimum 4.7 μF of capacitance is needed for stability.

To increase the overall PSRR of the solution at higher frequencies, use a pi-filter or ferrite bead before the input capacitor.

10 Layout

10.1 Layout Guidelines

An optimal layout can greatly improve transient performance, PSRR, and noise. To minimize the voltage droop on the input of the device during load transients, connect the capacitance on IN and BIAS as close as possible to the device. This capacitance also minimizes the effects of parasitic inductance and resistance of the input source and can therefore improve stability. To achieve optimal transient performance and accuracy, connect the top side of R₁ in Figure 27 as close as possible to the load. This connection minimizes the voltage droop on BIAS during transient conditions and can improve the turn-on response.

10.2 Layout Example

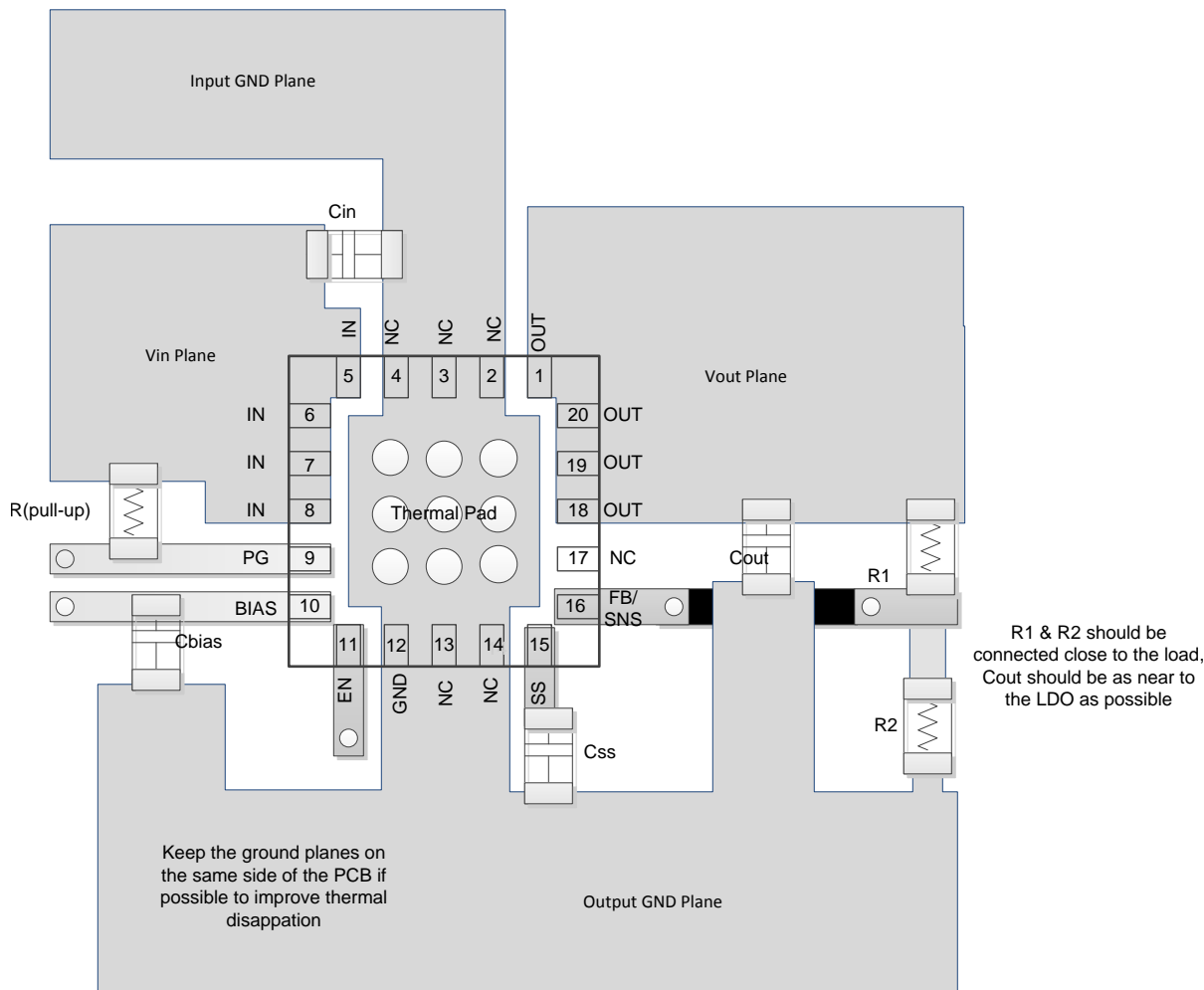


Figure 40. Layout Schematic (VQFN Packages)

10.3 Power Dissipation

Knowing the device power dissipation and proper sizing of the thermal plane that is connected to the tab or pad is critical to avoiding thermal shutdown and ensuring reliable operation.

Power dissipation of the device depends on input voltage and load conditions, and can be calculated using Equation 5:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (5)$$

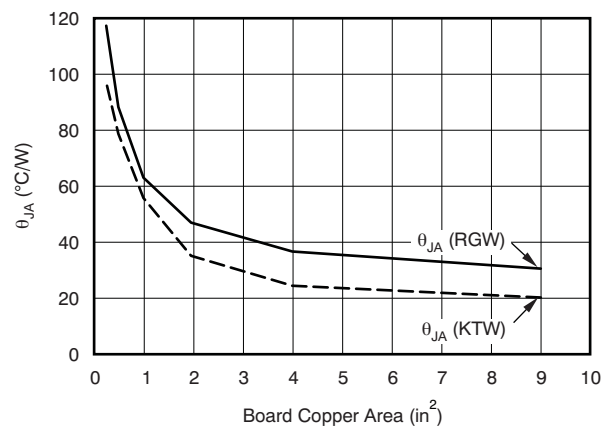
Power Dissipation (continued)

Power dissipation can be minimized and greater efficiency can be achieved by using the lowest possible input voltage necessary to achieve the required output voltage regulation.

On the VQFN (RGW, RGR) packages, the primary conduction path for heat is through the exposed pad to the PCB. The pad can be connected to ground or left floating; however, the pad must be attached to an appropriate amount of copper PCB area to ensure the device does not overheat. On the DDPAK (KTW) package, the primary conduction path for heat is through the tab to the PCB. Connect that tab to ground. The maximum junction-to-ambient thermal resistance depends on the maximum ambient temperature, maximum device junction temperature, and power dissipation of the device and can be estimated using [Equation 6](#):

$$R_{\theta JA} = \frac{(+125^{\circ}\text{C} - T_A)}{P_D} \quad (6)$$

Knowing the maximum $R_{\theta JA}$, the minimum amount of PCB copper area needed for appropriate heatsinking can be estimated using [Figure 41](#).



Note: θ_{JA} value at board size of 9 in² (that is, 3 in × 3 in) is a JEDEC standard.

Figure 41. θ_{JA} versus Board Size

[Figure 41](#) shows the variation of θ_{JA} as a function of ground plane copper area in the board. [Figure 41](#) is intended only as a guideline to demonstrate the affects of heat spreading in the ground plane; do not use [Figure 41](#) to estimate actual thermal performance in real application environments.

NOTE

When the device is mounted on an application PCB, TI strongly recommends using Ψ_{JT} and Ψ_{JB} , as explained in the section.

10.4 Thermal Considerations

A better method of estimating the thermal measure comes from using the thermal metrics Ψ_{JT} and Ψ_{JB} , as shown in [Thermal Information](#). These metrics are a more accurate representation of the heat transfer characteristics of the die and the package than $R_{\theta JA}$. The junction temperature can be estimated with the corresponding formulas given in [Equation 7](#).

$$\Psi_{JT}: T_J = T_T + \Psi_{JT} \cdot P_D$$

$$\Psi_{JB}: T_J = T_B + \Psi_{JB} \cdot P_D$$

where

- P_D is the power dissipation shown by [Equation 5](#),
- T_T is the temperature at the center-top of the IC package, and
- T_B is the PCB temperature measured 1 mm away from the IC package *on the PCB surface* (see [Figure 42](#)).

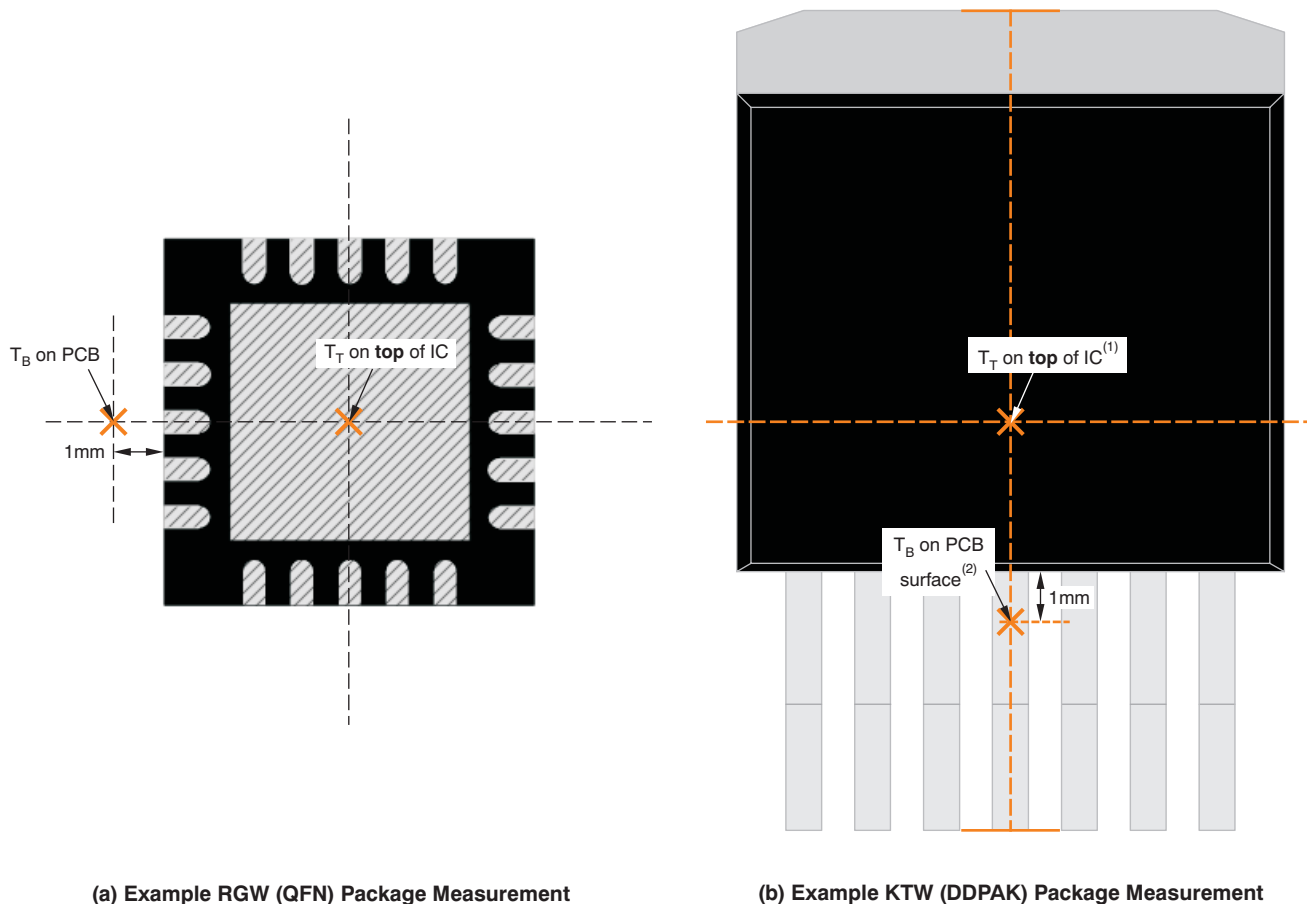
(7)

Thermal Considerations (continued)

NOTE

Both T_T and T_B can be measured on actual application boards using a thermo-gun (an infrared thermometer).

For more information about measuring T_T and T_B , see the application note *Using New Thermal Metrics (SBVA025)*, available for download at www.ti.com.



- (1) T_T is measured at the center of both the X- and Y-dimensional axes.
- (2) T_B is measured **below** the package lead **on the PCB surface**.

Figure 42. Measuring Points for T_T and T_B

Compared with θ_{JA} , the thermal metrics Ψ_{JT} and Ψ_{JB} are less independent of board size, but do have a small dependency on board size and layout. Figure 43 shows characteristic performance of Ψ_{JT} and Ψ_{JB} versus board size.

Referring to Figure 43, the RGW package thermal performance has negligible dependency on board size. The KTW package, however, does have a measurable dependency on board size. This dependency exists because the package shape is not point symmetric to an IC center. In the KTW package, for example (see Figure 42), silicon is not beneath the measuring point of T_T which is the center of the X and Y dimension, so that Ψ_{JT} has a dependency. Also, because of that non-point symmetry, device heat distribution on the PCB is not point symmetric either, so that Ψ_{JB} has a greater dependency on board size and layout.

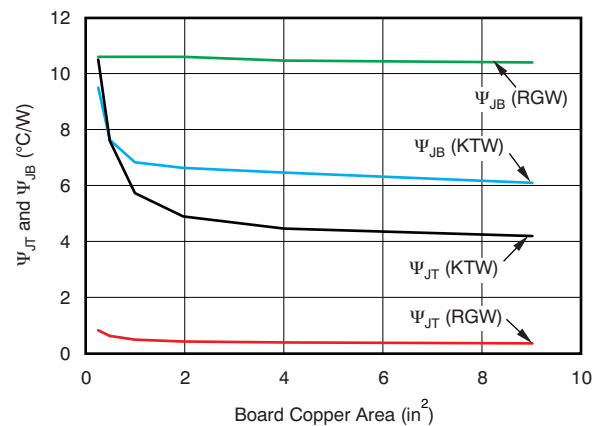


Figure 43. Ψ_{JT} and Ψ_{JB} versus Board Size

For a more detailed discussion of why TI does not recommend using $\theta_{JC(top)}$ to determine thermal characteristics, refer to the application note *Using New Thermal Metrics* (SBVA025), available for download at www.ti.com. Also, refer to the application note *IC Package Thermal Metrics* (SPRA953) (also available on the TI website) for further information.

11 器件和文档支持

11.1 器件支持

11.1.1 开发支持

11.1.1.1 评估模块

提供了评估模块 (EVM)，您可以借此来对使用 TPS74401 时的电路性能进行初始评估。[TPS74401EVM-118 评估模块](#)（和[相关的用户指南](#)）可在德州仪器 (TI) 网站上的产品文件夹中获取，也可直接从 [TI 网上商店](#) 购买。

11.1.1.2 Spice 模型

分析模拟电路和系统的性能时，使用 SPICE 模型对电路性能进行计算机仿真非常有用。您可以从产品文件夹中的工具与软件下获取 TPS74401 的 SPICE 模型。

11.2 文档支持

11.2.1 相关文档

相关文档如下：

- [《6A 电流共享双 LDO》参考设计](#)
- [《使用新的热度量指标》应用报告](#)
- [《IC 封装热度量指标》应用报告](#)
- [《TPS74401EVM-118 评估模块用户指南》](#)

11.3 接收文档更新通知

如需接收文档更新通知，请访问 [www.ti.com.cn](#) 网站上的器件产品文件夹。点击右上角的[提醒我 \(Alert me\)](#) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

11.4 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](#), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 商标

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

11.6 静电放电警告



ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS74401KTWR	ACTIVE	DDPAK/ TO-263	KTW	7	500	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR	-40 to 125	TPS74401	Samples
TPS74401KTWRG3	ACTIVE	DDPAK/ TO-263	KTW	7	500	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR	-40 to 125	TPS74401	Samples
TPS74401KTWT	LIFEBUY	DDPAK/ TO-263	KTW	7	50	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR	-40 to 125	TPS74401	
TPS74401KTWTG3	LIFEBUY	DDPAK/ TO-263	KTW	7	50	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR	-40 to 125	TPS74401	
TPS74401RGR	ACTIVE	VQFN	RGR	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	12KA	Samples
TPS74401RGRT	ACTIVE	VQFN	RGR	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	12KA	Samples
TPS74401RGWR	ACTIVE	VQFN	RGW	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 74401	Samples
TPS74401RGWRG4	ACTIVE	VQFN	RGW	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 74401	Samples
TPS74401RGWT	ACTIVE	VQFN	RGW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 74401	Samples
TPS74401RGWTG4	ACTIVE	VQFN	RGW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 74401	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS74401KTWR	DDPAK/TO-263	KTW	7	500	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2
TPS74401KTWT	DDPAK/TO-263	KTW	7	50	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2
TPS74401RGRR	VQFN	RGR	20	3000	330.0	12.4	3.8	3.8	1.1	8.0	12.0	Q1
TPS74401RGRT	VQFN	RGR	20	250	180.0	12.5	3.8	3.8	1.1	8.0	12.0	Q1
TPS74401RGWR	VQFN	RGW	20	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
TPS74401RGWT	VQFN	RGW	20	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

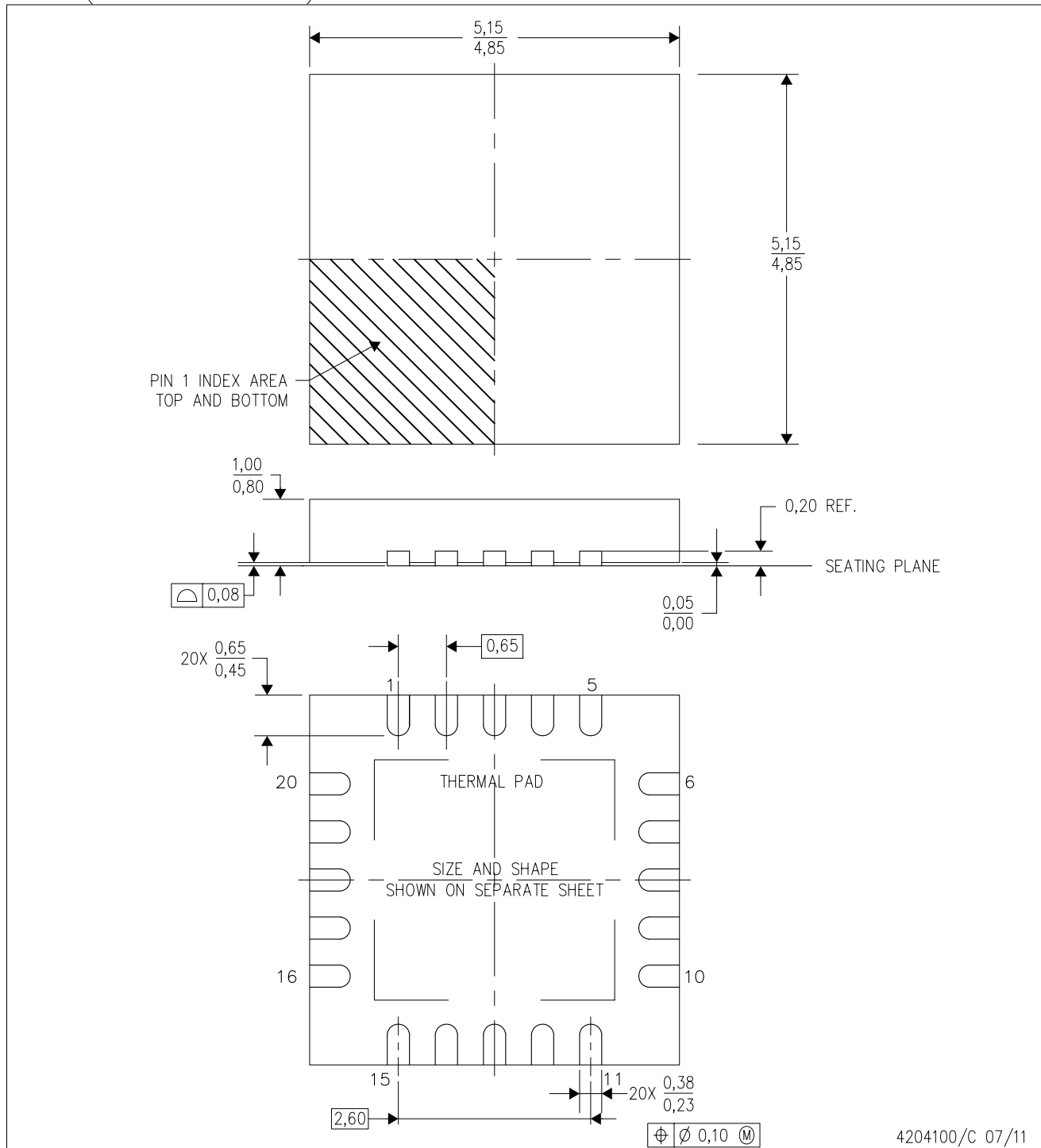


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS74401KTWR	DDPAK/TO-263	KTW	7	500	367.0	367.0	45.0
TPS74401KTWT	DDPAK/TO-263	KTW	7	50	367.0	367.0	45.0
TPS74401RGRR	VQFN	RGR	20	3000	338.0	355.0	50.0
TPS74401RGRT	VQFN	RGR	20	250	338.0	355.0	50.0
TPS74401RGWR	VQFN	RGW	20	3000	367.0	367.0	35.0
TPS74401RGWT	VQFN	RGW	20	250	210.0	185.0	35.0

RGW (S-PVQFN-N20)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5-1994.
 - B. This drawing is subject to change without notice.
 - C. Quad Flat pack, No-leads (QFN) package configuration
 - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - F. Falls within JEDEC MO-220.

THERMAL PAD MECHANICAL DATA

RGW (S-PVQFN-N20)

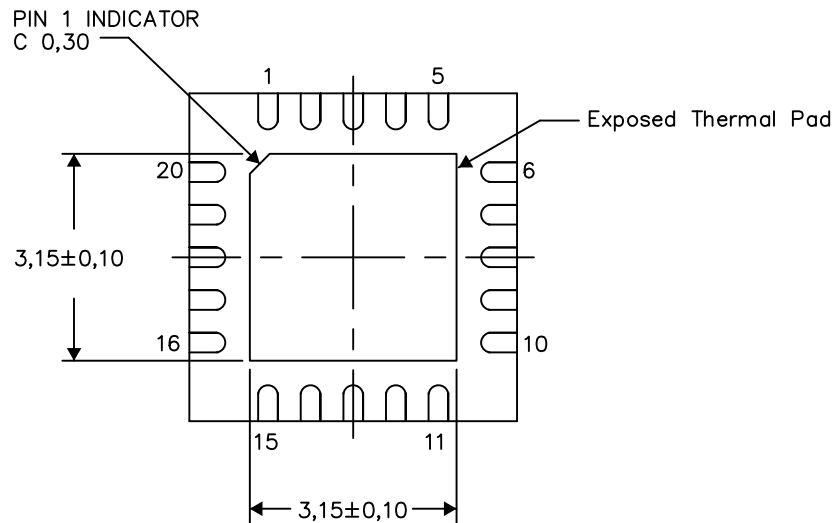
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

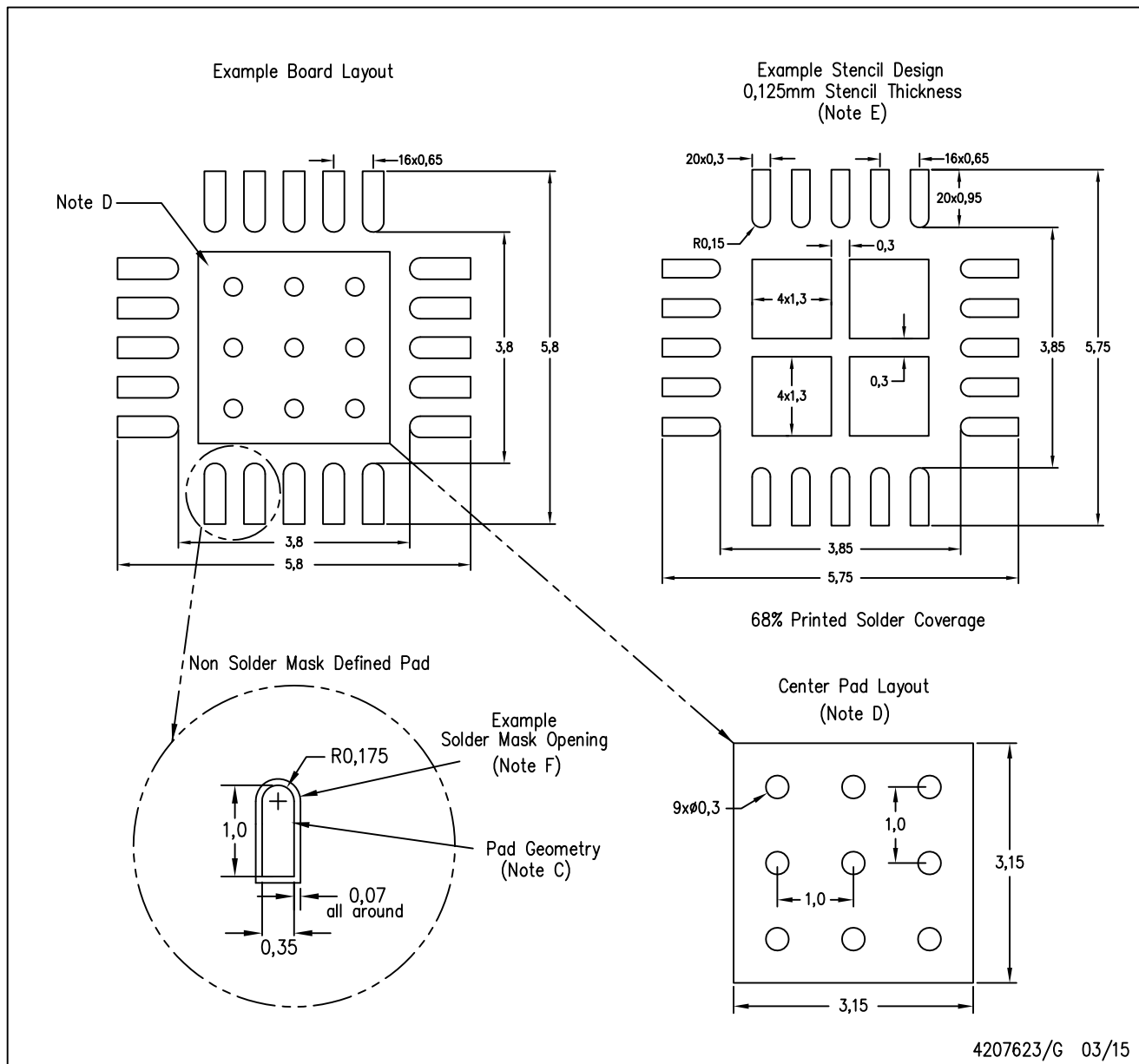
Exposed Thermal Pad Dimensions

4206352-2/M 06/15

NOTE: All linear dimensions are in millimeters

RGW (S-PVQFN-N20)

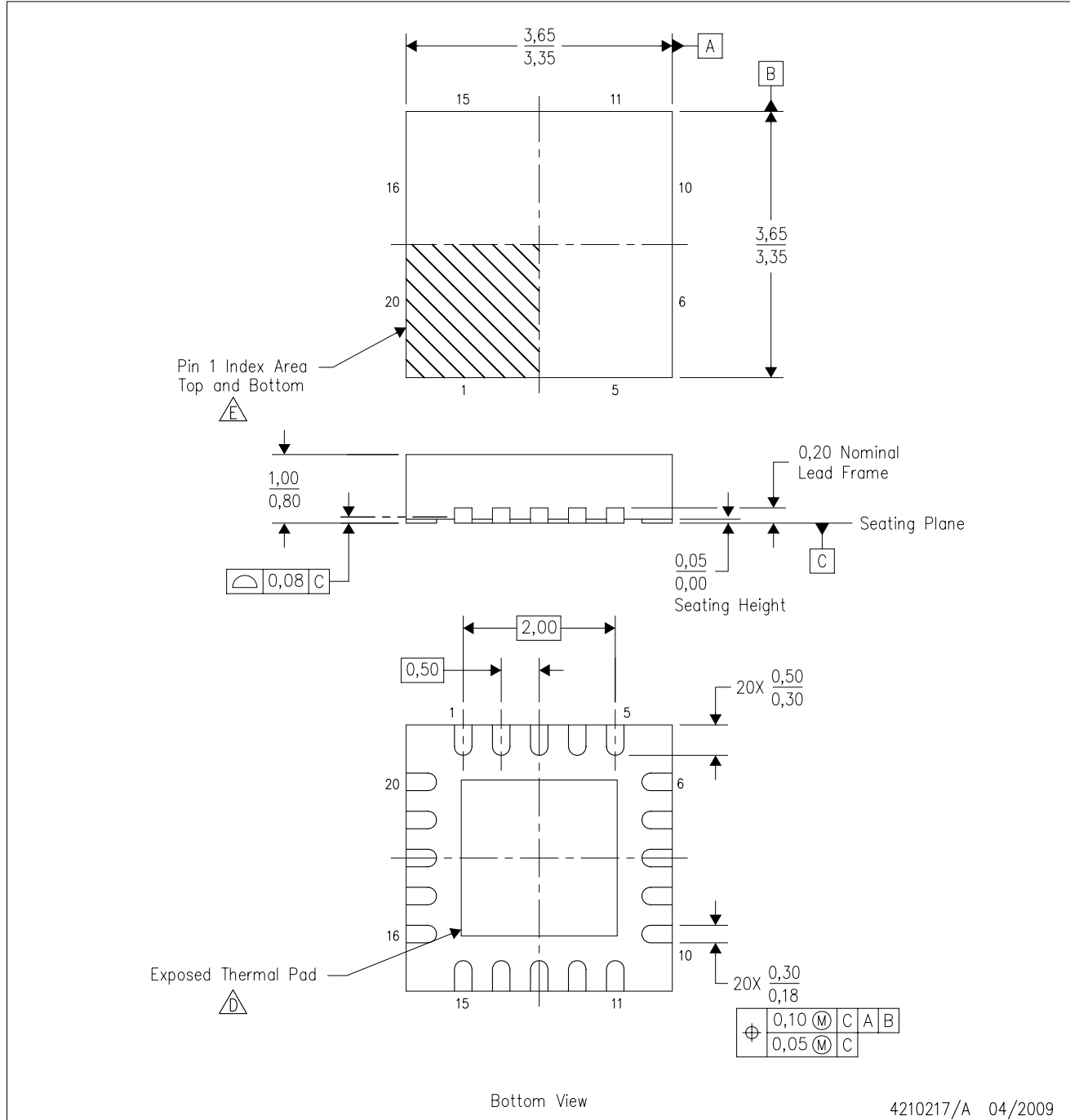
PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - F. Customers should contact their board fabrication site for solder mask tolerances.

RGR (S-PVQFN-N20)

PLASTIC QUAD FLATPACK NO-LEAD

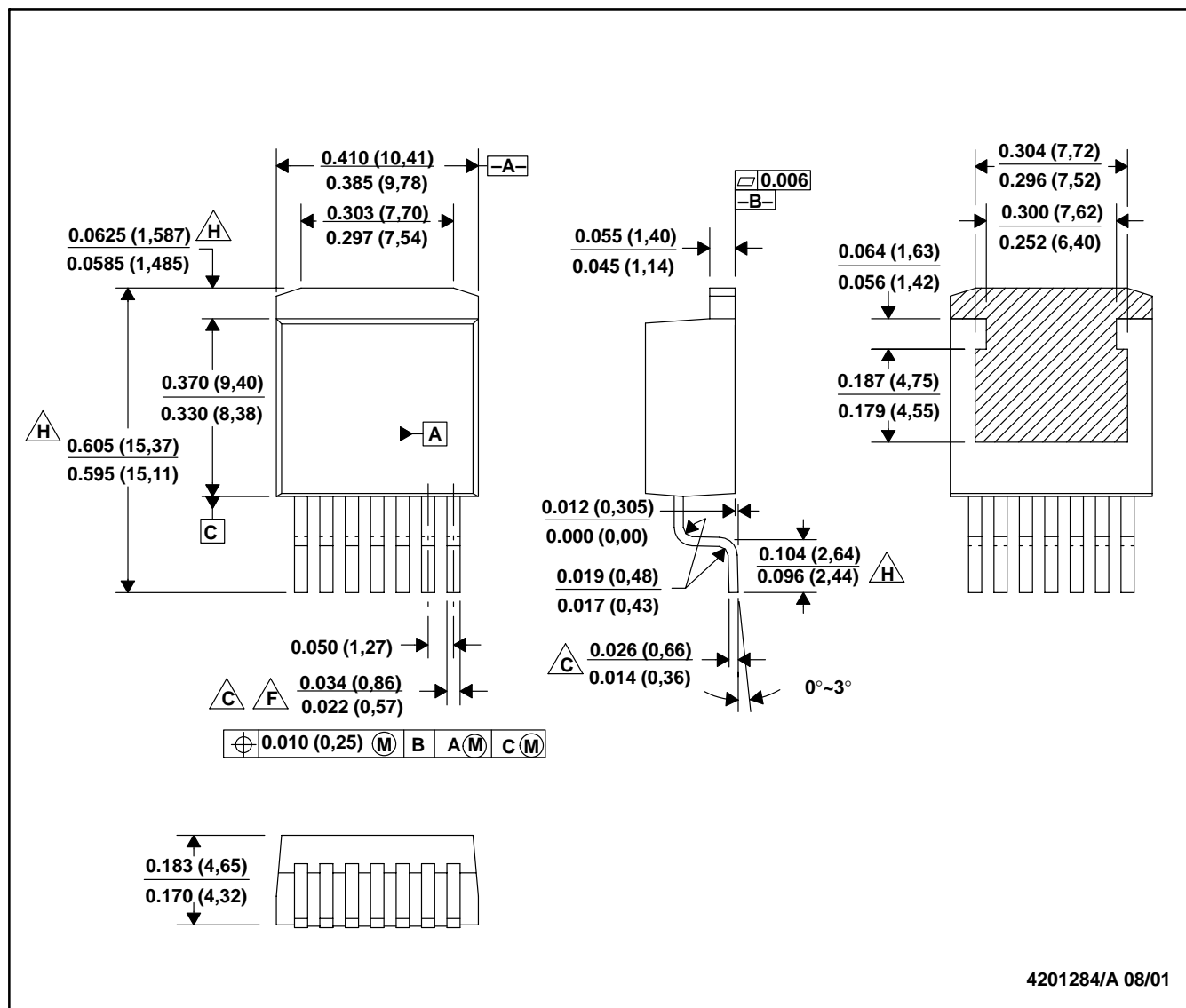


4210217/A 04/2009

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-Lead) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
 - Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.

KTW (R-PSFM-G7)

PLASTIC FLANGE-MOUNT



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - Lead width and height dimensions apply to the plated lead.
 - Leads are not allowed above the Datum B.
 - Stand-off height is measured from lead tip with reference to Datum B.
 - Lead width dimension does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum dimension by more than 0.003".
 - Cross-hatch indicates exposed metal surface.
 - Falls within JEDEC MO-169 with the exception of the dimensions indicated.

重要声明

德州仪器 (TI) 公司有权按照最新发布的 JESD46 对其半导体产品和服务进行纠正、增强、改进和其他修改，并不再按最新发布的 JESD48 提供任何产品和服务。买方在下订单前应获取最新的相关信息，并验证这些信息是否完整且是最新的。

TI 公布的半导体产品销售条款 (<http://www.ti.com/sc/docs/stdterms.htm>) 适用于 TI 已认证和批准上市的已封装集成电路产品的销售。另有其他条款可能适用于其他类型 TI 产品及服务的使用或销售。

复制 TI 数据表上 TI 信息的重要部分时，不得变更该等信息，且必须随附所有相关保证、条件、限制和通知，否则不得复制。TI 对该等复制文件不承担任何责任。第三方信息可能受到其它限制条件的制约。在转售 TI 产品或服务时，如果存在对产品或服务参数的虚假陈述，则会失去相关 TI 产品或服务的明示或暗示保证，且构成不公平的、欺诈性商业行为。TI 对此类虚假陈述不承担任何责任。

买方和在系统中整合 TI 产品的其他开发人员（总称“设计人员”）理解并同意，设计人员在设计应用时应自行实施独立的分析、评价和判断，且应全权负责并确保应用的安全性，及设计人员的应用（包括应用中使用的 TI 产品）应符合所有适用的法律法规及其他相关要求。设计人员就自己设计的应用声明，其具备制订和实施下列保障措施所需的一切必要专业知识，能够 (1) 预见故障的危险后果，(2) 监视故障及其后果，以及 (3) 降低可能导致危险的故障几率并采取适当措施。设计人员同意，在使用或分发包含 TI 产品的任何应用前，将彻底测试该等应用和该等应用所用 TI 产品的功能而设计。

TI 提供技术、应用或其他设计建议、质量特点、可靠性数据或其他服务或信息，包括但不限于与评估模块有关的参考设计和材料（总称“TI 资源”），旨在帮助设计人员开发整合了 TI 产品的应用，如果设计人员（个人，或如果是代表公司，则为设计人员的公司）以任何方式下载、访问或使用任何特定的 TI 资源，即表示其同意仅为该等目标，按照本通知的条款使用任何特定 TI 资源。

TI 所提供的 TI 资源，并未扩大或以其他方式修改 TI 对 TI 产品的公开适用的质保及质保免责声明；也未导致 TI 承担任何额外的义务或责任。TI 有权对其 TI 资源进行纠正、增强、改进和其他修改。除特定 TI 资源的公开文档中明确列出的测试外，TI 未进行任何其他测试。

设计人员只有在开发包含该等 TI 资源所列 TI 产品的应用时，才被授权使用、复制和修改任何相关 TI 资源。但并未依据禁止反言原则或其他法理授予您任何 TI 知识产权的任何其他明示或默示的许可，也未授予您 TI 或第三方的任何技术或知识产权的许可，该等产权包括但不限于任何专利权、版权、屏蔽作品权或与应用 TI 产品或服务的任何整合、机器制作、流程相关的其他知识产权。涉及或参考了第三方产品或服务的信息不构成使用此类产品或服务的许可或与其相关的保证或认可。使用 TI 资源可能需要您向第三方获得对该等第三方专利或其他知识产权的许可。

TI 资源系“按原样”提供。TI 兹免除对资源及其使用作出所有其他明确或默示的保证或陈述，包括但不限于对准确性或完整性、产权保证、无屡发故障保证，以及适销性、适合特定用途和不侵犯任何第三方知识产权的任何默认保证。TI 不负任何责任，包括但不限于因组合产品所致或与之有关的申索，也不为或对设计人员进行辩护或赔偿，即使该等产品组合已列于 TI 资源或其他地方。对因 TI 资源或其使用引起或与之有关的任何实际的、直接的、特殊的、附带的、间接的、惩罚性的、偶发的、从属或惩戒性损害赔偿，不管 TI 是否获悉可能会产生上述损害赔偿，TI 概不负责。

除 TI 已明确指出特定产品已达到特定行业标准（例如 ISO/TS 16949 和 ISO 26262）的要求外，TI 不对未达到任何该等行业标准要求而承担任何责任。

如果 TI 明确宣称产品有助于功能安全或符合行业功能安全标准，则该等产品旨在帮助客户设计和创作自己的符合相关功能安全标准和要求的的应用。在应用内使用产品的行为本身不会配有安全特性。设计人员必须确保遵守适用于其应用的相关安全要求和标准而设计。设计人员不可将任何 TI 产品用于关乎性命的医疗设备，除非已由各方获得授权的管理人员签署专门的合同对此类应用专门作出规定。关乎性命的医疗设备是指出现故障会导致严重身体伤害或死亡的医疗设备（例如生命保障设备、心脏起搏器、心脏除颤器、人工心脏泵、神经刺激器以及植入设备）。此类设备包括但不限于，美国食品药品监督管理局认定为 III 类设备的设备，以及在美国以外的其他国家或地区认定为同等类别设备的所有医疗设备。

TI 可能明确指定某些产品具备某些特定资格（例如 Q100、军用级或增强型产品）。设计人员同意，其具备一切必要专业知识，可以为自己的应用选择适合的产品，并且正确选择产品的风险由设计人员承担。设计人员单方面负责遵守与该等选择有关的所有法律或监管要求。

设计人员同意向 TI 及其代表全额赔偿因其不遵守本通知条款和条件而引起的任何损害、费用、损失和/或责任。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122
Copyright © 2018 德州仪器半导体技术（上海）有限公司