94 學年度全國大學院校積體電路設計競賽

E 組:大學組可程式邏輯

設計競賽初賽參考解答

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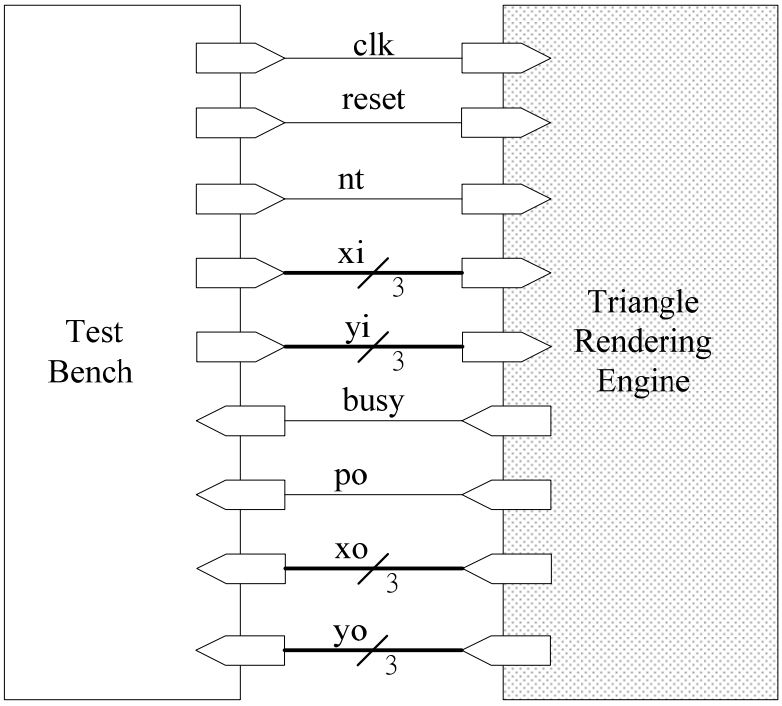
壹、說明

94 學年度可程式邏輯設計競賽初賽中，須完直角三角形(*Right-angled triangle*)之直角座標轉譯系統(*Rendering Engine*)。此直角三角形直角座標轉譯系統，將可於 testbench 所提供的直角三角形的三個頂點座標*(x1,y1),(x2,y2)*與*(x3,y3)*後，轉譯系統將依續完成涵蓋於直角三角形平面內的所有座標點之輸出。由於本試競賽並無區分參賽者所使用之不同 FPGA 及其相關軟體，因此本試題解答操作均以 Altera QuartusII 軟體工具做為示範之參考。

系統方塊圖及信號緻未說明如下圖一及表一所示，關於更詳盡的系統規格描述，請參考教育部主辦 94 學年度大學院校積體電路設計競賽可程式邏輯設計初賽之 *Right-angled triangle Rendering Engine* 試題題目。



圖一、系統方塊圖

表一、輸入/輸出訊號

Signal Name	Direction	Width	Description
reset	Input	1	高位準非同步之系統重置信號。
clk	input	1	時脈信號。此系統為同步於時脈正緣之同步設計。
nt	input	1	直角三角形座標的輸入標記。當 nt 信號為高位準，表示有 3 組直角三角形的頂點座標輸入。 (請注意!! 只有當 busy 信號為低位準時，nt 信號才能為高位準。)
xi	input	3	直角三角形頂點之 X 軸輸入。
yi	input	3	直角三角形座標之 Y 軸輸入。
busy	output	1	當 busy 信號為高位準時，表示直角三角形座標轉譯系統正在運作，並防止新的(下一個)直角三角形頂點座標輸入於系統中。
po	output	1	po 為有效的資料輸出指示信號。當信號 po 為高位準時，於 xo 及 yo 輸出埠所輸出之資料均為有效之座標軸資料。
xo	output	3	直角三角平面內所涵蓋的座標點 X 軸之輸出結果
yo	output	3	直角三角平面內所涵蓋的座標點 Y 軸之輸出結果

貳、暫存器轉換階層(RTL level)參考設計 (Verilog HDL)

本試題之參考解答原始碼如下所示。此原始碼未必是最佳化解，但完全符合試題題意，且能正確執行並完成試題要求之結果，僅供參賽者作為之設計參考。

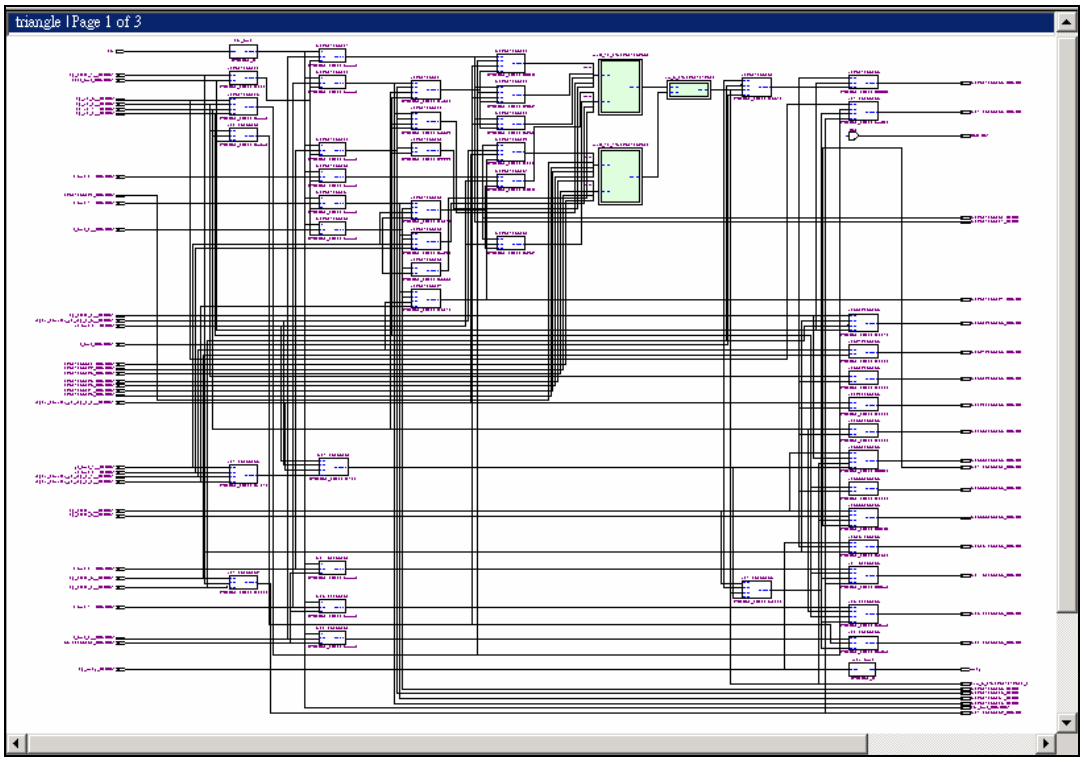
// triangle.v

```
module triangle(clk, reset, nt, xi, yi, busy, po,xo, yo, Lside); //, Rside);
input clk, reset, nt;
input [2:0] xi, yi;
output busy, po;
output [2:0] xo, yo;
output [7:0] Lside;

reg po;
reg [2:0] xo,yo;
reg busy;
reg [2:0] state;
reg [3:0] x1, x2, x3, xc, y1, y2, y3, yc;
parameter s0=3'b000, s1=3'b001, s2=3'b010, mv_r=3'b011, mv_u=3'b100, stop=3'b101;

reg [7:0] Lside;

always @(posedge clk)
begin
   if(reset)
   begin
      state=s0;
      busy=0;
      xc=0;
      yc=0;
      po=0;
   end
   else
   begin
      case(state)
         s0:
            begin
               if(nt)
```

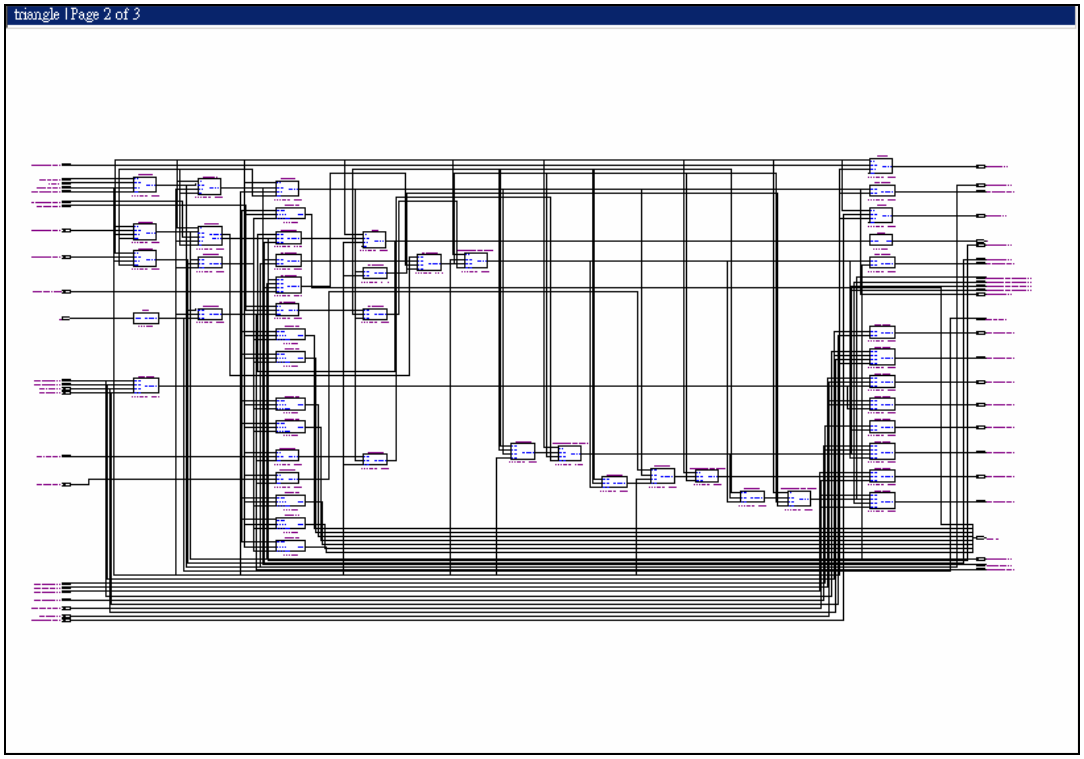
```
        begin
          x1={1'b0,xi}; // all positive
          y1={1'b0,yi}; // all positive
          state=s1;
        end
    end
  s1:
    begin
      x2={1'b0,xi}; // all positive
      y2={1'b0,yi}; // all positive
      state=s2;
      busy =1;
    end
  s2:
    begin
      x3={1'b0,xi}; // all positive
      y3={1'b0,yi}; // all positive
      xc=x1;    // start from left down corner
      yc=y1;
      state=mv_r;
    end
  mv_r:       // move_right
    begin
      xo=xc[2:0];
      yo=yc[2:0];
      po=1;
      xc=xc+1;

Lside = (x2-xc)*(y3-y2)- (yc-y2)*(x2-x3);
     if(Lside[7])       // Lside[5] sigh bit
      begin
        xc=x1;
        yc=yc+1;
        state=mv_u;
      end
    end
  mv_u:       // move_up
    begin
```

```
            xo=xc[2:0];
            yo=yc[2:0];
            xc=xc+1;

      Lside = (x2-xc)*(y3-y2)- (yc-y2)*(x2-x3);

            if(yc==y3)
               state=stop;
            else if(Lside[7])       // else if 此測試點是否超出線外, 若超出則直接跳stop, 否則跳mv_r
            begin
               xc=x1;
               yc=yc+1;
               state=mv_u;
            end
            else
               state=mv_r;


         end
       stop:
         begin
            busy = 0;
            po=0;
            xo=0;
            yo=0;
         end
     endcase
  end

end


endmodule
```

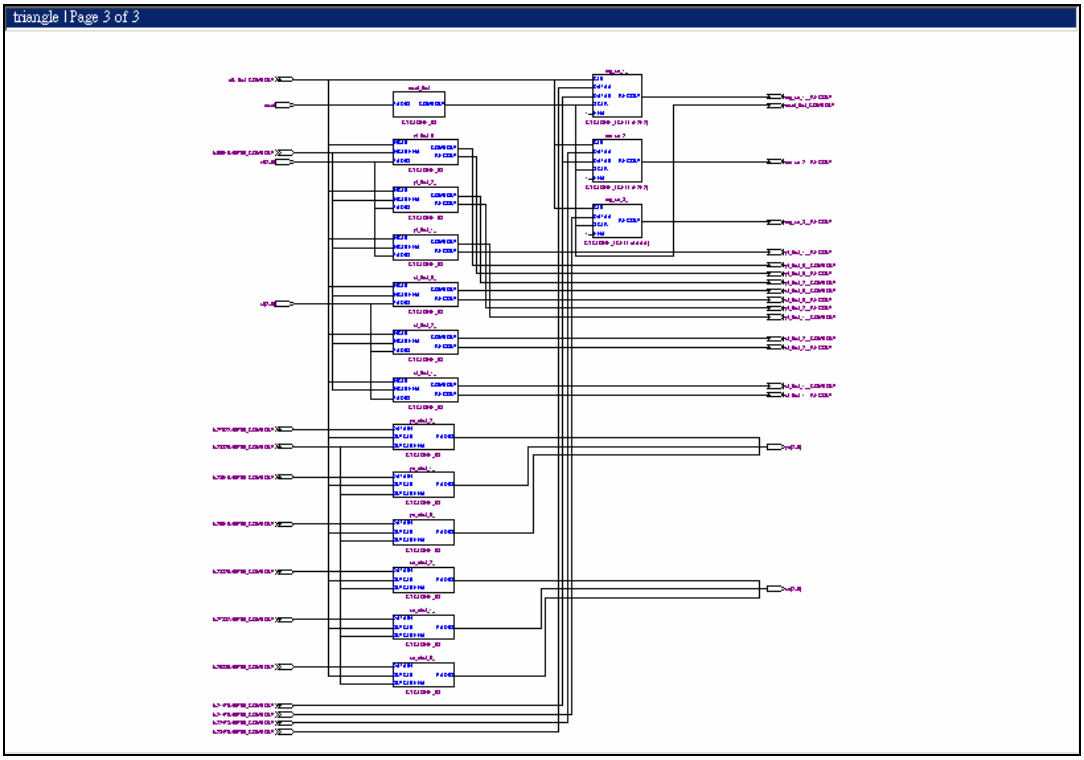
參、合成(Synthesis)結果



圖二、RTL Schematic View (1) (Quartus II)



圖三、RTL Schematic View (2) (Quartus II)



圖四、RTL Schematic View (3) (Quartus II)

肆、模擬(Simulation)結果

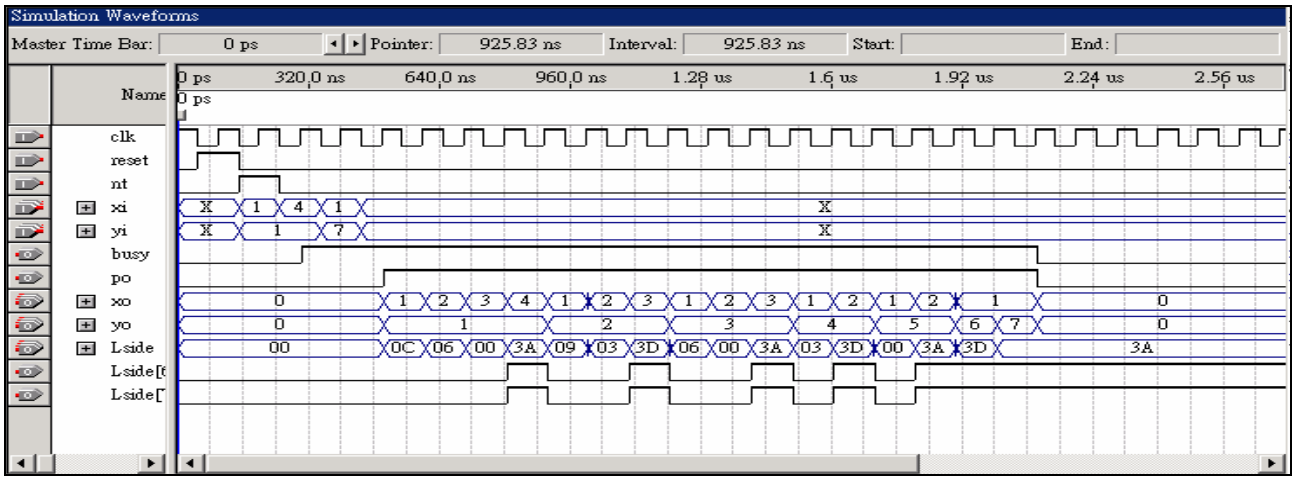
請設計者依據 *Right-angled triangle Rendering Engine* 試題題目之附錄 A-直角三角形座標轉譯系統測試樣本(Testbench)所提供之信號輸入樣本進行測試，並應產生相對之直角座標軸輸出結果。

直角三角形 A 之頂點座標輸入:

(1,1), (4,1) and (1,7)

直角三角形 A 平面內所涵蓋的座標點依序輸出如下:

(1,1), (1,2), (1,3), (1,4), (2,1), (2,2), (2,3), (3,1), (3,2), (3,3), (4,1), (4,2), (5,1), (5,2), (6,1), (7,1)



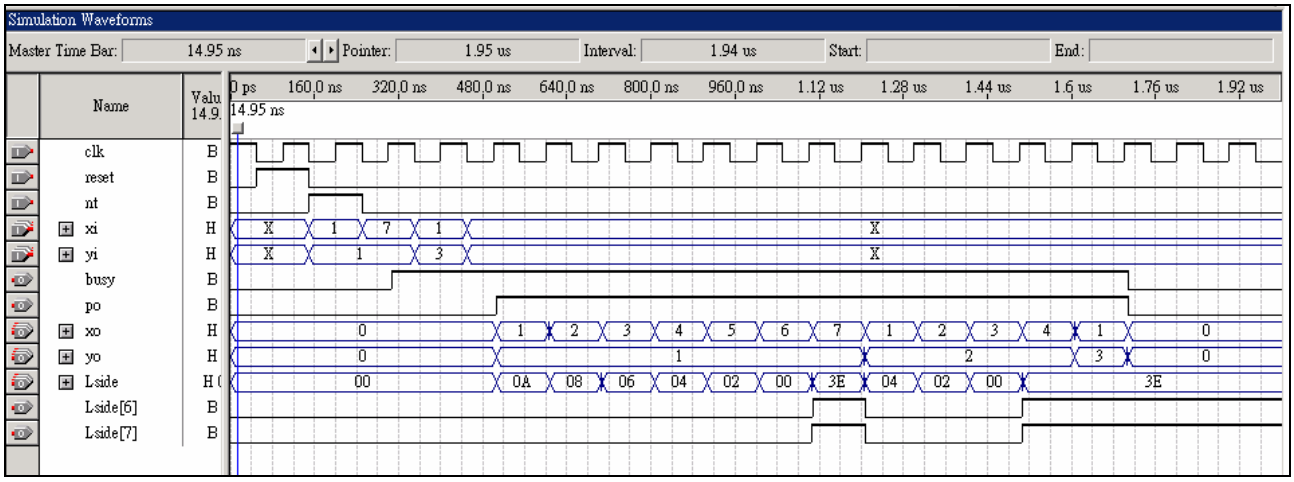
圖五、Post-layout Gate Level Simulation Waveform I (Quartus II)

直角三角形 B 之頂點座標輸入:

(1,1), (7,1) and (1,3)

直角三角形 B 平面內所涵蓋的座標點依序輸出如下:

(1,1), (1,2), (1,3), (1,4), (1,5), (1,6), (1,7), (2,1), (2,2), (2,3), (2,4), (3,1)



圖六、Post-layout Gate Level Simulation Waveform II (Quartus II)

伍、配置及繞線(Place & Route)結果

5.1 經由 QuartusII 5.0v 執行配置及繞線的文字訊息輸出結果如下所示。

```
Info: *******************************************************************
Info: Running Quartus II Analysis & Synthesis
    Info: Version 5.0 Build 148 04/26/2005 SJ Full Version
    Info: Processing started: Mon May 22 14:19:40 2006
Info: Command: quartus_map --read_settings_files=on --write_settings_files=off qts -c triangle
Info: Found 4 design units, including 4 entities, in source file triangle.edf
    Info: Found entity 1: mult_10_0
    Info: Found entity 2: mult_10_1
    Info: Found entity 3: sub_8_0
    Info: Found entity 4: triangle
Info: Elaborating entity "triangle" for the top level hierarchy
Info: Elaborating entity "sub_8_0" for hierarchy "sub_8_0:ix29521z19320"
Info: Elaborating entity "mult_10_0" for hierarchy "mult_10_0:ix29521z59360"
Info: Elaborating entity "mult_10_1" for hierarchy "mult_10_1:ix29521z59379"
Info: Resynthesizing 146 WYSIWYG logic cells and I/Os using "balanced" technology mapper which leaves 48
    WYSIWYG logic cells and I/Os untouched
Info: Implemented 199 device resources after synthesis - the final resource count might be different
    Info: Implemented 9 input pins
    Info: Implemented 16 output pins
    Info: Implemented 174 logic cells
Info: Quartus II Analysis & Synthesis was successful. 0 errors, 0 warnings
    Info: Processing ended: Mon May 22 14:19:44 2006
    Info: Elapsed time: 00:00:04
Info: *******************************************************************
Info: Running Quartus II Fitter
    Info: Version 5.0 Build 148 04/26/2005 SJ Full Version
    Info: Processing started: Mon May 22 14:19:47 2006
Info: Command: quartus_fit --read_settings_files=off --write_settings_files=off qts -c triangle
Info: Selected device EP1C3T100C8 for design "triangle"
Info: Fitter is performing an Auto Fit compilation, which may decrease Fitter effort to reduce compilation time
Info: Device migration not selected. If you intend to use device migration later, you may need to change the pin
    assignments as they may be incompatible with other devices.
Info: No exact pin location assignment(s) for 25 pins of 25 total pins
    Info: Pin busy not assigned to an exact location on the device
    Info: Pin Lside[0] not assigned to an exact location on the device
```

```
    Info: Pin Lside[1] not assigned to an exact location on the device
    Info: Pin Lside[2] not assigned to an exact location on the device
    Info: Pin Lside[3] not assigned to an exact location on the device
    Info: Pin Lside[4] not assigned to an exact location on the device
    Info: Pin Lside[5] not assigned to an exact location on the device
    Info: Pin Lside[6] not assigned to an exact location on the device
    Info: Pin Lside[7] not assigned to an exact location on the device
    Info: Pin po not assigned to an exact location on the device
    Info: Pin xo[0] not assigned to an exact location on the device
    Info: Pin xo[1] not assigned to an exact location on the device
    Info: Pin xo[2] not assigned to an exact location on the device
    Info: Pin yo[0] not assigned to an exact location on the device
    Info: Pin yo[1] not assigned to an exact location on the device
    Info: Pin yo[2] not assigned to an exact location on the device
    Info: Pin reset not assigned to an exact location on the device
    Info: Pin clk not assigned to an exact location on the device
    Info: Pin nt not assigned to an exact location on the device
    Info: Pin yi[2] not assigned to an exact location on the device
    Info: Pin yi[0] not assigned to an exact location on the device
    Info: Pin yi[1] not assigned to an exact location on the device
    Info: Pin xi[0] not assigned to an exact location on the device
    Info: Pin xi[1] not assigned to an exact location on the device
    Info: Pin xi[2] not assigned to an exact location on the device
Info: Timing requirements not specified -- optimizing circuit to achieve the following default global requirements
    Info: Assuming a global fmax requirement of 1 MHz
    Info: Not setting a global tsu requirement
    Info: Not setting a global tco requirement
    Info: Not setting a global tpd requirement
Info: Performing register packing on registers with non-logic cell location assignments
Info: Completed register packing on registers with non-logic cell location assignments
Info: Completed User Assigned Global Signals Promotion Operation
Info: DQS I/O pins require 0 global routing resources.
Info: Automatically promoted signal "clk" to use Global clock in PIN 10
Info: Completed Auto Global Promotion Operation
Info: Starting register packing
Info: Started Fast Input/Output/OE register processing
Info: Finished Fast Input/Output/OE register processing
Info: Fitter is using Normal packing mode for logic elements with Auto setting for Auto Packed Registers logic option
Info: Moving registers into I/O cells, LUTs, and RAM blocks to improve timing and density
Info: Finished moving registers into I/O cells, LUTs, and RAM blocks
```

Info: Finished register packing
Info: Statistics of I/O pins that need to be placed that use the same VCCIO and VREF, before I/O pin placement
    Info: Number of I/O pins in group: 24 (unused VREF, 3.30 VCCIO, 8 input, 16 output, 0 bidirectional)
    Info: I/O standards used: LVTTL.
Info: I/O bank details before I/O pin placement
    Info: Statistics of I/O banks
    Info: I/O bank number 1 does not use VREF pins and has unused VCCIO pins. 3 total pin(s) used -- 11 pins available
    Info: I/O bank number 2 does not use VREF pins and has unused VCCIO pins. 0 total pin(s) used -- 17 pins available
    Info: I/O bank number 3 does not use VREF pins and has unused VCCIO pins. 0 total pin(s) used -- 17 pins available
    Info: I/O bank number 4 does not use VREF pins and has unused VCCIO pins. 0 total pin(s) used -- 17 pins available
Info: Fitter placement preparation operations beginning
Info: Fitter placement preparation operations ending: elapsed time is 00:00:00
Info: Fitter placement operations beginning
Info: Fitter placement was successful
Info: Estimated most critical path is register to register delay of 14.931 ns
Info: 1: + IC(0.000 ns) + CELL(0.000 ns) = 0.000 ns; Loc. = LAB_X25_Y10; Fanout = 11; REG Node = 'y2_0_'
Info: 2: + IC(1.259 ns) + CELL(0.590 ns) = 1.849 ns; Loc. = LAB_X21_Y11; Fanout = 4; COMB Node = 'ix29521z55783~110'
Info: 3: + IC(0.604 ns) + CELL(0.114 ns) = 2.567 ns; Loc. = LAB_X21_Y11; Fanout = 7; COMB Node = 'ix29521z55781~109'
Info: 4: + IC(1.137 ns) + CELL(0.590 ns) = 4.294 ns; Loc. = LAB_X26_Y10; Fanout = 2; COMB Node = 'mult_10_0:ix29521z59360|ix44952z55796~1'
Info: 5: + IC(1.601 ns) + CELL(0.692 ns) = 6.587 ns; Loc. = LAB_X22_Y11; Fanout = 2; COMB Node = 'mult_10_0:ix29521z59360|nx44952z38'
Info: 6: + IC(0.000 ns) + CELL(0.679 ns) = 7.266 ns; Loc. = LAB_X22_Y11; Fanout = 3; COMB Node = 'mult_10_0:ix29521z59360|nx44952z37'
Info: 7: + IC(0.769 ns) + CELL(0.442 ns) = 8.477 ns; Loc. = LAB_X21_Y11; Fanout = 3; COMB Node = 'mult_10_0:ix29521z59360|nx43955z1'
Info: 8: + IC(1.255 ns) + CELL(0.432 ns) = 10.164 ns; Loc. = LAB_X20_Y10; Fanout = 2; COMB Node = 'sub_8_0:ix29521z19320|nx44952z2~COUT1_1'
Info: 9: + IC(0.000 ns) + CELL(0.608 ns) = 10.772 ns; Loc. = LAB_X20_Y10; Fanout = 4; COMB Node = 'sub_8_0:ix29521z19320|nx44952z1'
Info: 10: + IC(0.301 ns) + CELL(0.590 ns) = 11.663 ns; Loc. = LAB_X19_Y10; Fanout = 5; COMB Node = 'ix21476z55766~133'
Info: 11: + IC(1.582 ns) + CELL(0.114 ns) = 13.359 ns; Loc. = LAB_X24_Y10; Fanout = 1; COMB Node = 'reg_xc_1_~207'

```
Info: 12: + IC(1.263 ns) + CELL(0.309 ns) = 14.931 ns; Loc. = LAB_X24_Y11; Fanout = 7; REG Node = 'xc_1_'
Info: Total cell delay = 5.160 ns ( 34.56 % )
Info: Total interconnect delay = 9.771 ns ( 65.44 % )
Info: Fitter placement operations ending: elapsed time is 00:00:00
Info: Fitter routing operations beginning
Info: Fitter routing operations ending: elapsed time is 00:00:00
Info: Fitter performed an Auto Fit compilation. Optimizations were skipped to reduce compilation time.
Info: Completed Fixed Delay Chain Operation
Info: Started post-fitting delay annotation
Info: Delay annotation completed successfully
Info: Completed Auto Delay Chain Operation
Info: Quartus II Fitter was successful. 0 errors, 0 warnings
Info: Processing ended: Mon May 22 14:19:54 2006
Info: Elapsed time: 00:00:08
Info: ******************************************************************
Info: Running Quartus II Assembler
Info: Version 5.0 Build 148 04/26/2005 SJ Full Version
Info: Processing started: Mon May 22 14:19:55 2006
Info: Command: quartus_asm --read_settings_files=off --write_settings_files=off qts -c triangle
Info: Quartus II Assembler was successful. 0 errors, 0 warnings
Info: Processing ended: Mon May 22 14:19:57 2006
Info: Elapsed time: 00:00:02
Info: ******************************************************************
Info: Running Quartus II Timing Analyzer
Info: Version 5.0 Build 148 04/26/2005 SJ Full Version
Info: Processing started: Mon May 22 14:19:58 2006
Info: Command: quartus_tan --read_settings_files=off --write_settings_files=off qts -c triangle
--timing_analysis_only
Info: Clock "clk" has Internal fmax of 56.91 MHz between source register "y2_0_" and destination register "xc_1_"
(period= 17.571 ns)
Info: + Longest register to register delay is 17.310 ns
Info: 1: + IC(0.000 ns) + CELL(0.000 ns) = 0.000 ns; Loc. = LC_X25_Y10_N7; Fanout = 11; REG Node = 'y2_0_'
Info: 2: + IC(2.265 ns) + CELL(0.590 ns) = 2.855 ns; Loc. = LC_X21_Y11_N9; Fanout = 4; COMB Node =
'ix29521z55783~110'
Info: 3: + IC(0.435 ns) + CELL(0.590 ns) = 3.880 ns; Loc. = LC_X21_Y11_N8; Fanout = 7; COMB Node =
'ix29521z55781~109'
Info: 4: + IC(1.556 ns) + CELL(0.590 ns) = 6.026 ns; Loc. = LC_X26_Y10_N2; Fanout = 2; COMB Node =
'mult_10_0:ix29521z59360|ix44952z55796~1'
Info: 5: + IC(1.549 ns) + CELL(0.583 ns) = 8.158 ns; Loc. = LC_X22_Y11_N4; Fanout = 2; COMB Node =
'mult_10_0:ix29521z59360|nx44952z38'
```

Info: 6: + IC(0.000 ns) + CELL(0.621 ns) = 8.779 ns; Loc. = LC_X22_Y11_N5; Fanout = 3; COMB Node = 'mult_10_0:ix29521z59360|nx44952z37'
Info: 7: + IC(1.098 ns) + CELL(0.442 ns) = 10.319 ns; Loc. = LC_X21_Y11_N6; Fanout = 3; COMB Node = 'mult_10_0:ix29521z59360|nx43955z1'
Info: 8: + IC(1.229 ns) + CELL(0.575 ns) = 12.123 ns; Loc. = LC_X20_Y10_N6; Fanout = 2; COMB Node = 'sub_8_0:ix29521z19320|nx44952z2~COUT1_1'
Info: 9: + IC(0.000 ns) + CELL(0.608 ns) = 12.731 ns; Loc. = LC_X20_Y10_N7; Fanout = 4; COMB Node = 'sub_8_0:ix29521z19320|nx44952z1'
Info: 10: + IC(0.856 ns) + CELL(0.292 ns) = 13.879 ns; Loc. = LC_X19_Y10_N3; Fanout = 5; COMB Node = 'ix21476z55766~133'
Info: 11: + IC(1.548 ns) + CELL(0.114 ns) = 15.541 ns; Loc. = LC_X24_Y10_N5; Fanout = 1; COMB Node = 'reg_xc_1_~207'
Info: 12: + IC(1.291 ns) + CELL(0.478 ns) = 17.310 ns; Loc. = LC_X24_Y11_N1; Fanout = 7; REG Node = 'xc_1_'
Info: Total cell delay = 5.483 ns (31.68 %)
Info: Total interconnect delay = 11.827 ns (68.32 %)
Info: - Smallest clock skew is 0.000 ns
Info: + Shortest clock path from clock "clk" to destination register is 2.781 ns
Info: 1: + IC(0.000 ns) + CELL(1.469 ns) = 1.469 ns; Loc. = PIN_10; Fanout = 48; CLK Node = 'clk'
Info: 2: + IC(0.601 ns) + CELL(0.711 ns) = 2.781 ns; Loc. = LC_X24_Y11_N1; Fanout = 7; REG Node = 'xc_1_'
Info: Total cell delay = 2.180 ns (78.39 %)
Info: Total interconnect delay = 0.601 ns (21.61 %)
Info: - Longest clock path from clock "clk" to source register is 2.781 ns
Info: 1: + IC(0.000 ns) + CELL(1.469 ns) = 1.469 ns; Loc. = PIN_10; Fanout = 48; CLK Node = 'clk'
Info: 2: + IC(0.601 ns) + CELL(0.711 ns) = 2.781 ns; Loc. = LC_X25_Y10_N7; Fanout = 11; REG Node = 'y2_0_'
Info: Total cell delay = 2.180 ns (78.39 %)
Info: Total interconnect delay = 0.601 ns (21.61 %)
Info: + Micro clock to output delay of source is 0.224 ns
Info: + Micro setup delay of destination is 0.037 ns
Info: tsu for register "xc_2_" (data pin = "reset", clock pin = "clk") is 8.561 ns
Info: + Longest pin to register delay is 11.305 ns
Info: 1: + IC(0.000 ns) + CELL(1.475 ns) = 1.475 ns; Loc. = PIN_78; Fanout = 23; PIN Node = 'reset'
Info: 2: + IC(5.957 ns) + CELL(0.590 ns) = 8.022 ns; Loc. = LC_X24_Y9_N7; Fanout = 4; COMB Node = 'reg_xc_0_~144'
Info: 3: + IC(1.273 ns) + CELL(0.442 ns) = 9.737 ns; Loc. = LC_X24_Y10_N4; Fanout = 1; COMB Node = 'reg_xc_2_~82'
Info: 4: + IC(1.259 ns) + CELL(0.309 ns) = 11.305 ns; Loc. = LC_X23_Y11_N9; Fanout = 4; REG Node = 'xc_2_'
Info: Total cell delay = 2.816 ns (24.91 %)
Info: Total interconnect delay = 8.489 ns (75.09 %)
Info: + Micro setup delay of destination is 0.037 ns
Info: - Shortest clock path from clock "clk" to destination register is 2.781 ns

Info: 1: + IC(0.000 ns) + CELL(1.469 ns) = 1.469 ns; Loc. = PIN_10; Fanout = 48; CLK Node = 'clk'
Info: 2: + IC(0.601 ns) + CELL(0.711 ns) = 2.781 ns; Loc. = LC_X23_Y11_N9; Fanout = 4; REG Node = 'xc_2_'
Info: Total cell delay = 2.180 ns (78.39 %)
Info: Total interconnect delay = 0.601 ns (21.61 %)
Info: tco from clock "clk" to destination pin "Lside[5]" through register "Lside_obuf_5_~0" is 7.750 ns
Info: + Longest clock path from clock "clk" to source register is 2.781 ns
Info: 1: + IC(0.000 ns) + CELL(1.469 ns) = 1.469 ns; Loc. = PIN_10; Fanout = 48; CLK Node = 'clk'
Info: 2: + IC(0.601 ns) + CELL(0.711 ns) = 2.781 ns; Loc. = LC_X20_Y10_N5; Fanout = 1; REG Node = 'Lside_obuf_5_~0'
Info: Total cell delay = 2.180 ns (78.39 %)
Info: Total interconnect delay = 0.601 ns (21.61 %)
Info: + Micro clock to output delay of source is 0.224 ns
Info: + Longest register to pin delay is 4.745 ns
Info: 1: + IC(0.000 ns) + CELL(0.000 ns) = 0.000 ns; Loc. = LC_X20_Y10_N5; Fanout = 1; REG Node = 'Lside_obuf_5_~0'
Info: 2: + IC(2.637 ns) + CELL(2.108 ns) = 4.745 ns; Loc. = PIN_40; Fanout = 0; PIN Node = 'Lside[5]'
Info: Total cell delay = 2.108 ns (44.43 %)
Info: Total interconnect delay = 2.637 ns (55.57 %)
Info: th for register "y3_0_" (data pin = "yi[0]", clock pin = "clk") is -3.784 ns
Info: + Longest clock path from clock "clk" to destination register is 2.781 ns
Info: 1: + IC(0.000 ns) + CELL(1.469 ns) = 1.469 ns; Loc. = PIN_10; Fanout = 48; CLK Node = 'clk'
Info: 2: + IC(0.601 ns) + CELL(0.711 ns) = 2.781 ns; Loc. = LC_X24_Y11_N2; Fanout = 7; REG Node = 'y3_0_'
Info: Total cell delay = 2.180 ns (78.39 %)
Info: Total interconnect delay = 0.601 ns (21.61 %)
Info: + Micro hold delay of destination is 0.015 ns
Info: - Shortest pin to register delay is 6.580 ns
Info: 1: + IC(0.000 ns) + CELL(1.469 ns) = 1.469 ns; Loc. = PIN_73; Fanout = 3; PIN Node = 'yi[0]'
Info: 2: + IC(4.996 ns) + CELL(0.115 ns) = 6.580 ns; Loc. = LC_X24_Y11_N2; Fanout = 7; REG Node = 'y3_0_'
Info: Total cell delay = 1.584 ns (24.07 %)
Info: Total interconnect delay = 4.996 ns (75.93 %)
Info: Quartus II Timing Analyzer was successful. 0 errors, 1 warning
Info: Processing ended: Mon May 22 14:19:59 2006
Info: Elapsed time: 00:00:01
Info: Quartus II Full Compilation was successful. 0 errors, 0 warning

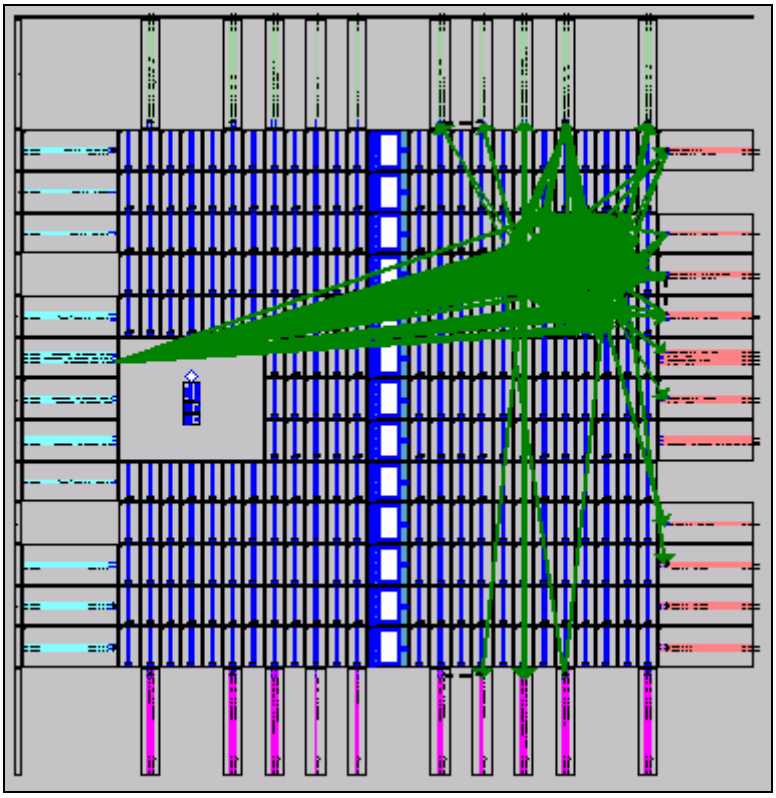
5.2 經由 QuartusII 4.2v 執行配置及繞線後之晶片內部資源使用率如圖七及圖八所示。圖九則為 Floorplan View 之輸出結果。

Analysis & Synthesis Resource Usage Summary		
	Resource	Usage
1	Total logic elements	174
2	Total combinational functions	146
3	-- Total 4-input functions	51
4	-- Total 3-input functions	31
5	-- Total 2-input functions	60
6	-- Total 1-input functions	4
7	-- Total 0-input functions	0
8	Combinational cells for routing	0
9	Total registers	48
10	Total logic cells in carry chains	48
11	I/O pins	25
12	Maximum fan-out node	clk
13	Maximum fan-out	48
14	Total fan-out	592
15	Average fan-out	2.97

圖七、Analysis & Synthesis Resource Usage Summary

Flow Status	Successful - Wed Mar 22 14:20:22 2006
Quartus II Version	5.0 Build 148 04/26/2005 SJ Full Version
Revision Name	triangle
Top-level Entity Name	triangle
Family	Cyclone
Device	EP1C3T100C8
Timing Models	Final
Met timing requirements	Yes
Total logic elements	148 / 2,910 (5 %)
Total pins	25 / 65 (38 %)
Total virtual pins	0
Total memory bits	0 / 59,904 (0 %)
Total PLLs	0 / 1 (0 %)

圖八、Fitter Summary



圖九、FPGA Floorplan View (QuartusII 5.0v / Device:EPM1270T144C5ES)