2020 Digital IC Design Homework 2: Divider

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Simulation Result

Functional simulation	Pass	Gate-level simulation	Pass	Gate-level simulation time	6553610 (ns)

```
#       65529 data is correct
#       65530 data is correct
#       65531 data is correct
#       65532 data is correct
#       65533 data is correct
#       65534 data is correct
#       65535 data is correct
#       65536 data is correct
# --------------------PASS--------------------
# All data have been generated successfully!
# ** Note: $finish    : D:/Code/git/DIGITAL-IC-DESIGN/I
#    Time: 6553610 ns  Iteration: 0  Instance: /div_tb
```


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```


Synthesis Result

Total logic elements	302 / 68,416 (< 1 %)
Total memory bit	0 / 1,152,000 (0 %)
Embedded multiplier 9-bit element	0 / 300 (0 %)

Flow Status	Successful - Tue Apr 07 14:57:56 2020
Quartus II Version	10.0 Build 262 08/18/2010 SP 1 SJ Full Version
Revision Name	div
Top-level Entity Name	div
Family	Cyclone II
Device	EP2C70F896C8
Timing Models	Final
Met timing requirements	Yes
Total logic elements	302 / 68,416 (< 1 %)
Total combinational functions	302 / 68,416 (< 1 %)
Dedicated logic registers	0 / 68,416 (0 %)
Total registers	0
Total pins	25 / 622 (4 %)
Total virtual pins	0
Total memory bits	0 / 1,152,000 (0 %)
Embedded Multiplier 9-bit elements	0 / 300 (0 %)
Total PLLs	0 / 4 (0 %)

Description of your design

參考了這個網站的演算法 https://ithelp.ithome.com.tw/articles/10161144，利用兩個 16bit reg 儲存{8’ d0, in1}(餘數)、{in2, 8’ d0}(除數)，若是餘數>=除數，餘數-除數，除數>>1，且把 out<<1 之後 out[0]=1，反之若是餘數<除數，除數>>1，out<<1 之後 out[0]=0，總共做 8+1 次之後就會得到結果

*Scoring = (Total logic elements + total memory bit + 9*embedded multiplier 9-bit element) × (gate-level simulation time in ns)*