2020 Digital IC Design Homework 1: 4-bit binary adder-subtractor

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| NAME | | 崔濟鵬 | | | | | | |
| Student ID | | F74056069 | | | | | | |
| **Simulation Result** | | | | | | | | |
| Functional simulation | Pass | | Gate-level simulation | Pass | | | Gate-level simulation time | 25700 (ns) |
|  | | | | | |  | | |
| **Synthesis Result** | | | | | | | | |
| Total logic elements | | | | | 8 / 68,416 ( < 1 % ) | | | |
| Total memory bit | | | | | 0 / 1,152,000 ( 0 % ) | | | |
| Embedded multiplier 9-bit element | | | | | 0 / 300 ( 0 % ) | | | |
|  | | | | | | | | |
| **Description of your design** | | | | | | | | |
| 用了三個wire來儲存B xor sel, A xor B, C，因為每個FA前都會將B xor sel後，當成FA的B輸入，故先用4個xor()來運算給4個FA的B，而在FA中會重複利用到A xor B運算S跟C，故一樣用4個xor()來運算FA中的A xor B，最終使用assign來算4組S跟C，O為C[2] xor C[3] | | | | | | | | |

*Scoring = (Total logic elements + total memory bit + 9\*embedded multiplier 9-bit element) (gate-level simulation time in ns)*