2020 Digital IC Design Homework 2: Divider

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| NAME | | 崔濟鵬 | | | | | | |
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| **Simulation Result** | | | | | | | | |
| Functional simulation | Pass | | Gate-level simulation | Pass | | | Gate-level simulation time | 6553610 (ns) |
|  | | | | | |  | | |
| **Synthesis Result** | | | | | | | | |
| Total logic elements | | | | | 302 / 68,416 ( < 1 % ) | | | |
| Total memory bit | | | | | 0 / 1,152,000 ( 0 % ) | | | |
| Embedded multiplier 9-bit element | | | | | 0 / 300 ( 0 % ) | | | |
|  | | | | | | | | |
| **Description of your design** | | | | | | | | |
| 參考了這個網站的演算法<https://ithelp.ithome.com.tw/articles/10161144>，利用兩個16bit reg儲存{8’d0, in1}(餘數)、{in2, 8’d0}(除數)，若是餘數>=除數，餘數-除數，除數>>1，且把out<<1之後out[0]=1，反之若是餘數<除數，除數>>1，out<<1之後out[0]=0，總共做8+1次之後就會得到結果 | | | | | | | | |

*Scoring = (Total logic elements + total memory bit + 9\*embedded multiplier 9-bit element) (gate-level simulation time in ns)*