

**AEC – Q005 - REV-**  
**PB-FREE TEST REQUIREMENTS**

**Automotive Electronics Council****Component Technical Committee****Acknowledgment**

Any document involving a complex technology brings together experience and skills from many sources. The Automotive Electronics Council would especially like to recognize the following significant contributors to the development and initial release of this document:

**Sustaining Members:**

Earl Fischer	Autoliv	Gary Fisher	Johnson Controls
Mark A. Kelly	Delphi Corporation	Thomas VanDamme	TRW Automotive
Bob Hulka, Jr.	Delphi Corporation	Larry Dudley	TRW Automotive
Rick Forster	Continental Corporation	Robert V. Knoell	Visteon Corporation
Hadi Mehrooz	Continental Corporation	Ken Kirby, Jr.	Visteon Corporation
Jim Peace	Continental Corporation	Ron Haberl	Visteon Corporation

**Technical Members:**

Tim Haifley	Altera	James Williams	Texas Instruments
James Molyneaux	Analog Devices	Diana Siddall	Texas Instruments
Mike Gibson	Analog Devices	Guillemette Paour	Tyco Electronics
Heinz Reiter	Austriamicrosystems	Robert Cid	Tyco Electronics
Herwig Klimesch	Austriamicrosystems	Ted Krueger	Vishay
Mike Klucher	Cirrus Logic	Arthur Chiang	Vishay
Xin Miao Zhao	Cirrus Logic	Anca Voicu	Xilinx
Rene Rodgers	Cypress Semiconductor	Daniel Joo	Xilinx
Fred Whitwer	Cypress Semiconductor		
George Platko	Fairchild Semiconductor		
Joe Fazio	Fairchild Semiconductor		
Nick Lycoudes	Freescale	<b><u>Associate Members:</u></b>	
Kenton Van Klompenberg	Gentex	Andrew Yap	Grace Semiconductor
Werner Kanert	Infineon Technologies	Arthur Cheng	Grace Semiconductor
Alexander Mueller	Infineon Technologies	Kuotung Cheng	TSMC
John Bertaux	International Rectifier	Ken Wu	TSMC
Lyn Zastrow	ISSI		
Banjie Bautista	ISSI	<b><u>Guest Members:</u></b>	
Peter Blais	Kemet	David Locker	AMRDEC
Holger Zillgen	Kemet	Jeff Jarvis	AMRDEC
Tom Lawler	Lattice Semiconductor		
Sohail Malik	Lattice Semiconductor		
Joe Wurts	Maxim	<b><u>Other Contributors:</u></b>	
Tom Tobin	Maxim	Maurice Brodeur	Analog Devices
Mike Buzinski	Microchip	Brian Jendro	Continental Corporation
Nick Martinez	Microchip	John Timms	Continental Corporation
Annette Nettles	NEC Electronics	Jeff Price	Delphi Corporation
Tony Walsh	NEC Electronics	Marc Dittes	Infineon
Michael Wieberneit	NEC Electronics	Harry Sax	Infineon
Zhongning Liang	NXP Semiconductors	Mary Carter-Barrios	Kemet
Di Bayes	NXP Semiconductors	Masamichi Murase	NEC Electronics
Mark Gabrielle	ON Semiconductor	Pascal Oberndorff	NXP Semiconductors
Daniel Vanderstraeten	ON Semiconductor	Bruce Townsend	Spanion
Ken Berry	Renesas Technology	Michael Hundt	STMicroelectronics
Francis Classe	Spanion	Harry Siegel	STMicroelectronics
Adam Fogle	Spanion	Doug Romm	Texas Instruments
Brian Mielewski	STMicroelectronics	John Kampell	Texas Instruments
Steve Maloy	TDK	Patrick Neyman	Tyco Electronics
Richard Tse	TDK	Huixian Wu	Vishay
		Bill Hopfe	Visteon Corporation

# **Automotive Electronics Council**

**Component Technical Committee**

## **NOTICE**

AEC documents contain material that has been prepared, reviewed, and approved through the AEC Technical Committee.

AEC documents are designed to serve the automotive electronics industry through eliminating misunderstandings between manufacturers and purchasers, facilitating interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining with minimum delay the proper product for use by those other than AEC members, whether the standard is to be used either domestically or internationally.

AEC documents are adopted without regard to whether or not their adoption may involve patents or articles, materials, or processes. By such action AEC does not assume any liability to any patent owner, nor does it assume any obligation whatever to parties adopting the AEC documents. The information included in AEC documents represents a sound approach to product specification and application, principally from the automotive electronics system manufacturer viewpoint. No claims to be in conformance with this document shall be made unless all requirements stated in the document are met.

Inquiries, comments, and suggestions relative to the content of this AEC document should be addressed to the AEC Technical Committee on the link <http://www.aecouncil.com>.

Published by the Automotive Electronics Council.

This document may be downloaded free of charge, however AEC retains the copyright on this material. By downloading this file, the individual agrees not to charge for or resell the resulting material.

Printed in the U.S.A.

All rights reserved

Copyright © 2009 by the Automotive Electronics Council. This document may be freely reprinted with this copyright notice. This document cannot be changed without approval from the AEC Component Technical Committee.

# Automotive Electronics Council

---

Component Technical Committee

## PB-FREE TEST REQUIREMENTS

### 1. SCOPE

This document contains a set of tests and defines the minimum requirements for qualification of lead free (Pb-free) metallurgy for components to be used in any automotive electronics application. For a component to be considered Pb-free compatible, its properties, including but not limited to plating materials and package configuration, must be compatible with Pb-free manufacturing processes. Use of this document does not relieve the supplier of their responsibility to meet their own company's internal qualification program. In this document, "user" is defined as all customers using a component qualified per this specification. The user is responsible to confirm and validate all qualification data that substantiates conformance to this document.

#### 1.1 Purpose

The purpose of this specification is to determine that a component is capable of passing the specified stress tests and thus can be expected to give a certain level of quality/reliability in the application. The science of whisker growth, including growth models and accelerated test methods, is not fully understood at the time of release of this standard. Further, the existence of tin whiskers over time does not ensure component or system failure. The environmental tests specified in this document for whisker growth evaluation require conditions of temperature, humidity and temperature cycling which are currently believed to best exacerbate whisker growth in Sn-plated leads and terminations. The user and supplier need to consider the applicable risks when using components with Sn-plated leads in sensitive applications.

#### 1.2 Reference Documents

Current revision of the referenced documents will be in effect at the date of agreement to the qualification plan. Subsequent qualification plans will automatically use updated revisions of these referenced documents.

##### 1.2.1 JEDEC

JESD201 Environmental Acceptance Requirements for Tin Whisker Susceptibility of Tin and Tin Alloy Surface Finishes  
JESD22-A104 Temperature Cycling  
JESD22-A111 Evaluation Procedure for Determining Capability to Bottom Side Board Attach by Full Body Solder Immersion of Small Surface Mount Solid State Devices  
JESD22-A113 Preconditioning of Nonhermetic Surface Mount Devices Prior to Reliability Testing  
JESD22-A121 Test Method for Measuring Whisker Growth on Tin and Tin Alloy Surface Finishes  
JESD22-B102 Solderability  
JESD22-B106 Resistance to Solder Heat  
JP002 Current Tin Whiskers Theory and Mitigation Practices Guideline

##### 1.2.2 IPC/JEDEC

J-STD-020 Moisture/Reflow Sensitivity Classification for Plastic Integrated Circuit Surface Mount Devices

##### 1.2.3 EIA/IPC/JEDEC

EIA/IPC/JEDEC J-STD-075 - Classification of Non-IC Electronic Components for Assembly Processes

# Automotive Electronics Council

---

## Component Technical Committee

### 1.3 Terms and Definitions

**1.3.1 Lead Free (Pb-free) Plating Finish:** A component plating finish is considered Pb-free if the following requirements are met:

- a. Complies with the latest version of the Global Automotive Declarable Substance List (GADSL). Refer to GADSL ([www.gadsl.org](http://www.gadsl.org)) for detailed requirements and exemptions.
- b. Is compliant to Pb-free board assembly process reflow profile(s) and material(s) as required herein.

### 1.3.2 Preferred Pb-Free Finishes

Due to the risk of Sn whiskers, non Sn-based finishes may be preferred. However, solderability performance may indicate a preference of (matte) Sn plating. Therefore, careful consideration must be given to the plating finish material and the intended component manufacturing process.

A verified whisker mitigation practice is required when Sn-based finishes are used, unless otherwise agreed between user and supplier on a case-by-case basis. Refer to Section 5 of JP002 for information and examples of verified mitigation practices.

### 1.3.3 Restricted Pb-Free Finishes

**1.3.3.1 Tin-Bismuth (SnBi) alloy finishes containing greater than 5% Bismuth may not be acceptable for use in SnPb solder processes** due to the formation of a low-melting point ternary eutectic compound (SnPbBi). Refer to JP002 for details on SnBi. Use of SnBi alloy finishes in SnPb solder processes requires user approval and must meet the requirements stated in this specification.

**1.3.3.2 Plated Tin-Copper (SnCu) alloy finishes are not acceptable for use in any solder process** due to enhanced whisker formation and growth resulting from the introduction of Copper. Refer to JP002 for details on SnCu. Use of SnCu alloy finishes requires user approval and must meet the requirements stated in this specification.

## 2. EQUIPMENT

Not Applicable

## 3. QUALIFICATION TESTS

When a component involves Pb-free and/or Pb-free compatible materials, certain tests (as defined in this document) must be performed and resulting data submitted for review before the component can be approved for use. These tests are in addition to all electrical/mechanical testing required in the applicable part specification and include solderability, resistance to solder heat (if applicable), moisture sensitivity (MSL), and Sn whisker testing. Where applicable, tests should include exposure to and/or use of standard SnPb (e.g., Sn60/Pb40, Sn63/Pb37, Sn25/Pb75, etc.) and Pb-free (SAC305 or similar Pb-free alloy with liquidus of 217°C to 227°C) solder to examine and confirm forward and backward assembly compatibility of the Pb-free components. **The user must approve any deviation from the test requirements defined herein.**

# Automotive Electronics Council

## Component Technical Committee

### 3.1 Solderability

All plated component terminations and/or surfaces shall be tested for solderability per JESD22-B102. All through-hole components shall be solderability tested using the "Dip and Look" method.

All coarse pitch (external lead pitch > 0.5mm) Surface mount components shall be tested using either the "Surface Mount Process Simulation Test" method or "Dip and Look" test method. It is recommended that all fine external lead pitch ( $\leq$  0.5mm) surface mount components be tested using the "Surface Mount Process Simulation Test" method due to solder bridging issues. If "Dip and Look" is used for fine pitch components, a technique for addressing solder bridging must be documented and included in the test report defined in Section 3.5.

Issues have been observed with the Dip and Look Test for certain metallurgies and package configurations. For these cases, the Surface Mount Process Simulation Test should also be performed as verification.

All exceptions to the applicable test method(s) must be noted in the part specification.

#### 3.1.1 Preconditioning

All components are to be preconditioned according to conditions A, C, or E per JESD22-B102 (see Table 1 for exposure requirements). Refer to the applicable AEC Stress Test Qualification document (e.g., Q100, Q101, and/or Q200) for required precondition type.

**Table 1: Preconditioning Requirements**

Condition	Precondition Type	Exposure Time	Leadfinish Material
A	Steam Precondition	1 Hour $\pm$ 5 min.	nontin and nontin-alloy
C		8 Hours $\pm$ 15 min.	tin and tin-alloy
E *	150°C Dry Bake	16 Hours $\pm$ 30 min.	Alternative to steam precondition

\* **Note:** Refer to the applicable AEC Stress Test Qualification document (e.g., Q100, Q101, and/or Q200) to determine if Dry Bake precondition is allowed.

#### 3.1.2 Solderability - Dip and Look Test

Solderability testing using the Dip and Look test method shall be performed per JESD22-B102 Method 1 and shall include both Pb-free and backward compatibility (SnPb) test conditions.

#### 3.1.3 Solderability - Surface Mount Process Simulation Test

Solderability testing using the Surface Mount Process Simulation Test method shall be performed per JESD22-B102 Method 2 and shall include both Pb-free and backward compatibility (SnPb) test conditions. Unless otherwise agreed upon between user and supplier, the nominal stencil thickness, solder alloy, and reflow parameters (e.g., temperature and time) shall be as defined in JESD22-B102 Method 2.

# Automotive Electronics Council

## Component Technical Committee

### 3.1.4 Wetting Balance Solderability Test

**Wetting balance solderability testing is NOT REQUIRED for Pb-free solderability evaluation.** It is a test that can augment the other required solderability test methods during problem-solving. Further details can be found in Appendix A.

### 3.2 Resistance to Solder Heat

Resistance to Solder Heat testing must be performed per the applicable JEDEC JESD22-B106 (for Through-Hole Mounted Devices), or, if requested by the user, JESD22-A111 (for Small Surface Mount Devices). Deviation requires agreement between user and supplier on a case-by-case basis. All exceptions to the applicable test specification(s) must be noted in the part specification.

#### 3.2.1 Through-Hole Components

Resistance to solder heat testing of through-hole components shall be performed using the Pb-free solder bath test conditions per JESD22-B106.

#### 3.2.2 Full Body Immersion Wave Solder of Small Surface Mount Components

**Note: It is strongly recommended that active SMT components not be attached by bottom-side wave solder processes. Full Body Immersion testing shall only be performed if requested by the user.** The user **MUST** consult the supplier to understand the risks (e.g., MSL change, maximum reflow temperature, ramp rates, etc.) and safeguards (e.g., dry storage, pre-bake, etc.) needed if an active SMD component is to be attached via bottom-side wave solder process.

Resistance to solder heat testing of surface mount components (if applicable) shall be performed per JEDEC JESD22-A111. Testing shall use dry samples (no moisture soak) and use dual wave simulation at the 260°C classification test condition as defined in Table 1 of JESD22-A111.

### 3.3 Moisture Sensitivity

Components representative of device families shall be tested to determine moisture sensitivity level (MSL) classification per one of the following standards for both SnPb and Pb-free solder profiles. The user shall be notified of any change in existing MSL classification when transitioning from SnPb to Pb-free. All exceptions must be noted in the part specification.

#### 3.3.1 IPC/JEDEC J-STD-020 - Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices

The purpose of this standard is to identify the classification level of nonhermetic solid state surface mount devices (SMDs) that are sensitive to moisture-induced stress so that they can be properly packaged, stored, and handled to avoid damage during assembly solder reflow attachment and/or repair operations. This standard may be used to determine what classification/preconditioning level should be used for SMD package qualification. Passing the criteria in this test method is not sufficient by itself to provide assurance of long-term reliability.

# Automotive Electronics Council

## Component Technical Committee

### 3.3.2 EIA/IPC/JEDEC J-STD-075 - Classification of Non-IC Electronic Components for Assembly Processes

This standard outlines a process to classify and label non-semiconductor electronic component's Process Sensitivity Level (PSL) and Moisture Sensitivity Level (MSL) consistent with the semiconductor industry's classification levels (J-STD-020 *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Devices* and J-STD-033 *Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices*). This specification does not establish re-work conditions.

### 3.4 Tin (Sn) Whisker Acceptance Testing

#### 3.4.1 Whisker acceptance testing shall be compliant to JESD201, with additional requirements as defined herein.

#### 3.4.2 Additional Requirements (addendum to JESD201)

##### 3.4.2.1 Test Samples

Samples shall be representative of actual package configuration and surface finish technology using the proposed Pb-free finish, including any trim and form operations that occur after the plating process. Similarity acceptance qualification for changes in package configuration and/or component assembly process requires agreement between user and supplier on a case-by-case basis. Refer to Table 1 and Section 5.2 of JESD201 for more information.

##### 3.4.2.2 Sample Preconditioning - Board Mounting

Due to the addition of solder alloy material and its interaction with the Pb-free plating finish material, use of a solder alloy or attaching test samples to a printed circuit board using a soldering operation is prohibited. Deviation requires agreement between user and supplier on a case-by-case basis.

##### 3.4.2.3 Validation of Whisker Acceptance Test Conditions

The test conditions defined in JESD201 have been shown to generate whiskers. If whisker growth is not detected on test samples during the required test duration for the Temperature Cycling or High Temperature / Humidity Storage (55°C  $\pm$ 3°C and 85%  $\pm$ 3% RH) test conditions, data demonstrating capability to generate whisker growth (e.g., additional samples, coupons, etc.) must be provided to validate the test conditions that were used.

**NOTE:** The lower Temperature / Humidity Storage test condition (30°C  $\pm$ 2°C and 60%  $\pm$ 3% RH) per JESD201 is exempt from this requirement.

### 3.4.3 Acceptance Criteria

A component will be defined as passing Sn whisker acceptance testing if all test samples meet the criteria established by the Class level 2 requirements as defined in JESD201 or as negotiated between the user and supplier.



# Automotive Electronics Council

## Component Technical Committee

### 3.5 Reporting of Results

#### 3.5.1 Solderability, Resistance to Solder Heat, and Moisture Sensitivity Test Results

Upon completion of the required testing defined herein, a report of the testing performed and detailed results, as defined below, must be submitted to the user. Deviation requires agreement between user and supplier on a case-by-case basis.

- a. Plating Finish Details
  - Component type, package base metal, underlayer (if used), and finish material(s)
  - Material thickness values
- b. Sample Details
  - Package configuration (e.g., lead pitch, pin count, lead form, etc.)
  - Plating lot date
  - Preconditioning used
  - Sample sizes
- c. Test Details
  - Testing performed (e.g., solderability, MSL, etc.)
  - Documentation of solder alloy and/or solder profile/temperature used (e.g., SnPb, Pb-free, etc.)
  - Technique used for fine pitch solderability test “dip and look” method (if applicable).
  - Exceptions to any tests performed (e.g., test conditions, sample sizes, etc.)
- d. Test Results
  - Acceptance criteria (for all tests performed)
  - Summary of results and supporting test data

#### 3.5.2 Sn Whisker Acceptance Test Results

A report of the Sn Whisker Acceptance testing performed and detailed results compliant to JESD201 Section 7 must be submitted to the user. Additional information, as defined below, shall be included in the report. Deviation requires agreement between user and supplier on a case-by-case basis.

- a. Additional Sample Details
  - Package configuration (e.g., lead pitch, pin count, lead form, etc.)

# Automotive Electronics Council

---

Component Technical Committee

## APPENDIX A - Informative subjects:

### A.1 Wetting Balance Testing:

In the event that component solderability issues are encountered, the Wetting Balance Test method can be a valuable investigation technique. Wetting balance testing can be useful when used for a lot-to-lot comparison, where a method of plating variability identification is desired. Some considerations when using wetting balance as a quantitative investigation tool include:

- Not all wetting balance machines are equal, some are called solder checking or solderability machines, but in fact can not do the test properly and do not have the ability to adjust for different mediums
- The wetting balance baseline for SnPb solder has been established as:
  - Density of solder at 245°C (8150 kg/m<sup>3</sup>) for Sn60/Pb40 Alloy
  - Surface tension of solder = 0.4 mN/mm
- Recent testing is suggesting a wetting balance baseline for Pb-Free as:
  - Density of solder at 255°C (7410 kg/m<sup>3</sup>) for SAC305 Alloy
  - Surface tension of Pb-free solder = 0.5 mN/mm

Note that previously published SnPb wetting balance test data only applies to testing performed at 245°C and using Sn60/Pb40 solder alloy material. Any change to temperature (e.g., 215°C) or solder alloy (e.g., Pb-free alloy material) would require new data collection and possible adjustments to the test equipment and/or test procedure.

Previously published reports have shown that the wetting balance test does not correlate to actual solderability test results. Components failing a wetting balance test may experience no failures during the solder or assembly process, while components passing a wetting balance test may experience failures during the solder or assembly process.

**Automotive Electronics Council**  
Component Technical Committee

**Revision History**

<u>Rev #</u>	<u>Date of change</u>	<u>Brief summary listing affected sections</u>
-	Feb. 12, 2009	Initial Release.
A	June 1, 2010	Format Updated.