UNIT III
8086 MICROPROCESSOR INTERFACING

3.1 Introduction

This unit explains how to design and implement an 8086 based microcomputer system. To design an 8086 based system, it is necessary to know how to interface the 8086 microprocessor with memory and input and output devices. Due to the mismatch in the speed between the microprocessor and other devices, a set of latches and buffers are required to interface the microprocessor with other devices. In this unit, you will learn about the way in which address/data buses, latches and buffers are used in the process of interfacing. To understand the interfacing principles and concepts it is necessary to learn the various types of bus cycles and bus timings. Overall, this unit makes you to understand how 8086 microprocessor is interfaced with memory and peripherals and how an 8086 based microcomputer system works.

3.2 Learning Objectives

- To study about the operating modes of 8086
- To study about the components of an 8086 based microcomputer system
- To understand the address/data buses of an 8086 based system
- To understand the necessity of latches and buffers
- To learn the various types of bus cycles
- To learn the bus timings
- To study about the interfacing principles and ideas

3.3 8086-Based Microcomputer System

An 8086-based microcomputer system has the following components.
- 8086 CPU
- ROM
- RAM
- Peripherals
- Control bus
- Address bus
- Data bus
- Clock generator
- Interrupt Controller
- DMA Controller
- Latches

- Transceivers

The basic control bus consists of the signals labeled M/IO (Active Low), RD (Active Low) and WR (Active Low). If the operation to be performed by 8086 is a read (either from a memory location or from a port) the RD (Active Low) goes low and if the operation to be performed by 8086 is a write (either to a memory location or to a port) the WR (Active Low) signal is asserted. If the read or write operation involves a memory M/IO (Active Low) signal will be high and if the read or write operation involves a port M/IO (Active Low) signal goes low. The other two buses of 8086 are address bus and data bus. These two buses are represented as ADDR/DATA. The logic behind this is to save number of pins. The lower 16 bits of addresses are multiplexed on the data bus.

In any operation where 8086 accesses memory or a port, the 8086 sends out the lower 16 bits of the address on the data bus. External latches such as the 74LS373 octal devices are used to grab this address and hold it during the rest of the operation. To strobe these latches at the proper time, 8086 outputs a signal called Address Latch Enable or ALE. Once the address is stored on the outputs of the latches, the 8086 removes the address from the address/data bus and uses the bus for reading or writing data.

8286 transceiver is used by most of the devices such as ROMs, RAMs and ports. These devices connected on microprocessor buses have MOS inputs and hence they do not require much current. However, each input or output added to the system data bus acts like a capacitor of a few picofarads connected to ground. In order to change the logic state of these signal lines from low to high, all this added capacitance must be charged. To change the logic state to a low, the capacitance must be discharged. If we connect more than a few devices on the data bus lines, the 8086 outputs can not supply enough current drive to charge and discharge the circuit capacitance fast enough. Hence we add external high-current drive buffers to do the job. Buffers used on the data bus must be bidirectional because the 8086 sends data out on the data bus and also reads data in on the data bus. The DT/R (Active Low) from the 8086 sets the direction in which data will pass through the buffers. When DT/R (Active Low) is asserted high, the buffers will be set up to transmit data from the 8086 to ROM, RAM or ports. When DT/R (Active low) becomes low, the buffers will be setup to allow data to come into the 8086 from ROM, RAM or ports. When the DT/R (Active Low) is asserted low, the buffers will be set up to allow data to come into the 8086 from ROM, RAM or ports. The buffers used on the data bus must have three state outputs so the outputs can be floated when the bus is being used for other operations.

Clock generator uses a crystal to produce the stable-frequency clock signal which steps the 8086 through execution of its instructions in an orderly manner. The 8284A also synchronizes the RESET signal and the READY signal with the clock so that these signals are applied to the 8086 at the proper times. When the RESET input is asserted, the 8086 goes to address FFFF0H to get its next instruction. The first instruction of the system start-up program is usually located at this address, so asserting this signal is a way to boot or start the system.

Have you understood?

1. What is the difference between a microprocessor and a microcomputer?
2. Mention the functional components of a microcomputer system.

3.4 Operating modes of 8086

There are two modes of operation for Intel 8086 namely the minimum mode and the maximum mode. When only one 8086 CPU is to be used in a micro computer system the 8086 is used in the minimum mode of operation. In this mode the CPU issues the control signals required by memory and I/O devices. In a multi processor system it operates in the maximum mode. In case of maximum mode of operation control signals are issued by Intel 8288 bus controller which is used with 8086 for this purpose. The level of the pin MN/MX (active low) decides the operating mode of 8086. When MN/MX (active low) is high the CPU operates in a minimum mode. When it is low the CPU operates in the maximum mode. From pin 24 to 31 issue two different sets of signals. One set of signals is issued when the CPU is operating in the minimum mode. The other sort of signal is issued when the CPU is operating in the maximum mode. Thus the pins from 24-31 have alternate functions.

Pin description for minimum mode
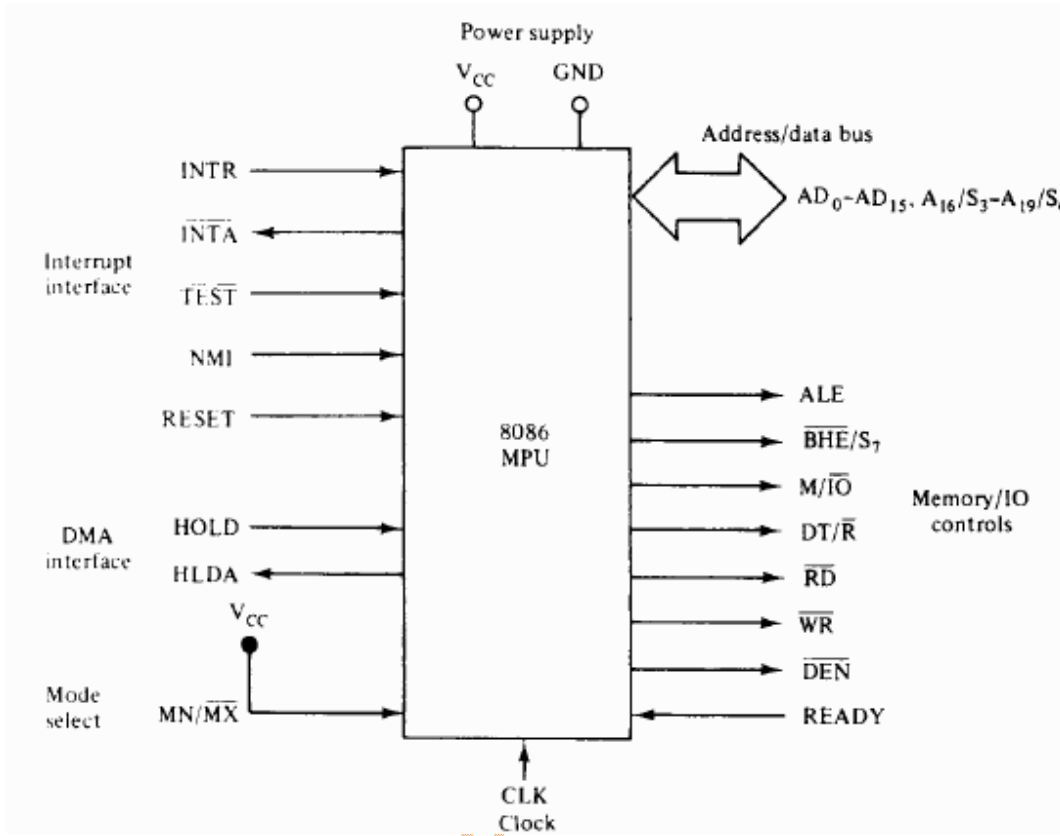
The minimum mode block diagram is shown in figure 3.1

Figure 3.1 8086 Minimum Mode Block diagram

For the minimum mode of operation the pin MN/MX (active low) is connected to 5V DC supply that is MN/MX (active low) is equal to Vcc. The description of the pins from 24 to 31 for the minimum mode is as follows:

INTA (active low)(output) Pin No 24. Interrupt Acknowledge. On receiving interrupt signal the processor issues an interrupt acknowledge signal.

ALE (output) Pin No 25. Address Latch Enable. It goes high during T1. The microprocessor sends the signal to latch the address in to the Intel 8282/8283 latch.

DEN (output) Pin No 26. Data Enable. When Intel 8286/8287 octal bus transceiver is used, this signal acts as an output enable signal. It is active low.

DT/R (active low)(output) Pin No 27. Data Transmit/Receive. When Intel 8286/8287 octal bus transceiver is used, this signal controls the direction of data

flow through the transceiver. When it is high data are sent out. When it is low data are received.

N/IO (active low)(output)   Pin No 28. Memory or I/O access. When it is high the CPU wants to access memory. When it is low, the CPU wants to access IO device.

WR (active low)(output)   Pin No 29. Write. When it is low the CPU performs memory or I/O write operation.

HLDA (output)   Pin No 30. Hold Acknowledge. It is used by the processor when it receives hold signal. When hold request is removed, HLDA goes low.

HOLD (input)   Pin No 31. Hold. When another device in the complex microcomputer system wants to use the address and the data bus, it sends a hold request through this pin.

Pin description for maximum mode

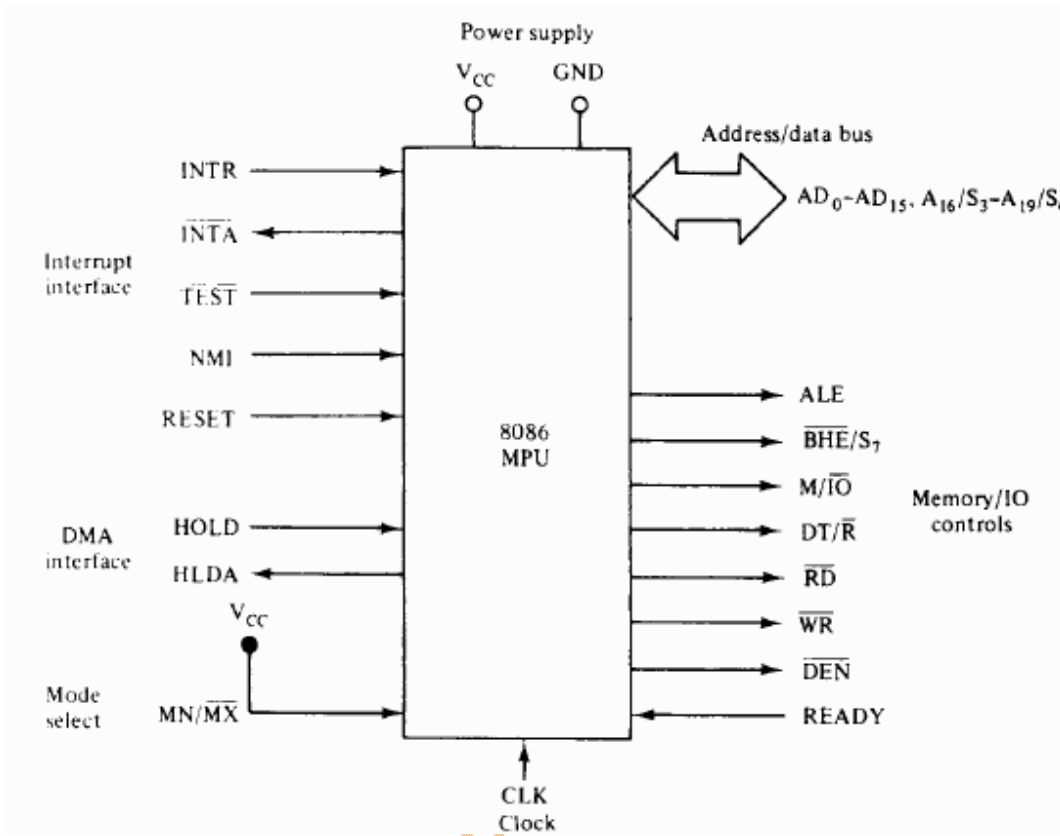The maximum mode block diagram is shown as

Figure 3.2 Maximum Mode Block diagram of 8086

For the maximum mode of operation the pin MN/MX (active low) is made low. It's grounded. The major difference between the minimum mode and the maximum mode configurations is the need for the additional circuitry to translate the control signals. The circuitry is for converting the status bits S1 (Active Low), S2 (Active Low) and S3 (Active Low) into the I/O and memory transfer signals needed to direct data transfers, and for controlling the 8282 latches and 8286 transceivers. From the status the 8288 is able to originate the address latch enable signal to the 8282s, the enable and direction signals to the 8286 transceivers and the interrupt acknowledge signal to the interrupt controller. The description of the pins from 24 to 31 is as follows:

QS1, QS0 (output) Pin no 24 and 25. Instruction Queue Status. These two pins allow the system external to the processor to interrogate the status of the processor instruction queue so that it can determine which instruction it is currently executing. The meaning of QS1 and QS0 are as follows:

QS1	QS0	Meaning
0	0	No operation
0	1	1st byte of opcode from queue
1	0	Empty the queue
1	1	Subsequent byte from queue

S0, S1, S2 (active low) (output)   Pin No 26, 27 and 28. Status Signals. These signals are connected to the bus controller Intel 8288. The bus controller generates memory and I/O access control signals. The meaning of S2, S1, and S0 (active low) are as follows:

S2 (AL)	S1 (AL)	S0 (AL)	Meaning
0	0	0	Interrupt acknowledge
0	0	1	Read data from I/O port
0	1	0	Write data into I/O port
0	1	1	Halt
1	0	0	Opcode fetch
1	0	1	Memory reading
1	1	0	Memory writing
1	1	1	Passive state

LOCK (active low) (output) Pin No 29. When it is low al interrupts are masked and no hold request is granted. In a multi processor system all other systems are informed by the signal that they should not ask the CPU for relinquishing the bus controller.

RQ (active low)/GT1 (active low), RQ (active low)/GT0 (active low)(bidirectional)   Pin No 30 and 31. Local bus priority control. Other processors ask the CPU through these lines to release the local bus. RQ (active low)/GT1 (active low) has lower priority than RQ (active low)/GT0 (active low)(bidirectional). A request consists of a negative pulse arriving before the start of the current bus cycle. The grant is a negative pulse that is issued at the beginning of the current bus cycle provided that

1. The previous bus transfer was not the low byte of a word to or from an odd address if the CPU is an 8086. For an 8088, regardless of the address alignment, the grant signal will not be sent until the second byte of a word reference is accessed.
2. The first pulse of an interrupt acknowledgement did not occur during the previous bus cycle.
3. An instruction with a LOCK prefix is not being executed.

If the condition 1 or 2 is not met, then the grant will not be given until the next bus cycle, and if the condition 3 is not met, the grant will wait until the locked instruction is completed. In response to the grant the three-state pins are put in their high impedance state and the next bus cycle, and if condition 3 is not met, the grant will wait until the locked instruction is completed. In response to the grant the three state pins are put in their high impedance state and the next bus cycle will be given the requesting master. The processor will be effectively disconnected from the system bus until the master sends a second pulse to the processor through the RQ (Active Low) / GT (Active Low).

In the maximum mode of operation signals WR, ALE, DEN, DT/R (active low) extra are not available from the processor. These signals are available from the controller 8288.

Figure 3.3 shows a typical 8086 system in the minimum mode configuration.
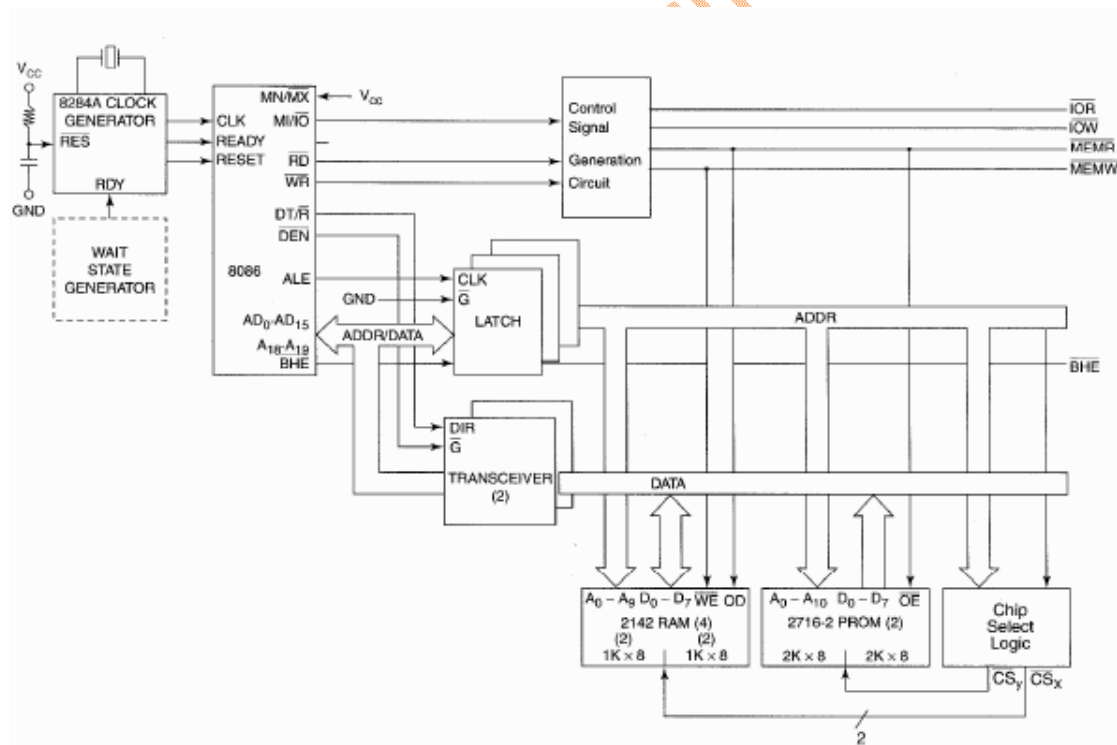

Figure 3.3 Minimum Mode Configuration

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Figure 3.4 shows a typical 8086 system in the maximum mode configuration. In maximum mode configuration, in addition to the latches and bus transceivers, a bus controller is also employed for this configuration. The bus controller provides control signals as shown in figure. The important signals are

MRDC (Active Low)   Memory Read Command
MWTC (Active Low)   Memory Write Command
IORC (Active Low)   I/O Read Command
IOWC (Active Low)   I/O Write Command
AMWC (Active Low)   Advanced Memory Write Command. It is a memory write

command issued earlier in the machine cycle. It gives

memory an early indication of a write instruction.
AIOWC (Active Low)   Advanced I/O Write Command

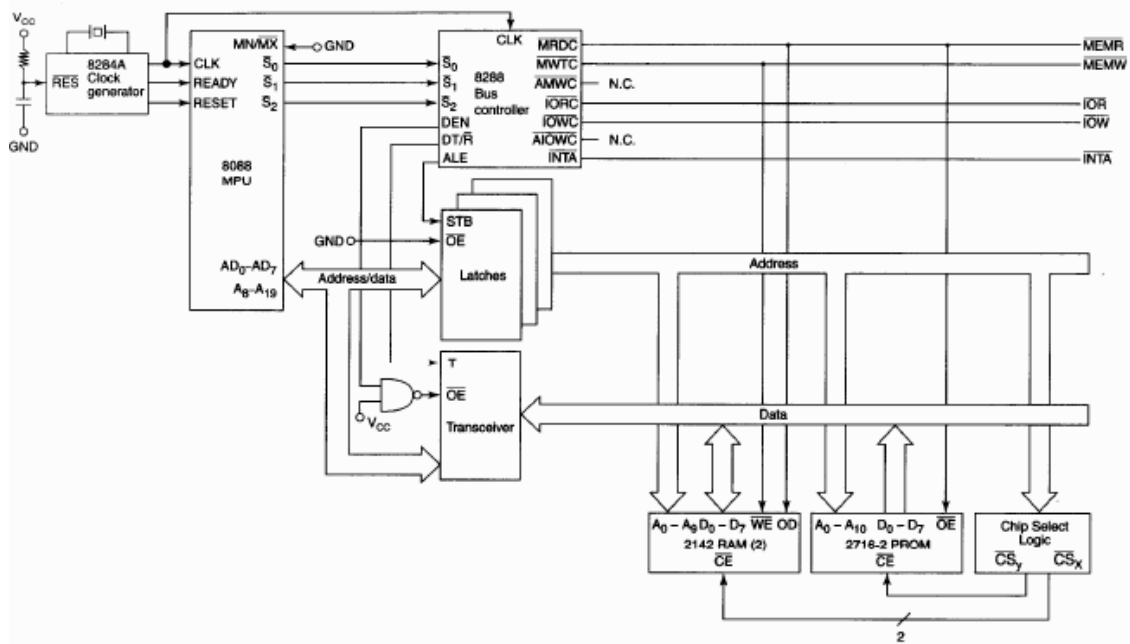
Figure 3.4 Maximum Mode Configuration

Have you understood?

1. What are the two operating modes of 8086?

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2. Which mode of 8086 is required for the multiprocessor system?
3. Which pins of 8086 processor have different prescriptions for the two different modes?
4. What is the purpose of the bus controller in the maximum mode of 8086?
5. What is the role played by pin numbers 24 and 25 in minimum mode and maximum
   mode?

3.5 Bus Cycles

There are four basic types of bus cycles: read, write, interrupt acknowledge and halt. Interrupt acknowledge and halt bus cycles define special bus operations. Read bus cycles include memory, I/O and instruction prefetch bus operations. Write bus cycles include memory and I/O bus operations. All read and write bus cycles have the same basic format. A particular type of read or write cycle is decided by the status signals. The various types of read cycles are shown as follows.

S2	S1	S0	Bus Cycle Type
0	0	1	Read I/O – Initiated by the Execution Unit or the Refresher Control Unit. A19:16 are driven to zero
1	0	0	Institution Prefetch – Initiated by the BIU. Data read from the bus fills the prefetch queue
1	0	1	Read Memory – Initiated by the Execution Unit or the Refresher Control Unit. A19-0 select the desired byte or word memory location

Various types of write cycles are shown as follows.

S2	S1	S0	Bus Cycle Type
0	1	0	Write I/O – Initiated by executing IN, OUT, INS, OUTS instructions. A15:0 select the desired I/O port. A19:16 are driven to zero
1	1	0	Write Memory – Initiated by any one of the Byte/Word memory instructions. A19:0 selects the desired byte or word memory location

The basic operations a microprocessor has to do are to read a byte from a memory location or an input port and to write a byte into a memory location or an output port. All these operations require a set of signal activities in address, data and control buses. These activities are represented in the form a timing diagram. Let us explain the timing diagram of 8086 in terms of a memory read operation in its minimum mode.

3.5.1 Read Bus Cycle

Figure 3.18 shows timing diagram for memory read of minimum mode of operation.

CLK represents the crystal controlled clock signal sent to the 8086 from an external clock generator device such as 8284 clock generator. One cycle of this clock pulse is called a state. The duration of a clock pulse is measured from the falling edge of one clock pulse to the falling edge of the next clock pulse. The clock frequency of 8086 varies between 5MHz and 10MHz and hence the time for one clock varies between 100ns and 200ns. In microprocessors, the timing diagram is explained in terms of the following terminology.
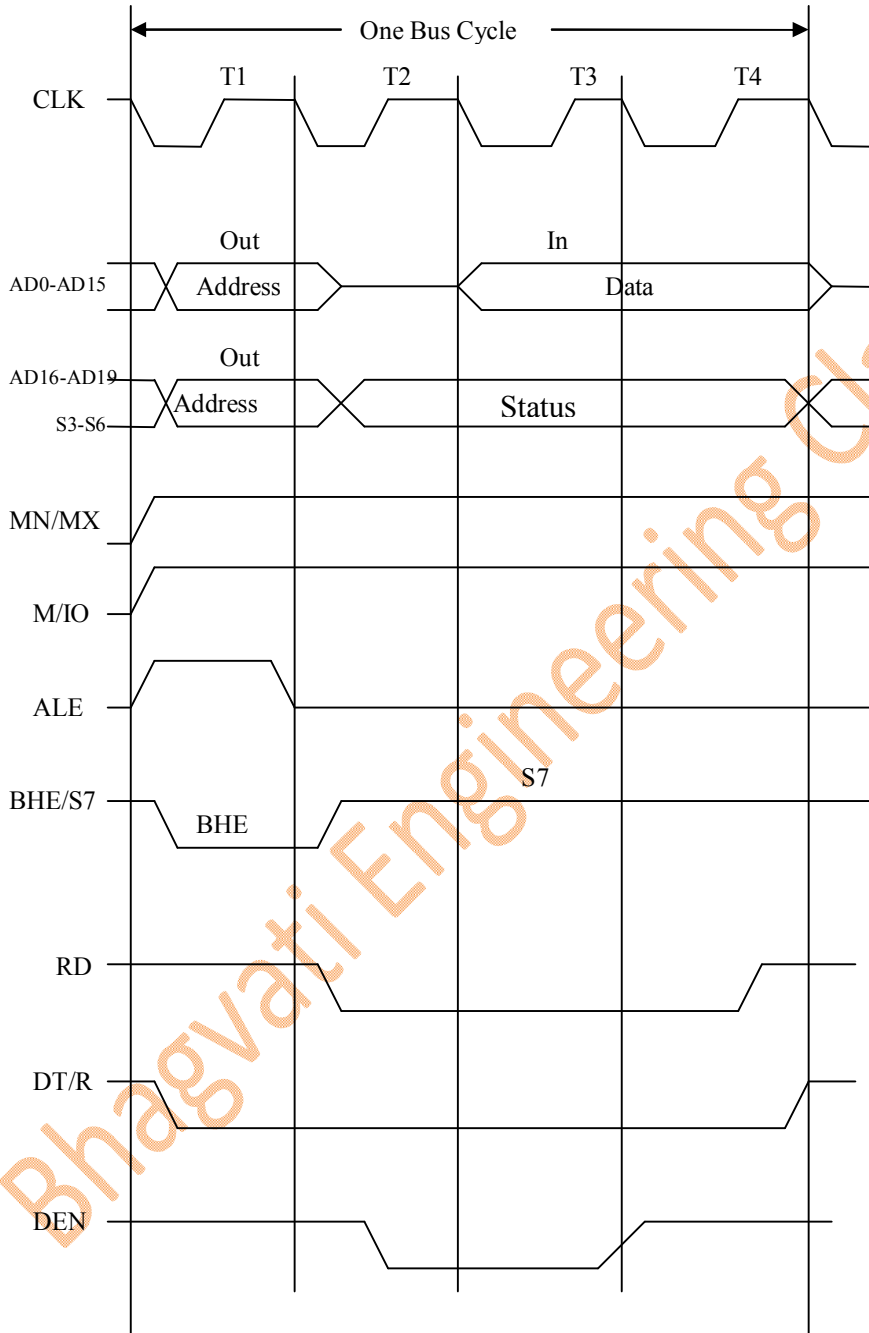
Figure 3.18 Timing Diagram for Memory Read

Machine Cycle

The basic operation of reading/writing a byte from/to a memory location/a port is called a machine cycle. The time taken to complete a machine cycle is represented as T_{cy}. A machine cycle is made up of many states.

Instruction Cycle

The time taken to fetch and execute an entire instruction is referred to as an instruction cycle. An instruction cycle consists of one or more machine cycles.

In 8086, the concept of a machine cycle is not so relevant. The Execution Unit (EU) executes instruction in certain clock periods. These clock cycles do not constitute any form of machine cycles. The Bus Interface Unit (BIU) fetches instructions and operands from the memory. Any external access either to the memory or I/O device requires four clock periods. This group of four clock cycles is called the bus cycle. There is memory or I/O read bus cycle; memory or I/O write bus cycle.

One bus cycle consists of four clock periods. 20-bit address is sent on the address bus. AD0-AD15 carry 16 LSBs of the address and A16-A19 carry four MSBs of the address. The address remains on the address lines only during T1 because these lines operate in multiplexed mode. AD0-AD15 lines remain in high impedance state during T2. During T3 and T4 data are transmitted on AD0-AD15. During T2, T3 and T4 status signals S3, S4, S5 and S6 are carried by A16-A19 lines. The ALE signal goes high during T1 to latch the address into external latch. MN/MX (Active Low) is high indicating that the CPU is operating in the minimum mode. M/IO (Active Low) is high. It indicates that the address sent by the CPU is for memory. RD (Active Low) goes low during T2. When it goes low data can be read by the CPU. It goes high again in T4. DT/R (Active Low) goes low during T1. This signal is used by transceiver 8286 or 8287 if it is used in the system. DEN goes low during T2 and again it becomes high during T4. It is provided for data enable for 8286/8287 if it is used in the system. DT/R (Active Low) and DEN signals are used to control bidirectional latched buffers. These are specially designed to work with 8286/8287. BHE (Active Low) in conjunction with A0 decides whether a byte or a word is to be transferred from/to memory locations. BHE (Active Low) identifies high order byte of memory word whereas

A0 identifies low order byte. On BHE (Active Low) the status signal S7 is transmitted during T2, T3 and T4. For word and byte access the status of BHE (Active Low) and A0 is as follows:

BHE (Active Low)	A0	Meaning
0	0	Whole word is transferred
0	1	Upper byte from/to odd address
1	0	Lower byte from/to even address
1	1	None

S3 and S4 identify the memory segment which is being accessed. S5 is interrupt enable status. For memory access S6 is always zero and S3 and S4 are as follows.

S4	S3	Meaning
0	0	Extra segment access
0	1	Stack segment access
1	0	Code segment access
1	1	Data segment access

The various events that take place in the read cycle (memory or I/O) can be summarized as follows.

- The 4 processor clock cycles are called T states. Four cycles is the shortest time that the processor can use for carrying out a read or an input cycle.
- At the beginning of T1, the processor outputs S2, S1, S0, A16/S3...A19/S6, AD0..AD15 and BHE#/S7.
- The 8288 bus controller transitions the ALE signal from low to high, thereby allowing the address to pass through the transparent latches (74HC373). The address, along with the BHE# signal is latched when ALE goes low, providing the latched address A0..A19.
- During T2 the processor removes the address and data. S3..S6 status is output on the upper 4 address/status lines of the processor.
- The AD0..AD15 signals are floated as inputs, waiting for data to be read.
- Data bus transceivers (74HC245) are enabled towards the microprocessor (the READ direction) by the DT/R# and DEN signals.
- The MRDC# (ie MEMR#) or IORC# (IOR#) signal is asserted.

- The signals are maintained during T3. At the end of T3 the microprocessor samples the input data.
- During T4 the memory and I/O control lines are de-asserted.

3.5.2 Write Bus Cycle

Figure 3-19 illustrates a typical write bus cycle. The bus cycle starts with the transition of ALE high and the generation of valid status bits S2:0. The bus cycle ends when WR transitions high (inactive), although data remains valid for one additional clock. The two types of write bus cycles are as follows.
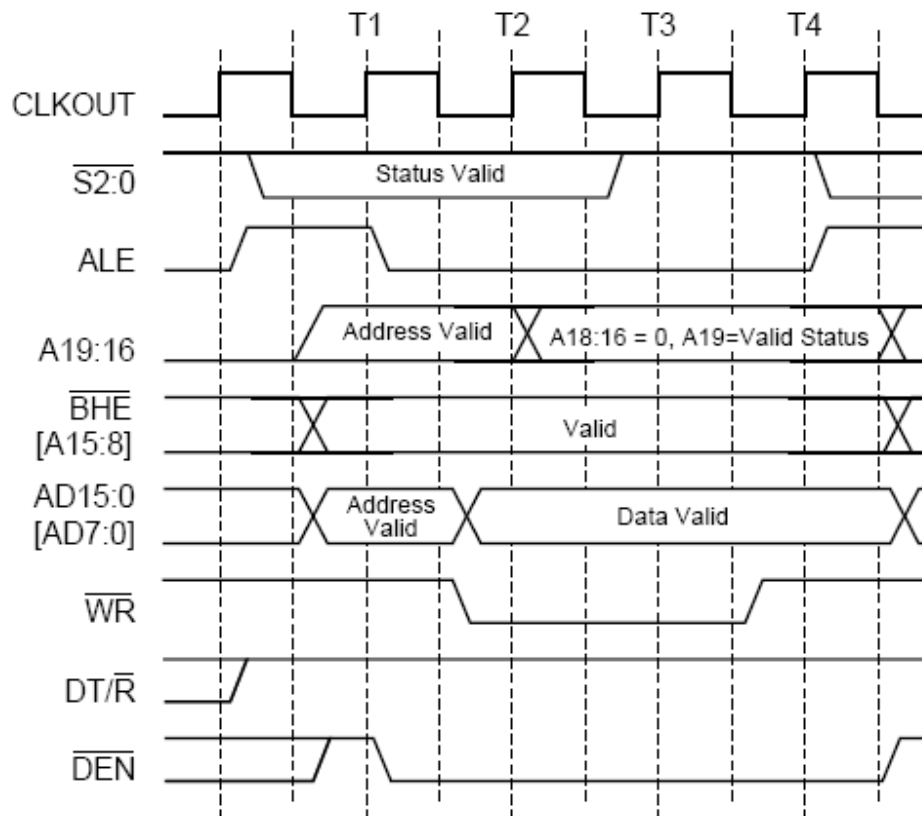

Figure 3.19 Write Bus Cycle

The various events that take place in the read cycle (memory or I/O) can be summarized as follows.

- The 4 processor clock cycles are called T states. Four cycles is the shortest time that the processor can use for carrying out a write or an output cycle.
- At the beginning of T1, the processor outputs S2, S1, S0, A16/S3…A19/S6, AD0..AD15 and BHE#/S7.
- The 8288 bus controller transitions the ALE signal from low to high, thereby allowing the address to pass through the transparent latches (74HC373). The address, along with the BHE# signal is latched when ALE goes low, providing the latched address A0..A19.
- During T2 the processor removes the address and data. S3..S6 status is output on the upper 4 address/status lines of the processor.
- Output data is driven out on the AD0..AD15 lines.
- Data bus transceivers (74HC245) are enabled away from the microprocessor (the WRITE direction) by the DT/R# and DEN signals.
- The MWRC# (ie MEMW#) or IOWC# (IOW#) signal is asserted at the beginning of T3.
- The signals are maintained during T3.
- During T4 the memory and I/O control lines are de-asserted. In simple Intel Architecture systems, the data is usually written to the memory or output device at the rising edge of the MWRC# or IOWC# signal.

3.5.3 Typical 16-bit Interface Connection

Figure 3-20 illustrates a typical 16-bit interface connection to a read/write device. Write bus cycles have many parameters that must be evaluated in determining the compatibility of a memory (or I/O) device. Some critical write bus cycle parameters are listed in the table.

Most memory and peripheral devices latch data on the rising edge of the write strobe. Address, chip-select and data must be valid (set up) prior to the rising edge of WR. TAW, TCW and TDW define the minimum data setup requirements. The value calculated by their respective equations must be greater than the device requirements. To increase the calculated value, insert wait states.
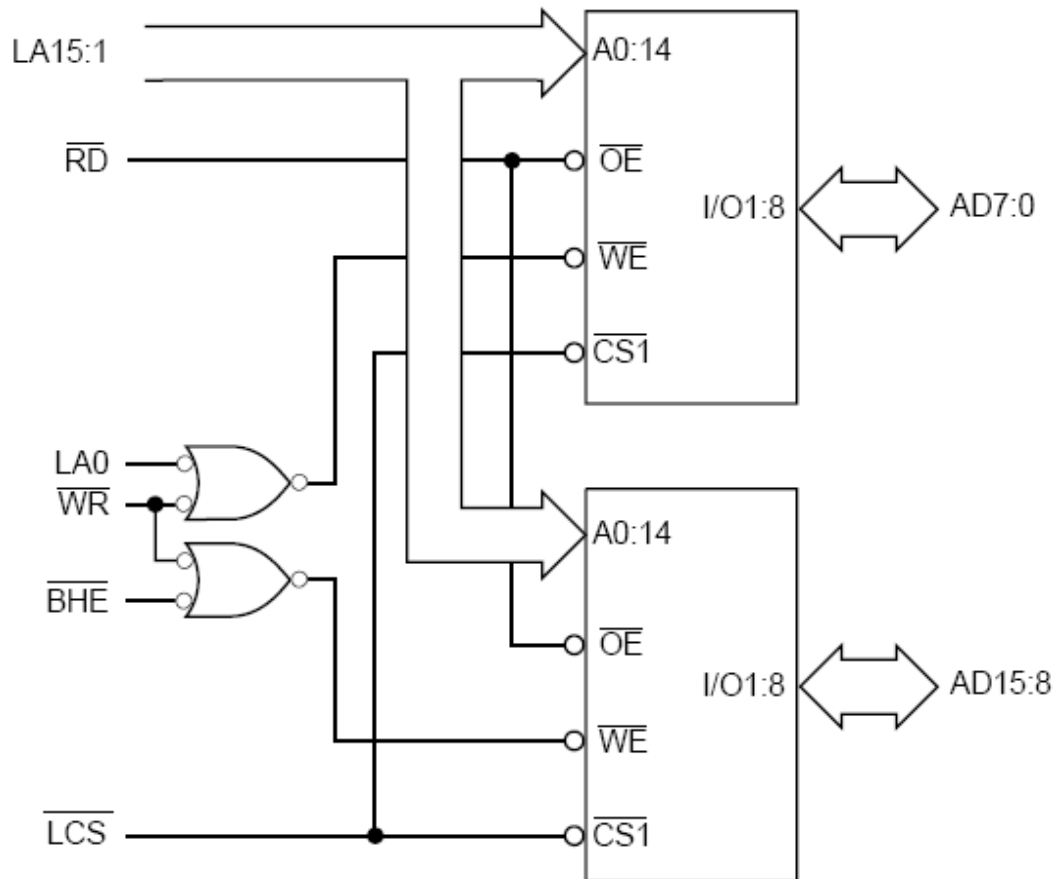
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Figure 3.18 16-bit Interface Connection to a Read/Write device

The minimum device data hold time (from WR high) is defined by TDH. The calculated value must be greater than the minimum device requirements; however, the value can be changed only by decreasing the clock rate.

Memory Device Parameter	Description	Equation
T_{WC}	Write cycle time	4T
T_{AW}	Address valid to end of write strobe ($\overline{WR}$ high)	$3T - T_{ADLTCH}$
T_{CW}	Chip enable ($\overline{LCS}$) to end of write strobe ($\overline{WR}$ high)	3T
T_{WR}	Write recover time	T_{WHLH}
T_{DW}	Data valid to write strobe ($\overline{WR}$ high)	2T
T_{DH}	Data hold from write strobe ($\overline{WR}$ high)	T_{WHDX}
T_{WP}	Write pulse width	T_{WLWH}

TWC and TWP define the minimum time (maximum frequency) a device can process write bus cycles. TWR determines the minimum time from the end of the current write cycle to the start of the next write cycle. All three parameters require that calculated values be greater than device requirements. The calculated TWC and TWP values increase with the insertion of wait states. The calculated TWR value, however, can be changed only by decreasing the clock rate.

Have you understood?

1. What is meant by an instruction cycle?
2. What is meant by machine cycle?
3. Why bus cycle is more relevant than machine cycle in 8086?
4. What are the operations take place during T1 state of a bus cycle?
5. During which T state RD and WR control signals are issued?

3.6 Address and Data Bus

The BIU has a combined address and data bus, commonly referred to as a time-multiplexed bus. Time multiplexing address and data information makes the most efficient use of device package pins. A system with address latching provided within the memory and I/O devices can directly connect to the address/data bus. The local bus can be demultiplexed with a single set of address latches to provide non-multiplexed address and data information to the system.

The programmer views the memory or I/O address space as a sequence of bytes. Memory space consists of 1 Mbyte, while I/O space consists of 64 Kbytes. Any byte can contain an 8-bit data element, and any two consecutive bytes can contain a 16-bit data element (identified as a word). The discussions in this section apply to both memory and I/O bus cycles. For brevity, memory bus cycles are used for examples and illustration.

The memory address space on a 16-bit data bus is physically implemented by dividing the address space into two banks of up to 512 Kbytes each (see Figure 3.21). One bank connects to the lower half of the data bus and contains even-addressed bytes (A0=0). The other bank connects to the upper half of the data bus and contains odd-addressed bytes (A0=1). Address lines A19:1 select a specific byte within each bank. A0 and Byte High Enable (BHE) determine whether one bank or both banks participate in the data transfer.
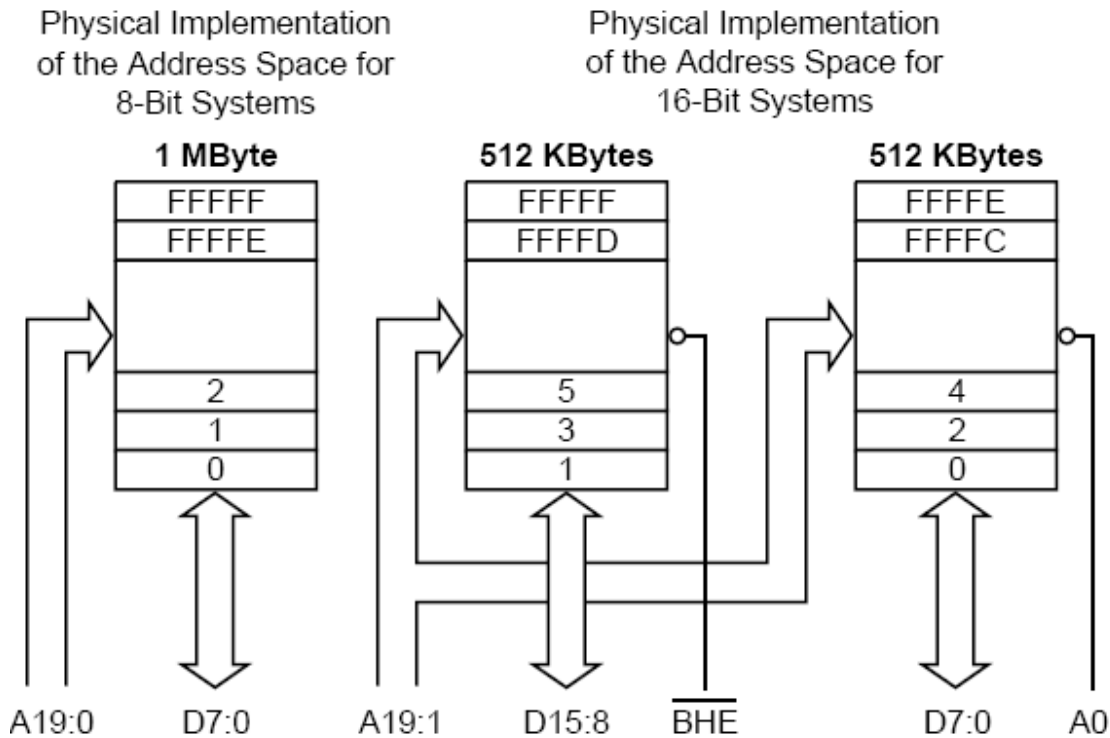
Figure 3.21 Physical Databus Models

Byte transfers to even addresses transfer information over the lower half of the data bus (see Figure 3-22a). A0 low enables the lower bank, while BHE high disables the upper bank. The data value from the upper bank is ignored during a bus read cycle. BHE high prevents a write operation from destroying data in the upper bank. Byte transfers to odd addresses transfer information over the upper half of the data bus (see Figure 3-22b). BHE low enables the upper bank, while A0 high disables the lower bank. The data value from the lower bank is ignored during a bus read cycle. A0 high prevents a write operation from destroying data in the lower bank. To access even-addressed 16-bit words (two consecutive bytes with the least-significant byte at an even address), information is transferred over both halves of the data bus (see Figure 3-23).
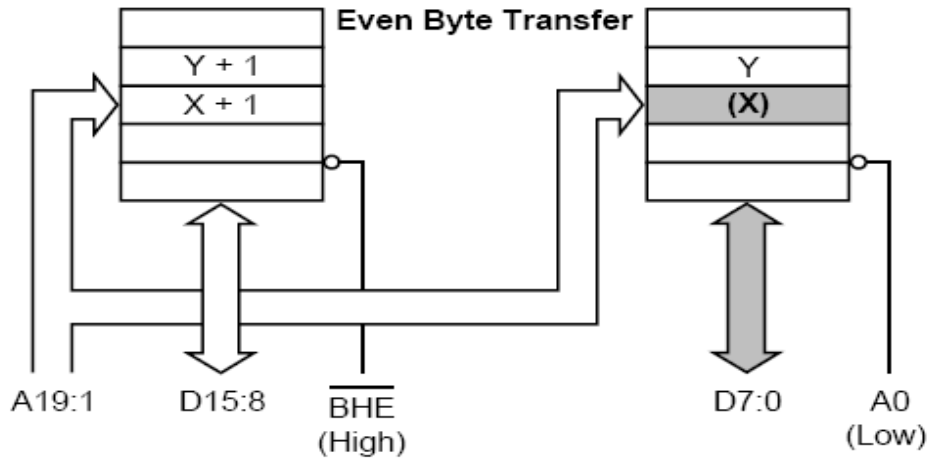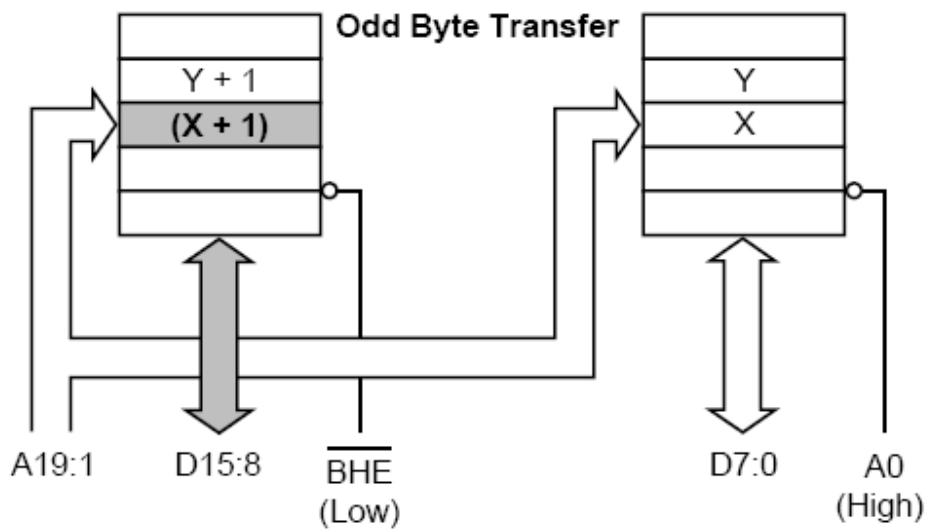
Figure 3.22a 16-bit Data Bus Byte Transfers

Figure 3.22b 16-bit Data Bus Byte transfers

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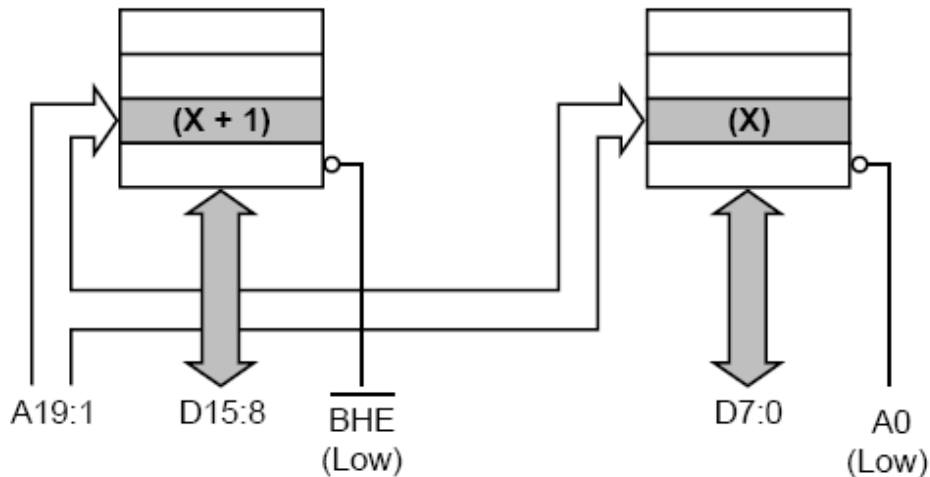
Figure 3.23 16-Bit Data Bus Even Word Transfers

A19:1 select the appropriate byte within each bank. A0 and BHE drive low to enable both banks simultaneously. Odd-addressed word accesses require the BIU to split the transfer into two byte operations (see Figure 3-24). The first operation transfers data over the upper half of the bus, while the second operation transfers data over the lower half of the bus. The BIU automatically executes the two-byte sequence whenever an odd-addressed word access is performed.

Figure 3.24 16-Bit data Bus Odd Word Transfers
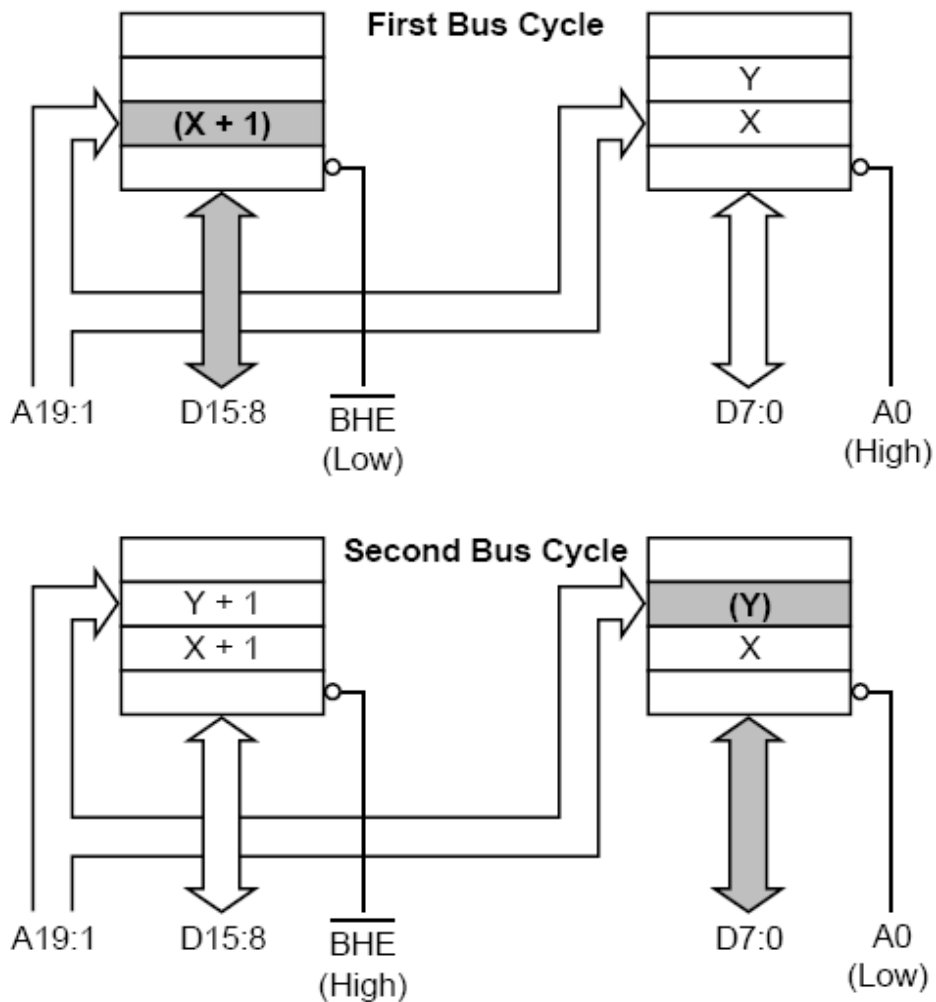
Have you understood?

1. What is the advantage of time multiplexing the address/data bus?
2. List down the steps required to access odd byte transfer.
3. What are the steps required to access even word transfer?

3.7 Memory Interfacing and I/O Interfacing

3.7.1 8086 Memory Banks

8086 has a 20 bit address bus and hence it can address 2^{20} or 1,048,576 addresses. In each location a byte is stored. So when a word is stored in the memory, it is stored in two consecutive memory locations. Strictly speaking, both memory read and memory write operations require more than one memory cycle. If we want 8086 to complete memory read and memory write operations to be completed with one machine cycle, the memory is to be organized in the form of two banks. Each bank will have 524,288 bytes each.

One memory bank contains all the even addressed locations like 00000, 00002 and 00004. The data lines of this bank are connected to the lower eight data lines, D0 through D7 of the 8086. The other memory bank has all the odd addressed locations like 00001, 00003 and 00005. The data lines of this bank are connected to the upper eight data lines, D8 through D15 of the 8086. Address line A0 is used as part of the enabling for memory in the lower bank. Address lines A1 through A19 are used to select the desired memory device in the bank to address the desired byte in the service. These address lines from A1 through A19 are also used to access a particular location in the upper bank. An additional signal called Bus High Enable (BHE – Active Low) is used to enable the upper memory bank. An external latch, strobed by ALE, grabs the BHE (Active Low) signal that holds it stable for the rest of the machine cycle. The following table shows the required logic levels on the BHE (Active Low) and A0 signals for various types of memory accesses.

ADDRESS	DATA TYPE	BHE (ACTIVE LOW)	A0	BUS CYCLES	DATA LINES USED
0000	BYTE	1	0	ONE	D0-D7
0000	WORD	0	0	ONE	D0-D15
0001	BYTE	0	1	ONE	D7-D15
0001	WORD	0	1	FIRST	D0-D7
		1	0	SECOND	D7-D15

Case 1

Read/Write a byte form/to an even address – A0 will be low and BHE (Active Low) will be high – Byte is transferred to/from low bank through D0-D7
Example – MOV AH,DS:BYTE PTR[0000]

Case 2

Similar to case 1 except the word access instead of the byte access – Both A0 and BHE (Active Low) will be asserted low – Low byte of the word through D0-D7 and high byte of the word through D8-D15
Example – MOV AX,DS:WORD PTR[0000]

Case 3

Read/Wrire a byte from/to an odd address – A0 will be high and BHE (Active Low) will be asserted low – Low bank is disabled and high bank is enabled – Byte is transferred through D0-D7
Example – MOV AL,DS:BYTE PTR[0001]

Case 4

Read/Write a word from/to an odd address – 8086 requires two bus cycles – During the first machine cycle assert BHE (Active Low) as low and A0 as high – First byte is transferred through D0-D7 and the second byte is transferred through D8-D15
Example – MOV AX,DS:WORD PTR[0001H]

3.7.2 Address Decoding

Two of the EPROMs have their eight data outputs connected in parallel to system data lines D0-D7. These two EPROMs give 4 Kbytes of storage in the lower memory bank. The other two EPROMs have their data outputs connected in parallel to system data lines D8-D15 to give 4 Kbytes of storage in the upper bank of ROM. Eleven address lines are needed to address the 2 Kbytes in each device. Therefore system address lines A1-A11 are connected to all the EPROMs in parallel. A2716 has two enable inputs. CE(Active Low) and OE(Active Low). The CE (Active Low) inputs of the two devices in the lower bank are connected to system address line A0. Hence the CE (Active Low) inputs of these devices will be asserted if A0 is low. The CE (Active Low) inputs of the two 2716s in the upper bank are connected to the BHE (Active Low) line. The CE (Active Low) inputs of these devices will be asserted whenever BHE (Active Low) is asserted low. A 3625 is a 1K x 4 bipolar PROM which functions as an address decoder. PROM functions as a better decoder since it is programmable and it has large pins and hence it allows us to select a specific area in the memory without using external gates. The CS1 (Active Low) is an enable input of the PROM decoder which is tied to the ground and hence permanently enabled. The CS2 (Active Low) enable input is tied to the RD (Active Low) signal from the 8086, so that the decoder will be enabled only if the 8086 is doing a read

operation. The truth table for the PROM inputs, PROM outputs and the corresponding address blocks that will be selected is shown in the figure.

PROM INPUTS				PROM OUTPUTS				ADDRESS BLOCK SELECTED
M/IO	A14-A19	A13	A12	O4	O3	O2	O1	
1	1	1	1	1	1	1	0	FF000H-FFFFFH
1	1	1	0	1	1	0	1	FE000H-FEFFFH
1	1	0	1	1	0	1	1	FD000H-FDFFFH CSX (Active Low)
1	1	0	0	0	1	1	1	FC000H-FCFFFH CSY (Active Low)
ALL OTHER STATES				1	1	1	1	NONE

M/IO (Active Low) is asserted as high to ensure that memory access is enabled and port devices are disabled. The address lines A14-A19 have the corresponding bit sequence according to the address block that is to be selected. The address lines select the corresponding PROM outputs and the PROM selects the appropriate address blocks. Similarly the following truth table explains the decoding process for RAM.

PROM INPUTS				PROM OUTPUTS				BYTE(S) SELECTED (ADDRESS BLOCK)
A12-A18	A11	BHE	A0	O4	O3	O2	O1	
0	0	0	0	1	1	0	0	BOTH BYTES (0H-07FFH)
0	0	0	1	1	1	0	1	HIGH BYTE (0H-07FFH)
0	0	1	0	1	1	1	0	LOW BYTE (0H-07FFH)
0	1	0	0	0	0	1	1	BOTH BYTES (0800H-0FFFH)
0	1	0	1	0	1	1	1	HIGH BYTE (0800H-0FFFH)
0	1	1	0	1	0	1	1	LOW BYTE (0800H-0FFFH)
ALL OTHER STATES				1	1	1	1	NONE

3.7.3 Direct I/O of 8086

Some microprocessors use the same address space for both memory and input/output devices. In this arrangement all instructions that are capable of accessing the memory locations can also access the input/output devices. However, 8086 microprocessor permit the establishment of two separate address

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spaces for memory and input/output devices. Having separate address space for the input/output devices is called direct I/O.

Whenever the 8086 executes an IN and OUT instruction to access a port, none of the segment registers are involved in producing the physical address sent out by the 8086. The port address is sent out directly from the 8086 on lines AD0-AD15, and 0's are output on lines A16-A19. In an 8086 system which uses direct I/O, the M/IO (Active Low) signal is used to enable a memory decoder or a port decoder. You please remember that the M/IO (Active Low) signal being high was one of the enabling conditions for the memory decoding as we discussed previously. The opposite of this enables the port decoder. During the execution of an IN instruction, the RD (Active Low) signal from the 8086 will be low. This signal can be used to enable an addressed input port device. During the execution of an OUT instruction the WR (Active Low) signal from the 8086 will be low. This signal can be used to enable an output port device. Since the 8086 microprocessor outputs up to 16-bit address for direct I/O operations, it can address any one of the 65536 input ports and any one of the 65536 output ports. However to achieve this direct I/O, the 8086 microprocessor should be provided with the appropriated decoding circuitry.

Have you understood?

1. How many address locations 8086 can address?
2. What is the reason for organizing the memory as two banks in an 8086 based system?
3. Mention the various types of memory accesses supported by an 8086 based system.
4. Why is PROM preferred to function like a decoder?
5. What are the advantages of having direct I/O over memory mapped I/O?

Summary

1. Besides the 8086 microprocessor chip, an 8086 based microcomputer system includes memory, I/O devices and the interfacing circuits required to connect these devices to the 8086 microprocessor.
2. There are two modes of operation for Intel 8086 namely the minimum mode and the maximum mode. When only one 8086 CPU is to be used in a micro computer system the 8086 is used in the minimum mode of operation. In a multi processor system it operates in the maximum mode.
3. In the minimum mode, the 8086 CPU itself issues the control signals required by memory and I/O devices.
4. In case of maximum mode of operation, control signals are issued by Intel 8288 bus controller which is used with 8086 for this purpose.

5. From pin 24 to 31 issue two different sets of signals. One set of signals is issued when the 8086 CPU is operating in the minimum mode. The other sort of signal is issued when the 8086 CPU is operating in the maximum mode.

6. A bus cycle defines the basic operation that a microprocessor performs to communicate with external devices. Examples of bus cycles are memory read, memory write, input/output read and input/output write.

7. A bus cycle corresponds to a sequence of events that starts with an address being output on the system bus followed by a read or write data transfer. During these operations, a series of control signals are also produced by the MPU to control the direction and timing of the bus.

8. Memory access is probably the most common CPU activity. Memory access is definitely an operation synchronized around the system clock. That is, reading a value from memory or writing a value to memory occurs no more often than once every clock cycle. Indeed, on many 80x86 processors, it takes several clock cycles to access a memory location. The memory access time is the number of clock cycles the system requires to access a memory location; this is an important value since longer memory access times result in lower performance.

9. Memory access time is the amount of time between a memory operation request (read or write) and the time the memory operation completes.

10. A wait state is nothing more than an extra clock cycle to give some device time to complete an operation.

11. An idle condition occurs between bus cycles and may last an indefinite period of time, depending on the instruction sequence.

12. The basic operation of reading/writing a byte from/to a memory location/a port is called a machine cycle. A machine cycle is made up of many states.

13. The time taken to fetch and execute an entire instruction is referred to as an instruction cycle. An instruction cycle consists of one or more machine cycles.

In this unit, you have learnt about the way to construct an 8086 based microcomputer system. Moreover, this unit has made you to understand the machine cycle and instruction cycle of a microprocessor in interacting with the peripherals. After this unit, you are in a position to clearly understand memory interfacing and I/O interfacing. As we have already mentioned, even though 8086 was designed and implemented with the intention of using it in a general purpose digital computer, it was never used due to the incompatibility problem that existed with the peripherals of that time. In the next unit, we are going to study about the

processor chips that are used as the CPU in the existing personal computer systems.

Exercises

1. What is the major difference between an 8086 operating in minimum mode and an 8086 operating in maximum mode?
2. What are the functions of 8086 DT/R (Active Low) and DEN (Active Low) signals?
3. When information appears on the address/data bus of the 8088 while ALE is active?
4. Which bus connections on the 8086 microprocessor are typically demultiplexed?
5. Which TTL integrated circuit is often used to demltiplex the buses on the 8086/8088?
6. List the differences between 8086 and 8088 mocroprocessors.
7. Briefly describe the purpose of each T state in a bus cycle.
8. Why is the 8086 memory set up as 2-byte wide banks?
9. What logic levels would you find on BHE (Active Low) and A0 when an 8086 is writing a byte to address 04274H?
10. What main function is provided by 8288 bus controller when used with 8086/8088 maximum mode operation?

Answers

1. The minimum mode is enough if an 8086 based system uses only one microprocessor. The maximum mode is required when more than one microprocessor is required in a system.
2. When Intel 8286/8287 octal bus transceiver is used, this signal controls the direction of data flow through the transceiver. When it is high data are sent out. When it is low data are received.
3. Address bits A7-A0
4. AD19-AD0
5. An 8-bit transparent latch (74LS373)
6. 8086 is a 16-bit processor both internally and externally. 8088 is a 16-bit processor internally and an 8-bit processor externally. 8086 was not used in PCs whereas 8088 is the first microprocessor to be used inside a PC.
7. State T1 is used by the microprocessor to provide the memory or I/O with the address. State T2 provides access time to the memory and also is where the READY input is sampled. State T3 is where the data are sampled or sent to the memory or I/O. State T4 is used to deactivate the control signals.

8. To make it possible to read or write a word with one machine cycle, the memory for an 8086 is set up as two blanks of up to 524,288 bytes each.

9. BHE (Active Low) = 1, A0 = 0

10. The 8288 bus controller must be used in the maximum mode to provide the control bus signals to the memory and I/O. This because the maximum mode operation of the 8086/8088 removes some of the system's control signal lines in favor of control signals for the coprocessors. The 8288 reconstructs these removed signals.