

Quick CMOS delay speed run

C_a Define $C_o = C_{ox}WL$ ($C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$) \rightarrow parallel plate capacitance between the gate and the bulk.

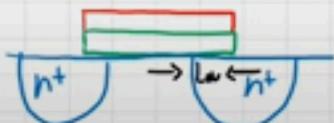
	Cutoff	Linear	Sat.
C_{GB}	$\leq C_o$	0	0
C_{as}	0	$C_o/2$	$2/3 C_o$ \leftarrow Why? b/c of channel pinch-off
C_{ad}	0	$C_o/2$	~ 0
C_a	C_o	C_o	$2/3 C_o$

Overlap: The gate overlaps the S/D by L_{ov}

Cool CMOS Logic

Overlap: The gate overlaps the S/D by L_{ov}

$$C_{as,ov} = C_{ox}WL_{ov} = C_{ad,ov} \text{ (prob)}$$

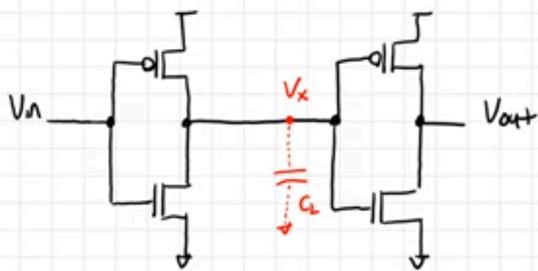


provided there is no variation.

$$We can say C_{as, tot} = C_{gs} + C_{gs, out}$$

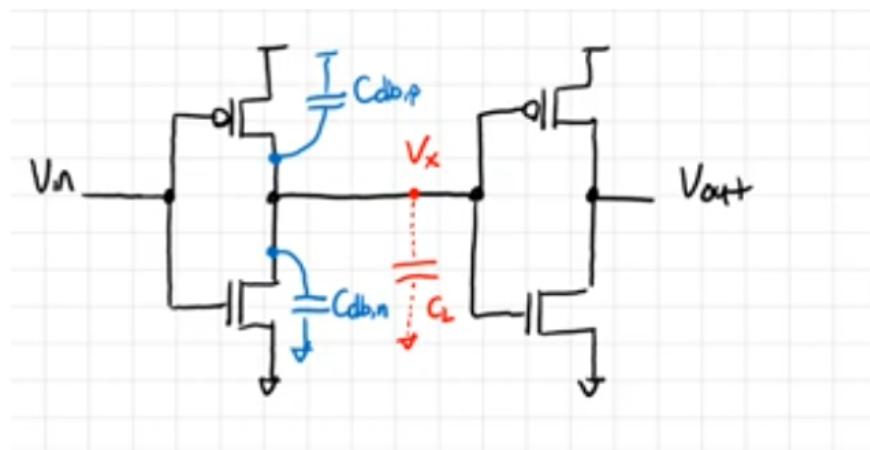
I'm so sorry I am not making proper notes! I just don't have the time!

e.g. What is the capacitance seen by a loaded inverter?

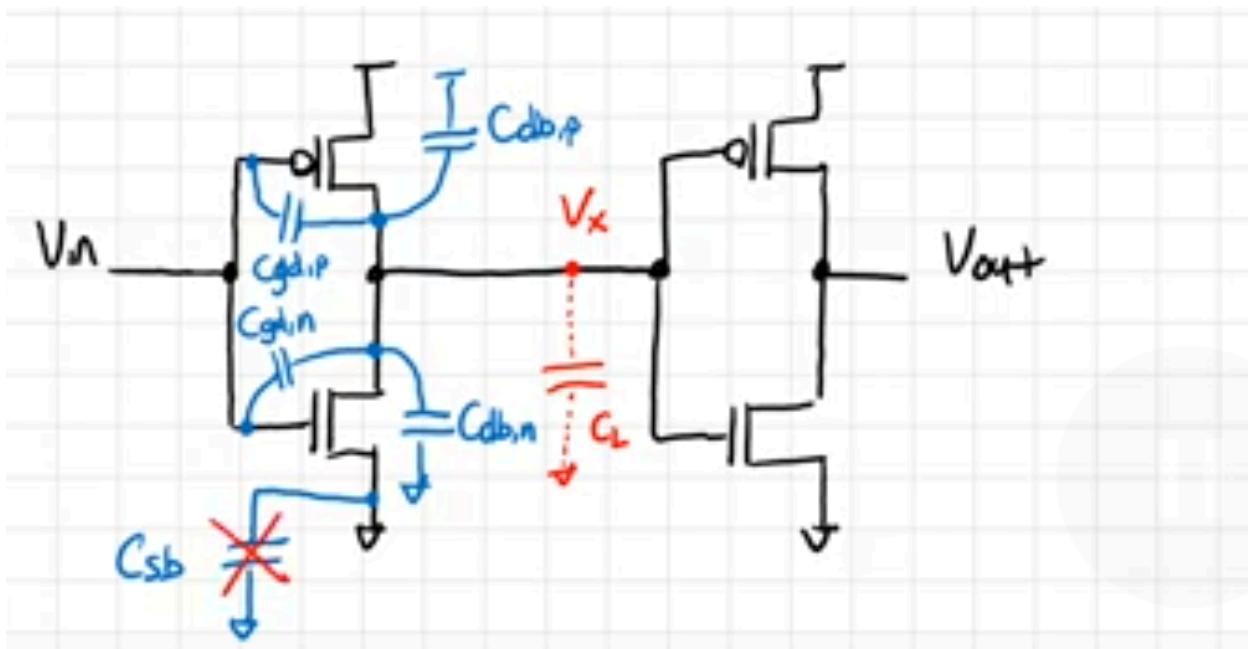


we wish to be able to draw a red inverter like that, to do that - we must find the caps connected to that node

Let's do it then!! :)



Why did we consider V_x connecting to V_{dd} as well??? Well V_{dd} really is a gnd as well in a way, cuz normally caps are useful for like trans analysis, small signal analysis etc.., so its a ac ground in way cuz it doesn't change!! Sir, says we shall discuss this more clearly soonly :)



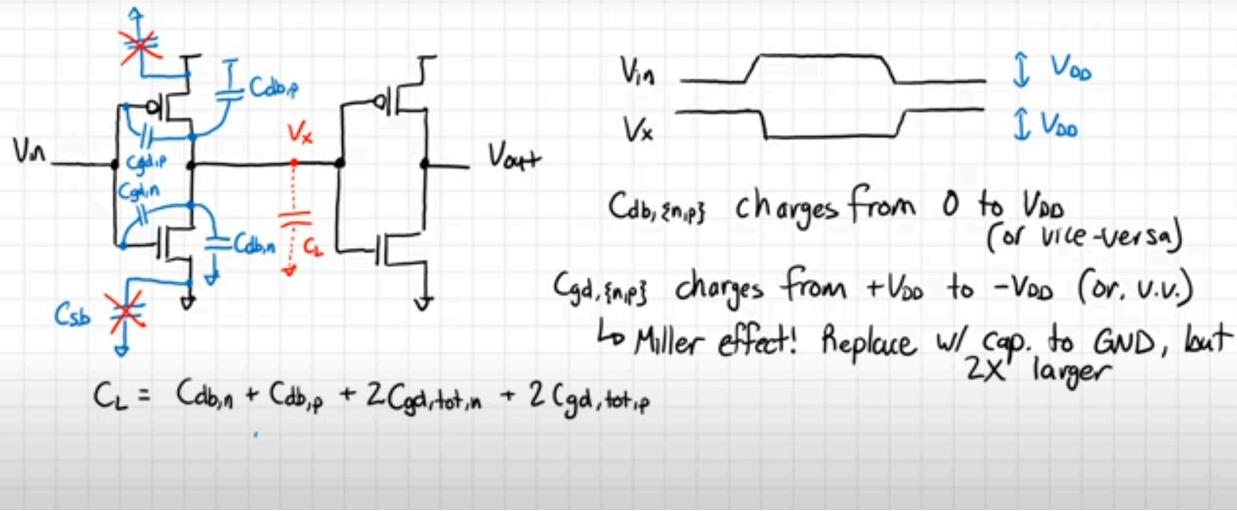
A few more! Again keep small signal

Csb is zero since its connected between 2 ground!

```
C0 n1 in1 0.0591f
C1 n2 n1 0.0591f
C2 VDD in1 0.02018f
C3 0 in1 0.05635f
C4 n2 VDD 0.52347f
C5 n2 0 0.22976f
C6 n1 VDD 0.54367f
C7 n1 0 0.28611f
C8 0 0 0.30886f
C9 n2 0 0.17115f
C10 n1 0 0.39114f
C11 in1 0 0.22803f
C12 VDD 0 3.40649f
```

Look C8 !

eg. What is the capacitance seen by a loaded inverter?

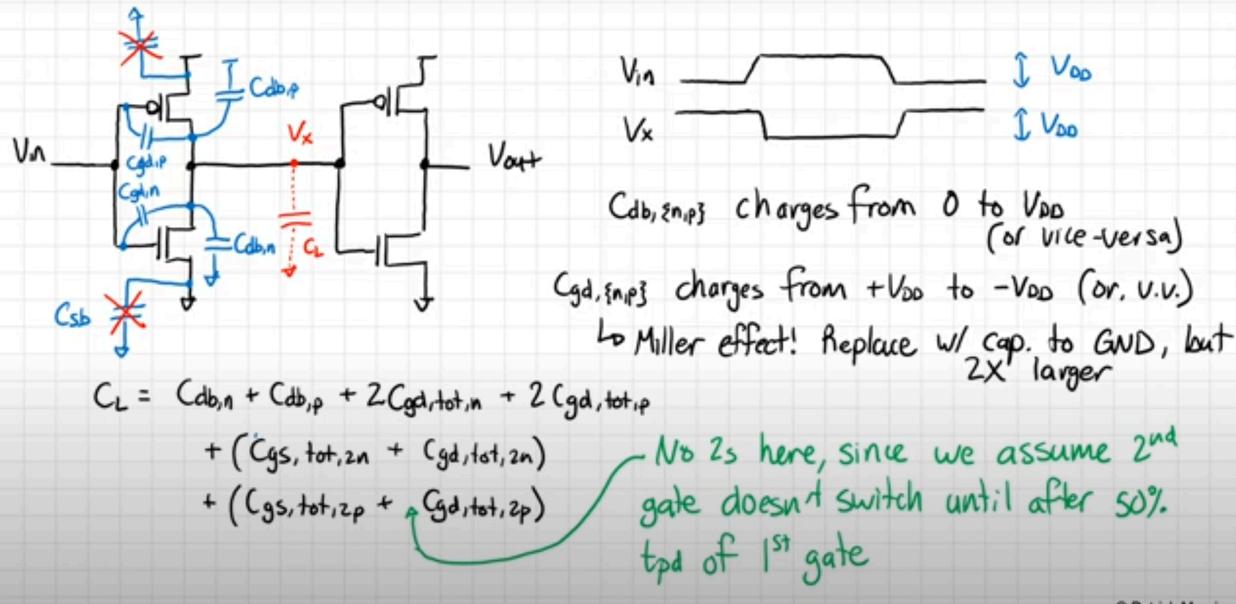


Miller effect lets us connect it to ground. And its twice as big cuz if it were connected to gnd it wud only swing from 0 to V_{dd} , but in reality it swings $-V_{dd}$ to V_{dd} , which is twice that, so we just replace it with a 2x cap?

OKi, that's that for this inverter! But we also have to include the net inverter's effect!!

so let's list all caps connected to V_x and next CMOS also

e.g. What is the capacitance seen by a loaded inverter?



Apparently it's cuz the seocnd CMOS doest start inverting until V reacehs its 50 percent point (rmebeer we only wish to know delay between 50 percents, so if we do analysis until 50 percent thats enough) so no -vdd vdd business cuz no switching in second cmos until 50 percent (cuz there is some delay in to second output! think!! think of how 1st cmos gets it 2, you shall get it!)

Implications of capacitance

Given that transistors output finite current (eg. I_{DSAT}), o

i.e the max current you can draw is more or less fixed

Implications of capacitance

Given that transistors output finite current (eg. I_{DSAT}), a finite load capacitance means that transitions from V_{DD} to GND (and v.v.) require finite time

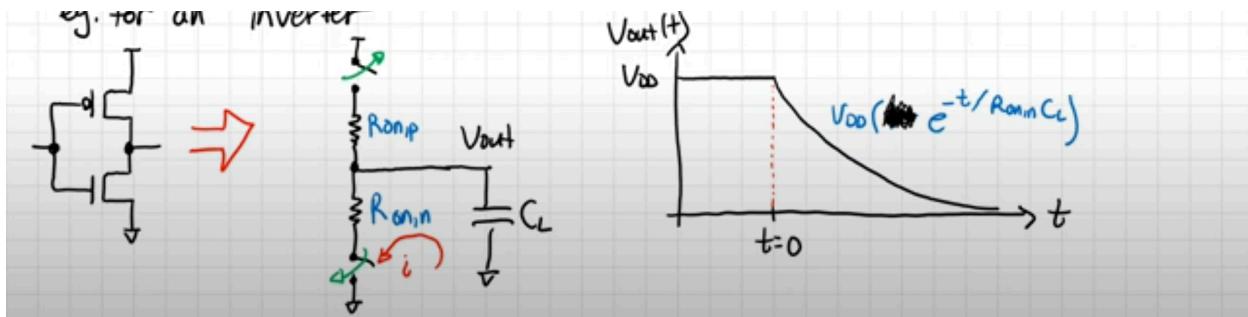
makes sense, cuz if current you can draw is fixed and you wish to reach this much voltage (or charge really on cap) you shall need a fixed time! Unlike a raw wire which can draw infinite current and produce charge instantly, you cant do it here.

THE SPEED AT WHICH A CMOS CAN REACH A PARTICULAR V IS THEREFORE LIMITED BY ITS CAPACITANCE and of course the kind of current you can give// more current faster V reach, less Cap, faster V reach

There are a bunch of ways in which we can model this charging discharging of cap to reach a particular V, but we often do it with an equivalent resistance model (not necessarily the phenomenon hapneing here, but just model sake, ok i will let sir talk now)

limited by capacitance (and charging current). We often idealize charging using an equivalent resistance.

Equivalent Resistance Model



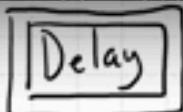
green is at $t = 0$, say PMOS turns off and NMOS turns on, we can model the entire NMOS PMOS behaviour as that of changing resistor —> we shall take it's avg value

You could also have modeled using a current source- that also changes as mode of operation changes, but we shall use this simple model instead.

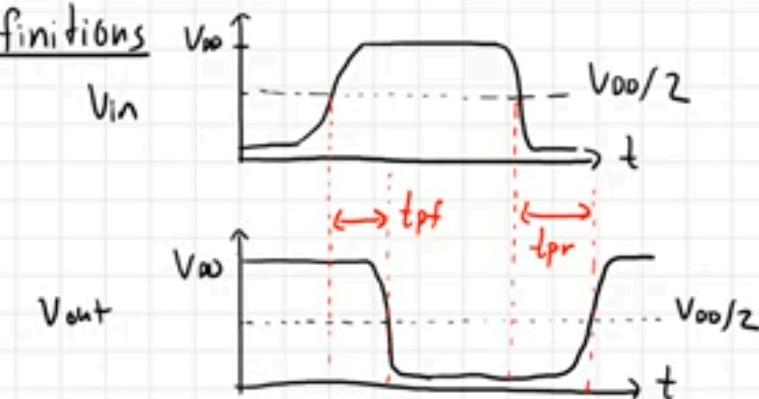
Delay

Some definitions first -

ECE 165 - Lecture 4: MOS Capacitances and Delay (2021)

 → Chap. 4, W:H

Definitions



50 to 50, called propagation delay

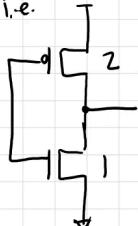
ECE 165 - Lecture 4: MOS Capacitances and Delay (2021)



Class convention → for lectures and homeworks only!

For equal drive strength, set $(W/L)_p = 2(W/L)_n$

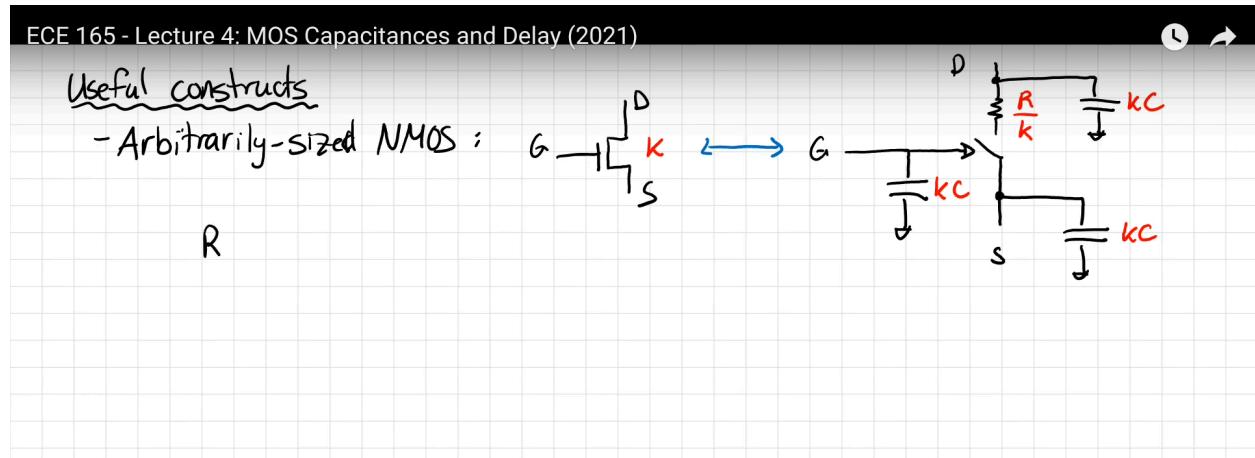
i.e.



Have symmetric VTC around $V_{DD}/2$, $t_{pr} = t_{pf}$

Rise time is fall time - approx

Okay, it might be getting a little complicated now -



that's since C is prop to K (w rather cuz L is fixed) and R / k cuz R is inversely prop to K (just get it from any mos current equation)

tors of width k with contacted diffusion on both source and drain. The pMOS transistor has approximately twice the resistance of the nMOS transistor because holes have lower mobility than electrons. The pMOS capacitors are

Therefore, we can write it as -

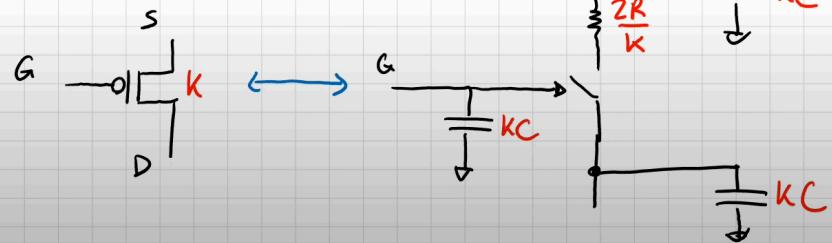
- Arbitrarily-sized PMOS :

$$R_{new,p} = \frac{2 R_{min,n}}{k}; \quad C_{new,p} = k C_{min}$$

The cap however has nothing to do with mobility, only magnitude of charge, therefore, it remains the same!

- Arbitrarily-sized PMOS:

$$R_{new,p} = \frac{2R_{min,n}}{k}; C_{new,p} = kC_{min}$$



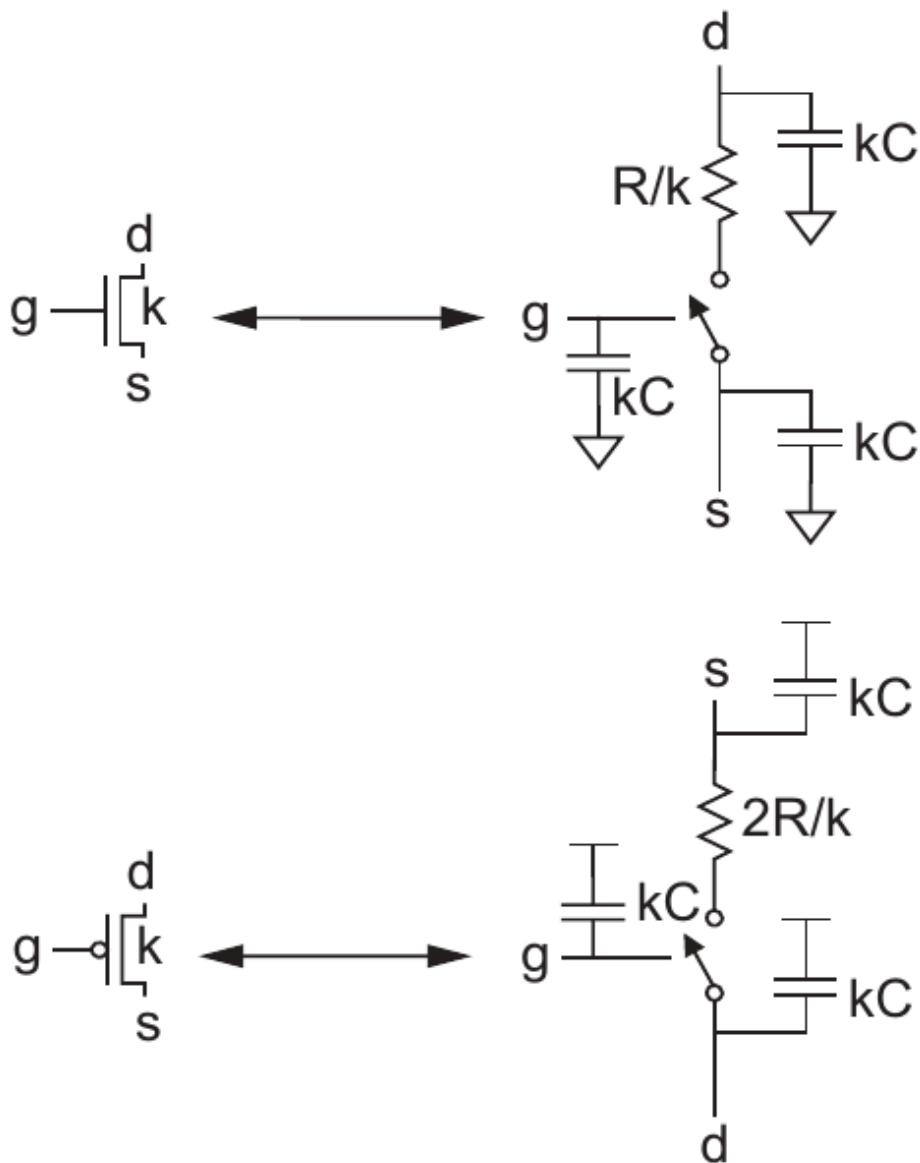
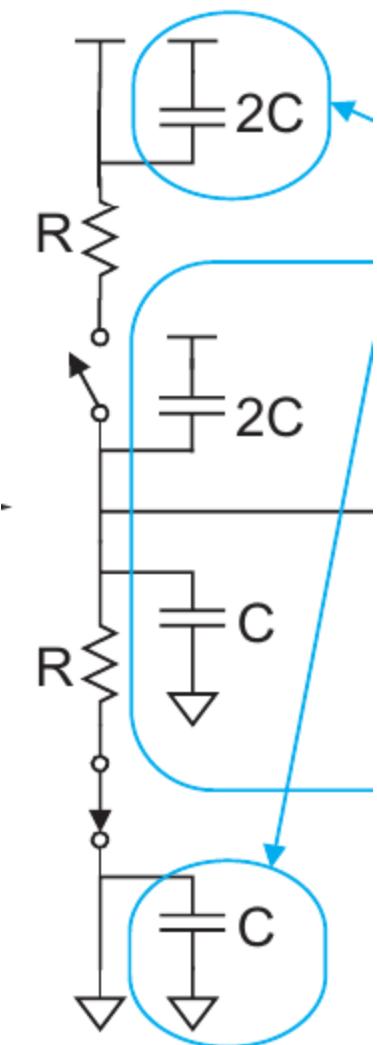


FIGURE 4.5

Equivalent circuits for transistors

He made a mistake they are connected to Vdd instead for PMOS

Conside an inverter chain with a fan out of 0 (its not connected to any inverter)



(b)

Then,

Q: What is t_{pd} for an unloaded inverter?

A:

$$t_{pd} = 3RC$$

Convention: $\tau = 3RC \rightarrow$ intrinsic delay of a unit-sized inverter

1:01:35 / 1:05:42 Full screen

We get t_{pd} $t_{dpr} = 3RC$, which we can label as tau - the intrinsic delay

Q: How does one design for speed?

A: $\tau \propto R \cdot C$

- ↳ keep capacitance small (eg. 14nm instead of 45nm)
- ↳ keep R small by limiting self-loading (see HW2)
- ↳ Increase V_{dd} (effectively reduces R by having a larger V_{gs})

Elmore Delay

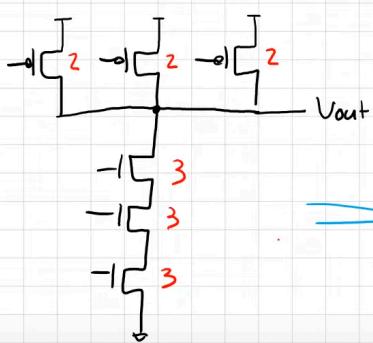
Check Janakiraman sir's notes as well :P

Elmore Delay

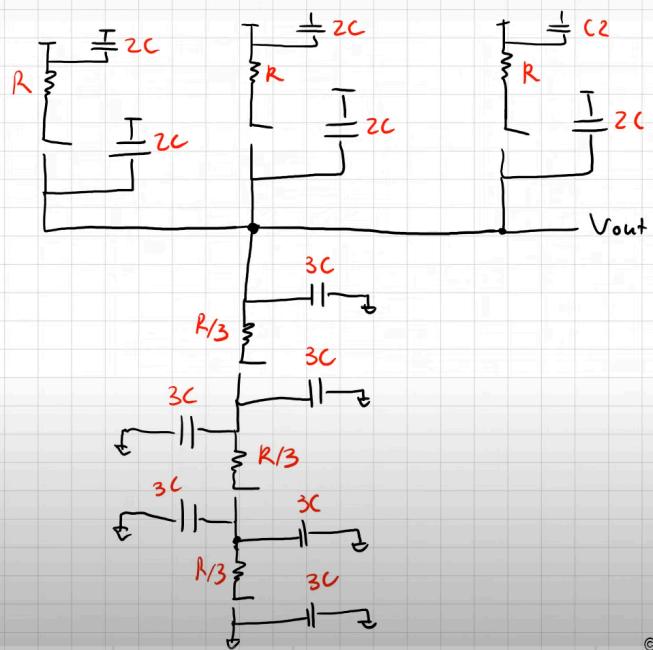
Most digital circuits can be modeled as an RC tree.

The Elmore delay technique can approximate this delay

eg. Design a 3-input NAND gate with equal PUN and PDN drive strength, and estimate t_{pd} .

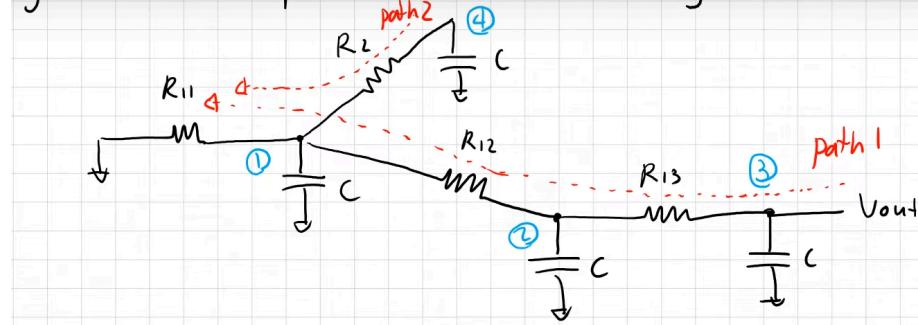


\Rightarrow



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eg. A more complex PDN. Calc. delay to V_{out} .

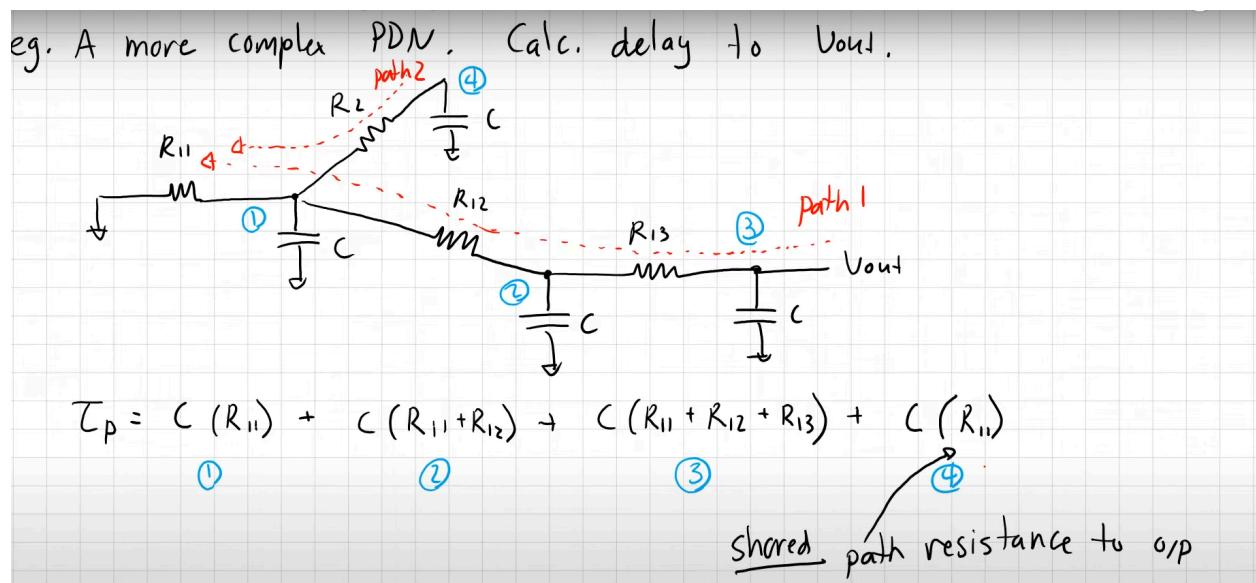


So steps :

Are you charging or discharging Vout? Discharging, then choose that path..

Now you must discharge every cap to that main ground

and then apply the janakiraman sir's method! all caps but only those resistors that share the path



Logical Delay

I am going to write this in the CMOS notes instead of here, cuz its important.