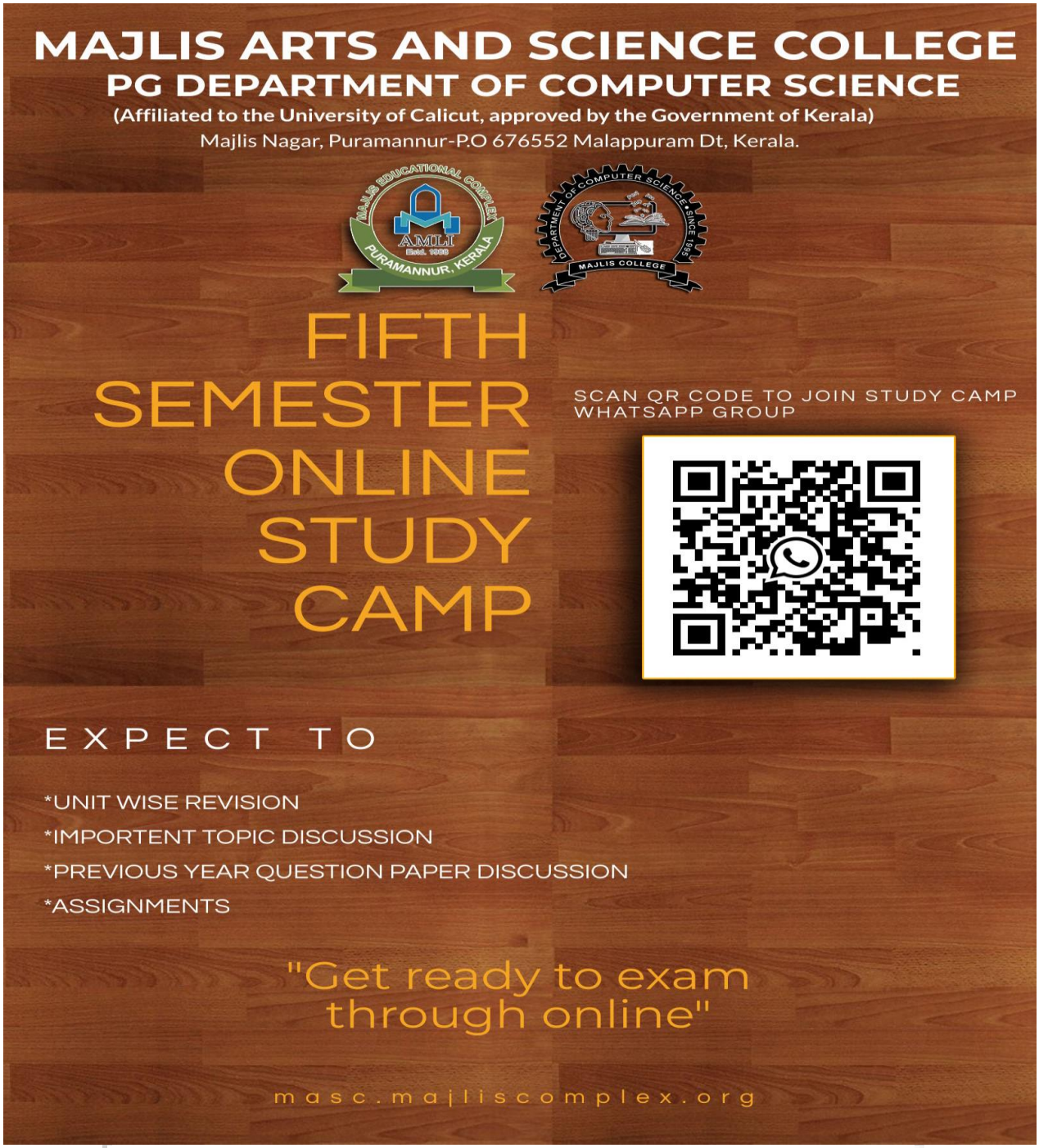


COMPUTER ORGANIZATION AND ARCHITECTURE

2nd MODULE

1. Define edgetriggering?

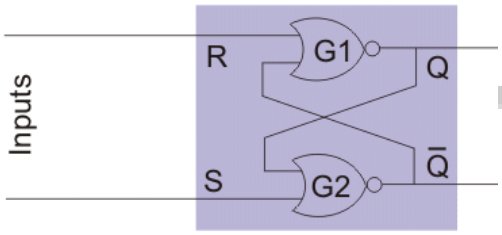
   a)In edge triggering the circuit becomes active at negative or positive edge of the clock signal.

2. Define pulse triggering?

   a)pulse-triggered means that data are entered into the flip-flop on the rising edge of the clock pulse, but the output does not reflect the input state until the falling edge of the clock pulse

3. Define SR latch

   An SR latch (Set/Reset) is an asynchronous device: it works independently of control signals and relies only on the state of the S and R inputs. In the image we can see that an SR latch can be created with two NOR gates that have a cross-feedback loop.

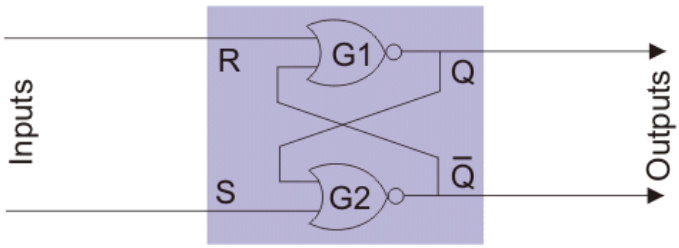


S	R	Q	Q_{+1}	STATE
0	0	0	X	INVALID
0	0	1	X	
0	1	0	1	SET
1	0	0	0	RESET
1	1	0	1	NC

4. What is an SR Flip Flop?

   An SR Flip Flop (also referred to as an SR Latch) is the most simple type of flip flop. It has two inputs S and R and two outputs Q and $\overline{Q}$. The state of this latch is determined by the condition of Q. If Q is 1 the latch is said to be SET and if Q is 0 the latch is said to be RESET. This SR Latch or Flip flop can be designed either by two cross-coupled NAND gates or two-cross coupled NOR gates.

   When we design this latch by using NOR gates, it will be an active high S-R latch. That means it is SET when S = 1. When we design this latch by using NAND gates, it will be an active low S-R latch. That means it is SET when S = 0. SR Flip Flop is also called SET RESET Flip Flop.



5. What are asynchronous counter?

   Asynchronous counters are those whose output is free from the clock signal. Because the flip flops in **asynchronous counters** are supplied with different clock signals, there may be delay in producing output.

6. What are synchronous counter?

   All flip flops are clocked together at the same time with the same clock signal. Due to this common clock pulse all output states switch or change simultaneously.
   ... Synchronous counters are sometimes called parallel counters as the clock is fed in parallel to all flip-flops

7. What are 3-bit Asynchronouscounter?

   The 3-bit Asynchronous binary up counter contains three T flip-flops and the T-input of all the flip-flops are connected to '1'. ... So, the output of first T flip-flop toggles for every negative edge of clock signal. The output of first T flip-flop is applied as clock signal for second T flip-flop.

8. What is a shift register? Can a shift register be used as a counter

   A **shift register** is a type of digital circuit using a cascade of flip flops where the output of one flip-flop is connected to the input of the next.
   Shift registers are also **used** as **counters**

9. What is a flip flop? What is the difference between latch and flip flop?

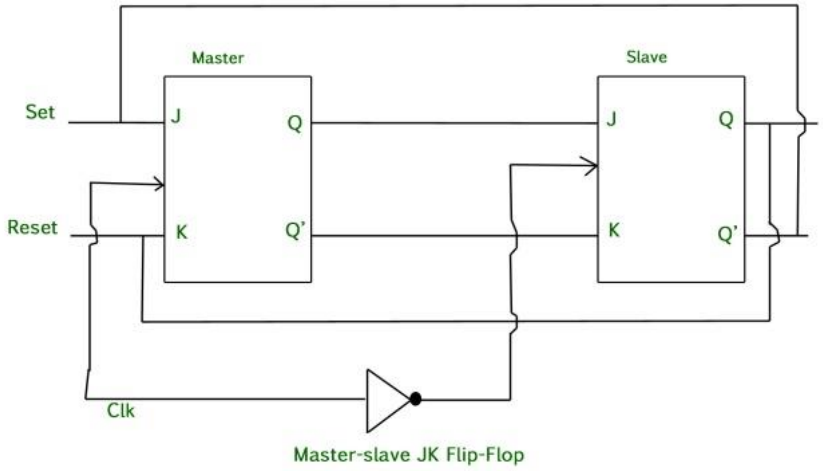
   A **flip-flop** is a device which stores a single bit (binary digit) of data; one of its two states represents a "one" and the other represents a "zero"
   The **difference between** a **latch** and a **flip-flop** is that a **latch** is level-triggered (outputs can change as soon as the inputs changes) and **Flip-Flop** is edge-triggered (only changes state when a control signal goes from high to low or low to high)

10. What is the application of flip flop?

    flip-flop applications are for temporary data storage, as frequency dividers, and in counters.

11. Explain the working of master slave J K flip flop with truth table and logic diagram?

Master Slave JK flip flop –
The Master-Slave Flip-Flop is basically a combination of two JK flip-flops connected together in a series configuration. Out of these, one acts as the “master” and the other as a “slave”. The output from the master flip flop is connected to the two inputs of the slave flip flop whose output is fed back to inputs of the master flip flop.
In addition to these two flip-flops, the circuit also includes an inverter. The inverter is connected to clock pulse in such a way that the inverted clock pulse is given to the slave flip-flop. In other words if CP=0 for a master flip-flop, then CP=1 for a slave flip-flop and if CP=1 for master flip flop then it becomes 0 for slave flip flop.

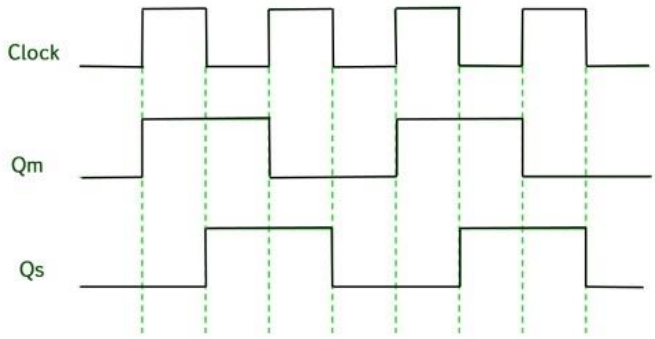


Master-slave JK Flip-Flop

Working of a master slave flip flop –

1. When the clock pulse goes to 1, the slave is isolated; J and K inputs may affect the state of the system. The slave flip-flop is isolated until the CP goes to 0. When the CP goes back to 0, information is passed from the master flip-flop to the slave and output is obtained.
2. Firstly the master flip flop is positive level triggered and the slave flip flop is negative level triggered, so the master responds before the slave.
3. If J=0 and K=1, the high Q' output of the master goes to the K input of the slave and the clock forces the slave to reset, thus the slave copies the master.
4. If J=1 and K=0, the high Q output of the master goes to the J input of the slave and the Negative transition of the clock sets the slave, copying the master.
5. If J=1 and K=1, it toggles on the positive transition of the clock and thus the slave toggles on the negative transition of the clock.
6. If J=0 and K=0, the flip flop is disabled and Q remains unchanged.

Timing Diagram of a Master flip flop –



1. When the Clock pulse is high the output of master is high and remains high till the clock is low because the state is stored.

2. Now the output of master becomes low when the clock pulse becomes high again and remains low until the clock becomes high again.
3. Thus toggling takes place for a clock cycle.
4. When the clock pulse is high, the master is operational but not the slave thus the output of the slave remains low till the clock remains high.
5. When the clock is low, the slave becomes operational and remains high until the clock again becomes low.
6. Toggling takes place during the whole process since the output is changing once in a cycle.
7. This makes the Master-Slave J-K flip flop a Synchronous device as it only passes data with the timing of the clock signal.

Trigger	Inputs		Output				Inference
			Present State		Next State		
CLK	J	K	Q	Q'	Q	Q'	
⊠	x	x	-		-		Latched
⊓	0	0	0	1	0	1	No Change
⊓			1	0	1	0	
⊓	0	1	0	1	0	1	Reset
⊓			1	0	0	1	
⊓	1	0	0	1	1	0	Set
⊓			1	0	1	0	
⊓	1	1	0	1	1	0	Toggles
⊓			1	0	0	1	

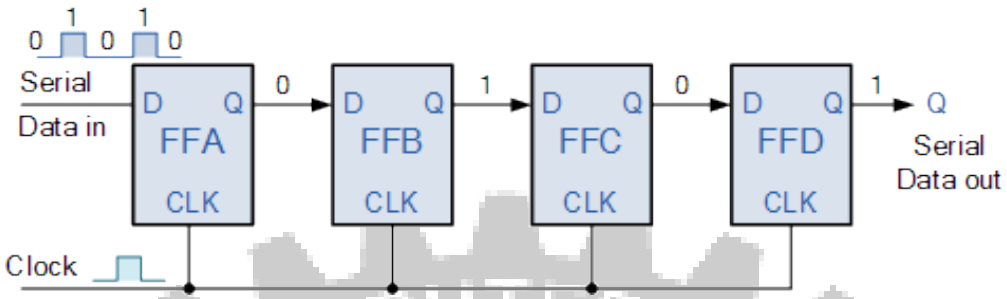
12. A device which convert BCD to seven segment is called -----
    Decoder
13. For JK flip flop for J=1 and K=0, the output after clock pulse will be ----
    1
14. Explain serial in serial out shift register

Serial-in to Serial-out (SISO) Shift Register

There is only one output, the DATA leaves the shift register one bit at a time in a serial pattern, hence the name **Serial-in to Serial-Out Shift Register** or **SISO**.

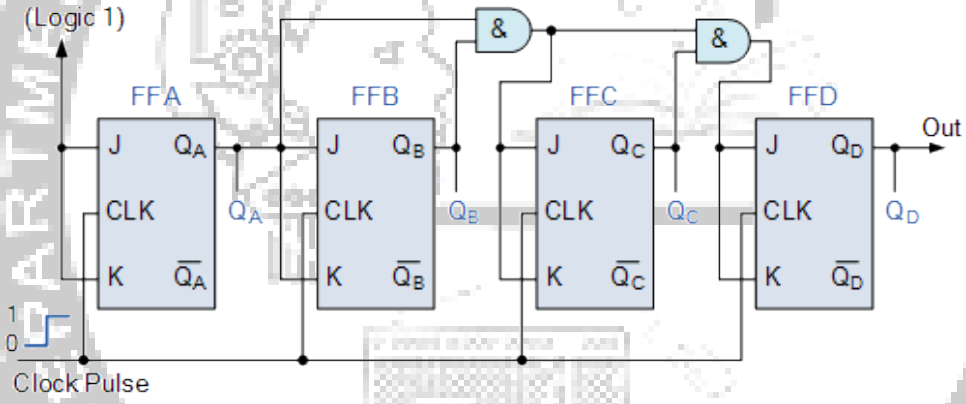
The SISO shift register is one of the simplest of the four configurations as it has only three connections, the serial input (SI) which determines what enters the left hand flip-flop, the serial output (SO) which is taken from the output of the right hand flip-flop and the sequencing clock signal (Clk). The logic circuit diagram below shows a generalized serial-in serial-out shift register.

4-bit Serial-in to Serial-out Shift Register



we may think what's the point of a SISO shift register if the output data is exactly the same as the input data. Well this type of **Shift Register** also acts as a temporary storage device or it can act as a time delay device for the data, with the amount of time delay being controlled by the number of stages in the register, 4, 8, 16 etc or by varying the application of the clock pulses.

15. Give the circuit representation of 4 bit synchronous counter and explain its function



16. What are the different types of counters? Explain 4 bit ripple counter.

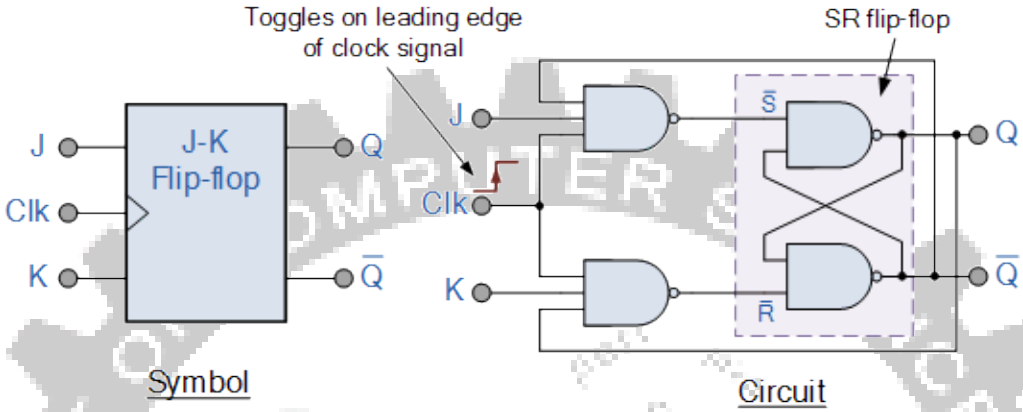
counters (asynchronous
& synchronous),
up/down counter,
decade counter,
mod N counter,
Ring counter,
Johnson'scounter

17. Write the difference between **JK flip flop and** SR flip-flop

The **JK flip flop** is basically a gated SR flip-flop with the addition of a clock input circuitry that prevents the illegal or invalid output condition that can occur when both inputs S and R are equal to logic level "1". Due to this additional clocked input, a JK flip-flop has four possible input combinations, "logic 1", "logic 0", "no change" and "toggle".

The symbol for a JK flip flop is similar to that of an *SR Bistable Latch* as seen in the previous tutorial except for the addition of a clock input.

18. Explain JK Flip-flop



Both the S and the R inputs of the previous SR bistable have now been replaced by two inputs called the J and K inputs, respectively after its inventor Jack Kilby. Then this equates to: J = S and K = R.

The two 2-input AND gates of the gated SR bistable have now been replaced by two 3-input NAND gates with the third input of each gate connected to the outputs at Q and Q. This cross coupling of the SR flip-flop allows the previously invalid condition of S = "1" and R = "1" state to be used to produce a "toggle action" as the two inputs are now interlocked.

If the circuit is now "SET" the J input is inhibited by the "0" status of Q through the lower NAND gate. If the circuit is "RESET" the K input is inhibited by the "0" status of Q through the upper NAND gate. As Q and Q are always different we can use them to control the input. When both inputs J and K are equal to logic "1", the JK flip flop toggles as shown in the following truth table.

The Truth Table for the JK Function

Truth Table

J	K	CLK	Q
0	0	↑	Q_0 (no change)
1	0	↑	1
0	1	↑	0
1	1	↑	$\overline{Q}_0$ (toggles)

Then the JK flip-flop is basically an SR flip flop with feedback which enables only one of its two input terminals, either SET or RESET to be active at any one time under normal

switching thereby eliminating the invalid condition seen previously in the SR flip flop circuit.

19. What is the difference between a ring counter and a Johnson counter

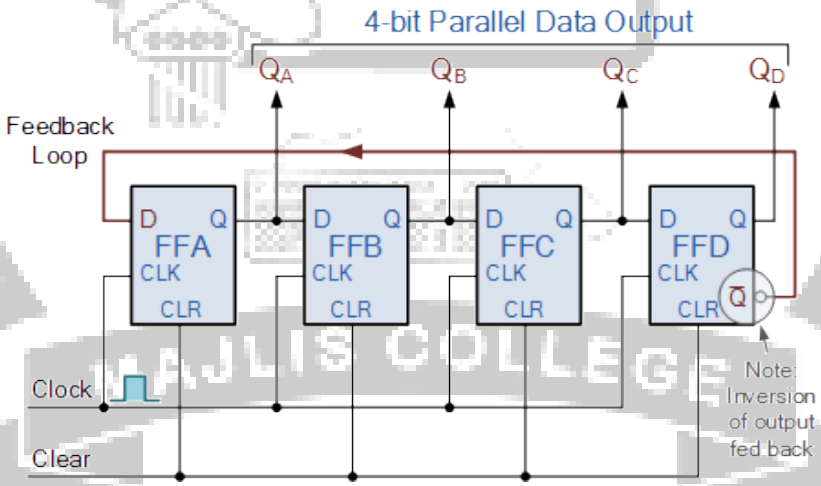
The **difference between a ring counter and a Johnson counter** is which output of the last stage is fed back (Q or Q'). ... Recirculating a single 1 around a **ring counter** divides the input clock by a factor equal to the number of stages. Whereas, a **Johnson counter** divides by a factor equal to twice the number of stages.

20. Johnson Ring Counter

The **Johnson Ring Counter** or "Twisted Ring Counters", is another shift register with feedback exactly the same as the standard *Ring Counter* above, except that this time the inverted output Q of the last flip-flop is now connected back to the input D of the first flip-flop as shown below.

The main advantage of this type of ring counter is that it only needs half the number of flip-flops compared to the standard ring counter then its modulo number is halved. So a "n-stage" Johnson counter will circulate a single data bit giving sequence of 2n different states and can therefore be considered as a "mod-2n counter".

4-bit Johnson Ring Counter



This inversion of Q before it is fed back to input D causes the counter to "count" in a different way. Instead of counting through a fixed set of patterns like the normal ring counter such as for a 4-bit counter, "0001"(1), "0010"(2), "0100"(4), "1000"(8) and repeat, the Johnson counter counts up and then down as the initial logic "1" passes through it to the right replacing the preceding logic "0".

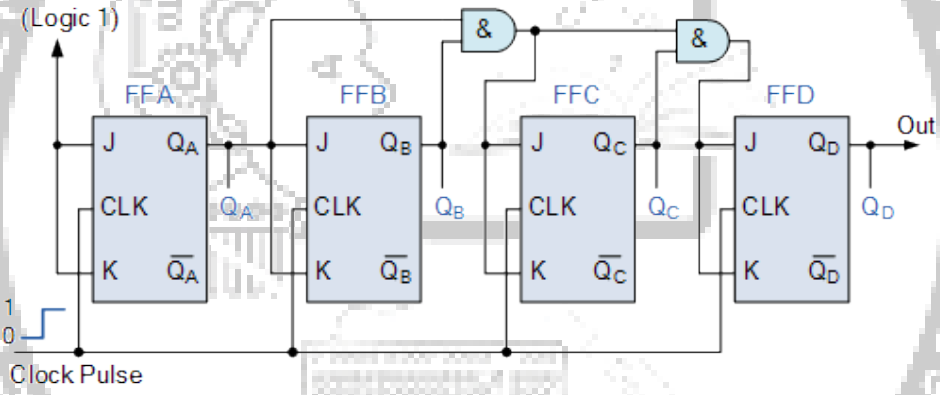
A 4-bit Johnson ring counter passes blocks of four logic "0" and then four logic "1" thereby producing an 8-bit pattern. As the inverted output Q is connected to the input D this 8-bit pattern

continually repeats. For example, “1000”, “1100”, “1110”, “1111”, “0111”, “0011”, “0001”, “0000” and this is demonstrated in the following table below.

Truth Table for a 4-bit Johnson Ring Counter

Clock Pulse no		FFA	FFB	FFC	FFD
0	0	0	0	0	
1	1	0	0	0	
2	1	1	0	0	
3	1	1	1	0	
4	1	1	1	1	
5	0	1	1	1	
6	0	0	1	1	
7	0	0	0	1	
8	0	0	0	1	

Explain Binary 4-bit Synchronous Up Counter



In this the external clock pulses (pulses to be counted) are fed directly to each of the **J-K flip-flops** in the counter chain and that both the J and K inputs are all tied together in toggle mode, but only in the first flip-flop, flip-flop FFA (LSB) are they connected HIGH, logic “1” allowing the flip-flop to toggle on every clock pulse. Then the synchronous counter follows a predetermined sequence of states in response to the common clock signal, advancing one state for each pulse.

The J and K inputs of flip-flop FFB are connected directly to the output Q_A of flip-flop FFA, but the J and K inputs of flip-flops FFC and FFD are driven from separate AND gates which are also supplied with signals from the input and output of the previous stage. These additional AND gates generate the required logic for the JK inputs of the next stage.

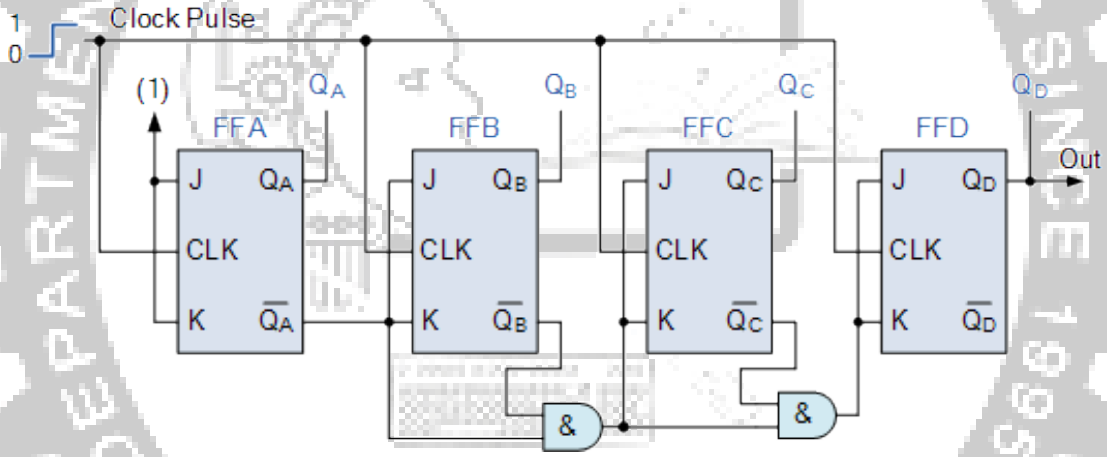
If we enable each JK flip-flop to toggle based on whether or not all preceding flip-flop outputs (Q) are “HIGH” we can obtain the same counting sequence as with the asynchronous circuit but without the ripple effect, since each flip-flop in this circuit will be clocked at exactly the same time.

Then as there is no inherent propagation delay in synchronous counters, because all the counter stages are triggered in parallel at the same time, the maximum operating frequency of this type of frequency counter is much higher than that for a similar asynchronous counter circuit.Because this 4-bit synchronous counter counts sequentially on every clock pulse the resulting outputs count upwards from 0 (0000) to 15 (1111). Therefore, this type of counter is also known as a **4-bit Synchronous Up Counter**.

Explain Binary 4-bit Synchronous Down Counter

To construct a **4-bit Synchronous Down Counter** by connecting the AND gates to the Q output of the flip-flops as shown to produce a waveform timing diagram the reverse of the above. Here the counter starts with all of its outputs HIGH (1111) and it counts down on the application of each clock pulse to zero, (0000) before repeating again.

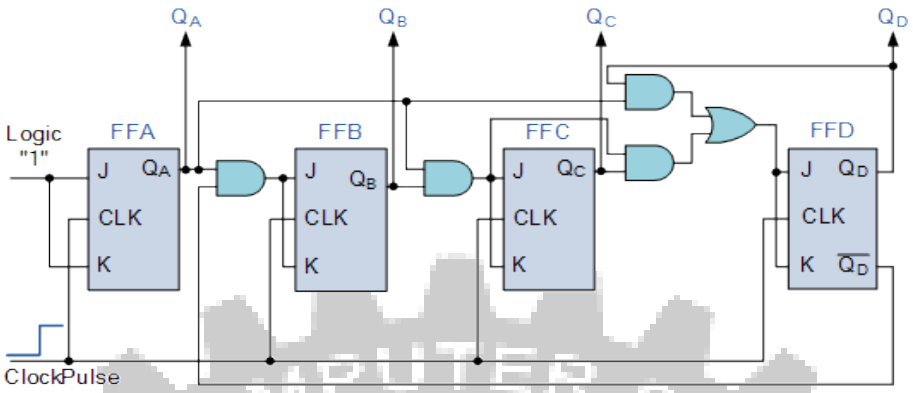
Binary 4-bit Synchronous Down Counter



As synchronous counters are formed by connecting flip-flops together and any number of flip-flops can be connected or "cascaded" together to form a "divide-by-n" binary counter, the modulo's or "MOD" number still applies as it does for asynchronous counters so a Decade counter or BCD counter with counts from 0 to 2^n-1 can be built along with truncated sequences. All we need to increase the MOD count of an up or down synchronous counter is an additional flip-flop and AND gate across it.

Explain Decade 4-bit Synchronous Counter

A 4-bit decade synchronous counter can also be built using synchronous binary counters to produce a count sequence from 0 to 9. A standard binary counter can be converted to a decade (decimal 10) counter with the aid of some additional logic to implement the desired state sequence. After reaching the count of "1001", the counter recycles back to "0000". We now have a decade or **Modulo-10** counter.



The additional AND gates detect when the counting sequence reaches “1001”, (Binary 10) and causes flip-flop FF3 to toggle on the next clock pulse. Flip-flop FF0 toggles on every clock pulse. Thus, the count is reset and starts over again at “0000” producing a synchronous decade counter.

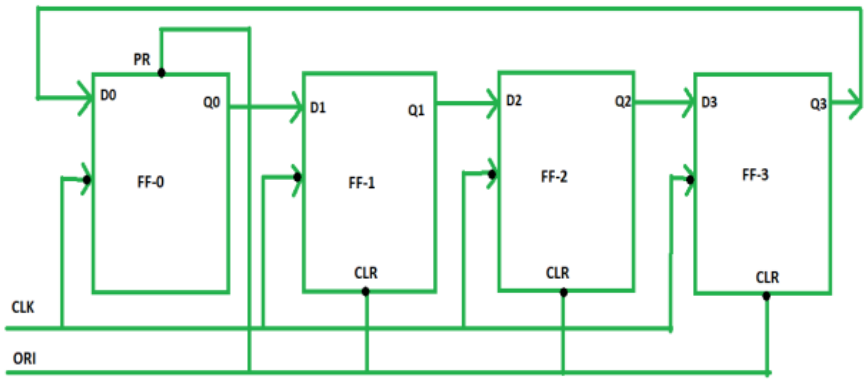
We could quite easily re-arrange the additional AND gates in the above counter circuit to produce other count numbers such as a Mod-12 counter which counts 12 states from”0000″ to “1011” (0 to 11) and then repeats making them suitable for clocks, etc.

Explain Ring Counter

Ring counter is a typical application of Shift resister. Ring counter is almost same as the shift counter. The only change is that the output of the last flip-flop is connected to the input of the first flip-flop in case of ring counter but in case of shift resister it is taken as output. Except this all the other things are same.

No. of states in Ring counter = No. of flip-flop used

So, for designing 4-bit Ring counter we need 4 flip-flop.



Ring Counter

In this diagram, we can see that the clock pulse (CLK) is applied to all the flip-flop simultaneously. Therefore, it is a Synchronous Counter.
Also, here we use Overriding input (ORI) to each flip-flop. Preset (PR) and Clear (CLR) are used as ORI.

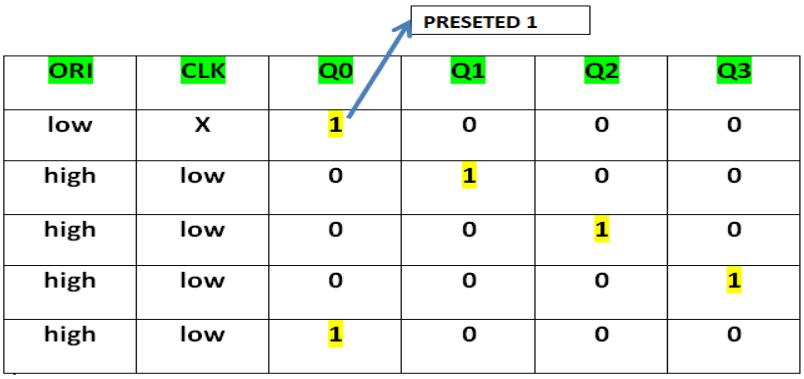
When PR is 0, then the output is 1. And when CLR is 0, then the output is 0. Both PR and CLR are active low signal that is always works in value 0.

PR = 0, Q = 1

CLR = 0, Q = 0

These two values are always fixed. They are independent with the value of input D and the Clock pulse (CLK).

Working –
Here, ORI is connected to Preset (PR) in FF-0 and it is connected to Clear (CLR) in FF-1, FF-2, and FF-3. Thus, output Q = 1 is generated at FF-0 and rest of the flip-flop generate output Q = 0. This output Q = 1 at FF-0 is known as Pre-set 1 which is used to form the ring in the Ring Counter.



ORI	CLK	Q0	Q1	Q2	Q3
low	X	1	0	0	0
high	low	0	1	0	0
high	low	0	0	1	0
high	low	0	0	0	1
high	low	1	0	0	0

This Preseted 1 is generated by making ORI low and that time Clock (CLK) becomes don't care. After that ORI made to high and apply low clock pulse signal as the Clock (CLK) is negative edge triggered. After that, at each clock pulse the preseted 1 is shifted to the next flip-flop and thus form Ring.

From the above table, we can say that there are 4 states in 4-bit Ring Counter.

4 states are:

1 0 0 0

0 1 0 0

0 0 1 0

0 0 0 1

In this way can design 4-bit Ring Counter using four D flip-flops.

Types of Ring Counter – There are two types of Ring Counter:
1. **Straight Ring Counter –**
2. **Twisted Ring Counter –**